*Application Note*

# *Design Considerations for Current Sensing in DC EV Charging Applications*

*Riccardo Ruffo, Lei Song, Harald Parzhuber* *Systems Engineering and Marketing*

**ABSTRACT**

The shift from combustion engines to electric vehicles (EVs) seems inevitable as governments around the world commit to environmental sustainability goals and the automotive industry plans to invest more to accelerate vehicle electrification. The capacity of DC fast-charging stations has increased significantly in recent years. Where the standard was once 150 kW, capacities are now 350 kW and beyond — and the improvements continue. To get to 350 kW and above, a common technology is to stack modules with 20 kW to 40 kW in parallel and perform load balancing of those modules in parallel in a higher level control loop. The current and voltage-sensing technology plays an essential role in the power module control loop of DC fast-charging stations. This application report looks into design considerations for current sensing in EV charging applications, especially with a focus on the gain error, offset, bandwidth, and latency concerning system performance.

## Table of Contents



## List of Figures

## List of Tables



## Trademarks

All trademarks are the property of their respective owners.

# 1 Introduction

## 1.1 DC Charging Station for Electric Vehicles

To supply or drain the power from the vehicle battery to the grid, multiple conversion stages are necessary between the AC and the DC rails, as Figure 1-1 shows.

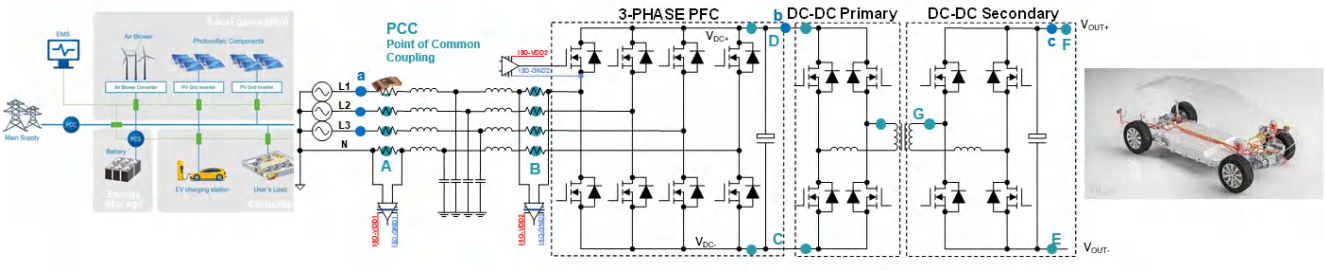


**Figure 1-1. Current Sensing Points of an EV Charging System**

AC/DC converters are responsible to convert AC into DC power by keeping under control the current Total Harmonic Distortion (THD) on the Point of Common Coupling (PCC) together with the DC voltage. At the same time, isolated DC/DC converters are mainly used for galvanic isolation between the grid and the car and to achieve Constant Current (CC) and Constant Voltage (CV) charging functionalities.

Figure 1-1 depicts typical current sensor locations of an EV charging system.

- Power regulation and protections of the AC/DC stage are achieved by means of sensors placed in point A, B, C, and D:
  - **Point A** is the main connection point of the converter toward the PCC. By placing sensors at this location, the currents pushed into or pulled from the grid can be most accurately monitored and controlled, thereby achieving accurate control of active and reactive powers interchanged with the grid.
  - **Point B** has the capability to measure the switch current in the Switching Node (SN). By placing the current sensors in this location, protection of power switches and control loop speed can be improved. Furthermore, when an isolated power supply is required by the current sensing circuit, gate driver supply can be leveraged, thus reducing the total cost of the design. However, the measurement does not include the losses in the EMI filter, therefore this location is less suitable for reactive power compensation.
  - **Point C** is the measurement point of the DC bus current. Placement of the current-sensing circuit in this location allows cost reduction when the power supply is shared with the bottom switch-driver supply.
  - **Point D** is the measurement point of the DC bus current placed on the positive rail of the DC bus.
- Power regulation and protection of the DC/DC stage are achieved by means of sensing placed in point G, F, and E.
  - **Point G** is required to control the windings currents.
  - **Point F** is the measurement point of the battery current located on the positive terminal.
  - **Point E** is the measurement point of the battery current located on the negative terminal. The benefit of sensing the current flowing to the negative terminal is that the gate-driver supply of the low-side FET can be leveraged for powering the current-sensing circuit.

In this application note, a study based on simulation results was conducted with the aim to define the minimal specifications required by the current sensors when used in DC charging applications for EVs. Optimal values of bandwidth, gain error, offset, and latency were derived for an 11-kW system presenting the system specifications listed in Table 1-1. Two different isolated DC/DC topologies are considered in this document: DAB (Dual Active Bridge) with phase-shift control and DAB with CLLLC resonant converter.

Section 2 discusses design considerations for AC/DC input current sensing Point A and B respectively with DC link current measurements in C and D. Section 3 details the requirements for the current sensing points in the DC/DC stage (G, F, E) in how proprieties as bandwidth, gain and offset errors impact the performance of the DC/DC stage.

**Table 1-1. Target Specifications for EV Charger**

| Condition | Description |
|---|---|
| Power ratings and power flow | 11-kW bidirectional operation to support V2G/V2H |
| AC ratings | 400 $V_{AC}$ (3-phase each 230 $V_{AC}$)<br>16 $A_{RMS}$ (each phase) |
| Total harmonic distortion of AC current | 3.6% at PCC at full load |
| DC Ratings | $V_{DCBUS}$ 800 V nominal ( from 650 V to 800 V)<br>$I_{DCBUS}$ 14 A ( from 14 A to 17 A)<br>$V_{BAT}$ 400 V (from 250 V to 450 V)<br>$I_{OUT}$ 27.5 A ( from 24 A to 44 A) |
| Switching frequency of AC/DC | 70 kHz (dead-time = 250 ns) |
| Switching frequency of DC/DC | 100 kHz for phase-shifted DAB<br>500 kHz nominal for resonant CLLLC DAB |
| Accuracy required by the power controlled in the DC side | $V_{DCBUS}$ ±1%<br>$V_{BAT}$ ±1%<br>$I_{BAT}$ ±1% |
| Implemented AC/DC bandwidths of the current and voltage loops | 3-kHz grid current loops (id, iq)<br>400-Hz DC bus voltage loop |
| Implemented bandwidths of the voltage measurements: grid and DC link | 100 kHz |

## 1.2 Current-Sensing Technology Selection and Equivalent Model

### 1.2.1 Sensing of the Current With Shunt-Based Solution

In this application note, only shunt-based current sensing with isolated amplifiers or isolated delta-sigma modulators are considered. All products discussed have a linear input voltage range of ±50 mV which allows use of very small shunt-resistor values to keep power a low energy dissipation compared to the overall power of the system.

In the reference application, for an 11-kW AC/DC, the input currents have a maximum value or 16 $A_{RMS}$ for 400 $V_{AC}$ three-phase system. This results in ±22.5 $A_{peak}$. With a 2-mΩ shunt resistor, the maximum voltage across the shunt can be kept well below 50 mV (peak is 45 mV), meaning that at maximum power operation of 11 kW the power dissipation within the shunt is only 0.5 W per shunt. Assuming three shunts in a 3-phase system this is still negligible loss and does not add any important hot spot on the PCB. Conversely, the currents in the DC/DC converter can be as high as 44 A as indicated in Table 1-1. This result drives the requirements to select a 1-mΩ shunt resistor for the 50-mV input voltage range of the isolated amplifier which results in a power dissipation lower than 2 W for each measurement point (negligible with respect to 11-kW total power).

### 1.2.2 Equivalent Model of the Sensing Technology

The analysis of each current-sensing point is done at a system level by considering four parameters: bandwidth, latency, gain error, and offset. Figure 1-2 shows an equivalent model of the current sensing by showing all the mentioned parameters of the sensor.

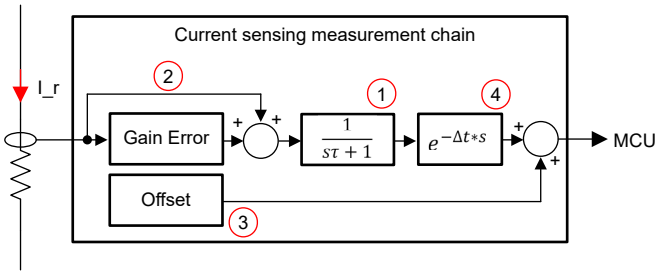


**Figure 1-2. Current Sensing Measurement Model**

A description of each single stage of the equivalent model follows:

1. Represents the bandwidth limitation presented by the current sensor. In this note, the sensing stage has been modeled as a first-order low-pass filter, where the constant time can be described as follows: $\tau = 1/(2\pi f_b)$.

   where

   - τ is the bandwidth of the current sensor
2. Represents the gain error and is modeled as follows: $i_m = (1 + \varepsilon)i_r$

   where

   a. $i_r$ is the real current
   b. ε is the gain error of the sensor
   c. $i_m$ is the measurement
3. Represents the offset which in this study was defined with respect to the measurement range. The offset is represented as a percentage of the full-scale range.
4. Represents the time delay introduced by sensing stage, which becomes critical when overcurrents and short-circuits need to be detected as fast as possible.

# 2 Current Sensing in AC/DC Converters

## 2.1 Basic Hardware and Control Description of AC/DC

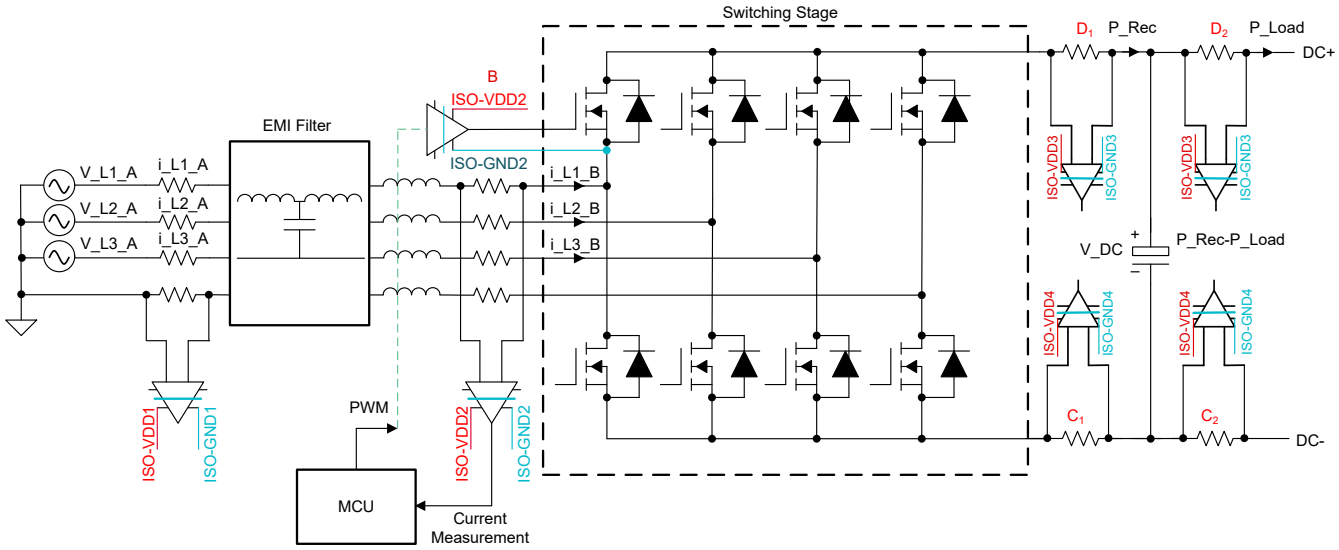


**Figure 2-1. Schematic Representation of a Two-Level AC/DC Converter**

Figure 2-1 illustrates a typical AC/DC converter. The following list describes each part of the converter:

- EMI filter used for mitigating the electromagnetic noise generated by the converter and to be compliant to the standards[7]
- Current sensors and voltage sensors (not represented in the scheme) on both the AC and DC side used for monitoring, control, and protection of the power converter
- Switching stage used for conversion of the power from AC to DC, which can be realized by using multiple topologies such as T-Type and ANPC converters[8, 9]
- Microcontroller used for taking the measurements and calculating the PWM duty cycles for the switches in the power stage to have controlled currents synchronous with the grid voltages

Section 2.1.1 and Section 2.1.2 provide descriptions of the control routines executed internally by the microcontroller. The correlation between the current-sensing parameters and the digital control loops is described in detail.

### 2.1.1 AC Current Control Loops

Controlled power conversion between AC and DC is achieved by synchronizing the control unit with the grid frequency, achieving controlled amplitude and phase of the currents drained by the grid. To get the MCU synchronized with the grid, grid voltages (V_L1_A, V_L2_A, V_L3_A) are sampled by the MCU and fed to a phase-locked loop (PLL)[11]. By using the outcomes of the PLL (cos(φ), sin(φ)), plus Clarke and Park transforms, the three-phase system can be controlled by using the rotating frame reference technique (dq frame control), which allows the control to be simplified and improved.

Figure 2-2 is a schematic representation of the current control loop implemented in an AC/DC by using the rotating frame where measured Id and Iq can be derived by applying the Clarke and Park transformation to either I_L1_A, I_L2_A, I_L3_A or I_L1_B, I_L2_B, I_L3_B.

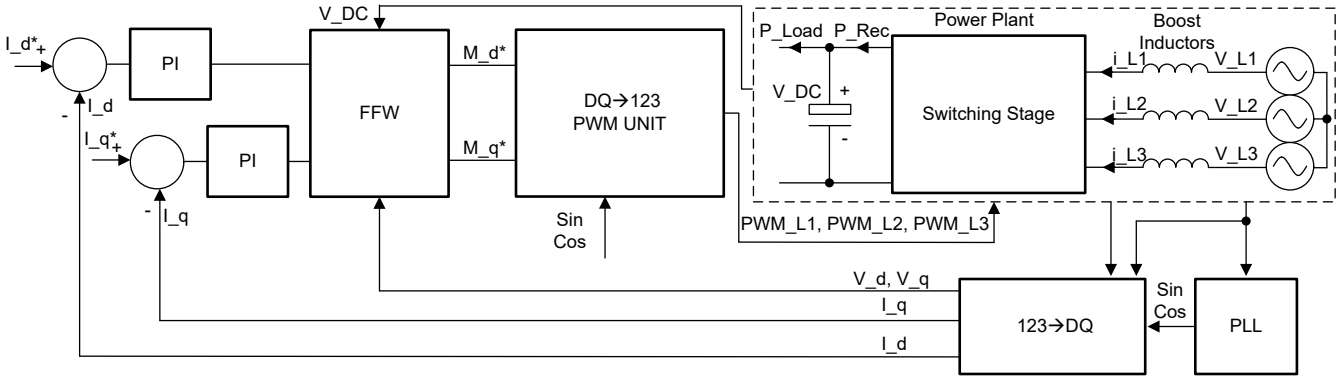


**Figure 2-2. dq Current Control (Feedforward, PI Proportion Integral Control)**

Figure 2-2 illustrates that the currents can be controlled by means of two PI controllers:

- By changing the reference current called direct current (I_d*), the three-phase currents can be controlled in phase with respect to the corresponding grid voltages. This feature allows a direct control of the active power drained or sourced by the AC/DC, as represented in Equation 1, where P_Rec is the three-phase active power. Changing the sign of the reference current makes it possible to drain and source power correspondingly.
- By changing the reference current called quadrature current (I_q*), the three-phase currents can be controlled 90° phase shifted with respect to the corresponding grid voltages. By changing this value, a direct control of the reactive power can be achieved, as shown in Equation 2, where Q is the total three-phase reactive power. By changing the sign of the reference current, it is possible to change the capacitive or inductive power drained by the equipment.

$$\text{P\_Rec} = {}^{3}\!/_{2} V_d I_d^* \tag{1}$$

$$Q = {}^{3}\!/_{2} V_d I_q^* \tag{2}$$

In addition to the PI controllers, feedforwards (FFW) are typically implemented in the current loops to decrease the response time and remove dependencies of the control loop bandwidths when variables in the system change (for example, if V_DC is not compensated, when V_DC decreases, control loop bandwidth can increase causing possible instabilities).

### 2.1.2 DC Voltage Control Loop

In multiple applications, the load or source connected on the DC side of the rectifier stage is not always behaving as a voltage source, indeed the load can act as resistor or current sink or source. When no voltage source behavior is presented by the DC/DC stage, a dependency on the DC bus voltage with the requested power (P_Rec) can lead to no controlled voltage in the output. An uncontrolled DC bus voltage can cause the AC/DC to become unstable, triggering possible current and voltage protections or even damaging the converter itself. To address this, implement an additional control with a higher hierarchical level, with respect to the current loops, as Figure 2-3 shows. A voltage control loop which has the capability to control the active power drained or sourced from the grid by means of I_d* of the lower level control loop Idq was added. The additional PI controller generates a reference (I_d*), which allows matching the rectifier and the load powers (P_Rec and P_Load), by achieving V_DC* equal to V_DC since no power is flowing in the DC-link cap. The matching between the rectifier power and load power is achieved by means of the integrative part.

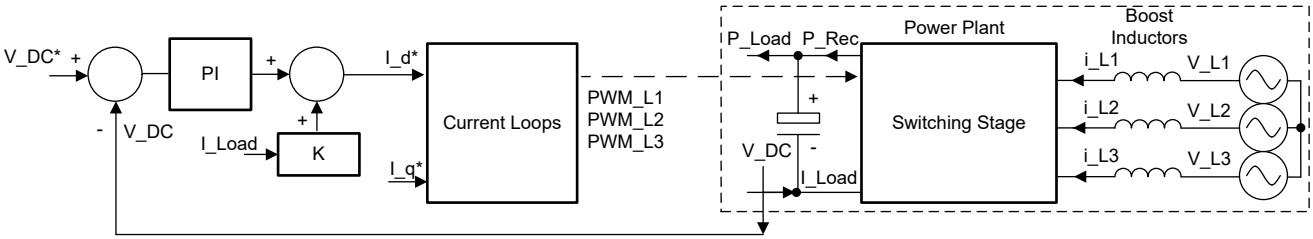


**Figure 2-3. Voltage Plus Current Control Loops**

As Figure 2-3 shows, a feedforward which can be achieved by means of a DC current measurement was implemented to decrease the response time of the loop. A generic factor, K, was implemented since this factor is dependent on the voltages, currents, and control technique implementation. This feature is not critical for the converter operation itself but can improve the performance significantly as demonstrated in Section 2.3.

The I_q* reference is independent from the voltage loop since the reference is not involved in the active power regulation, thus in the charging and discharging process of the DC-link cap. As previously mentioned, I_q* directly controls the reactive power of the system.

## 2.2 Point A and B – AC/DC AC Phase-Current Sensing

This section describes design considerations of current sensors placed in the point of common coupling (point A) or switching node (point B). Investigation results of the control loop performances mentioned in Section 2.1 when sensing parameters are changed are provided.

Offset, bandwidth, gain error, and latency of the current sensors are discussed at a system level with the aim to determine the minimum requirements. Not all scenarios are covered for both points A and B since many cases turned out to be a repetition, only the worst cases are described to determine minimum requirements. The following list shows all the details about the analysis of each current-sensor specification:

- **Sensor Bandwidth**: Analysis was conducted on both points A and B. In point A because the phase error needs to be negligible for the reactive power control. In point B because the AC currents need to be controlled as fast as possible.
- **Highest Latency**: Analysis was conducted only in the switching node because point B is the closest point to the power switches which require protection. Furthermore, between point A and B there is an EMI filter which can create a mismatch between the current present from the switching node with respect to the PCC.
- **Gain Error**: The impact of gain error is the same in both PCC and switching node. The analysis was conducted in the switching node because in point B higher current control loop bandwidth can be achieved, leading to a higher THD of the current when accuracy error is present. Subsequently, when the higher bandwidth is present in the system, the voltage loop injects noise in the grid currents.
- **Offset Error**: The impact of offset error is the same in both PCC and switching node. The analysis was conducted in the switching node because the switching node is the place where higher current control loop bandwidth can be achieved, leading to a higher THD of the current when an offset is present.

### 2.2.1 Impact of Bandwidth

Steady-state and transient analyses were conducted with the aim to observe the control-loop performance as a function of the current sensor bandwidth, defining the minimum bandwidth.

#### *2.2.1.1 Steady State Analysis: Fundamental and Zero Crossing Currents*

In this analysis, grid currents are controlled in the switching nodes (point-B) and a typical profile of the controlled currents are shown in Figure 2-4. Figure 2-4 shows that the three currents and the three voltages are in phase, allowing an active power conversion from the DC toward the AC grid (11 kW toward the grid). The zoomed-in portion in Figure 2-5 shows the current in the switching node is composed of a fundamental component at 50 Hz, plus an important current ripple amplitude caused by the switching of a 2-level converter.

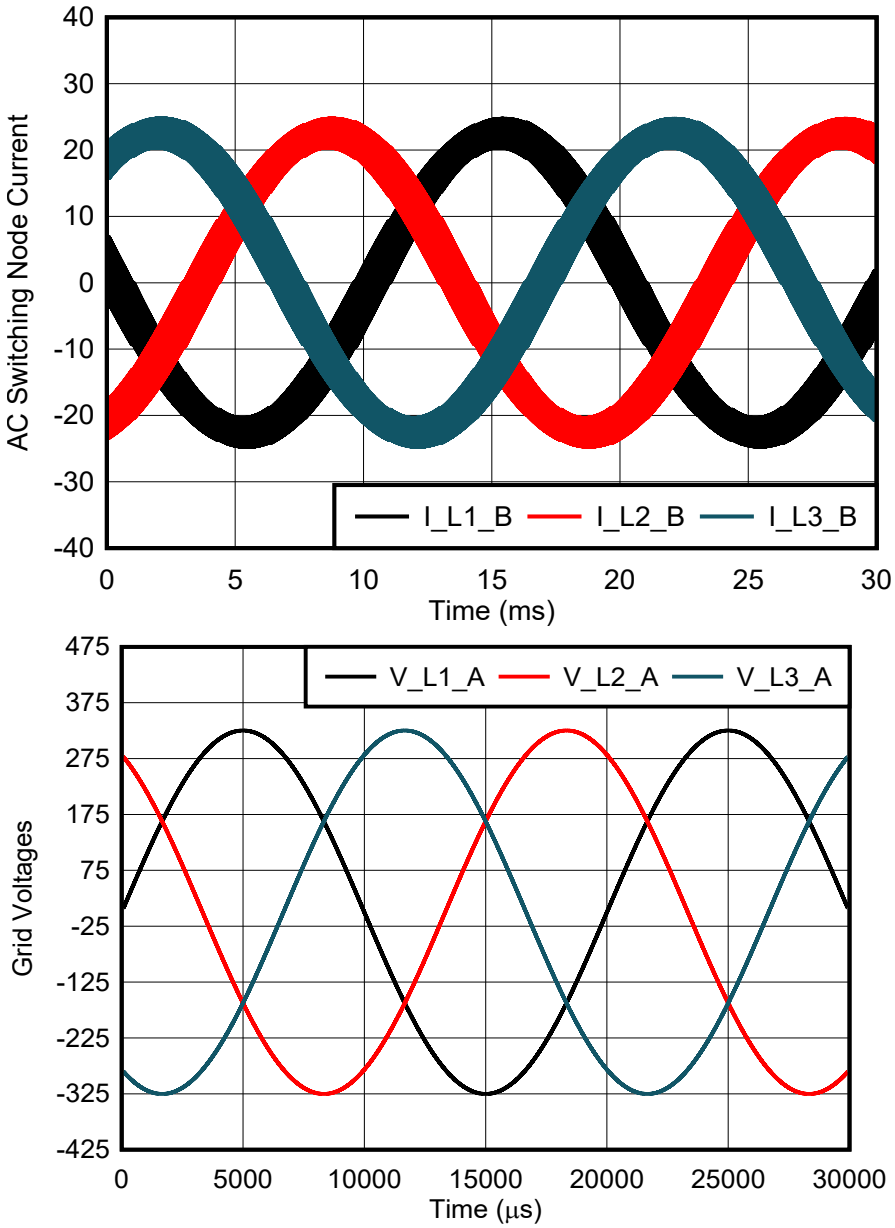


**Figure 2-4. Grid Voltages and Currents of an AC/DC Converter Working at the Nominal Load of 11 kW**

Figure 2-5 is a zoomed-in view of Figure 2-4 which shows the rectifier current plus the average current having a fundamental harmonic of 50 Hz.

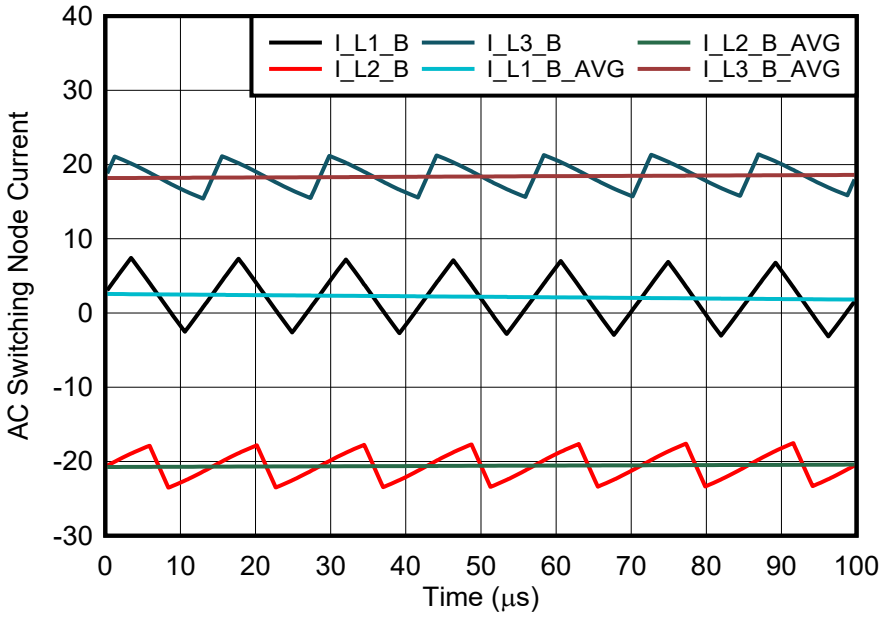


**Figure 2-5. Zoomed in Portion at t = 0s (Span 100µs)**

Power conversion between AC and DC is achieved by means of the currents controlled at the grid frequency. Therefore, the measurement of the fundamental harmonic of the current (for example, I_L1_B_AVG) with correct amplitude and no important phase-delay needs to be delivered to the MCU. The 50-Hz or 60-Hz component can be derived by means of sampling technique as synchronous sampling, average control, and so forth. By adopting these techniques, no important phase delay in the digital control loop is introduced, allowing a faster response of the loop[12]. Conversely, current sensors cannot be considered an ideal choice since current sensors have a bandwidth limitation. The current sensors can lead to important phase-delay and amplitude errors present at the MCU terminals. This error can be reflected in an error of the active and reactive powers exchanged and are expressed as in Equation 3.

$$\varphi = a\tan(2\pi f_e \tau) \quad (3)$$

where

- φ is the phase delay between the measured current and the real current
- $f_e$ is the electrical frequency of the measured signal, which is equal for this application to 50 Hz or 60 Hz
- τ is the constant time of the low-pass filter behavior presented by the measurement chain

By using Equation 3, with a cutoff frequency higher than a hundred times the grid electrical frequency (6 kHz when having a grid at 60 Hz) a phase-angle delay lower than 0.6°can be achieved. This phase shift results in 50 Hz or 60 Hz to a negligible error of the active and reactive controlled power. The component to which the power conversion occurs, a 6-kHz bandwidth, is more than sufficient for controlling grid currents.

In general, 50 Hz or 60 Hz are not the only component to be controlled but there are higher frequency components in the grid currents introduced by the dead time in the power stage, leading to a significant increase of the THD. The high frequency component must be captured by the measurement such that the MCU can correct them, allowing a software cancellation. Increasing the dead time leads to higher distortions, in particular at the zero crossing of the current (at 11 ms) as shown in Figure 2-6. In this picture, current waveforms in point A drained by an AC/DC converter working at 11 kW are shown when the dead time of the controller is changed. The top graph shows the current waveform with 250-ns dead time, the bottom graph with 1.5-µs dead time.

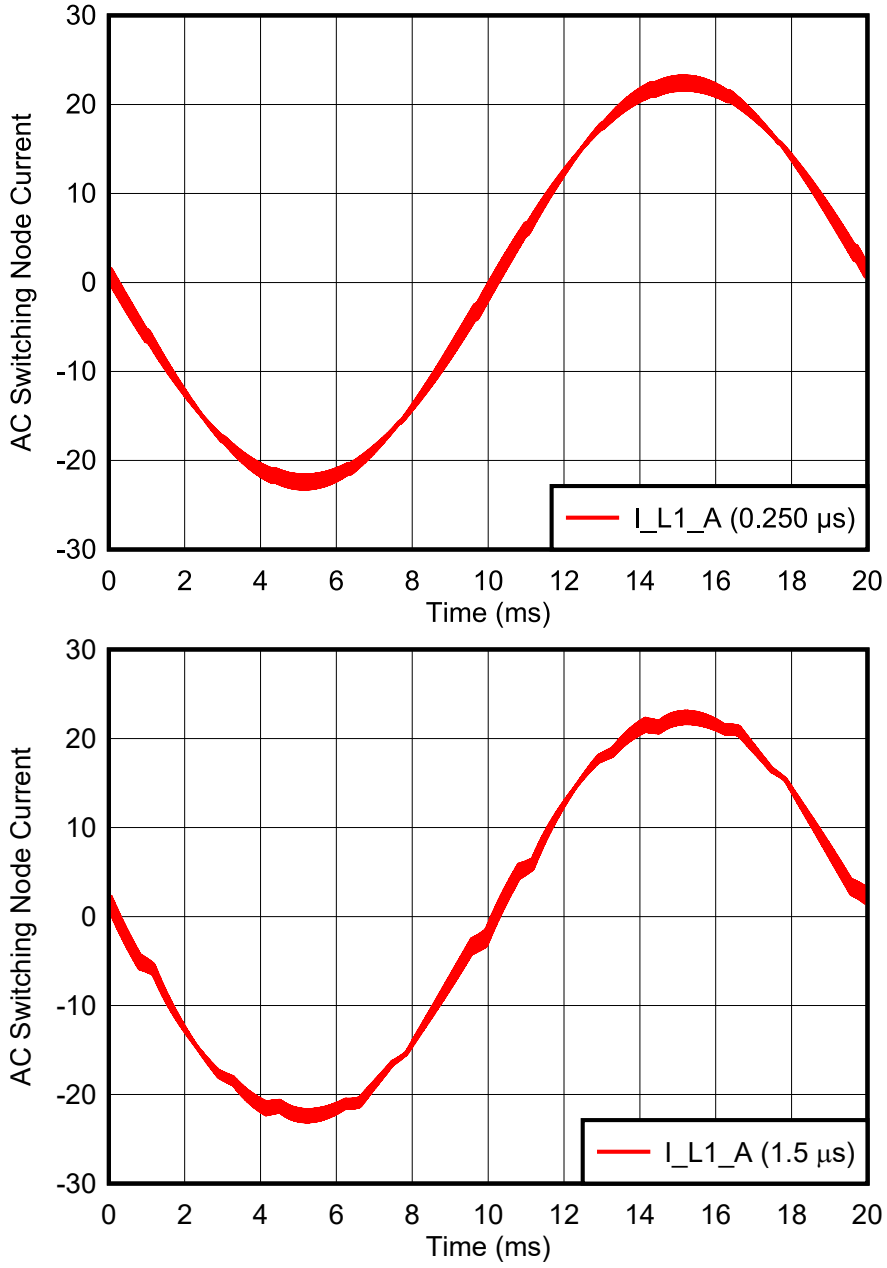


**Figure 2-6. Current Drained From the PCC When a Dead Time of 250ns and 1.5µs are Implemented (50-Hz Operation)**

Excessive dead time can lead to significant THD which exceeds the limits set by the standards. To comply with the standards, either a large output filter is needed or adequate software control must be provided. Multiple control techniques were developed with the aim to compensate this disturbance; however, all these options require sufficient bandwidth of the current sensor. To determine the minimum bandwidth requirements, an fast Fourier transform (FFT) transformation of the current waveform is performed to analyzed the frequency content of the disturbance.

Figure 2-7 shows the results of FFTs of the currents in the PCC when full power is required by the grid.

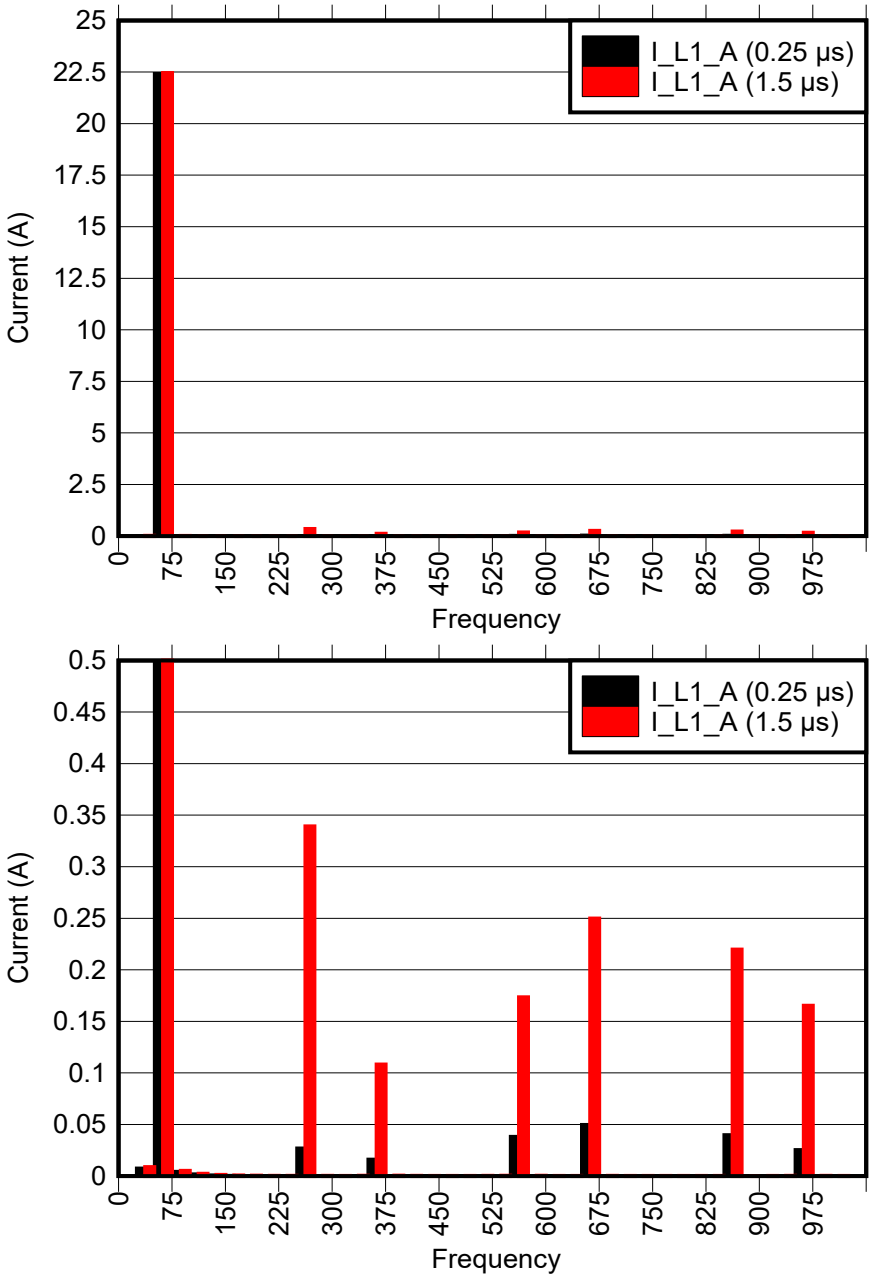


**Figure 2-7. FFT of the Currents Depicted in Figure 2-6 Plus Zoomed Portion (50 Hz)**

The most important frequencies to be compensated in Figure 2-7 are the $5^{th}$, $13^{th}$, and $17^{th}$ harmonics, leading to 250 Hz, 650 Hz, and 850 Hz when the grid is working at 50 Hz. Correspondingly, when the grid operates at 60 Hz the frequencies are 300 Hz, 780 Hz, and 1020 Hz. By applying Equation 3 to the new frequencies, a minimum bandwidth from the current sensing stage of 102 kHz needs to be provided to make sure a proper compensation of the harmonics.

In conclusion, from steady-state analysis, a minimum bandwidth of 102 kHz when having a 60-Hz grid is necessary to improve the total harmonic distortion of the currents when an important dead-time is present in the PFC stage. When the grid is operating at 50 Hz, the minimum bandwidth can be scaled down to 95 kHz. The current sensor bandwidth is required in either point A or B depending where the currents are controlled because harmonic content generated by dead time is the same in both the measurement points. The reason is due to the fact that the EMI filter (see Figure 2-1) is optimized for much higher frequency content; therefore, no important mitigation can be achieved at low frequency.

### 2.2.1.2 Transient Analysis: Step Power and Voltage Sag Response

This section analyzes the performance of the control current loops with the aim of determining the minimum bandwidth of the current-sensing stage when transients caused by the grid are injected. The goal of the study is to find the minimum bandwidth allowed to keep the converter tied to the grid when no major malfunctions are present in the PCC without running in overcurrent protection status. Multiple stress scenarios which can cause overcurrents were analyzed: AC voltage sag, step-power response, and AC overvoltage. Between the mentioned faults, only voltage sag and step-power response are explained.

Figure 2-8 depicts switching node currents (Point B) with respect to grid voltages when a converter operating with sensors has a bandwidth of 6 kHz. In the top graph, the output power of the AC/DC converter is stepped from zero to 11 kW at 3ms, resulting in an overcurrent in L1 (I_L1_B). In the bottom graph, the AC line voltage is dropped by 20% at 26ms, resulting in significant overcurrent in L2 (I_L2_B) that can lead to an unwanted converter shut-down.

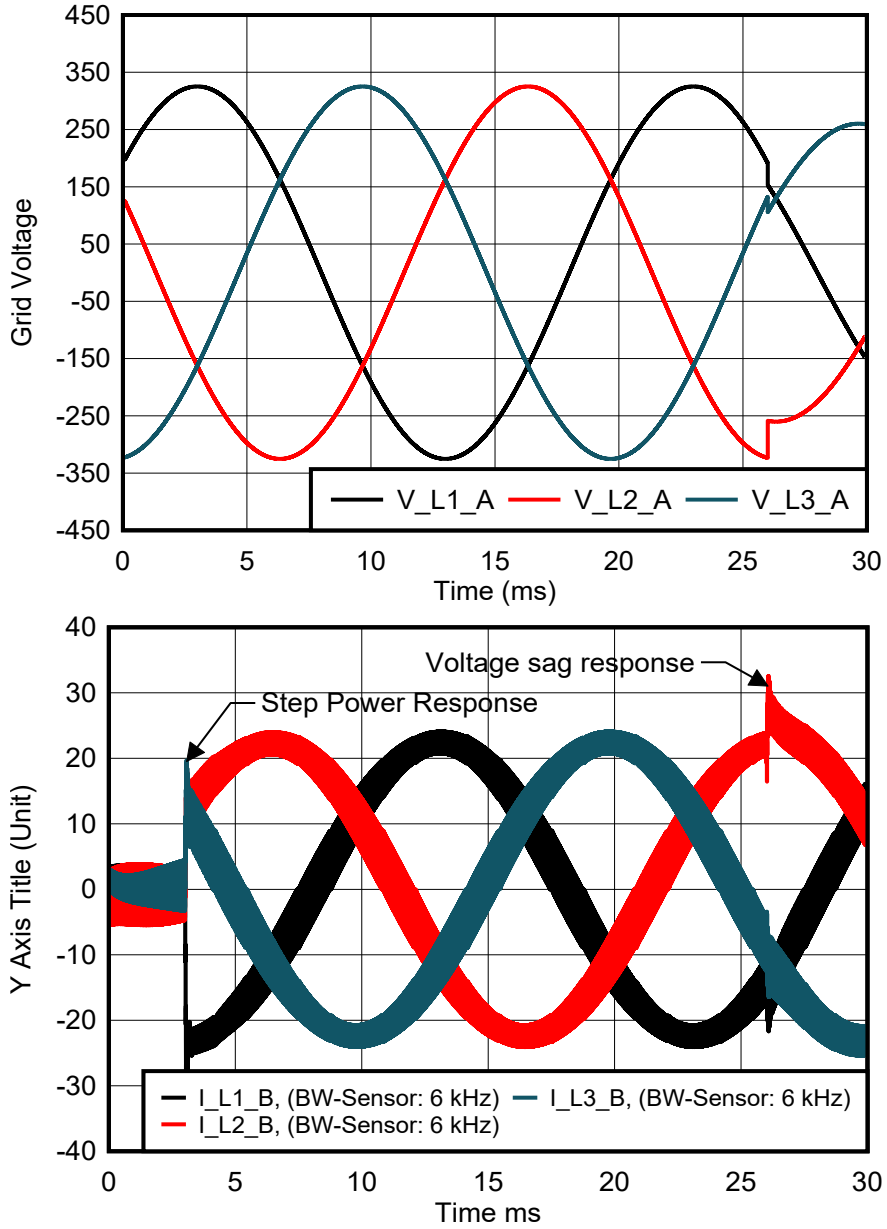


**Figure 2-8. Grid Voltages and Currents of AC/DC Converter: Step Power and Voltage Sag Responses**

Multiple simulations were run by only changing the bandwidth of the current sensor (6 kHz, 30 kHz, 60 kHz), then comparing of the peak overcurrent in the switching node when a step power is requested by the battery.

Figure 2-9 shows the results of the simulations. With a 6-kHz current sensor, the current in L1 overshoots by 30% (33-A peak) relative to the prime transient response that is achieved with a 30-kHz current sensor (10 times higher than the bandwidth of the current control loop). An additional increase in current-sensing bandwidth (from 30 kHz to 60 kHz) brings no additional benefit because both the curves overlap.

Figure 2-9 shows the zoomed-in portion at t = 3 ms (span 200 µs) of the step power response (11 kW) of the AC/DC converter with the current-sensor bandwidth as the parameter.

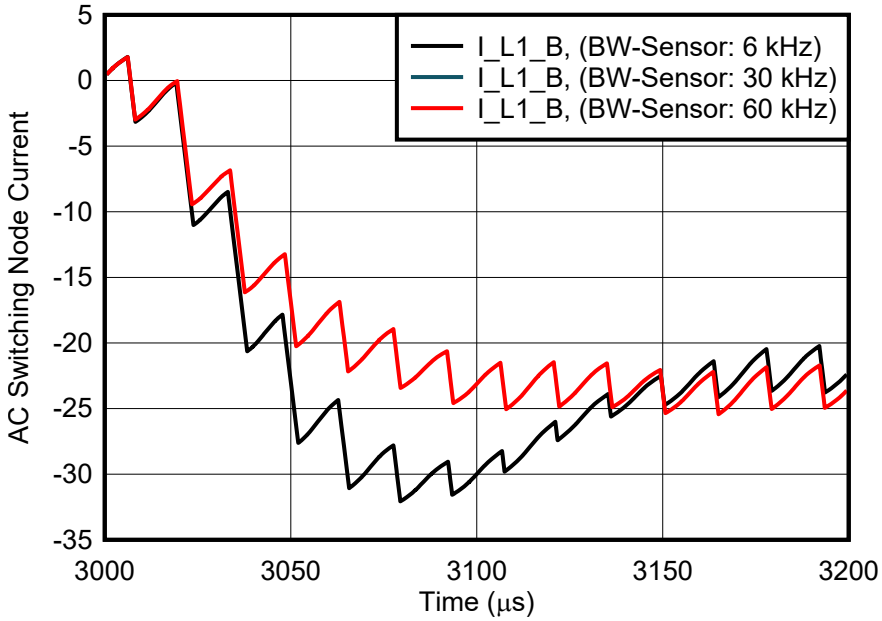


**Figure 2-9. Zoomed Portion at t = 3ms (Span 200µs)**

Multiple simulations were run by only changing the bandwidth of the current sensor. Comparisons of the peak current in the switching node when the converter is working at full load and unpredictable voltage sag on the grid occurs were conducted. Figure 2-10 shows the line-transient response with 6 kHz, 30 kHz, and 60 kHz current sensors. With a 6-kHz current sensor, the current in L2 overshoots by > 2 A (to an approximate 33-A peak) relative to the prime transient response that is achieved with a 30-kHz current sensor (10 times higher than the bandwidth of the current control loop). An additional increase in current-sensing bandwidth (from 30 kHz to 60 kHz) brings no additional benefit (both curves overlap).

Figure 2-10 shows the zoomed-in portion at t = 26ms (span 200µs) of the AC/DC converter voltage sag response with the current-sensor bandwidth as the parameter.

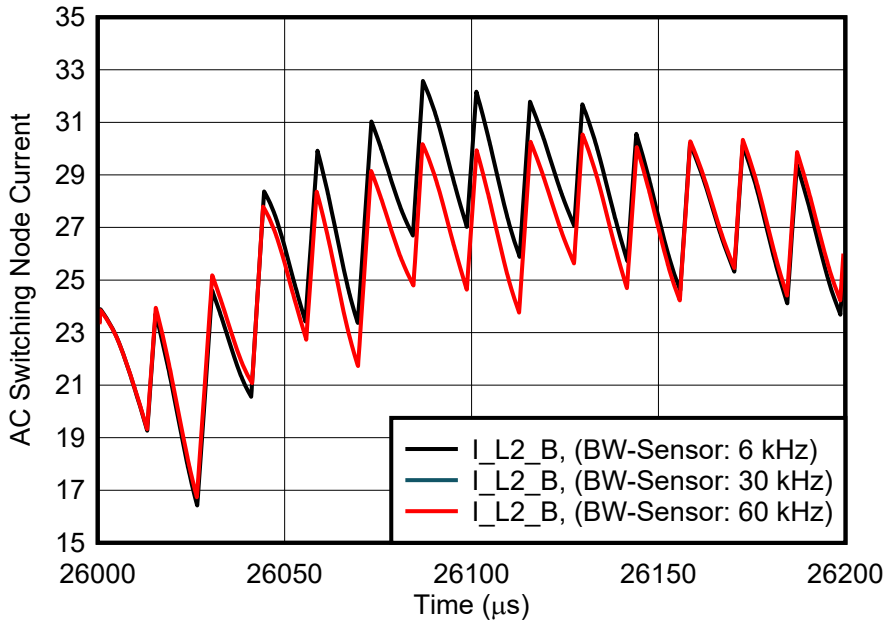


**Figure 2-10. Zoomed Portion at t = 26ms (Span 200µs)**

To take full advantage of the available current control loop bandwidth, keep the sensing bandwidth at least 10 times higher than the control loop bandwidth. By applying this guideline, the resolution of the current measurement is maximized because measurement range does not have to be sacrificed for overcurrent detection.

### 2.2.2 Impact of Latency

The latency is a critical parameter to consider when abnormal operation of the converter or faults from the grid occur. To protect the active power devices, the critical condition needs to be detected as soon as possible to shut the system down immediately and bring the system to a safe condition. The maximum acceptable latency was determined for the sensor located in B to be as close as possible to the power switches. From a multitude of possible faults in the AC/DC stage, only the ones caused by the grid were considered in this section.

#### *2.2.2.1 Fault Analysis: Grid Short-Circuit*

To evaluate the maximum latency required by the AC/DC to shut down safely, system simulations were performed by applying the following conditions:

- DC bus voltage working at the maximum rated voltage (800 V)
- Converter operating at the nominal current (16 $A_{RMS}$)
- Short circuit injected when the maximum current of a phase is drained
- No linear inductance of boost inductors with flux versus current profile of soft-magnetics materials; the inductance versus current is optimized for an 11-kW AC/DC and the inductance decreases down to 30% of the nominal value when saturation is achieved
- The overcurrent threshold of the current sensing in point B is set up at 30 A (93.7% of measurement range)
- Based on available data sheets of power components used in 11-kW applications, a maximum-allowed current of 60 A was selected

When a short-circuit is happening in the grid the converter is still switching, thus leading to uncontrolled currents. Since the fault is happening suddenly, there is not enough time for the MCU to update and correct the duty cycles. PWM updates typically happen at a fixed frequency (70 kHz or every 14.2µs in this example). By following single and double update refresh techniques, the minimum reaction time of the MCU can be 1/fs or 1/2fs. Within this time, the current in the inductor can exceed the short-circuit current rating of the power switch.

Figure 2-11 depicts the voltage and currents of the AC/DC converter. Figure 2-11 shows that in the time frame between 0ms and 19ms, the converter is operating at the nominal condition with a grid voltage equal to 400 $V_{RMS}$ and a current transferred from the DC to the AC. At 19ms, a short-circuit event is simulated by dropping the phase voltage to 10% of the nominal value. Simultaneously to the grid fault, the currents in the switching

node start to increase due to the voltage difference between the grid and the applied one from the switching stage, as shown in Figure 2-12.

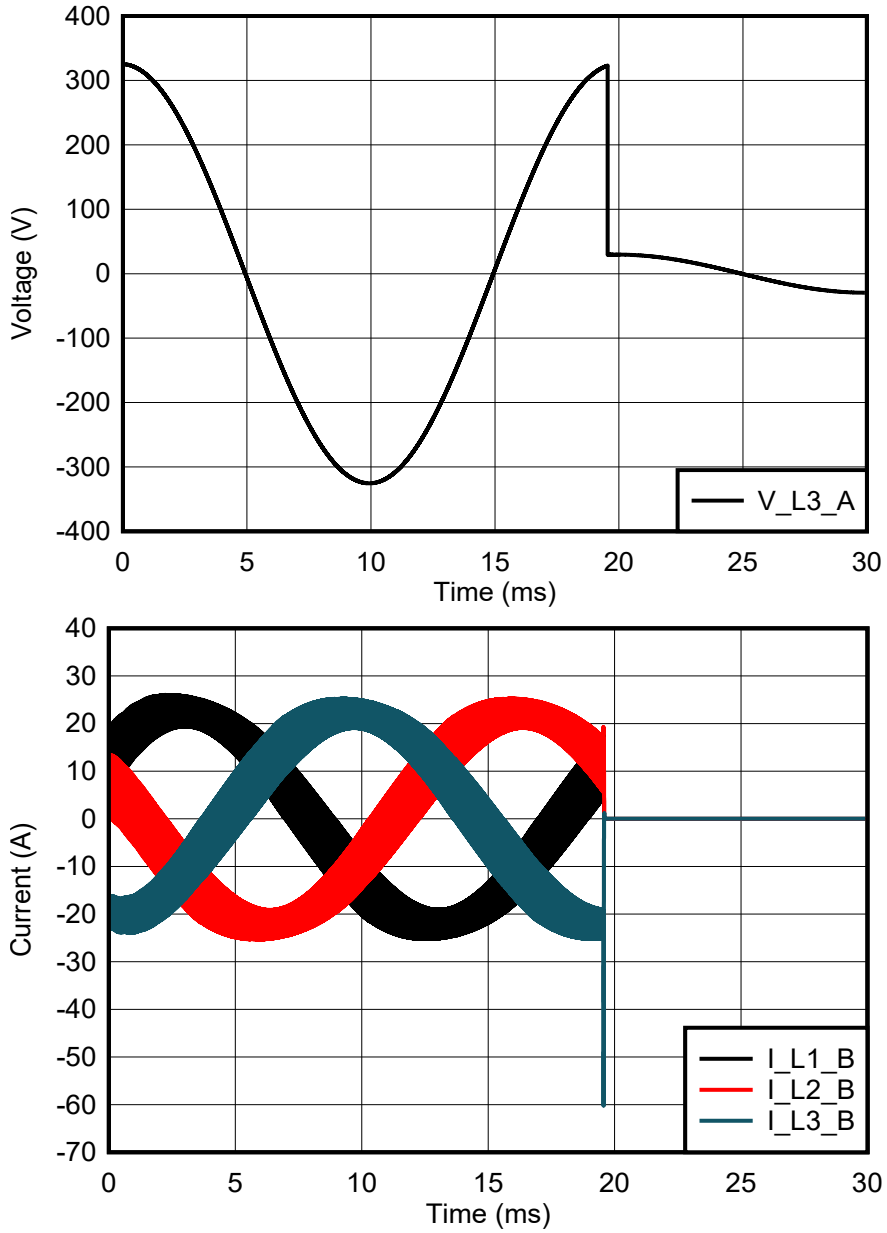


**Figure 2-11. Grid Voltages and Currents of AC/DC Converter: Short-Circuit Response of the AC/DC Converter**

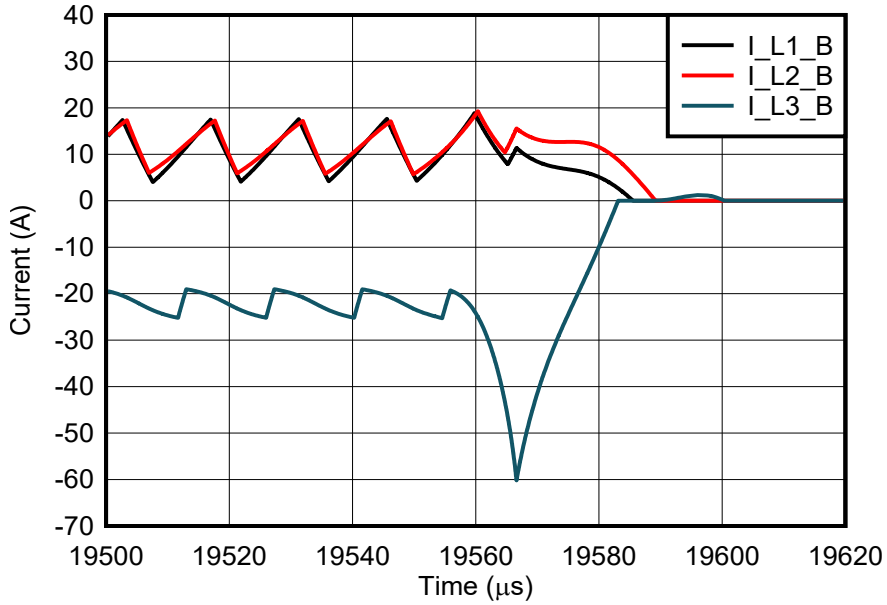


**Figure 2-12. Zoomed-in Portion at t = 19.5ms (Span 120µs): Short-Circuit Response of the AC/DC Converter**

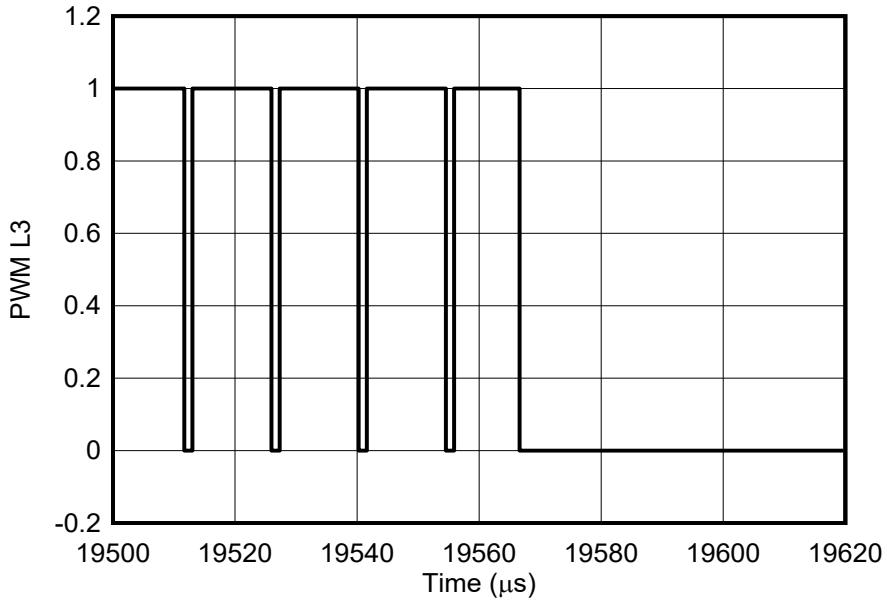


**Figure 2-13. Zoomed-in Portion of PWM at t = 19.5ms (Span 120µs): PWM Turn-off Behavior**

At the beginning, the current start-to-rise linearly is because the core is not saturated and is following a fixed di/dt since the inductance is nearly constant:

$$di/dt = V_{DC}/(1.5L(i)) \quad (4)$$

where

- L is the AC/DC boost current in function of the current
- $V_{DC}$ is the DC bus voltage at the moment of the fault

When the saturation current of the core is reached, the inductance value drops significantly, leading to a sudden increase of the current. When the real current in phase L3 reaches 30 A (overcurrent threshold), the MCU must be able to detect the overcurrent as soon as possible, since the MCU cannot detect higher currents, and shuts

down before the current reaches a level above 60 A. Based on the simulation results, the current takes 4µs to reach the critical value. After this timing is reached, turn off the PWM signals as shown in Figure 2-13.

In conclusion, the system must turn off within 4µs to avoid damage to power switches. Consider the latency of the current sensing together with those of the MCU and driver stage shut down. Based on typical values of latency time of the MCU and driver stage, a maximum latency of 3.5µs must be provided by the current sensor.

### 2.2.3 Impact of Gain Error

Figure 1-2 depicts the equivalent model of the current sensor by showing the presence of a gain error block. In this study, gain error is modeled as a fixed value as represented in Section 1.2.2.

#### *2.2.3.1 Power Disturbance in AC/DC Caused by Gain Error*

The goal of the current control loops of the AC/DC stage is to keep the currents detected by the MCU under control without determining the real currents in the system. If the measurement does not match the reality, there is an unwanted power disturbance in the system caused by the gain error, which is expressed in Equation 5.

$$\Delta P_{GAIN} = 0.5\ VI[(\varepsilon_1 + \varepsilon_2 + \varepsilon_3) + (0.5(\varepsilon_2 + \varepsilon_3) - \varepsilon_1)\cos(2\omega t) + (0.87(\varepsilon_2 - \varepsilon_3))\sin(2\omega t)] \quad (5)$$

where

- ΔP is the power disturbance caused by the gain errors in function of time, where this power is drained from the grid toward the DC link
- $\varepsilon_1$, $\varepsilon_2$ and $\varepsilon_3$ are the relative gain errors of each current-sensing stage
- V is the phase-to-neutral RMS voltage
- I is the RMS current controlled by the converter
- ω is the electrical pulsation derived from the grid frequency

The power disturbance is a function of the converter power between the AC and DC stage and reaches the maximum when the maximum power is requested by the AC/DC converter. Furthermore, Equation 5 can be divided in two parts as in Equation 6 and Equation 7.

$$P_{GAIN\_DC} = 0.5\ VI[(\varepsilon_1 + \varepsilon_2 + \varepsilon_3)] \quad (6)$$

$$P_{GAIN\_AC} = 0.5\ VI[(0.5(\varepsilon_2 + \varepsilon_3) - \varepsilon_1)\cos(2\omega t) + (0.87(\varepsilon_2 - \varepsilon_3))\sin(2\omega t)] \quad (7)$$

where

- $P_{GAIN\_DC}$ represents the presence of a fixed power disturbance drained by the PFC during the operation
- $P_{GAIN\_AC}$ represents a power ripple at double the grid frequency exchanged with the grid

Impacts of these power disturbances in the DC and AC sides are investigated by observing the voltage control loops together with the imperfection that was detected.

#### *2.2.3.2 AC/DC Response to Power Disturbance Caused by Gain Error*

Figure 2-14 shows a generic voltage controller and equivalent model of the power plant.

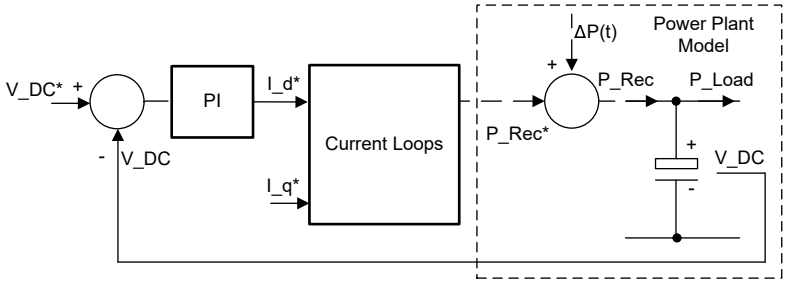


**Figure 2-14. Simplified DC Bus Voltage Control Loop With Power Plant Model**

As Figure 2-14 shows, the term derived analytically before (Equation 5 ) was introduced in the loop as a disturbance to check the voltage control performance. By observing the control loop topology, it can be demonstrated that, thanks to the presence of an integrative part of a PI controller, the steady-state error caused

by the DC disturbance Equation 5 is completely rejected. Conversely, the AC component of the disturbance cannot be rejected completely, thus leading to a voltage ripple.

To evaluate the maximum acceptable gain error of a current sensor used in the AC side, simulations were run by applying the following hypothesis:

- DC bus voltage working at the minimum rated voltage to maximized the ripple voltage (650 V)
- Maximum power exchange between the AC and DC side, thus increasing the power disturbance (11 kW)
- Gain error for the three phases applied to reach the worst-case scenario, as follows: $\varepsilon_1 = -\varepsilon_2 = -\varepsilon_3$;
- Current control loop bandwidth kept constant in all the simulations (3 kHz)
- The AC filter is designed to keep the THD below 3% at the nominal output power when using prime current sensing
- The power line frequency is 50 Hz

Figure 2-15 shows simulation results of an AC/DC converter working with sensors having different gain error.

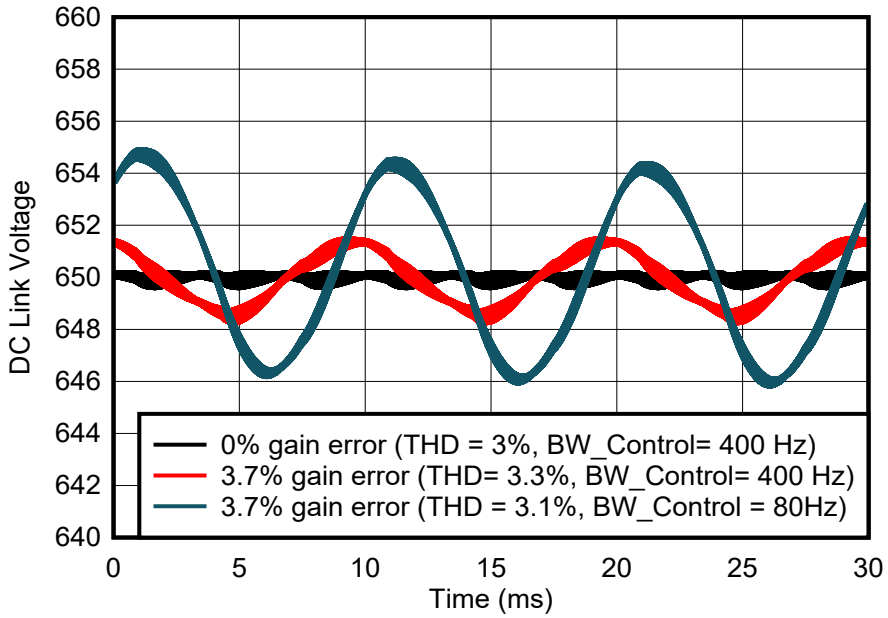


**Figure 2-15. DC Link Voltage Ripple Over Time With DC Link Bandwidth and Gain Error as Parameters**

The following results are present in Figure 2-15:

1. A 100-Hz ripple voltage on the DC-link. This is caused by the power ripple injected by the gain error of a current sensing stage.
2. The mean value of the voltage in all the cases is still the same when steady state is reached thanks to the integrative part of the PI controller, as confirmed by the theory.
3. The DC-link voltage ripple is correlated to the bandwidth of the DC-link voltage control loop. If the bandwidth of the voltage control loop is high enough, the controller tries to eliminate the ripple voltage by controlling very fast the current loops at the expense of grid THD.

In this example a 400-Hz bandwidth of the voltage control loop, paired with 3.7% gain error of the current sensor, leads to a THD of 3.3 % compared to a 3% THD with an ideal current sensor without gain error. Alternatively, a low bandwidth of the voltage control loop leads to low THD on the grid-side but the ripple voltage on the DC link can increase to an unacceptable level. Having a voltage ripple in the DC link can lead to power ripple on the battery which cannot be tolerated. Furthermore, low voltage control loop bandwidth leads to poor load-step response.

In conclusion, a current sensor located in the switching node with a gain error of 3.7% can lead to an increment of the grid current THD of more than 10%. To compensate for this increase, the input filter has to grow by more than 4% in volume to meet the design goal of < 3% THD at the grid-side of the converter.

### 2.2.4 Impact of Offset

Figure 1-2 shows the equivalent model of a real current sensor with offset. In this study, the current-sensor offset is modeled as a fixed-value normalized to the full scale of the measurement, see Equation 8.

$$I_O = I_{MAX} \quad \delta_O \tag{8}$$

where

- $I_0$ is the absolute offset value presented by the sensor
- $I_{MAX}$ is the maximum of the measurement scale
- $\delta_0$ is the per-unit value of the offset error introduced in the measurement

The goal of the current control loops of the AC/DC stage is to keep the currents detected by the MCU under control without determining the real currents in the system. If the measurement does not match the actual current due to an offset error, the current causes an undesired power disturbance in the system as is expressed with Equation 9.

$$\Delta P_O = V\left[I_{O1}\sin(\omega t) + I_{O2}\sin\left(\omega t - \tfrac{2}{3}\pi\right) + I_{O3}\sin\left(\omega t + \tfrac{2}{3}\pi\right)\right] \tag{9}$$

where

- $\Delta P_O$ is the power disturbance caused by the offset errors as function of time
- $I_{O1}$, $I_{O2}$, and $I_{O3}$ are offset errors of each current sensor
- V is the phase to neutral RMS voltage
- ω is the electrical pulsation derived from the grid frequency

The power disturbance is not a function of the power conversion between the AC and DC stage, as opposed to the gain error case; therefore, the issue is always present for any operating condition. This reflects by always having voltage ripple in the DC link. The offset introduces a power disturbance in the system with a frequency equivalent to the line frequency of the grid. As mentioned in the gain error chapter, the DC bus voltage loop is not able to fully reject the power ripple coming out from the sensing point. For this reason control loop versus current-sensing performance must be simulated. Simulations were run for the following use-case and assumptions:

- DC bus voltage working at the minimum rated voltage to maximize the ripple voltage (650 V)
- Maximum power exchange between AC and DC side. This has no effect on the result. The results are the same for the no-load condition.
- Offset error defined with respect to the full measurement scale per unit. When using a shunt-based design with ±50-mV isolated device, the maximum scale is ±32 A.
- Offset for the three-phases applied to reach the worst-case scenario as follows: $I_{O1} = -I_{O2} = -I_{O3}$
- Current control-loop bandwidth kept constant in all the simulations (3 kHz)
- AC filter designed with the aim to keep the grid THD at the nominal power at 3% when using ideal sensing
- Power line frequency is 50 Hz

Figure 2-16 shows the simulation results of a AC/DC converter working with different current sensing and with different offset errors.

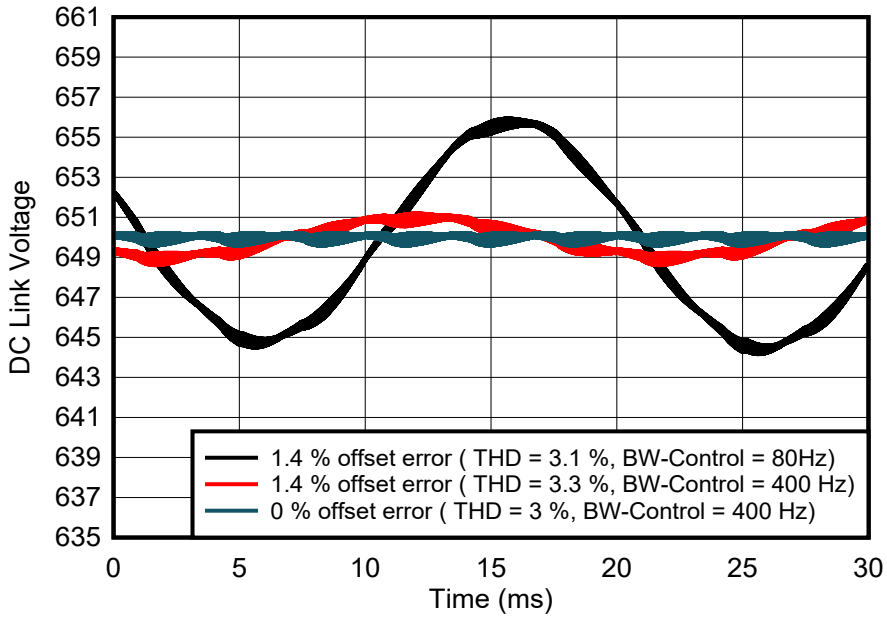


**Figure 2-16. DC-Link Voltage Ripple Over Time With DC Link Bandwidth and Offset Error as Parameters**

Observe the presence of a 50-Hz ripple voltage on the DC-link, caused by the power ripple injected by the current sensing stage with an offset. Additionally, the mean value of the voltage in all the cases is still the same when steady state is reached thanks to the integrative part of the PI controller.

The important correlation between the DC link voltage ripple and voltage control bandwidth is evident. If the bandwidth of the voltage control loop is high enough, the control loop tries to eliminate the ripple voltage by quickly controlling the current loops at the expense of the THD toward the grid. In fact, with a bandwidth of the control equal to 400 Hz, an offset of 1.4% offset error, leads to an increment of 10% of the THD (from 3% to 3.3%). Conversely, when the bandwidth of the voltage loop is not high, fluctuation in the DC link is very high because voltage loop is not trying to reject this variation, but this time not injecting any more harmonics in the grid. However, remember that having a voltage ripple in the DC-link can lead to power ripple on the battery which cannot be tolerated. Furthermore, if the voltage bandwidth is significantly reduced, the performance of the step load response becomes quite poor.

In conclusion, a current sensor located in the switching node with an offset error of 1.4% can lead to an increment of the grid current THD of more than 10%.

## 2.3 Point C and D – AC/DC DC Link Current Sensing

This chapter provides the design considerations of current sensors used in the DC link for AC/DC converter.

Current sensors in the DC link are not mandatory for the basic functionality of the power conversion but sensors can be used for implementing features such as power measurement, protection and feedforwards for the voltage loop.

Sensing in the DC-link can be placed in point C or point D, before and after the DC-link capacitors used for PWM ripple frequency filtering and energy storage (Figure 2-1), respectively.

Offset, bandwidth, accuracy, and latency of current sensors are discussed at a system level base with the goal of determining the minimum requirements for each of the desired additional functions. Not all scenarios are discussed for both points C and D as many cases turned out to be a repetition, only the worst-case scenarios were analyzed to determine current sensor requirements. Details about each analysis follows:

- **Gain Error**: impact of gain error is the same in both C and D points. Minimum gain error required by this sensor needs to be evaluated for power measurement and feedforwards.
- **Offset Error**: impact of gain error is the same in both C and D points. Minimum offset error required by this sensor needs to be evaluated only for power measurement. Offset error is not critical for the feedforward since the error is compensated out from the integrative part of the DC bus voltage PI controller.

- **Minimum Bandwidth**: impact of bandwidth is the same in both C and D points. Bandwidth is required for the feedforward application, and most effective when placed in point D.
- **Maximum Latency**: Low latency is important for protecting the active switches of the power-stage, so it is evaluated for point C, the closest point to the active switches.

### 2.3.1 Impact of Bandwidth on Feedforward Performance

To evaluate the minimum bandwidth required of a current sensor located in position D, when used for feedforward, system simulations were executed by applying the following conditions:

- DC bus voltage working at the minimum rated voltage (650 V)
- Step power applied on the DC-link of 11 kW
- Grid operating at 400 $V_{RMS}$

Simulations were performed to compare load transient performance with and without feedforward. Figure 2-17 shows the results. Without feedforward, the DC-link voltage drops significantly when the load is applied, leading to possible unstable converter operation. With feedforward, performance is drastically improved and the load transient response is reduced by a factor of 5. Conversely, the simulation results show how this additional sensor, in addition to the possibility to measure the power on the DC rail, is very useful when deployed with the load which connects and disconnects without giving a warning.

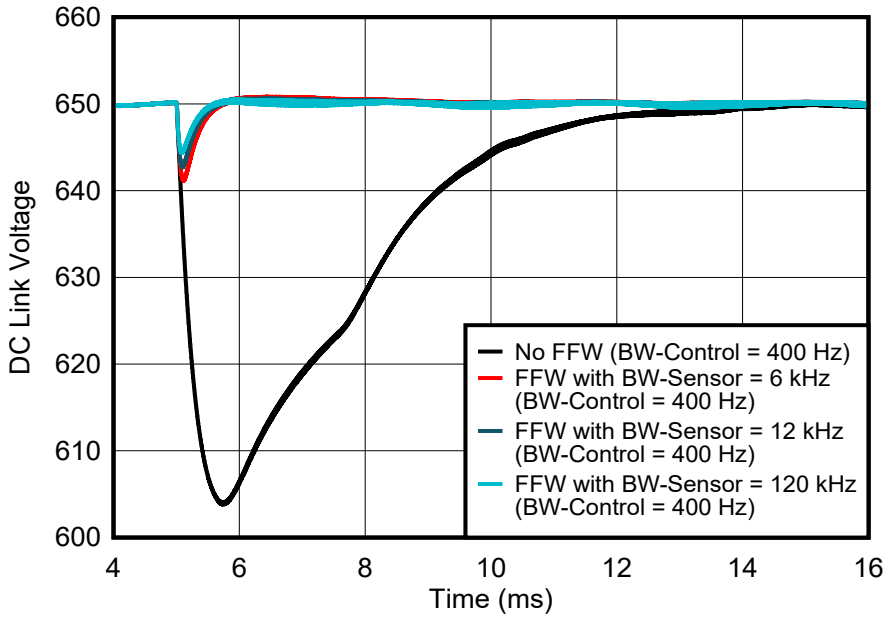


**Figure 2-17. DC-Link Voltage Response to Step Power With DC-Link Bandwidth as Parameter, With and Without Feedforward**

Figure 2-18 shows that the bandwidth of the current sensor only plays a minor role in the performance improvement since the overall bandwidth is limited by the dq current loop.

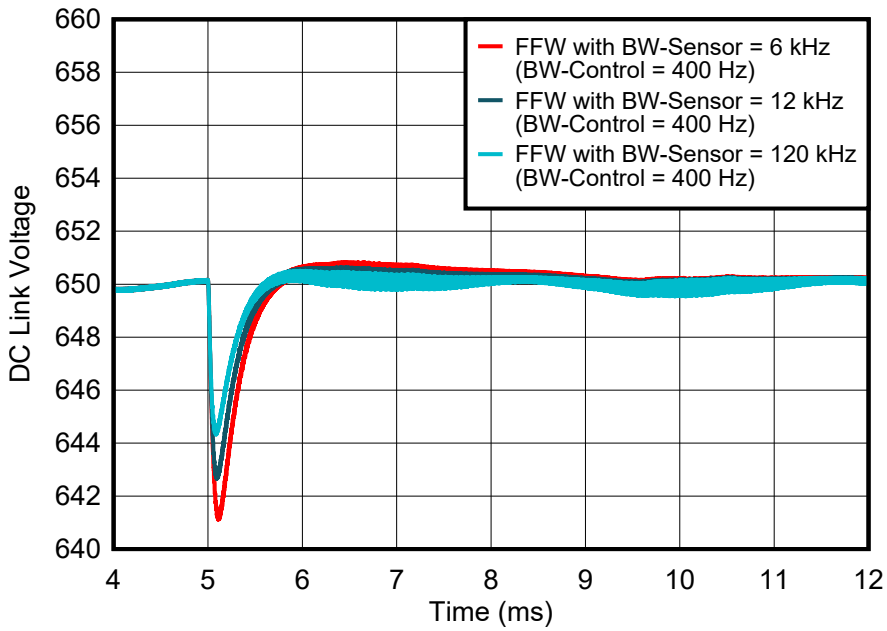


**Figure 2-18. DC-Link Voltage Response to Step Power With DC-Link Bandwidth as Parameter, With Feedforward**

In summary, when placing a current sensor in point D for feedforward purposes, a low bandwidth of < 10 kHz is sufficient. In general, the bandwidth of the current sensor needs to be at least two times higher than the bandwidth of the current loop.

### 2.3.2 Impact of Latency on Power Switch Protection

Maximum latency of the sensing stage needs to be evaluated only for point C, since point C is the closest one to the power devices. The position of this sensor allows detection of both overcurrent and short circuits but at the cost of increasing the parasitic inductances in the loop. Detection latency must be shorter than the short-circuit withstand time of the power switch and therefore depends on the switch technology. The following numbers are guidelines only. To make sure of the withstand time, refer to the device data sheets:

- SiC MOSFET: maximum latency of 1–3µs
- IGBT: maximum latency of 2–10µs
- GaN FETs < 3µs

In addition to the latency of the overcurrent sensor, the delay of the input filter, the response time of the MCU, and the turn-off-delay of the gate driver needs to be considered. To achieve an effective turn-off delay < 1.5µs, the latency of the overcurrent sensor must be < 1µs. TI offers a line of isolated comparators with latencies < 300ns that are specifically designed for this application.

### 2.3.3 Impact of Gain Error on Power Measurement

#### *2.3.3.1 Transient Analysis: Feedforward in Point D*

To evaluate the impact of the gain error of a current sensor on the performance of the feedforward, simulations were performed for the following operating condition:

- DC bus voltage working at the minimum rated voltage (650 V)
- 11-kW load step is applied to DC-link as t = 1ms
- Grid voltage is 400 $V_{RMS}$

As Figure 2-19 shows, with an increment in the gain error in point D has only deteriorate slightly. This demonstrates that gain error is not a critical parameter when considering feedforward applications.

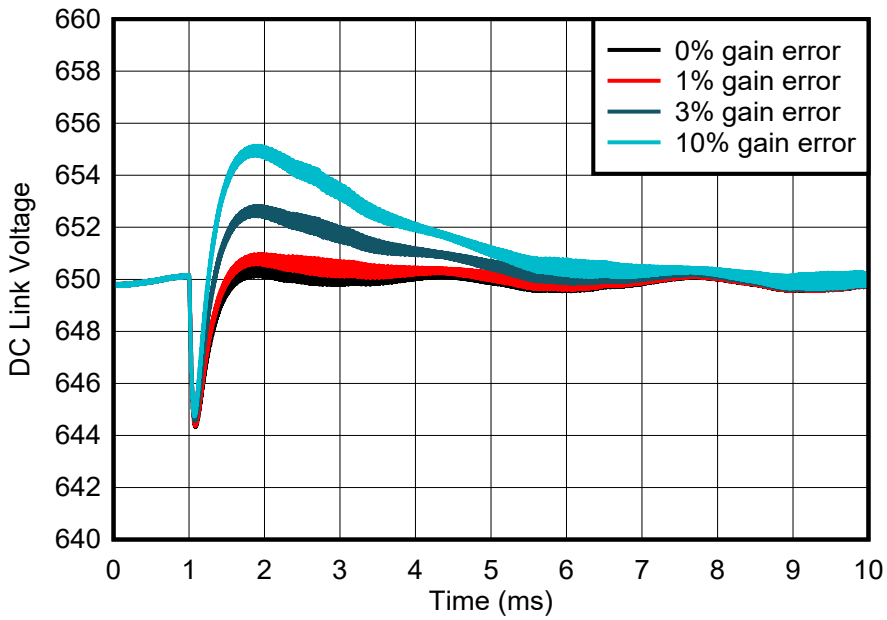


**Figure 2-19. DC-Link Voltage Response to Step Power With DC-Link Gain Error as Parameter, With Feedforward**

In summary, gain error in the DC-link current sensor has a minor effect on the overall transient load-step performance and gain errors up to 3% still achieve acceptable performance.

### 2.3.4 Impact of Offset

Offset of the sensing stage can only affect steady state. In dynamic applications, where the sensing is used for creating a feedforward, the voltage loop compensates automatically for the error introduced by the offset.

## 2.4 Summary of Positives and Negatives at Point A, B, $C_{1/2}$ and $D_{1/2}$ and Product Suggestions

Power switches are the most sensitive components that can be damaged by overload or overcurrent. The close proximity of power switches allows faster fault detection, leading to have sensing in B and C vitally important. For point B, the high-side power supply of the isolated amplifier can be shared with the high-side gate driver supply and fast overcurrent (OC) detection is possible. The current sensing at point B needs to be able to handle high Common Mode Transient Immunity (CMTI) and this measurement can get affected by noise during power-stage switching, in particular when GaN or SiC designs are adopted. The precise reactive power control is the best possible at point A, where the measurement is behind the filter far away from switching noise. The drawback is the requirement of an isolated power supply at point A. Only slow OC detection is possible. Table 2-1 summarizes the pros and cons of the various current-sensing points. Table 2-2 summarizes requirements and provides an excellent choice of products for each point.

**Table 2-1. Positives and Negatives of the Current-Sensing Points A, B, $C_{1/2}$, and $D_{1/2}$**

| | A | B | C1 | D1 | C2 | D2 |
|---|---|---|---|---|---|---|
| Accurate power regulation | (+)(1) | (–) | (+) | (+) | (++) | (++) |
| Feedforward loop | N/A | N/A | (–) | (–) | (+) | (+) |
| Fault protection | (–) | (++) | (++) | (+) | (–) | (–) |
| Sharing of power supply | (–) | (+) | (+) | (–)(2) | (+) | (–)(2) |

(1) Precise reactive power control at PCC is possible – accuracy to be defined by the manufacturer (often < 1%)
(2) $D_1$ and $D_2$ need a floating supply above VDC+

**Table 2-2. AC/DC Minimum Requirements and Available Products for Current Sensing at Points A, B, $C_{1/2}$, and $D_{1/2}$**

| I-Sensing Point | Primary Applications | Iso-Supply Voltage | Minimum Bandwidth | Maximum Latency | Requested CMTI | Minimum Accuracy(1) | TI Products (ISO-)AMP\| ISO-ΔΣ |
|---|---|---|---|---|---|---|---|
| A | Able to adjust precisely reactive power | Floating needed (ISO-VDD1) | > 102 kHz | - | Low | < 3.7 % | AMC3302\| AMC3306M05 |
| B | Overcurrent protection and control | From upper gate driver | > 102 kHz | < 3.5 µs | High | < 3.7 % | AMC1302 \| AMC1306M05 \| AMC23Cxx |
| C1 | Current in neg branch and fault detection | From lower gate driver | - | < 1.5 µs | Low | <1 % | AMC1302 \|AMC1306M05 \| AMC3302 \| AMC23Cxx\| AMC22Cxx |
| D1 | Current in positive branch and fault detection | Floating above VDC+ needed | - | < 1.5 µs | Low | <1 % | AMC3306M05 \|AMC3302 \| AMC23Cxx\| AMC22Cxx |
| C2 | Current in neg branch and fault detection | From lower Gate Driver | > 6 kHz | - | Low | <1 % | AMC1302\| AMC1306M05\|AMC3302 |
| D2 | Current in positive branch and fault protection | Floating above VDC+ needed | > 6 kHz | - | Low | <1 % | AMC3302\| AMC3306M05\| AMC23Cxx\| AMC22Cxx |

(1) 1% accuracy is only required in cases where it is necessary to measure the power precisely. 3% is sufficient for systems that do not require accurate power control.

# 3 Current Sensing in DC/DC Converters

There are many implementations for DC/DC converters applicable to be used for EV charging applications. Typically, an isolated architecture is chosen. Two topologies that are used frequently as bidirectional topologies are *Dual Active Bridge with Phase Shift Control* and *Dual Active Bridge in Resonant CLLLC* configuration. Both topologies are explained in detail and how to implement current sensing in the topologies are discussed in the next sections.

## 3.1 Basic Operation Principle of Isolated DC/DC Converter With Phase-Shift Control

Figure 3-1 shows a typical control loop of a phase-shift dual active bridge (DAB) DC/ DC converter. There are two control loops in this system: (a) an outer voltage loop and (b) an inner current loop.

For the voltage loop, the output voltage is fed into an ADC of a MCU (denoted as $V_{fb}$) in Figure 3-1. $V_{fb}$ is compared with a reference voltage (denoted as $V_{ref}$). The error between the measured voltage and reference voltage is fed to a compensator, which can be realized as a PID controller. The output of the voltage loop is used as reference ($I_{ref}$) for the inner current loop. The compensator of the inner current loop ($G_I$) compares the reference ($I_{ref}$) and actual value of sensed current ($I_{OUT}$) and uses this error to adjust the phase of a PWM waveform to the leading or lagging bridge depending on the direction of the current. For constant current charging, the voltage loop is optional or can be implemented for protections only. For constant power charging, both loops are needed. The theoretical limits for the phase shift are ±π, practical implementations are much smaller than this.

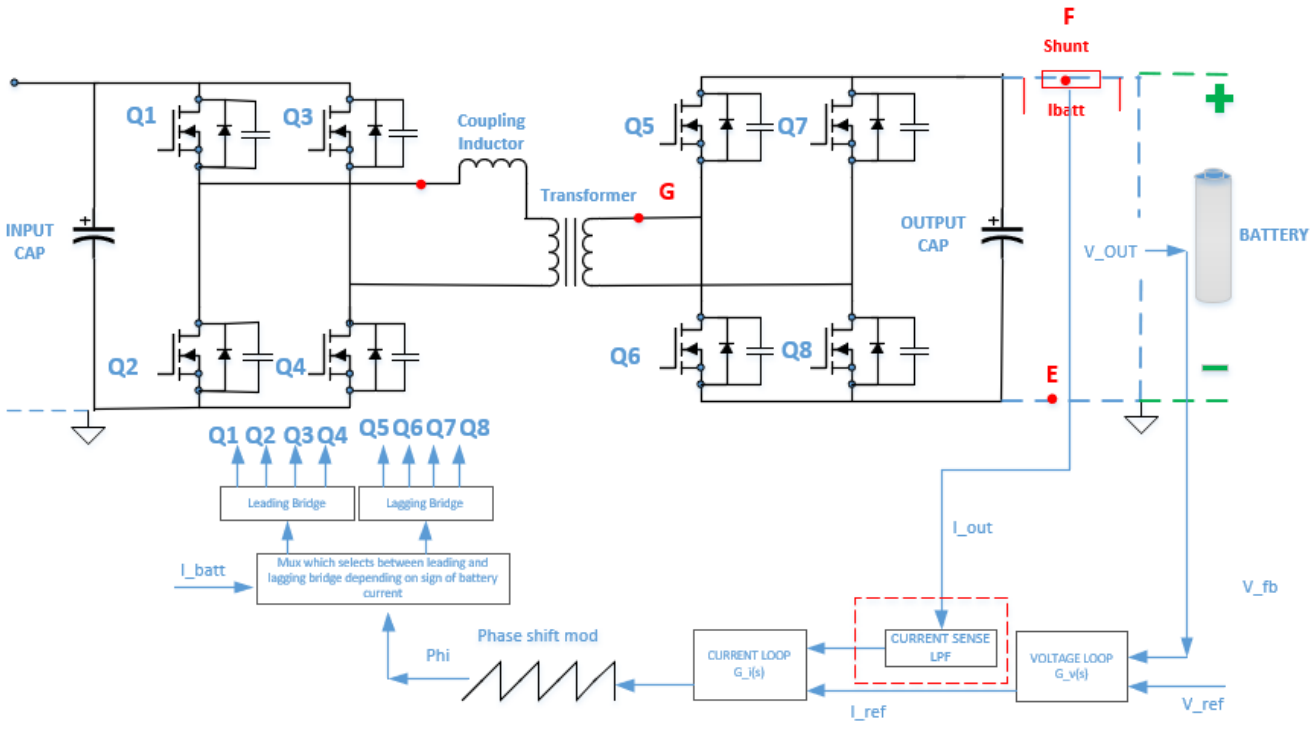


**Figure 3-1. Typical Control Loop of Dual Active Bridge (DAB) DC/DC Converter With Phase-Shift Control**

## 3.2 Point E, F - DC/DC Current Sensing

This section covers the output current sensing of the DC/DC stage. There is an option to place the current sensor at the negative battery connection (point E) or at positive battery connection (point F) as shown in Figure 3-2. Both options are equivalent from the control-loop regulation perspective. For point F, the power supply for the current sensor is floating above VBAT+ whereas for point E, the supply can be derived from the lower gate driver.

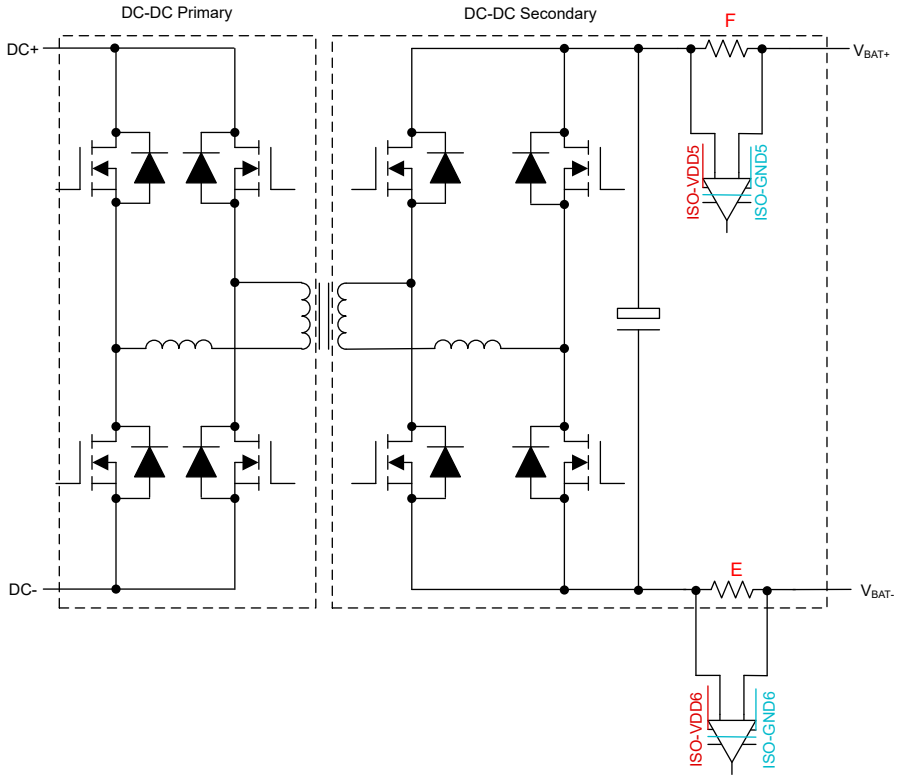


**Figure 3-2. Current-Sensing Point E, F**

To assess the impact of gain error, offset error, and bandwidth of the current sensor on the performance of the DC/DC converter, the model shown in Figure 1-2 was used for simulations.

### 3.2.1 Impact of Bandwidth

In this simulation, the dual active bridge with phase shift control is running at a switching frequency of 100 kHz and is configured as constant current source output that drives a fixed current of 20 A into a pure resistive 10-Ω load (that results in a 200-V DC output, representing a 4-kW load).

At time t1 = 2ms, the load is changed from 10 Ω to 20 Ω. This results in an immediate current change down to 10 A (since voltage is 200 V at that time). After some time, the control loop starts to regulate back to the 20-A constant current which forces the output voltage to increase to 400-V DC when settled (resulting in a load change from 4 kW to 2 kW). Figure 3-3 shows the transient response of the output current.

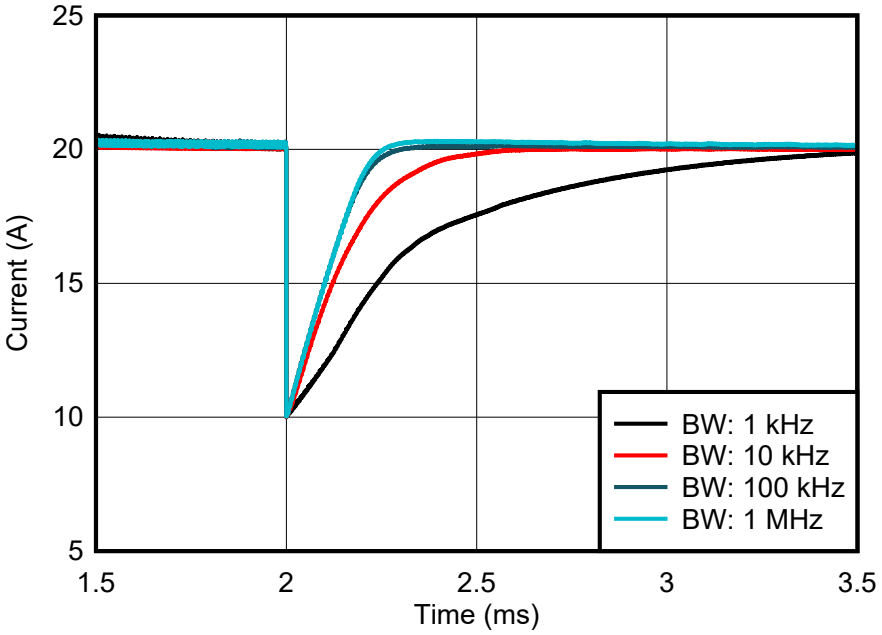


**Figure 3-3. DC/DC Step Load Response vs Current Sensor Bandwidth**

Figure 3-3 shows the response to the same load step for different bandwidth settings or the current sensor in the control loop. With a current sensor bandwidth of only 1 kHz, there is a long settling time of 1.6 ms. Increasing the bandwidth to 10 kHz and 100 kHz, brings the settling time (90% of end value) down to 0.6ms and 0.3ms, respectively. A further increase of current-sensor bandwidth does not improve the transient response significantly because the settling time is limited by the control-loop bandwidth of the current loop which was set to 10 kHz.

In conclusion, a current sensor at point E or F with a bandwidth lower than 100 kHz is sufficient to keep the settling time < 1ms for any load step change at the converter output.

### 3.2.2 Impact of Gain Error

Current sensors have gain error that may impact on the accuracy of the control loop. A simulation with the current sensor model from Figure 1-2 is performed to study the settling time at turn-on of the converter. The bandwidth of the sensor is set to 100 kHz and gain errors of 0%, 1%, and 2% are chosen. Figure 3-4 show the impact of the errors.

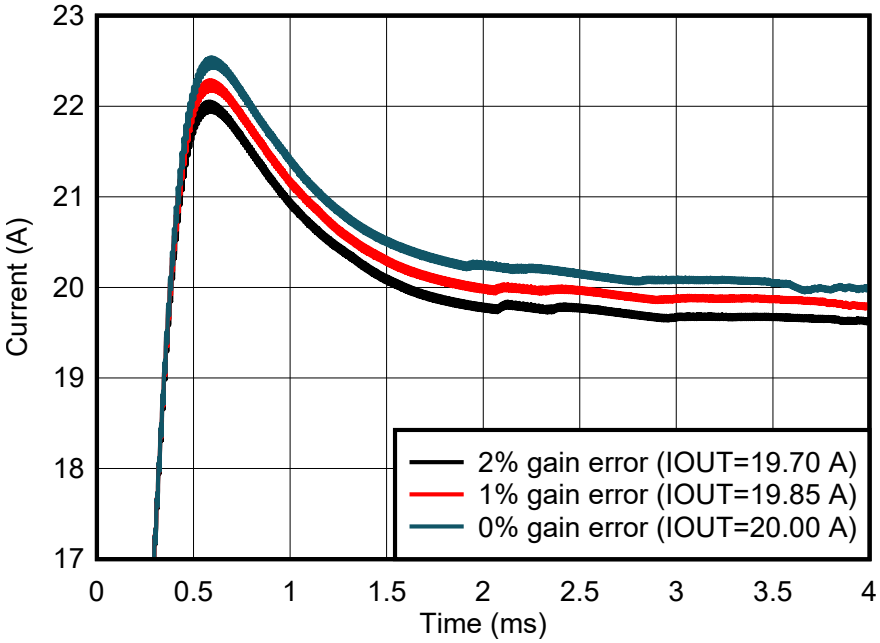


**Figure 3-4. Steady State Output Current Errors vs Current Sensor Gain Errors**

Settling time after a load change is quite similar since the bandwidth of the sensor is defining the settling time for all cases, meaning the gain error does not impact settling time significantly. But the gain error impacts the value to which the output current settles. This simulation shows that the remaining constant error at the output current is about 0.66% (about 0.15 A) below the ideal 20 A if the current sensor has gain error of 1% (about 1.33% / 0.32 A below the ideal 20-A output current if the current sensor has a gain error 2% respectively).

The gain error is defined as the error relative to full-scale of the current. In our example the full-scale current is 32 A. This means for a 20-A current, the resulting gain error is only about two thirds of the full-scale (about 0.66%). For a 2% full scale error, the remaining output current error settles at about 1.33%.

If the output current needs to settle within a 1% window, the full-scale gain error of a current sensor must not be bigger than 1%.

### 3.2.3 Impact of Offset Error

This chapter investigates offset error on the DC/DC converter. The same control-loop settings, current-sensor bandwidth of 100 kHz, and 0% gain error of the current sensor were assumed in the simulation for the settling time simulation shown in Figure 3-5. The offset error has been varied from 0%, 1%, to 2%.

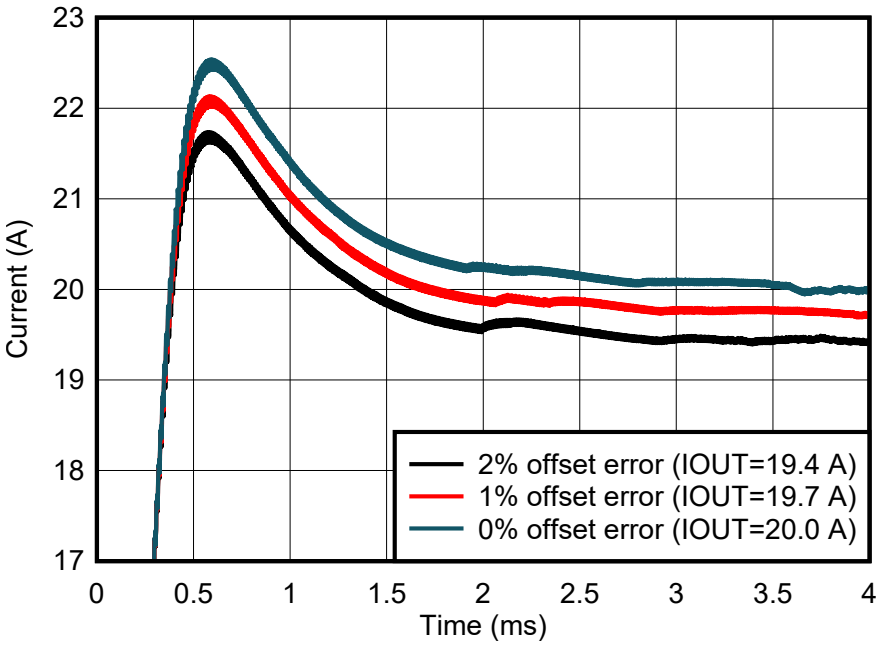


**Figure 3-5. Steady State Output Current Errors vs Current Sensor Offset Errors**

Again, settling time is unaffected by offset error. The settled output current is significantly affected. For 1% offset error the current output is 1.5% or 0.3 A lower (for 2% offset the output shows 3% or 0.6 A error, respectively).

Like the Gain Error, the Offset Error is specified to the full-scale error. In our example, the full-scale current was 32 A. This means at a 1% error, the absolute error is 0.3 A (for 2%, absolute 0.6 A). The simulation indicates these results are precise.

Unlike the gain error that scales relative to the output, the offset error adds in absolute to the output current that is set in a converter. Offset error is either calibrated out or compensated by feedforward techniques (adding the known error to the output).

In summary, both gain and offset error do not impact the settling time of the control loop as long as the current sensor has a high enough bandwidth not to limit the control-loop bandwidth. Both gain and offset error impacts the accuracy of the DC-charger output. For the target specifications of the EV-Charger defined in Table 1-1, this means the current sensor needs to have a bandwidth between 10 kHz and 100 kHz and total error (for both gain and offset) smaller than 1%. Use offset calibration to achieve the target.

## 3.3 Point G - DC/DC Tank Current Sensing

This section details the current-sensing requirement at the switching tank - point G. In a resonant CLLLC bidirectional isolated DC/ DC converter zero crossing detection (ZCD) is required for synchronous rectification, which helps reducing the conduction loss and improve system efficiency.

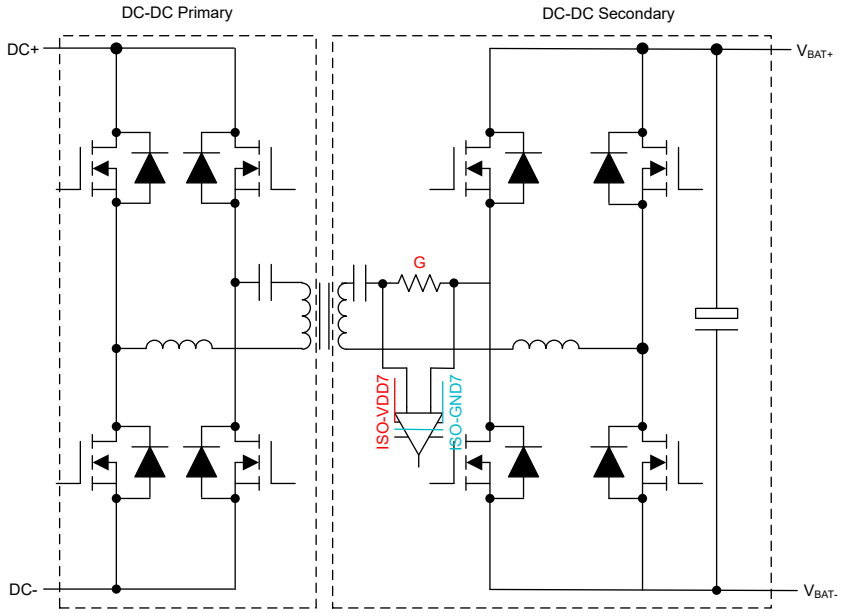


**Figure 3-6. Current Sensing at Primary or Secondary Tank of Isolated DC/ DC Converter**

In Figure 3-6, the two green cursor lines indicate the propagation delay between zero crossing and secondary side FET turn-on.

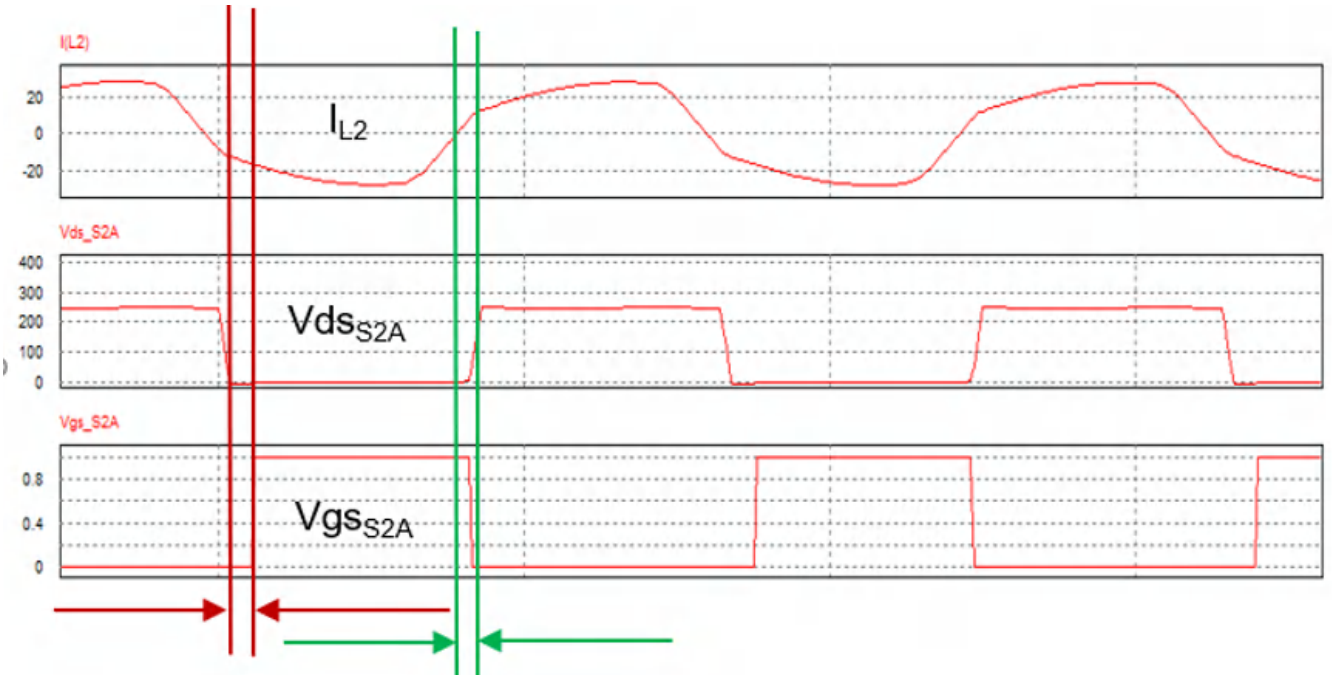


**Figure 3-7. Propagation Delay of Zero Crossing Detection**

A state-of-the-art implementation of the ZCD circuit in CLLLC topology is placing a Current Transformer (CT) or a Rogowski coil at the primary and secondary side in series with the resonant capacitor. Typical propagation delays of the CT or Rogowski coil approach are between 100ns and 200ns. This delay can cause significant losses in a CLLLC topology impacting overall efficiency of the DC/DC converter in a negative way. Assuming peak current is about 30 A, the resonate switching frequency of 500 kHz and turn-on delay of 100ns, the body diode (with a forward voltage of 4.5 V) the FET carries 9.3 A until the FET is turned on, which results in a peak energy loss of about 42 W per FET.

An alternative approach is shown in Figure 3-8. Here, the resonate capacitor voltage in conjunction with a differentiator circuit is implemented to recreate the sinusoidal current. The recreated sinusoidal signal is further processed by a differential-to-single-end OPA(OPA354) and a fast Comparator (TLV3501) for ZCD.

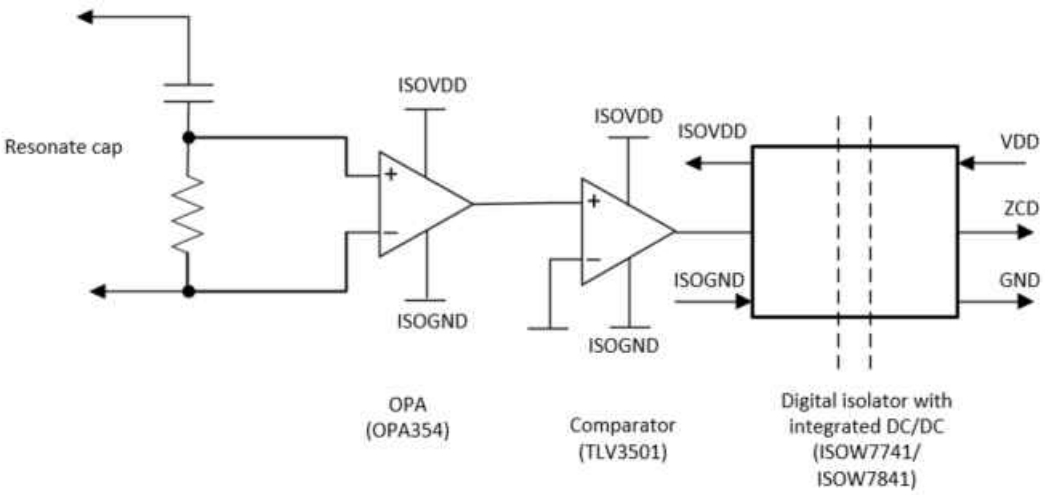


**Figure 3-8. ZCD Circuit With ISOW7741, ISOW7841**

The zero-crossing signal is isolated by a digital isolator (ISOW7741 or ISOW7841). These digital isolators have integrated isolated DC/DC converters to generate an isolated supply for the OPA and Comparator devices. The OPA354, TLV3501, and ISOW7741 have propagation delays of 0.6ns, 4.5ns, and 10.7ns, respectively, resulting in a total propagation delay 15.8ns for the complete design, which is about 10 times smaller than a CT or Rogowski coil approach. Assume the same switching frequency and peak current as in the previous example, the peak energy loss in one FET can be reduced from 42 W down to 6.7 W only (impacting overall efficiency positively).

## 3.4 Summary of Sensing Points E, F, and G and Product Suggestions

Table 3-1 summarizes the positives and negatives of current sensing points at E, F, and G. Fault protection needs to be handled with smart gate drivers, the current sensors cannot detect fast enough. A significant power loss improvement can be achieved by using the new ZCD shown in Figure 3-8.

**Table 3-1. Positives and Negatives of Current Sensing Point at E, F, and G**

| | E | F | G |
|---|---|---|---|
| Accurate current output regulation | (+) | (+) | (–) |
| Overcurrent fault protection | (–) | (–) | (+) |
| Power supply easy | (+) | (–)(1) | (–) |
| ZCD | N/A | N/A | (+) |

(1) Point F needs a floating supply above VOUT+

**Table 3-2. Products for Current Sensing at Points E, F, and G**

| I-Sensing Point | Comments, Challenge | Iso-Supply Voltage | Minimum Bandwidth | Maximum Latency | CMTI | Minimum Accuracy | Products (ISO-)AMP \| ISO-ADC |
|---|---|---|---|---|---|---|---|
| E | Current in negative branch and fault detection | From lower Gate Driver | > 10 kHz | – | Low | < 1% | AMC1302 AMC1306M05 \| AMC23Cxx\| AMC22Cxx |
| F | Current in positive branch and fault detection | Floating above OUT+ needed | > 10 kHz | – | Low | < 1% | AMC3302 AMC3306M05 \| AMC23Cxx\| AMC22Cxx |
| G | For ZCD | From upper Gate Driver | > 1 MHz | < 200 ns | High | – | OPA354\| TLV3501\| ISOW7841\| ISOW7741 |

## 4 Conclusion

The control loops regulation performances of the power conversion system in DC charging stations are significantly impacted by current-sensor parameters such bandwidth, gain, and offset error.

This application note defined system simulations of AC/DC and DC/DC, correspondingly, with the minimum requirements of current sensors based on the different features. The results in this document illustrate that in DC charging stations, shunt-based designs can match and even present higher performances in all the measurement points by having low power consumption. Challenges for the shunt-based current sensing were found in the switching node of the DC/DC converter when low-latency zero-crossing current detection needs to be achieved. An alternative method for detecting the zero crossing of the current was proposed.

In conclusion, the methodology applied in this application note is not valid only for an 11-kW system but can be scaled up to higher power, leading to a proper guideline in the selection of current sensors.

## 5 References

1. Texas Instruments, *AMC1302 Precision, ±50-mV Input, Reinforced Isolated Amplifier* data sheet
2. Texas Instruments, *AMC1306x Small, High-Precision, Reinforced Isolated Delta-Sigma Modulators With High CMTI* data sheet
3. Texas Instruments, *AMC3302 High-Precision, ±50-mV Input, Reinforced Isolated Amplifier With Integrated DC/DC Converter* data sheet
4. Texas Instruments, *AMC3306M05 High-Precision, ±50-mV Input, Reinforced Isolated Delta-Sigma Modulator With Integrated DC/DC Converter* data sheet
5. Texas Instruments, *ISOW784x High-Performance, 5000-VRMS Reinforced Quad-Channel Digital Isolators with Integrated High-Efficiency, Low-Emissions DC-DC Converter* data sheet
6. Texas Instruments, *ISOW774x Quad-Channel Digital Isolator with Integrated Low-Emissions, Low-Noise DC-DC Converter* data sheet
7. Texas Instruments, *An overview of conducted EMI specifications for power supplies* marketing white paper
8. Texas Instruments, *TIDA-01606 10-kW, bidirectional three-phase three-level (T-type) inverter and PFC* reference design
9. Texas Instruments, *TIDA-010210 11-kW, bidirectional, three-phase ANPC based on GaN reference design*
10. Texas Instruments, *TIDA-010054 Bidirectional, dual active bridge reference design for level 3 electric vehicle charging stations*
11. Texas Instruments, *Software Phase Locked Loop Design Using C2000™ Microcontrollers for Three Phase Grid Connected Applications* application note
12. *Multirate Harmonic Compensation Control for Low Switching Frequency Converters Scheme, Modeling, and Analysis*

# IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265