Application Note

A Basic Guide to Bridge Measurements

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ABSTRACT

Many precision sensors are formed from a Wheatstone bridge circuit configuration. This circuit configuration enables accurate differential measurements for resistive elements. These elements can be used to measure weight, pressure, temperature, and a variety of other types of sensor parameters. Achieving the most accurate bridge measurements with precision analog-to-digital converters (ADCs) requires a detailed understanding of how these sensors work, how they are calibrated, how they connect to an ADC, and how the ADC is configured. This application note presents an overview of the bridge circuit, how bridges are used to measure different forces, how the ADC measurement is set up, and what errors can arise in the measurement. This application note starts with an overview of bridge circuit basics, how they are constructed, and what parameters are important when designing a bridge measurement system. Circuits are presented showing connections to precision ADCs.

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1 Bridge Overview

A Wheatstone bridge is a circuit used to measure a change in resistance among a set of resistive elements. The circuit has two parallel resistive branches that act as voltage dividers for the excitation voltage, $V_{EXCITATION}$. The output of each resistor divider is nominally at $V_{EXCITATION}$ divided by two. With no applied load, the change in the resistance of the elements, ΔR, is equal to zero. Assuming an ideal system where the nominal resistance of each element is R, each voltage divider is at the same potential and the differential bridge output voltage, V_{OUT}, is zero. When a load is applied, one or more of the elements changes resistance such that ΔR ≠ 0 Ω. This causes a change in V_{OUT} that can be calculated very precisely by making a differential measurement across the bridge. Figure 1-1 shows the basic configuration of a simple bridge circuit using resistive elements.

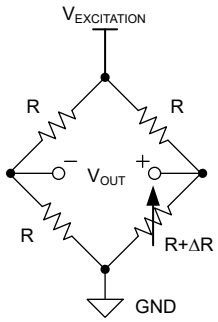

Figure 1-1. Basic Configuration of a Simple Bridge Circuit

The basic bridge circuit is constructed using resistive elements with a single variable element in the bridge. This element is a resistive transducer that translates some physical parameter into a change in resistance. If this change in resistance is proportional to a change in the physical parameter, measuring ΔR yields an accurate representation of the physical property being sensed. While this document focuses on bridges using resistive elements, it is possible to construct a bridge using inductive or capacitive elements as well.

Bridge operation can be better understood by analyzing each side of the bridge in more detail. For example, the right side of the bridge in Figure 1-1 looks like the voltage divider circuit shown in Figure 1-2:

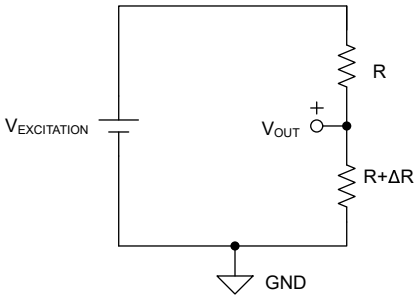

Figure 1-2. A Resistive Element Measured as a Voltage Divider

Equation 1 calculates V_{OUT} with respect to ground for the system in Figure 1-2:

$$V_{OUT} = V_{EXCITATION} \cdot \left(\frac{R + \Delta R}{R + R + \Delta R}\right) = V_{EXCITATION} \cdot \left(\frac{R + \Delta R}{2 \cdot R + \Delta R}\right) \quad (1)$$

Assuming $V_{EXCITATION}$ = 6 V, R = 3000 Ω, and ΔR = 3 Ω, Equation 1 can be used to calculate that V_{OUT} = 3.0015 V. Then, the voltage across R is calculated to be $V_R = V_{EXCITATION} - V_{OUT}$ = 2.9985 V. This yields a voltage across ΔR of $V_{\Delta R} = V_{OUT} - V_R$ = 0.003 V. While Equation 1 works in theory to calculate V_{OUT}, V_R, and $V_{\Delta R}$, a real system must measure V_{OUT} and V_R to be able to derive $V_{\Delta R}$. This can introduce additional challenges due to the limitations of standard measurement equipment.

For example, a simple 4-digit multimeter used to measure V_{OUT} and V_R could produce rounding errors that affect the calculation of $V_{\Delta R}$: if the multimeter rounds V_{OUT} = 3.0015 V up to 3.002 V and V_R = 2.9985 V down to 2.998 V, then $V_{\Delta R}$ = 0.004 V; or, if V_{OUT} is rounded down to 3.001 V and V_R is rounded up to 2.999 V, then $V_{\Delta R}$ = 0.002

V. Both of these cases yield a measurement error of 1 mV relative to a 3-mV signal, or ±33% error. Ultimately, the 4-digit multimeter does not have enough resolution to consistently determine the precise value of ΔR by measuring across either resistive element in the divider.

For better results, the single-ended measurement shown in Figure 1-2 is changed to a differential measurement by placing the resistive transducer in a bridge configuration. In Figure 1-3, the bridge uses a second resistive path in parallel with the transducer path. With no applied load, ΔR = 0 Ω and V_{OUT} = 0 V.

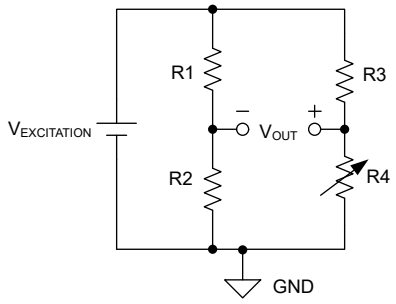

Figure 1-3. A Simple Bridge Using a Differential Measurement Across Two Resistive Paths

Equation 2 calculates the differential output voltage for the system shown in Figure 1-3 assuming R1 = R2 = R3 = R and R4 = R + ΔR.

$$V_{OUT} = V_{EXCITATION} \cdot \left(\frac{R + \Delta R}{2 \cdot R + \Delta R} - \frac{R}{2 \times R}\right) = V_{EXCITATION} \cdot \left(\frac{\Delta R}{2 \times (2 \cdot R + \Delta R)}\right) \quad (2)$$

Using the same values from the single-ended example where $V_{EXCITATION}$ = 6 V, R = 3000 Ω, and ΔR = 3Ω, V_{OUT} is now calculated to be 1.49925 mV. Importantly, the same 4-digit multimeter can measure V_{OUT} much more precisely and on a millivolt scale as either 1.499 mV (rounded down) or 1.500 mV (rounded up). Measuring V_{OUT} differentially in a bridge configuration yields a measurement error of <1 µV relative to a 1.5-mV signal, or 0.067%. This result occurs because a bridge configuration enables direct measurement of ΔR instead of a comparative measurement between ΔR and R. A direct measurement also enables V_{OUT} to be amplified to get a larger input signal to the ADC. This amplification enables higher-resolution measurements of smaller values of ΔR.

One challenge with a single active resistive element bridge is that it has an inherent non-linearity in the measurement. Different bridge constructions have different non-linearities, and some topologies eliminate this inherent non-linearity. This is discussed in more detail in the next section.

2 Bridge Construction

2.1 Active Elements in Bridge Topologies

As Figure 1-3 illustrates, a basic bridge has a single active resistive element while the other three elements are static resistances. These single active-element bridges are simpler to construct and less expensive. However, they have less sensitivity and more non-linearity through the full-scale range of the measurement.

Other bridge topologies may have two active resistive elements and two static resistors. In some cases, all four resistive elements can be active. These bridges increase the sensitivity and reduce the non-linearity in the bridge measurements. Regardless of the configuration, the bridge functionality remains the same: measuring the change in the resistive element as a function of the excitation voltage.

2.1.1 Bridge With One Active Element

The simplest bridge topology has a single active resistive element while the remaining three elements are static resistances, as shown in Figure 2-1. This is known as a quarter bridge.

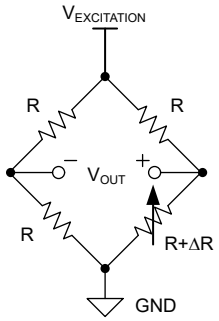

Figure 2-1. Bridge With One Active Element (Quarter Bridge)

Equation 3 calculates V_{OUT} between the two voltages dividers in Figure 2-1:

$$V_{OUT} = V_{EXCITATION} \cdot \left(\frac{R + \Delta R}{2 \cdot R + \Delta R}\right) - V_{EXCITATION} \cdot \left(\frac{R}{2 \cdot R}\right) \quad (3)$$

Collecting like terms and simplifying Equation 3 yields Equation 4:

$$V_{OUT} = V_{EXCITATION} \cdot \left(\frac{(R + \Delta R) - (2 \cdot R + \Delta R)/2}{2 \cdot R + \Delta R}\right) = \frac{V_{EXCITATION}}{2} \cdot \left(\frac{\Delta R}{2 \cdot R + \Delta R}\right) \quad (4)$$

Equation 4 shows that V_{OUT} is proportional to $V_{EXCITATION}$ and ΔR when ΔR is much smaller than R (ΔR << R). This relationship can be confirmed by plotting V_{OUT} against the change in ΔR from zero to full-scale (ΔR_{FS}). Figure 2-2 shows this plot when R = 1 kΩ, $V_{EXCITATION}$ = 10 V, and ΔR_{FS} = 1 Ω.

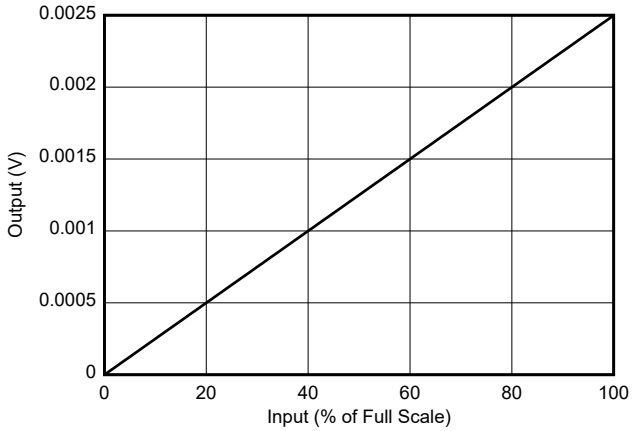

Figure 2-2. Quarter Bridge Differential Output (R = 1 kΩ, $V_{EXCITATION}$ = 10 V, ΔR_{FS} = 1 Ω)

Though not obvious from Figure 2-2, this bridge topology has a small inherent non-linearity because of the 2R + ΔR term in the denominator in Equation 4. Taking the endpoints of the plot in Figure 2-2 and removing the endpoint slope from the curve reveals the non-linearity of this bridge topology. Figure 2-3 illustrates this phenomenon by plotting non-linearity as a percent of the full-scale.

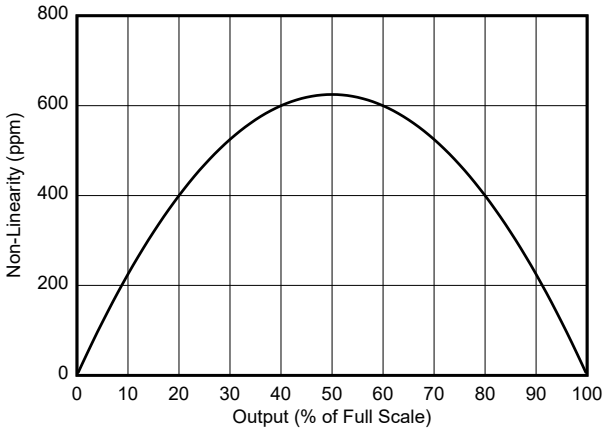

Figure 2-3. Quarter Bridge Non-Linearity

The non-linearity shown in Figure 2-3 directly results from the topology of the bridge with one active element, and does not include any non-linearity in the single active resistive element.

2.1.1.1 Reducing Non-Linearity in a Bridge With One Active Element Using Current Excitation

It is possible to reduce the non-linearity in a bridge with one active element by using current excitation instead of voltage excitation, as shown in Figure 2-4.

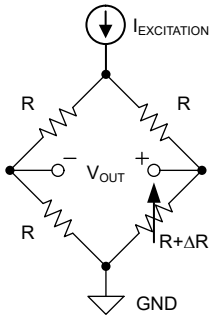

Figure 2-4. Current Excitation for a Bridge with One Active Element

Equation 5 calculates the resulting output voltage, V_{OUT}, when $I_{EXCITATION}$ splits between each branch of the bridge in Figure 2-4:

$$V_{OUT} = I_{EXCITATION} \cdot (R + \Delta R) \cdot \left(\frac{2 \cdot R}{4 \cdot R + \Delta R}\right) - I_{EXCITATION} \cdot R \cdot \left(\frac{2 \cdot R + \Delta R}{4 \cdot R + \Delta R}\right) \quad (5)$$

Converting and collecting like terms, Equation 5 simplifies to Equation 6:

$$V_{OUT} = I_{EXCITATION} \cdot \left(\frac{\left(2 \cdot R^2 + 2 \cdot R \cdot \Delta R\right) - \left(2 \cdot R^2 + R \cdot \Delta R\right)}{4 \cdot R + \Delta R}\right) = I_{EXCITATION} \cdot R \cdot \left(\frac{\Delta R}{4 \cdot R + \Delta R}\right) \quad (6)$$

Comparing the denominators for Equation 6 (4 · R + ΔR) and Equation 4 (2 · R + ΔR) reveals that the non-linearity error due to the topology of a one-active-element bridge using current excitation is reduced by approximately ½ relative to the same circuit using voltage excitation.

A bridge measurement system using current excitation has additional benefits and challenges. See Section 6.5 for more information about how this circuit is implemented.

2.1.2 Bridge With Two Active Elements in Opposite Branches

Bridges can also be constructed with more than one active element. Figure 2-5 shows a sensor with two active elements placed in different branches and on opposite sides of the bridge. This is known as a half bridge.

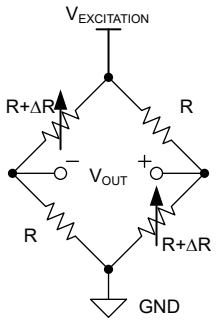

Figure 2-5. Bridge With Two Active Elements in Opposite Branches (Half Bridge)

Equation 7 calculates V_{OUT} for the bridge with two active elements in opposite branches shown in Figure 2-5:

$$V_{OUT} = V_{EXCITATION} \cdot \left(\frac{R + \Delta R}{2 \cdot R + \Delta R}\right) - V_{EXCITATION} \cdot \left(\frac{R}{2 \cdot R + \Delta R}\right) = V_{EXCITATION} \cdot \left(\frac{\Delta R}{2 \cdot R + \Delta R}\right) \quad (7)$$

Similar to the bridge with one active element, Equation 7 shows that V_{OUT} is proportional to $V_{EXCITATION}$ and ΔR when ΔR is small. Moreover, the V_{OUT} equation for both bridge types has a ΔR term in the denominator, resulting in the same non-linearity seen in Figure 2-3.

However, the important difference between a single-active-element bridge and a bridge with two active elements is the *sensitivity*. In the latter case, V_{OUT} is two times larger for a given $V_{EXCITATION}$. This larger output signal doubles the dynamic range compared to the single-active-element bridge, resulting in a better ADC measurement.

2.1.2.1 Eliminating Non-Linearity in a Bridge With Two Active Elements in Opposite Branches Using Current Excitation

Figure 2-6 illustrates how it is possible to eliminate the non-linearity in a bridge with two active elements in opposite branches by using current excitation instead of voltage excitation.

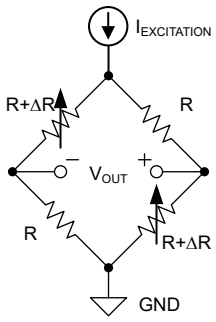

Figure 2-6. Current Excitation for a Bridge With Two Active Elements in Opposite Branches

Equation 8 calculates the resulting output voltage, V_{OUT}, when $I_{EXCITATION}$ splits between each branch of the bridge in Figure 2-6.

$$V_{OUT} = I_{EXCITATION} \cdot (R + \Delta R) \cdot \left(\frac{2 \cdot R + \Delta R}{4 \cdot R + 2 \cdot \Delta R}\right) - I_{EXCITATION} \cdot R \cdot \left(\frac{2 \cdot R + \Delta R}{4 \cdot R + 2 \cdot \Delta R}\right) \quad (8)$$

The ratio (2 · R + ΔR) / (4 · R + 2 · ΔR) in Equation 8 reduces to ½, which produces the simplified result in Equation 9:

$$V_{OUT} = \frac{I_{EXCITATION}}{2} \cdot \Delta R \quad (9)$$

Unlike the circuit using voltage excitation, Equation 9 has no ΔR term in the denominator. As a result, current excitation removes the non-linearity error due to the topology of a bridge with two active elements in opposite branches. Comparatively, the same circuit using voltage excitation has a non-linearity error proportional to 2 · R + ΔR.

A bridge measurement system using current excitation has additional benefits and challenges. Refer to Section 6.5 for more information about how this circuit is implemented.

2.1.3 Bridge With Two Active Elements in the Same Branch

Bridges can also be constructed with two active elements in the same branch. Figure 2-7 shows an example of this type of configuration, which can also be referred to as a half bridge.

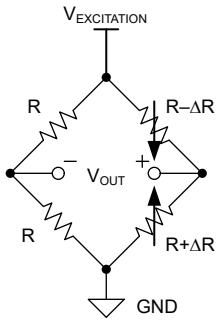

Figure 2-7. Bridge With Two Active Elements in the Same Branch (Half Bridge)

Equation 10 and Equation 11 calculate V_{OUT} for the bridge with two active elements in the same branch that is shown in Figure 2-7:

$$V_{OUT} = V_{EXCITATION} \cdot \left(\frac{R + \Delta R}{(R + \Delta R) + (R - \Delta R)}\right) - V_{EXCITATION} \cdot \left(\frac{R}{2 \cdot R}\right) = V_{EXCITATION} \cdot \left(\frac{R + \Delta R}{2 \cdot R} - \frac{R}{2 \cdot R}\right) \quad (10)$$

$$V_{OUT} = V_{EXCITATION}\left(\frac{\Delta R}{2 \cdot R}\right) \quad (11)$$

Similar to the previous bridge configurations, V_{OUT} is proportional to $V_{EXCITATION}$ and ΔR. Unlike the previous bridge topologies, Equation 11 does not have a ΔR term in the denominator. As such, a bridge with two active elements in the same branch does not have an inherent non-linearity, which is true for both voltage or current excitation. However, this does not include any non-linearity from the actual sensor.

2.1.4 Bridge With Four Active Elements

The final bridge configuration is constructed with four active elements that each have the same magnitude change in resistance for the same strain. However, this change is in opposite directions on opposite sides of the bridge. This configuration is known as a full bridge, and is shown in Figure 2-8.

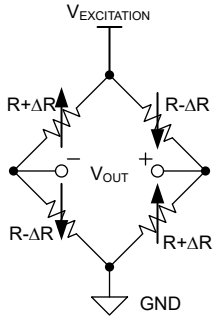

Figure 2-8. Bridge With Four Active Elements (Full Bridge)

Equation 12 and Equation 13 calculate V_{OUT} for the bridge with four active elements shown in Figure 2-8:

$$V_{OUT} = V_{EXCITATION} \cdot \left(\frac{R + \Delta R}{2 \cdot R}\right) - V_{EXCITATION} \cdot \left(\frac{R - \Delta R}{2 \cdot R}\right) = V_{EXCITATION} \cdot \left(\frac{2 \cdot \Delta R}{2 \cdot R}\right) \quad (12)$$

$$V_{OUT} = V_{EXCITATION} \cdot \left(\frac{\Delta R}{R}\right) \quad (13)$$

Similar to all of the previous bridge configurations, V_{OUT} is proportional to $V_{EXCITATION}$ and ΔR if ΔR is small. The benefit of a four-active-element bridge is that the sensitivity is two times greater than both two-active-element bridge configurations and four times greater than the single-active-element bridge. Moreover, a four-active-element bridge topology has no inherent non-linearity in the bridge output. This is true for both voltage and current excitation.

2.2 Strain Gauge and Bridge Construction

One example of a common use-case for a bridge measurement is a load cell comprised of strain gauge elements. A strain gauge is a wire or metallic foil whose resistance changes as the element deforms. When the strain gauge is tensioned (stretched), the foil elongates, causing the resistance to increase. When the strain gauge is compressed, the foil shortens, causing the resistance to decrease. Figure 2-9 illustrates the change in resistance as the strain gauge length changes. A resting strain gauge is shown in black, a tensioned strain gauge is shown in green, and a compressed strain gauge is shown in red.

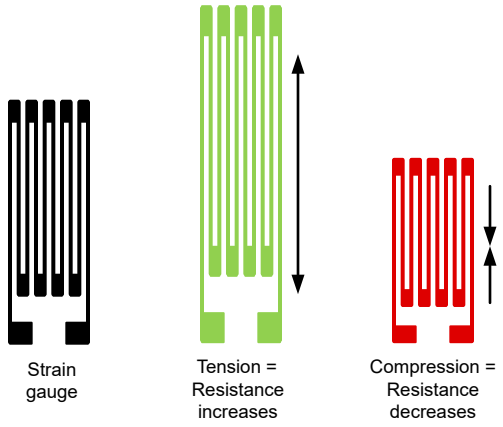

Figure 2-9. Strain Gauge Resistance vs Length: Resting (left), Tension (middle), and Compression (right)

Strain gauges are typically affixed to a structure that has some small amount of flexibility. For example, a rod holding a weight experiences some tension due to the applied load. A strain gauge affixed to the rod also tensions slightly as the rod deforms, increasing the strain gauge resistance so that the tensile force can be measured. Similarly, the strain gauge compresses if the rod compresses, causing a resistance change that directly relates to the amount of compressive force on the rod.

Another example of a slightly-flexible component that uses strain gauges is a load cell, similar to the one shown in Figure 2-10.

Figure 2-10. Photo of a Load Cell

Strain gauges are placed into a bridge configuration to construct a load cell. Figure 2-11 depicts a common single-point load cell with four strain gauges at different points around the aperture. As shown, an applied downward force causes the free end of the load cell to move parallel to the fixed end. In this configuration, opposite strain gauges are tensioned (in green) and compressed (in red). This mechanical orientation allows for a proper four-active-element bridge.

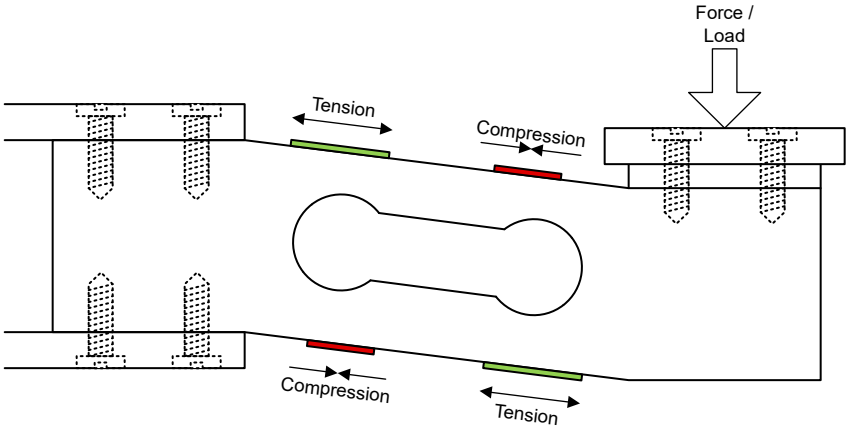

Figure 2-11. Single-Point Load Cell With Approximate Positions and Responses of the Four Strain Gauges

Figure 2-12 shows the four resistors in their electrical positions in the bridge. Redrawing the elements of the load cell for tension (in green) and compression (in red) shows how these elements have opposite reactions to the strain on opposite sides of the bridge.

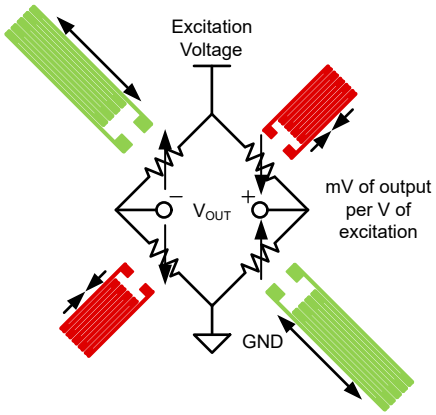

Figure 2-12. Equivalent Bridge Measurement of the Load Cell

A common application using these type of load cells is a weigh scale. A weigh scale may use one or more load cells measured at the same time. The sum of these load cell measurements is used to calculate the weight of the object being measured.

3 Bridge Connections

Connecting a bridge to an ADC typically requires implementing a ratiometric measurement while choosing between a four-wire or six-wire bridge. The next sections discuss these concepts in more detail as well as demonstrate how a bridge is connected to the excitation voltage and the ADC.

3.1 Ratiometric Measurements

Figure 3-1 illustrates how bridge measurements are typically made with a ratiometric reference configuration. The output of the bridge is measured by the ADC while a single source is used as both the bridge excitation voltage and the ADC reference voltage.

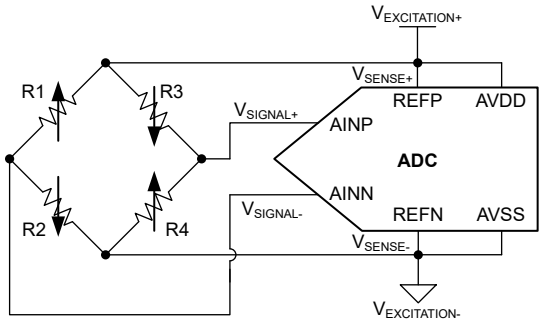

Figure 3-1. Example of a Ratiometric Bridge Measurement

The ADC samples the input voltage, V_{IN}, and compares it against the reference voltage, V_{REF}. V_{IN} is the voltage difference between $V_{SIGNAL+}$ and $V_{SIGNAL–}$ (or AINP and AINN) while V_{REF} is the difference between the voltage at V_{SENSE+} and $V_{SENSE–}$ (or REFP and REFN). The ADC generates an output code proportional to V_{REF} as per Equation 14:

$$\text{Output Code} \propto \frac{V_{IN}}{V_{REF}} = \frac{V_{IN}}{\text{AVDD}} \tag{14}$$

Equation 14 substitutes AVDD for the V_{REF} term because AVDD is connected to REFP and REFN is grounded in Figure 3-1. Also, recall that Equation 13 states that V_{OUT} is equal to $V_{EXCITATION}$ multiplied by ΔR divided by R. In Figure 3-1, AVDD = $V_{EXCITATION+}$ - $V_{EXCITATION-}$ while $V_{OUT\ (Bridge)}$ = $V_{IN\ (ADC)}$. These substitutions yield Equation 15:

$$V_{IN} = V_{EXCITATION} \cdot \left(\frac{\Delta R}{R}\right) = \text{AVDD} \cdot \left(\frac{\Delta R}{R}\right) \tag{15}$$

Substituting Equation 15 for the V_{IN} term in Equation 14 results in Equation 16:

$$\text{Output Code} \propto \frac{V_{IN}}{\text{AVDD}} = \frac{\Delta R}{R} \tag{16}$$

The output code in Equation 16 is directly proportional to ΔR. Moreover, Equation 16 shows that the exact values of AVDD and V_{IN} are unnecessary. Instead, the output code is directly proportional to the strain on the bridge.

One of the benefits of a ratiometric measurement is that the measurement is relatively invariant to changes in V_{REF}. This is also shown in Equation 16, where the output is proportional to ΔR / R and is therefore independent of the exact value of V_{REF} or $V_{EXCITATION}$. Therefore, the ratiometric measurement is less susceptible to any $V_{EXCITATION}$ drift over time and temperature. Any noise from the $V_{EXCITATION}$ source should also cancel out assuming that the noise at the reference input and the measurement input are correlated. Typically, these noise sources correlate well if the filter bandwidth for the reference input and the measurement input are the same.

3.2 Four-Wire Bridge

Figure 3-2 shows the connections for a four-wire bridge. There are two wires for excitation of the bridge ($V_{EXCITATION+}$ and $V_{EXCITATION–}$) and two wires for the measurement ($V_{SIGNAL+}$ and $V_{SIGNAL–}$). The ADC measures the differential bridge output voltage and the ADC positive and negative reference inputs connect to the excitation lines as $V_{EXCITATION+}$ and $V_{EXCITATION–}$, respectively.

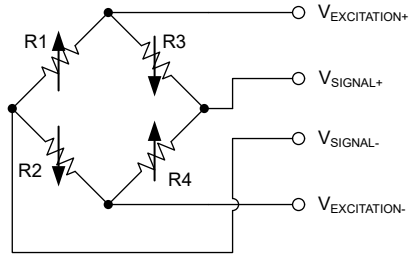

Figure 3-2. Connections for a Four-Wire Bridge

A four-wire bridge is suitable for a basic measurement in many data acquisition systems. However, long leads for $V_{EXCITATION+}$ and $V_{EXCITATION–}$ may have non-negligible resistance that add an error to the ADC measurement. Figure 3-3 shows an ADC connected to a four-wire bridge that has a series resistance, RP1 and RP2, in the excitation leads.

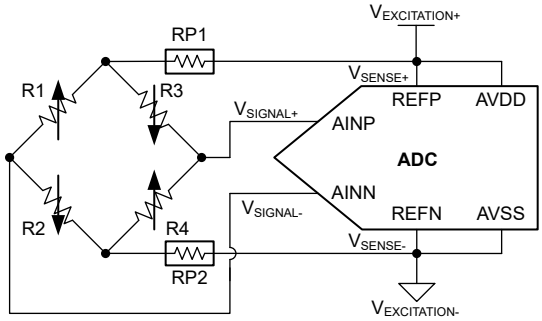

Figure 3-3. Four-Wire Bridge With Parasitic Resistance in $V_{EXCITATION±}$ Leads

Theoretically, $V_{EXCITATION+}$ at the REFP input and $V_{EXCITATION–}$ at the REFN input are the same as the voltage exciting the bridge. However, the series lead resistance lowers the voltage at the bridge itself, thereby changing the bridge output voltage as per Equation 17.

$$V_{OUT} = [V_{EXCITATION} - ([\mathrm{RP1} + \mathrm{RP2}] \cdot [I_{EXCITATION}])] \cdot \left(\frac{\Delta \mathrm{R}}{\mathrm{R}}\right) \quad (17)$$

Even if RP1 and RP2 are small, the current through the bridge ($I_{EXCITATION}$) can be substantial, resulting in a significant error. For example, $I_{EXCITATION}$ = 14.3 mA when $V_{EXCITATION}$ = 5 V and the bridge resistance is 350 Ω. Even if RP1 = RP2 = 1 Ω, the parasitic resistance results in a 0.6% measurement error.

Note that the leads for the bridge output ($V_{SIGNAL±}$ in Figure 3-2) may also have a series resistance of the same magnitude as RP1 and RP2. However, the ADC input impedance is typically high and the current pulled through $V_{SIGNAL±}$ is many orders of magnitude smaller than $I_{EXCITATION}$. Therefore, any current reacting with the $V_{SIGNAL±}$ lead resistance adds a negligible error.

3.3 Six-Wire Bridge

A six-wire bridge removes the lead resistance error associated with a four-wire bridge. A six-wire topology has the same four wires as the four-wire bridge, while an additional two wires ($V_{SENSE±}$) connect to the top and the bottom of the bridge. Figure 3-4 shows a six-wire bridge.

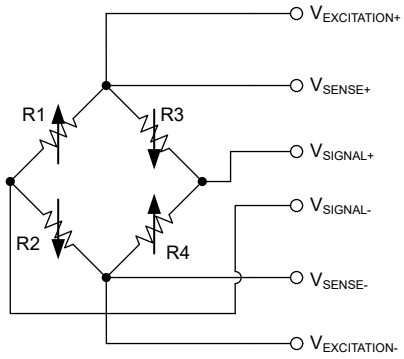

Figure 3-4. Connections for a Six-Wire Bridge

In this topology, the $V_{SENSE±}$ leads at the top and bottom of the bridge are used as a Kelvin (or force-sense) connection to remove the effect of the lead resistance. This connection uses the $V_{EXCITATION±}$ leads as a force line to drive the voltage to the bridge. $V_{EXCITATION±}$ can be high current and create a voltage drop across the parasitic resistances going to the bridge as discussed in Section 3.2. The $V_{SENSE±}$ leads are used to accurately measure the voltage at the top of the bridge by bypassing the parasitic lead resistance that carries the high current. At the same time, any resistance in the $V_{SENSE±}$ leads causes a significantly lower voltage error because of the much smaller input current flowing through each lead. Figure 3-5 shows how a six-wire bridge connects to the ADC. The series resistance in the $V_{EXCITATION±}$ leads is also shown.

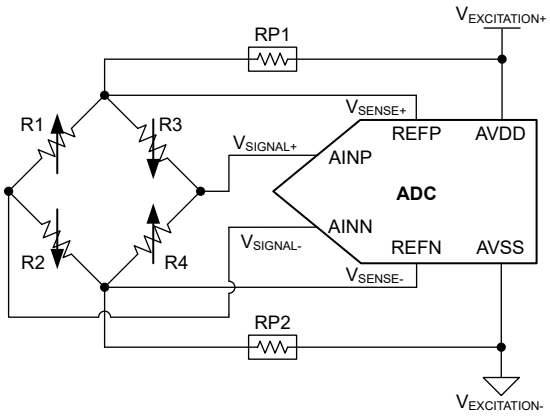

Figure 3-5. Six-Wire Bridge With Parasitic Resistance in $V_{EXCITATION±}$ Leads

Using a six-wire bridge topology ensures that the ADC V_{REF} is the same as the voltage driving the bridge. Similar to the four-wire topology, resistance in the $V_{SIGNAL±}$ and $V_{SENSE±}$ leads can add an error, though the current through these leads will be significantly smaller than $I_{EXCITATION}$. This lower current minimizes the error introduced to the ADC input and reference paths, thereby improving overall system accuracy compared to the four-wire bridge.

4 Electrical Characteristics of Bridge Measurements

An important consideration to achieving precise and accurate bridge measurements is how the electrical characteristics of the sensor affect the ADC performance. Table 4-1 shows a generic specification table for the resistive bridges used in a typical load cell.

Table 4-1. Example Load Cell Specifications

Specification Description	Specification Value	Specification Value for a Load Cell With a 2-kg Capacity
Bridge Sensitivity	2.0 ±15% mV/V	
Safe Overload	150 %FS	3 kg
Maximum Overload	200 %FS	4 kg
Non-linearity	±0.05 %FS	±1 g
Non-repeatability		
Hysteresis		
Creep (5 min.)		
Temperature Effect on Output	±0.05 %FS/°C	±1 g/°C
Temperature Effect on Zero	±2.0 %FS/°C	±40 g/°C
Zero Balance	±10 %FS	±0.2 kg
Bridge Resistance	1000 ± 10 Ω	
Excitation Voltage	≤ 15 V	
Operating Temperature Range	–10°C to +40°C	

Many of these characteristics are errors that can be calibrated, while other errors must be added to the total error budget. The following sections briefly introduce some of the more important electrical characteristics in Table 4-1 and are therefore not meant to be comprehensive.

4.1 Bridge Sensitivity

The bridge sensitivity is the maximum expected output voltage for each volt of excitation, $V_{EXCITATION}$, when the maximum load is applied. A typical bridge load cell has a sensitivity of 1 mV/V to 3 mV/V, such as the bridge in Table 4-1 that has a sensitivity of 2 mV/V. This value means that the bridge output increases by 2 mV for every 1 V of $V_{EXCITATION}$. For example, exciting this bridge with 5 V yields a maximum bridge output of 10 mV when the maximum load is applied.

This 10-mV output voltage is also the maximum differential input voltage measured by the ADC. Use this value to determine how much gain is required to increase the measured input signal and use more of the ADC full-scale range. Many ADCs incorporate a programmable gain amplifier that can be used for this purpose.

4.2 Bridge Resistance

Bridges come in a variety of nominal resistance values, though 120 Ω, 350 Ω, and 1000 Ω are the most common (see Table 4-1). Lower bridge resistances may require significant current to drive. For example, using $V_{EXCITATION}$ = 5 V to drive a 350-Ω bridge requires 14.3 mA of current. This may be significantly larger than the current consumed by the measurement circuitry including the ADC and amplifiers. In fact, power dissipation through the bridge may be the largest part of the system power budget.

Additionally, this large excitation current can react with any parasitic resistance in the excitation path to cause a mismatch between the actual voltage across the bridge and the reference voltage measured by the ADC. This error can be removed using a six-wire bridge.

4.3 Output Common-Mode Voltage

Typically, the desired output common-mode voltage of the bridge is at the midpoint of the ADC supply, AVDD, when AVDD = $V_{EXCITATION}$. This is the ideal common-mode input voltage for an ADC and enables the maximum gain.

Some systems use a $V_{EXCITATION}$ that is greater than AVDD. If this is the case, the bridge output common-mode voltage may not match the ADC input common-mode range. For example, choosing $V_{EXCITATION}$ = 10 V to maximize the sensor output sets the bridge common-mode voltage at 5 V. If AVDD = 5 V for the ADC, then this measurement may be very close to the ADC input range limit. Moreover, high-gain amplifiers used to amplify the bridge output typically limit the common-mode input range to well below AVDD, requiring alternative solutions. Section 6.3 and Section 6.4 show circuits that accommodate bridge configurations where $V_{EXCITATION}$ > AVDD.

4.4 Offset Voltage

The ideal bridge output should be 0 V with no applied load. However, a real bridge has a non-zero output with load applied. This error is an offset voltage that shifts the load response up or down, as shown in Figure 4-1.

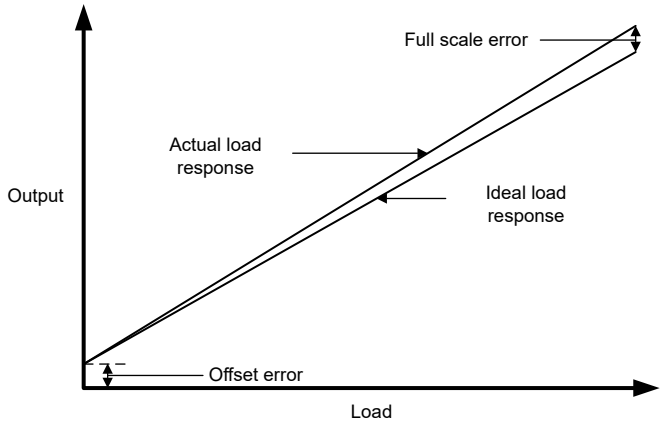

Figure 4-1. Actual vs Ideal Response of a Load on a Bridge

Offset voltage may come from a variety of sources. Manufacturing tolerances can result in difference nominal resistances among the bridge elements. This leads to an inherent offset error even with no applied load, and is typically specified in the sensor data sheet (see the *Zero Balance* parameter in Table 4-1).

Parasitic thermocouples external to the sensor in the bridge connection may give a small offset voltage that varies with temperature. Moreover, ADC input bias currents reacting with the bridge lead resistance or any ADC input filtering resistances may also give a small offset voltage.

Regardless of the offset voltage source, there are ways to calibrate this error through simple zeroing of the offset voltage digitally or other active circuit techniques such as AC excitation.

4.5 Full-Scale Error

Full-scale error or gain error is the difference in slope between the actual and ideal bridge measurement response under load with the offset removed. Figure 4-1 shows an example of the full-scale error. Sources of full-scale error can include wire impedance in a ratiometric measurement as discussed in Section 3.2 or the inherent gain error from an ADC. Additionally, the bridge sensitivity tolerance could change the slope of the load-vs-output-voltage curve and cause an error. For example, the ±15% tolerance given in Table 4-1 allows the typical 2-mV/V bridge sensitivity to span from 1.7 mV/V to 2.3 mV/V. Assuming $V_{EXCITATION}$ = 5 V, the ideal maximum bridge output signal is 2 mV/V • 5 V = 10 mV. However, the actual maximum bridge output signal could range from 8.5 mV (negative error) to 11.5 mV (positive error).

Fortunately, full-scale error is a measurement gain error that can typically be calibrated through testing of the measurement system against known inputs.

4.6 Non-Linearity Error and Hysteresis

Non-linearity error is the deviation of the output curve from the expected full-scale straight-line output as the bridge output increases. This non-linearity results from the characteristics of the bridge resistive elements and is different from the bridge topology error discussed in Section 2.1.1. For example, a resistive bridge element may be more non-linear if it exceeds a certain range or load. Bridge data sheets often characterize non-linearity (see Table 4-1) and suggest limiting the maximum load to keep non-linearity small.

Similar to non-linearity error, hysteresis is a small error that changes with the bridge output. However, this error may be different depending on whether the bridge output is increasing or decreasing. The addition of hysteresis to the non-linearity error is known as the *combined error*. The combined error is the maximum error from the straight line ranging from no load to the maximum load conditions (increasing and decreasing). Figure 4-2 graphically shows the non-linearity error, hysteresis, and the combined error.

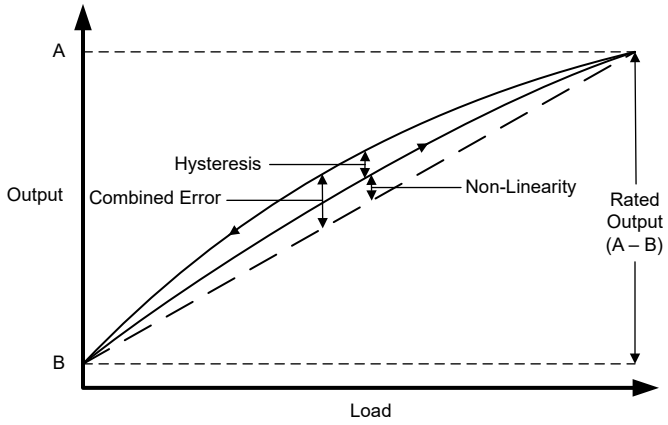

Figure 4-2. Hysteresis, Non-Linearity, and Combined Error

Non-linearity error and hysteresis are not easily calibrated. These errors may be different from unit-to-unit such that calibration requires many measurements across the full range of the bridge operation. However, these errors are typically much smaller than offset and full-scale errors. It is also worth noting that an ADC can contribute a non-linearity error, though this is generally negligible compared to bridge non-linearity.

4.7 Drift

Many of the parameters shown in Table 4-1 are specified at one temperature, typically 25°C. Drift errors specify how these parameters change over a temperature range. One common drift error is offset drift (*Temperature Effect on Zero* in Table 4-1), where the initial bridge offset voltage changes with temperature. Another common drift error is full-scale drift (*Temperature Effect on Output* in Table 4-1), which specifies how the slope of the bridge output changes with temperature. Similarly, ADCs have their own drift characteristics that affect measurement accuracy. Offset and gain drift errors are often described in %FS / °C, though other units are possible.

Temperature drift may be difficult to compensate due to non-linearity or different polarity. Moreover, accurately calibrating these errors can require measurements at different points across the temperature range of operation. In the design of any bridge measurement system, it is important to identify the operating temperature range and calculate the possible expected system error due to drift.

4.8 Creep and Creep Recovery

Creep is the change in the bridge output under a loaded condition while all other environmental factors are constant. This may be caused by deformations in a load cell under load over time. Creep recovery is the change in the bridge output after the load condition has been removed. Both errors are rated over a given amount of time and can be included in the bridge data sheet (see Table 4-1). However, these errors are not a function of the ADC measurement itself.

Similar to some of the other parameters, creep and creep recovery are errors that cannot be calibrated. The effects must fit within the error budget of the system design.

5 Signal Chain Design Considerations

After selecting a bridge based on its construction, connections, and characteristics, it is necessary to design a low-noise signal chain to measure the bridge output. This section delves into several important topics related to selecting the signal chain components:

- Amplification
- Noise
- Channel Scan Time and Signal Bandwidth
- AC Excitation
- Calibration

5.1 Amplification

As discussed in Section 4.1, a typical bridge has a sensitivity of 1 mV/V to 3 mV/V. Such low sensitivities often require selecting the largest value of $V_{EXCITATION}$ to increase the bridge output signal as much as possible. For example, the maximum $V_{EXCITATION}$ in Table 4-1 is 15 V and the bridge sensitivity is 2 mV/V, resulting in a maximum bridge output signal of 30 mV. This relatively low-level signal requires amplification to achieve precision measurements.

However, choosing $V_{EXCITATION}$ > AVDD can require level-shifting the reference or signal voltages to meet the ADC input limitations because most ADCs only support AVDD ≤ 5 V. In this case, use an external instrumentation amplifier (INA) in front of a gainless ADC to amplify the bridge signal and set the amplifier output common-mode voltage.

When $V_{EXCITATION}$ ≤ AVDD, choose an ADC with an integrated low-noise programmable gain amplifier (PGA) to reduce the system noise and improve dynamic range. Selecting an ADC with an integrated PGA also simplifies the signal chain and reduces PCB area.

The following subsections detail the operation of and use-cases for external INAs and integrated PGAs.

5.1.1 Instrumentation Amplifier

An INA may be necessary if the bridge signals extend beyond the ADC input limitations. This is generally the case when $V_{EXCITATION}$ > AVDD (see Section 6.3). Or, an external INA can be used to amplify the bridge output if the selected ADC does not have an integrated PGA.

5.1.1.1 INA Architecture and Operation

Although there are other topologies, a basic three op-amp INA is shown in Figure 5-1.

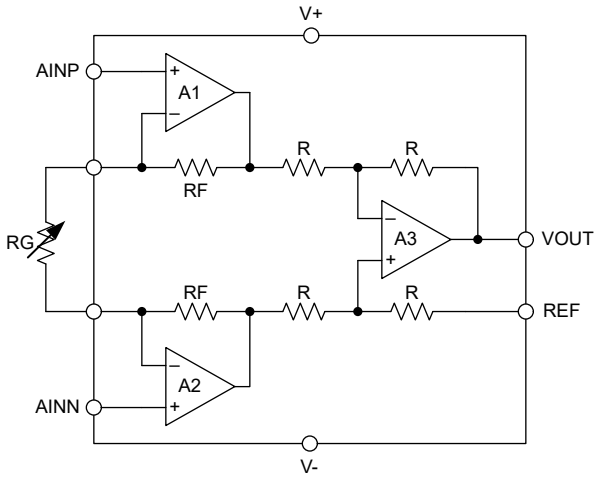

Figure 5-1. Topology of a Basic INA

The INA in Figure 5-1 amplifies the voltage between AINP and AINN. The amplifier gain is determined by an external gain-setting resistor, R_G, and the internal feedback resistors, R_F. The voltages at AINP and AINN are forced onto R_G via the output of A1 and A2 and both R_F resistors. This forces the same current through all three

resistors to create gain. A difference amplifier comprised of op amp A3 and four resistors, R, act as a unity gain buffer. The amplified voltage is measured between the REF and VOUT pins on the INA. The REF pin sets the reference point of the output voltage, and is typically chosen to match the ADC common-mode range. The INA gain is set by R_G and is determined by Equation 18:

$$G = 1 + (2 \cdot R_F) / R_G \quad (18)$$

Most INAs are capable of large voltage gains up to 1000 V/V. However, one practical challenge associated with high gain is that it limits the input signal common-mode voltage to approximately mid-supply. In the INA topology, the input common-mode voltage must match the output common-mode of the first op amp stage comprised of A1 and A2 in Figure 5-1. As the voltage of R_G is amplified to the output of A1 and A2, the output voltages of A1 and A2 are limited by how close those voltages are to either supply (V+ or V–). This limitation requires choosing the INA and bridge excitation supplies such that the bridge output is in the INA measurement range. The *INA Vcm vs Vout* tool in the Analog Engineer's Calculator simplifies this process by calculating the input common-mode range against the output voltage for a range of INAs. Figure 5-2 shows an example of this tool using the INA826.

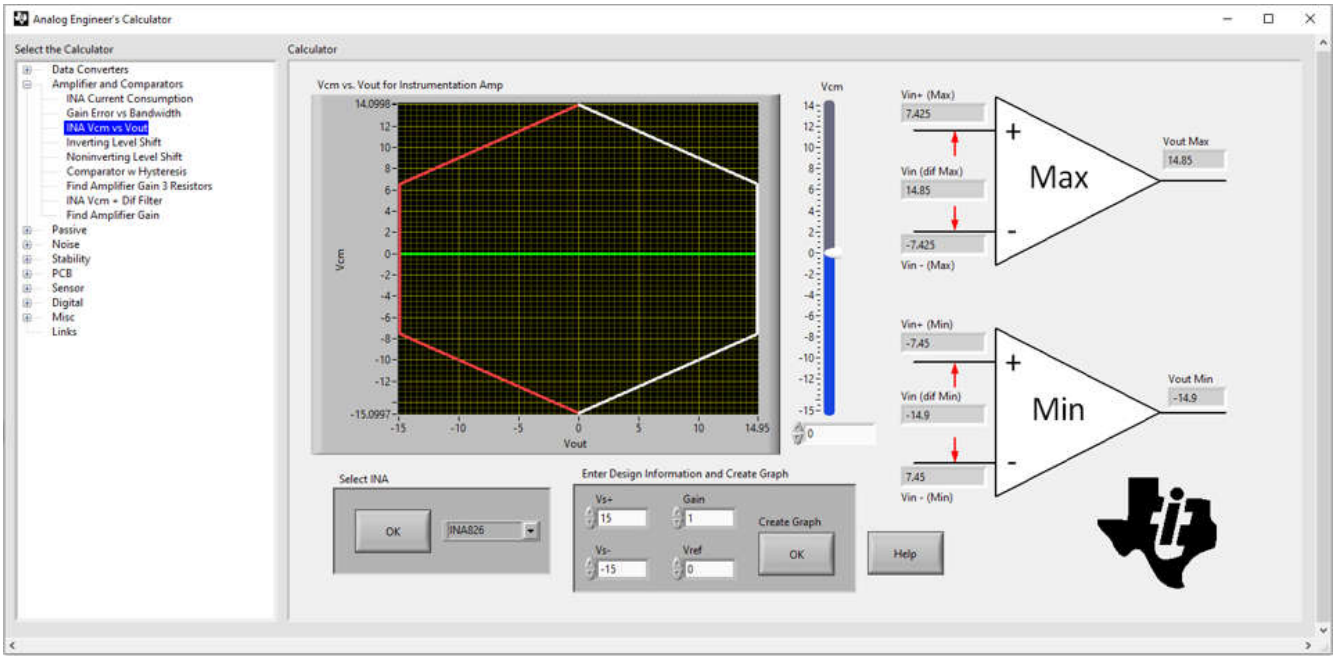

Figure 5-2. *INA Vcm vs Vout* Tool in the Analog Engineer's Calculator

5.1.1.2 INA Error Sources

Adding an INA into the signal path introduces several different errors. For example, the INA826 shown in Figure 5-2 has a gain error specification of ±0.04% (typical) and ±0.15% (maximum) when the gain is set to 100 V/V. This gain error results from slight mismatches in the factory trim of the resistor elements. The INA also has an offset error that is added to the measurement. The INA826 input-referred offset error is 150 µV (maximum). Additionally, resistor R_G contributes some gain error that directly adds to the overall system error.

An INA also adds noise to the measurement. The INA826 input-referred noise is 0.52 μV_{PP} in the 0.1-Hz to 10-Hz bandwidth. This noise may be greater than a PGA integrated into the ADC because of the INA topology. Refer to Section 5.2 for a more detailed discussion about the importance of noise in bridge measurements.

5.1.2 Integrated PGA

Choose an ADC with an integrated PGA when $V_{EXCITATION} \leq AVDD$. These circumstances typically allow for a ratiometric reference configuration similar to the circuit described in Section 6.1. Integrated PGAs also generally offer better performance compared to external devices because integrated PGAs are optimized for use with the associated ADC.

5.1.2.1 Integrated PGA Architecture and Operation

An integrated PGA is typically implemented as the front end of the basic INA. The circuit is similar to Figure 5-1 because it uses A1, A2, two R_F resistors, and a set of factory-trimmed, programmable R_G resistors that set the gain. As an example, the PGA in the ADS1235 is shown in Figure 5-3.

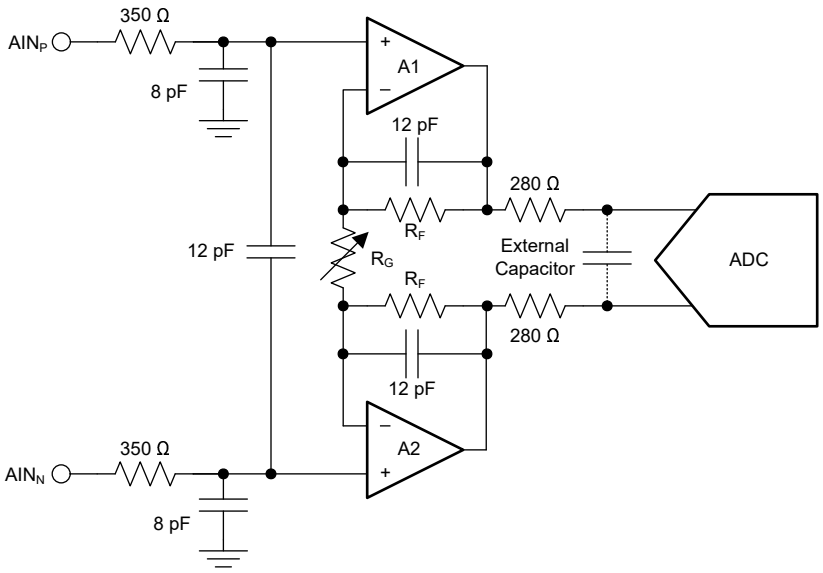

Figure 5-3. Simplified ADS1235 PGA Diagram

The PGA in Figure 5-3 also has low pass filters at both the input and output of the PGA. These filters help reduce sensitivity to electromagnetic interference (EMI). Some integrated PGAs also require an external capacitor that helps filter sample pulses caused by the modulator as well as perform anti-aliasing.

Similar to the INA, the integrated PGA has common-mode voltage requirements that are dictated by the gain and the output of the op amps. For example, the absolute input voltage (V_{AINP} or V_{AINN}) for the PGA integrated into the ADS1235 is limited by Equation 19:

$$AVSS + 0.3\ V + |V_{INMAX}| \cdot (Gain - 1) / 2 < V_{AINP}, V_{AINN} < AVDD - 0.3\ V - |V_{INMAX}| \cdot (Gain - 1) / 2 \quad (19)$$

where:

- $V_{INMAX} = V_{AINP} - V_{AINN}$, which describes the maximum differential input voltage.

Figure 5-4 graphically shows the relationship between the ADS1235 integrated PGA input to the PGA output.

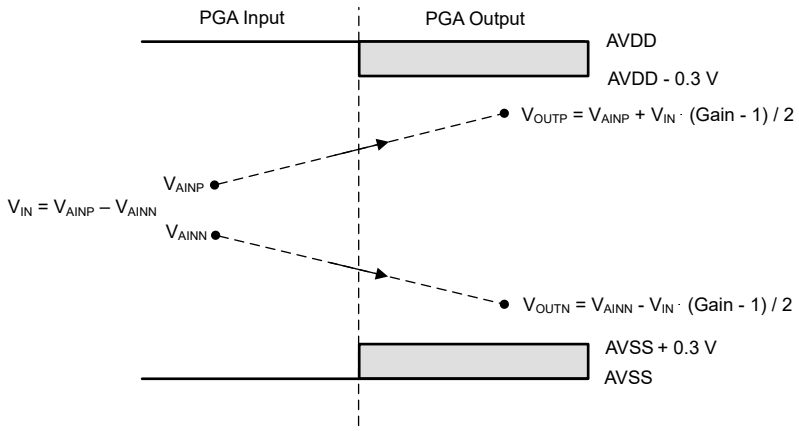

Figure 5-4. Graphical Representation of the ADS1235 PGA Input and Output Range

The PGA output voltages (V_{OUTP} and V_{OUTN}) in Figure 5-4 depend on the PGA gain and the input voltage magnitude, V_{IN}. For linear operation, the PGA output voltages must not exceed AVDD – 0.3 V or AVSS + 0.3 V. Note that Figure 5-4 depicts a positive differential input voltage that results in a positive differential output voltage, though negative differential voltages are also possible. See the ADS1235 Excel Calculator Tool for a common-mode input range calculator and other important design tools that help simplify projects using this ADC. Furthermore, the circuits in Section 6.3 and Section 6.6 demonstrate how to use these calculator tools to identify if the bridge output is within the PGA common-mode range.

5.1.2.2 Benefits of Using an Integrated PGA

One benefit of using an ADC with an integrated PGA is the integrated device does not require the output buffer difference amplifier in the INA solution (see Figure 5-1). Removing this component reduces the noise compared to using an external INA. For example, the INA826 has 0.52-μV_{PP} input-referred noise from 0.1 Hz to 10 Hz, while the ADS1235 noise at 10 samples per second (SPS) using the FIR filter is 0.096 μV_{PP}.

Another benefit of the integrated PGA is that the gain is factory-trimmed. This process typically results in much less error compared to the combined gain error of the INA and external R_G. For example, the typical gain error of the ADS1235 is 0.05%. While the INA826 gain error is 0.04%, this does not include any additional gain error from R_G. For example, choosing an R_G resistor that has an initial tolerance of 0.1% more than doubles the gain error compared to using the ADS1235 integrated PGA.

5.2 Noise

In data acquisition systems, noise is any unwanted signal that can interfere with or hide the signal of interest. Some noise is inherent to all electrical components, and it can come from sources internal (amplifiers, ADCs, voltage references, and so forth) or external (EMI, ground loops, line-cycle noise, and so forth) to the system. Noise is very important for bridge measurement systems because the bridge output voltage is typically on the order of 10s of millivolts. Such small signals require a low-noise, higher-resolution signal chain to achieve high dynamic range.

Even though noise is important for bridge measurement systems, complete signal chain noise analysis can be complex. As such, a comprehensive understanding of noise is beyond the scope of this application note. Instead, this document identifies how noise is reported in an ADC data sheet and how this information can be used to help achieve design targets for bridge measurement systems. For more information on noise in ADC measurements, see the *Fundamentals of Precision ADC Noise Analysis* e-book as well as the *ADC Noise* content in TI's Precision Labs training curriculum.

5.2.1 Noise in an ADC Data Sheet

ADC data sheets typically report noise with the inputs shorted (V_{IN} = 0 V). This configuration provides the purest measurement of ADC intrinsic noise, which also includes amplifier noise if the ADC has an integrated PGA. This measurement does not include voltage reference noise, which scales linearly with the input signal. However, this is generally not a concern for bridge measurement systems that use a ratiometric reference configuration where the voltage reference noise and drift tend to cancel out.

The actual values shown in an ADC noise table are comprised of several thousand data points or several seconds worth of data. Statistical analysis is performed on this data set to determine root-mean-square (RMS) and peak-to-peak values. For delta-sigma ADCs, this information is then reported for each combination of output data rate (ODR), filter type, and gain setting (if applicable).

For example, Table 5-1 shows a portion of the noise performance information from the ADS1235 data sheet. Each row in Table 5-1 is a different ODR and filter type combination while each column represents the available PGA gains.

Table 5-1. ADS1235 Noise and Resolution at T_A = 25°C and V_{REF} = 5 V

ODR	FILTER	Noise (μV_{RMS} (μV_{PP}))			Effective Resolution (bits)(Noise-Free Resolution (bits))		
		GAIN = 1	GAIN = 64	GAIN = 128	GAIN = 1	GAIN = 64	GAIN = 128
20 SPS	FIR	0.51 (2.1)	0.032 (0.16)	0.029 (0.16)	24 (22)	22.2 (19.9)	21.3 (18.9)
20 SPS	Sinc1	0.44 (2.1)	0.025 (0.13)	0.026 (0.13)	24 (22)	22.6 (20.2)	21.5 (19.2)
20 SPS	Sinc2	0.36 (1.2)	0.02 (0.12)	0.02 (0.1)	24 (22.8)	22.9 (20.4)	21.9 (19.5)
20 SPS	Sinc3	0.32 (1.5)	0.017 (0.089)	0.018 (0.096)	24 (22.5)	23.1 (20.8)	22 (19.6)
20 SPS	Sinc4	0.3 (1.2)	0.017 (0.084)	0.018 (0.1)	24 (22.8)	23.1 (20.8)	22.1 (19.6)
50 SPS	Sinc1	0.63 (3.6)	0.04 (0.25)	0.038 (0.23)	23.7 (21.2)	21.9 (19.2)	21 (18.4)
50 SPS	Sinc2	0.57 (3)	0.033 (0.21)	0.032 (0.18)	23.9 (21.5)	22.2 (19.5)	21.2 (18.7)
50 SPS	Sinc3	0.53 (2.4)	0.03 (0.19)	0.03 (0.17)	24 (21.8)	22.3 (19.7)	21.3 (18.8)
50 SPS	Sinc4	0.49 (2.4)	0.028 (0.15)	0.026 (0.16)	24 (21.8)	22.4 (20)	21.5 (18.9)
60 SPS	Sinc1	0.71 (3.9)	0.043 (0.27)	0.042 (0.26)	23.6 (21.1)	21.8 (19.1)	20.8 (18.2)
60 SPS	Sinc2	0.6 (3.3)	0.036 (0.24)	0.034 (0.21)	23.8 (21.4)	22.1 (19.3)	21.1 (18.5)
60 SPS	Sinc3	0.56 (3)	0.032 (0.19)	0.03 (0.17)	23.9 (21.5)	22.2 (19.6)	21.3 (18.8)
60 SPS	Sinc4	0.53 (2.7)	0.031 (0.19)	0.03 (0.18)	24 (21.6)	22.3 (19.7)	21.3 (18.7)

The noise values in Table 5-1 are referred to the input (RTI). The RTI noise of the ADC measurement is the magnitude of the equivalent noise as seen at the input of the ADC after gain. For example, the noise in Table 5-1 is referred to a ±5-V range when the gain = 1 V/V. When gain = 128 V/V, the noise is referred to a significantly smaller ±39.06-mV range.

Table 5-1 also includes two figures of merit derived from the noise values: *effective resolution* and *noise-free resolution*. Effective resolution in an ADC data sheet is the dynamic range of the full-scale range (FSR) relative to the RMS noise in the measurement, $V_{N,RMS}$. Comparatively, noise-free resolution in an ADC data sheet is the dynamic range of the FSR relative to the peak-to-peak (PP) noise in the measurement, $V_{N,PP}$. These noise parameters are calculated using Equation 20 and Equation 21:

$$\text{Effective resolution} = \log_2(\text{FSR} / V_{N,RMS}) \text{ (bits)} \quad (20)$$

$$\text{Noise-free resolution} = \log_2(\text{FSR} / V_{N,PP}) \text{ (bits)} \quad (21)$$

For example, at gain = 128 V/V and ODR = 20 SPS, Table 5-1 shows that the ADS1235 finite impulse response (FIR) digital filter offers noise performance of 0.029 μV_{RMS} or 0.16 μV_{PP}. Equation 22 and Equation 23, respectively, calculate the ADS1235 effective resolution and noise-free resolution at these settings:

$$\text{Effective resolution} = \log_2[(\pm 5 \text{ V} / 128 \text{ V/V}) / (0.029\ \mu V_{RMS})] = \log_2[2{,}693{,}966] = 21.3 \text{ bits} \quad (22)$$

$$\text{Noise-free resolution} = \log_2[(\pm 5 \text{ V} / 128 \text{ V/V}) / (0.16\ \mu V_{PP})] = \log_2[488{,}281] = 18.9 \text{ bits} \quad (23)$$

Note that the results in Equation 22 and Equation 23 match the reported values in the last column of Table 5-1.

Bridge measurements often characterize performance using a third parameter called noise-free counts (NFC), which is derived from noise-free resolution. This is especially important for weigh scale applications where the design requires that the smallest digit displayed in the scale measurement is stable (or noise-free). Designing a weigh scale using effective resolution targets would likely result in the last digit on the scale constantly moving because effective resolution is based on the RMS noise.

NFC is defined by Equation 24 while Equation 25 calculates NFC for the given ADC parameters:

$$\text{NFC} = 2^{(\text{Noise-free resolution})} \text{ (counts)} \quad (24)$$

$$\text{NFC} = 2^{(18.9)} = 488{,}000 \text{ counts} \quad (25)$$

A weigh scale with level of performance described in Equation 25 might be acceptable, though it is important to consider how this parameter is defined. Specifically, noise-free resolution and NFC are calculated assuming that the ADC input uses the entire FSR. However, if the weigh scale system does not use the entire ADC FSR, the system NFC performance will be different than the values shown in the ADC noise table. This reduction in NFC performance is described in the following section.

5.2.2 Calculating NFC for a Bridge Measurement System

As described in Section 4.1, a bridge sensitivity of 2 mV/V and $V_{EXCITATION}$ = 5 V yields a maximum bridge output signal of 10 mV. Furthermore, the minimum weight measured by a weigh scale is zero, resulting in a minimum bridge output signal of 0 V. Therefore, the bridge output signal range is 0 to 10 mV, which is significantly smaller than the FSR of most ADCs even at the highest gain. For example, the ADS1235 FSR at a gain of 128 V/V was given as ±39 mV in the previous section. As such, a 0- to 10-mV input signal uses approximately one-eighth of the ADC FSR.

Substitute the *system signal range* for the ADC FSR in Equation 21 to calculate the expected noise-free resolution for a given bridge measurement design. Equation 26 returns the noise-free resolution for the 0- to 10-mV weigh scale signal range using the ADS1235 at gain = 128 V/V, ODR = 20 SPS, and the FIR filter (assuming a ratiometric 5-V V_{REF}):

$$\text{Noise-free resolution}_{(System)} = \log_2[(10\ \text{mV}) / (0.16\ \mu V_{PP})] = \log_2[62{,}500] = 15.9\ \text{bits} \quad (26)$$

Applying the result of Equation 26 to Equation 24 yields a new value for NFC shown in Equation 27:

$$\text{NFC}_{(System)} = 2^{(15.9)} = 63{,}000\ \text{counts} \quad (27)$$

Regardless of the construction of the measurement system, this noise analysis yields the noise floor of the final system. Moreover, the results from Equation 27 help determine if the ADC is sufficient to meet the target design specifications. If the NFC value is insufficient, selecting a different measurement configuration, a higher-precision ADC, or averaging the data output may reduce the noise to an acceptable level.

To help determine if an ADC can meet the target design specifications, use the *Bridge Sensor + ADC* tool in the Analog Engineer's Calculator. Figure 5-5 introduces this tool and shows how it can be used. Enter the system requirements on the left and the tool returns available ADC options that meet the design goals. Converting voltage to bits, bits to effective resolution, or bits to noise-free resolution can also be performed.

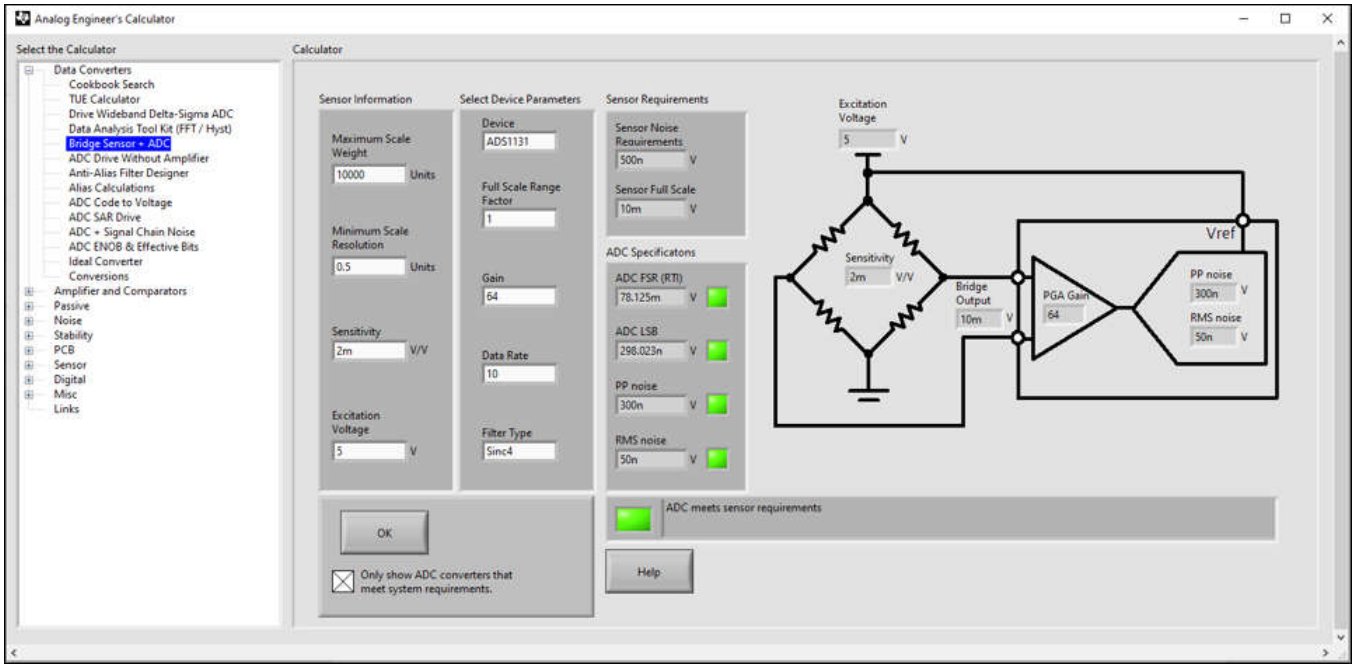

Figure 5-5. *Bridge Sensor + ADC* Tool in the Analog Engineer's Calculator

5.3 Channel Scan Time and Signal Bandwidth

In addition to low noise, bridge measurement systems often have channel scan time or input signal bandwidth requirements that can be affected by the ADC architecture. These applications typically use precision delta-sigma (ΔΣ) ADCs because they can offer resolution up to 32 bits and integrated PGAs. Precision ΔΣ ADCs use an oversampling topology where the input signal is sampled at a high frequency and converted to a digital bitstream by the ΔΣ ADC modulator. This bitstream is then filtered and decimated by the oversampling ratio (OSR) in the digital domain to yield a low-noise conversion result at the respective ODR.

The output noise depends on the OSR, where a larger OSR (or lower ODR) results in more data collected over a longer period of time and therefore lower noise. However, this also leads to extended ADC conversion latency and lower input signal bandwidth, though it may be possible to filter out line-cycle noise at lower data rates. The following subsections discuss these topics in more detail.

5.3.1 Noise Performance

As stated in the previous section, the ΔΣ ADC digital filter directly affects the system noise performance by taking data over a longer period of time as OSR increases (ODR decreases). This allows for lower measurement noise at lower data rates. Table 5-1 shows how the ADS1235 noise tends to reduce as ODR decreases.

It may also be possible to use external oversampling techniques to further reduce noise. If N number of ADC data points are collected and averaged by a microcontroller, the noise can be reduced by a factor of $\sqrt{N}$. For example, the ADS1235 noise at gain = 128 V/V, FIR filter, and ODR = 20 SPS is given in Table 5-1 as 0.029 μV_{RMS} and 0.16 μV_{PP}. Averaging 20 data points reduces the noise by a factor of $\sqrt{20}$ = 4.47 to 0.0065 μV_{RMS} and 0.036 μV_{PP}, respectively. However, the tradeoff to applying additional averaging is longer latency.

5.3.2 ADC Conversion Latency

One consequence of the digital filter is that it introduces some latency between the start of conversion and the final result. As previously stated, the ΔΣ ADC modulator output is collected over a specific period of time and the digital filter calculates the ADC data. Depending on the filter construction as well as other factors, the final ADC conversion data can be delayed by several conversion periods.

To quantify this delay, many precision ΔΣ ADCs include a conversion latency table in the data sheet. For example, Table 5-2 reports the ADS1235 conversion latency across all filter types (FIR and sinc) and ODRs.

Table 5-2. ADS1235 Conversion Latency

ODR (SPS)	CONVERSION LATENCY(1) - $t_{(STDR)}$ (ms)				
	FIR	SINC1	SINC2	SINC3	SINC4
2.5	402.2	400.4	800.4	1,200	1,600
5	202.2	200.4	400.4	600.4	800.4
10	102.2	100.4	200.4	300.4	400.4
16.6	—	60.43	120.4	180.4	240.4
20	52.23	50.43	100.4	150.4	200.4
50	—	20.43	40.43	60.43	80.43
60	—	17.09	33.76	50.43	67.09
100	—	10.43	20.43	30.43	40.43
400	—	2.925	5.425	7.925	10.43
1200	—	1.258	2.091	2.925	3.758
2400	—	0.841	1.258	1.675	2.091
4800	—	0.633	0.841	1.05	1.258
7200	—	0.564	0.702	0.841	0.98

(1) Chop mode off, conversion-start delay = 50 µs (DELAY[3:0] = 0001)

Table 5-2 shows that the FIR filter has a latency of approximately one conversion period, or about 50 ms, when ODR = 20 SPS for example. Table 5-2 also shows that the ADS1235 has sinc filters from first to fourth order. The sinc filter is the equivalent of a moving average filter of the previous data periods. For example, the $sinc^3$ filter is a third-order filter using a moving average of the previous three data points. Therefore, first data does not

appear until after the first three conversion periods, resulting in a latency of approximately 150 ms when ODR = 20 SPS. Second and subsequent conversion data may appear after the next conversion period depending on the conversion mode. Refer to the application note explaining ΔΣ ADC conversion latency for more detailed information on this topic.

Ultimately, bridge measurement systems requiring fast channel scan time or switching between multiple channels should always consider how ODR and digital filter type affect ADC conversion latency.

5.3.3 Digital Filter Frequency Response

Digital filters also have a specific frequency response that can affect how the signal is converted by the ADC. This response depends on the frequency of the input signal because the digital filter is collecting modulator outputs over a period of time. Figure 5-6 shows the frequency response of the different sinc filters in the ADS1235 at ODR = 50 SPS.

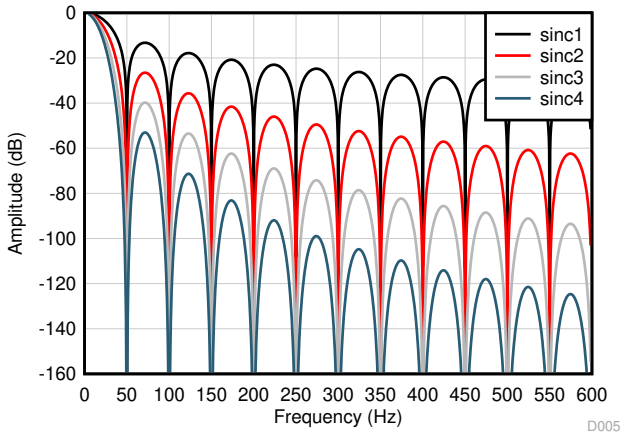

Figure 5-6. ADS1235 Sinc Filter Frequency Responses at ODR = 50 SPS

While not shown in Figure 5-6, the bandwidth of the ADS1235 sinc filters is significantly lower than the ODR. For example, the sinc[1] cutoff frequency is only 22.1 Hz at ODR = 50 SPS. Therefore, bridge measurement systems that need to sample signals with higher frequency components require a higher ODR or a wider bandwidth digital filter. Refer to the *Digital Filter Types in Delta-Sigma ADCs* application note for more detailed information on this topic.

Another consideration of the digital filter frequency response is the rejection of specific frequencies. Figure 5-7 shows the frequency response for the ADS1235 FIR filter at ODR = 20 SPS, while Figure 5-8 zooms in on the response at 50 and 60 Hz.

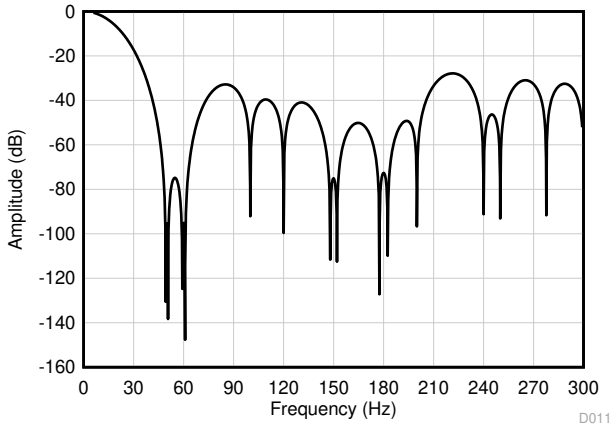

Figure 5-7. ADS1235 FIR Filter Frequency Response at ODR = 20 SPS

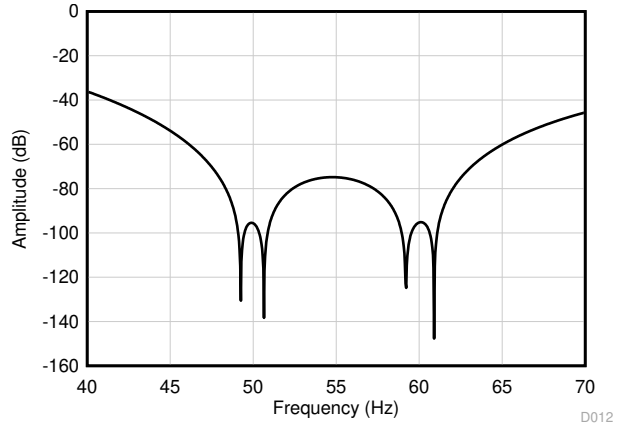

Figure 5-8. ADS1235 FIR Frequency Response Detail at ODR = 20 SPS

As Figure 5-8 shows, this digital filter frequency response is designed to reject 50-Hz and 60-Hz frequencies. For example, the ADS1235 attenuates an input signal at 50 Hz or 60 Hz (with up to a ±2 Hz deviation) by 94 dB. This is particularly useful to reduce line-cycle noise in the system. Moreover, the ADC digital filter can help reject this noise whether it couples in from the system supply or comes from other line-induced EMI.

5.4 AC Excitation

In addition to low noise, bridge measurement systems typically require high accuracy. As discussed in Section 4.4, AC excitation is one solution to remove offset error from a bridge measurement. This method is similar to amplifier chopping where the input channel is swapped between the positive and negative inputs. However, AC excitation swaps the polarity of $V_{EXCITATION}$ between the top (Phase 1) and bottom (Phase 2) of the bridge. The ADC measures the output of the bridge during both phases, subtracts the Phase 2 measurement from the Phase 1 measurement, and averages the result. This process cancels any systemic offsets after the bridge that can be caused by parasitic thermocouples or external amplifier offsets for example. This technique produces a measured result that is just the bridge output voltage.

Figure 5-9 shows an ADC bridge measurement during Phase 1 where $V_{EXCITATION}$ is at the top of the bridge, the bottom of the bridge is grounded, and an offset (V_{OS}) is shown as a source voltage between the bridge and the ADC.

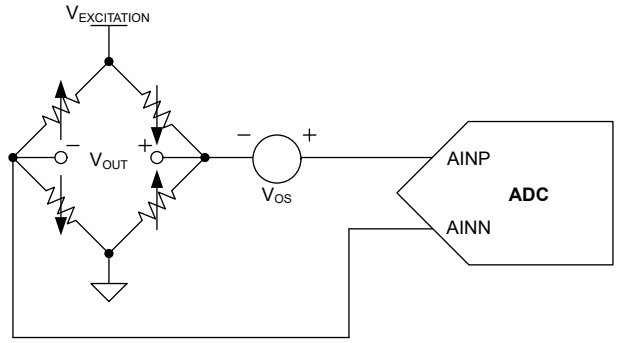

Figure 5-9. Bridge Measurement During AC Excitation (Phase 1)

Equation 28 calculates the voltage measured by the ADC during Phase 1:

$$\text{Phase 1} = \text{AINP} - \text{AINN} = +V_{OUT} + V_{OS} \quad (28)$$

After the first ADC measurement completes, Phase 2 swaps the bridge polarity such that $V_{EXCITATION}$ is routed to the bottom of the bridge and the top of the bridge is grounded. This swapping inverts the output voltage while maintaining the polarity of V_{OS}. The Phase 2 configuration is shown in Figure 5-10.

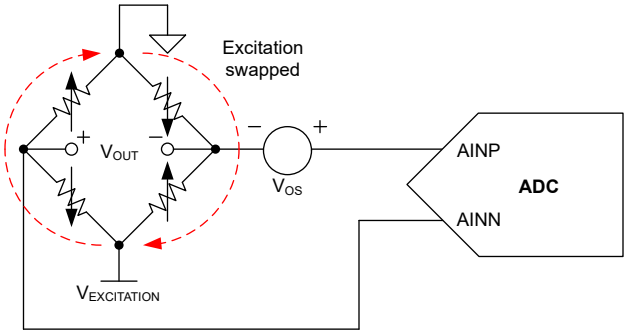

Figure 5-10. Bridge Measurement During AC Excitation (Phase 2)

Equation 29 calculates the voltage measured by the ADC during Phase 2:

$$\text{Phase 2} = \text{AINP} - \text{AINN} = -V_{OUT} + V_{OS} \quad (29)$$

Subtracting the result of Equation 29 from Equation 28 and dividing by two yields Equation 30:

$$(\text{Phase 1} - \text{Phase 2}) / 2 = [(+V_{OUT} + V_{OS}) - (-V_{OUT} + V_{OS})] / 2 = V_{OUT} \quad (30)$$

Ultimately, Equation 30 shows that V_{OS} cancels out and the final result is just V_{OUT}, thereby removing the total offset error after the bridge. However, it is important to note that systemic offsets that occur inside the bridge or before the chopping circuitry are not removed by AC excitation. Instead, use calibration to remove the inherent bridge offset.

Implementing AC excitation requires external transistors, gate drivers, or other switches to swap the bridge excitation voltage polarity. General purpose outputs (GPOs) from the ADC or host typically control the switching, and should be implemented with non-overlapping clocks to prevent bridge cross-conduction during voltage reversal.

Several TI precision ADCs are designed to implement AC excitation. The ADS1235 has specific pins to control external switches that swap the bridge polarity. For more information about implementing AC excitation for bridge measurements, see the *Reduce Bridge Measurement Offset and Drift Using the AC Excitation Mode* application note.

5.5 Calibration

Achieving high-accuracy results from a bridge measurement system can require calibration. Choose one of three calibration methods depending on the overall accuracy requirements:

- A one-point offset error calibration – easy to implement, offers some accuracy improvement
- A two-point offset and gain error calibration – improved accuracy, requires two measurements
- A piecewise-linear calibration – highest accuracy, ideal for nonlinear systems and calibration over temperature, requires several calibration points or a look-up table (LUT)

This document focuses on the two-point calibration method because it can significantly improve the system accuracy through a relatively simple calibration process.

The first step of a two-point calibration calculates the offset error, while the second step uses a test load to determine the gain error. A two-point calibration assumes that both the bridge response and the ADC measurement are linear. This assumption helps the user determine how the actual measurements deviate from the ideal measurements using the equation for a line:

$$y = M \cdot x + B \quad (31)$$

Figure 5-11 plots the ideal response of a bridge measurement with a green line that has some slope (M_{Ideal}) and y-intercept (B_{Ideal}) that is equal to zero. Comparatively, the actual bridge measurement response in red has a slope (M_{Actual}) that is not equal to M_{Ideal} as well as a nonzero y-intercept (B_{Actual}).

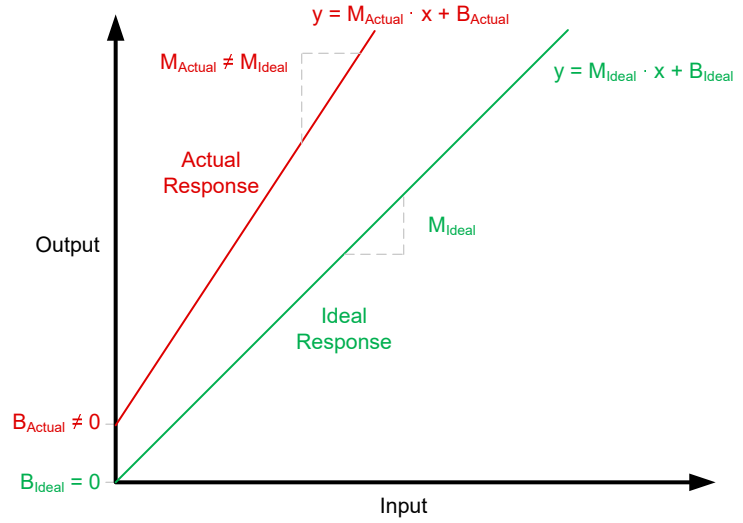

Figure 5-11. Bridge Measurement Response: Ideal vs Actual

The calibration process calculates the values of B_{Actual} and a scaling factor related to M_{Actual} in Figure 5-11, which helps remove the offset error and gain error, respectively. Figure 5-11 specifically shows a positive offset and gain error, though it is possible for one or both of these errors to be negative. This information is then used to accurately correlate the system input to the ADC output. For example, Figure 5-12 shows how calibration might be implemented for a weigh scale system.

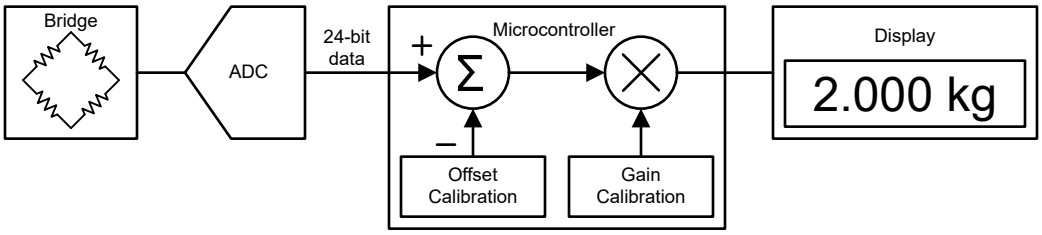

Figure 5-12. Block Diagram for a Weigh Scale Application with Calibration

In Figure 5-12, an ADC measures a bridge using a ratiometric configuration. A microcontroller captures the data from the ADC, then calculates and stores the calibration values. The offset calibration stores a value for B_{Actual}, while the gain calibration stores a scaling factor, M, that is related to M_{Actual}. The microcontroller then subtracts B_{Actual} from the ADC measurement and scales the result by M. Finally, a display shows the calculated result.

The following two subsections step through the offset and gain calibration process for a generic bridge system that might measure physical parameters such as weight, pressure, or flow. The final subsection applies this information to an example calculation for the weigh scale system shown in Figure 5-12.

5.5.1 Offset Calibration

The first calibration step is to measure and remove the offset voltage. Offset may come from an inherent bridge imbalance, from the signal conditioning circuitry, or both. Offset is the measured value that represents zero applied load, and can be either positive or negative. During an offset calibration, the ADC measures the system output with no applied load. The resulting ADC code is stored as the offset calibration constant. The microcontroller subtracts this offset value from subsequent ADC measurements before calculating the measured weight. Note that the offset measurement itself has some noise. Reduce the noise of the stored offset voltage by averaging multiple consecutive offset measurements.

Figure 5-13 shows how an offset calibration changes the bridge measurement response before (red) and after (blue) the calibration process.

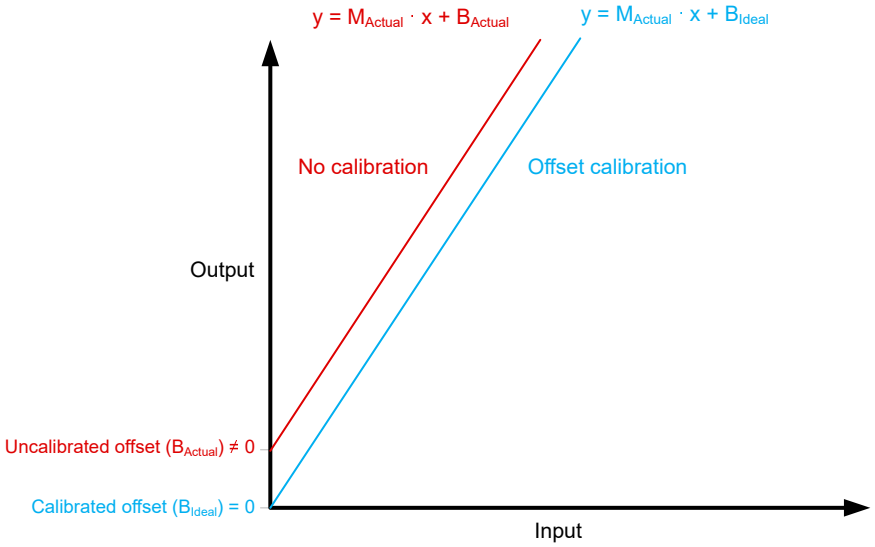

Figure 5-13. First Calibration Step Calculates and Remove Offset (B_{Actual})

Figure 5-13 reveals that the purpose of an offset calibration is to measure the y-axis intercept (B_{Actual}) of the uncalibrated response. This value is then removed from the final result so that the system output is zero with no load applied, similar to B_{Ideal}. The calibration process therefore shifts the bridge measurement response from the red, uncalibrated plot to the blue, calibrated plot. This first step describes a one-point calibration as per Section 5.5.

One important characteristic of both plots in Figure 5-13 is that the blue, calibrated response has the same slope (M_{Actual}) as the red, uncalibrated response. In other words, the blue, calibrated response can still have a significant gain error compared to the green, ideal response from Figure 5-11. The second calibration step corrects this issue by calculating the slope of the actual bridge response to help determine the gain error.

5.5.2 Gain Calibration

After completing offset calibration, correct any gain error by first applying a calibrated test load to the system. For example, a weigh scale would use a calibrated weight. This test load does not necessarily need to be the maximum load of the measurement system. Instead, the test load should be large enough to accurately determine the slope of the bridge measurement response over the target measurement range. Typically, choosing a test load that is 80% or more of the target measurement range is sufficient. A scaling factor relative to the slope of the bridge measurement response is then stored in the microcontroller as the gain calibration coefficient. Similar to offset calibration, gain calibration measurements have noise that can be reduced by averaging multiple ADC samples.

Figure 5-14 illustrates how measuring the test load helps identify a gain error between the blue plot (offset calibration only) and the green, ideal response.

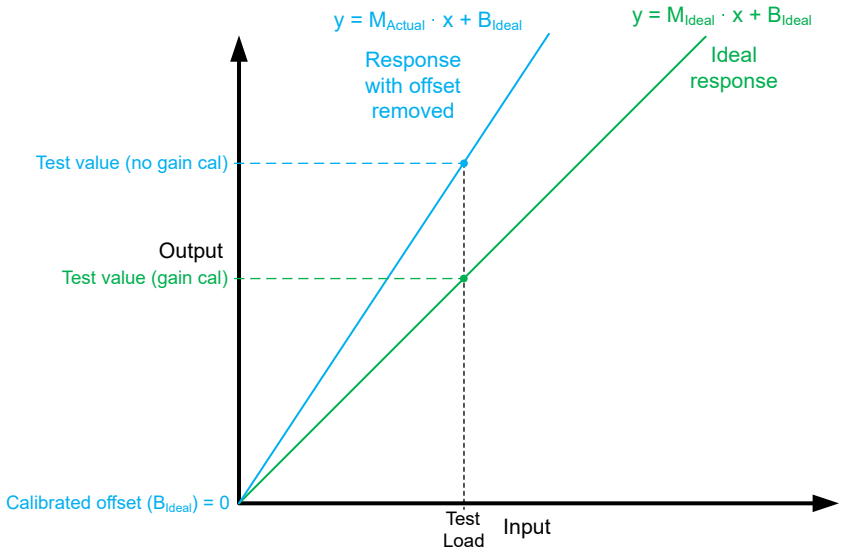

Figure 5-14. Gain Calibration Calculates the Scaling Factor (M_{Actual}) from the Test Load

The gain calibration in Figure 5-14 identifies the slope of the blue curve, M_{Actual}, using the test load as a reference. A scaling factor, M, related to M_{Actual} is then stored in a microcontroller similar to the block diagram in Figure 5-12. This value of M as well as B_{Actual} from the offset calibration are used to accurately determine the value of any arbitrary applied load: first, subtract B_{Actual} from the measured ADC code; and second, multiply the result by M.

While this simple, two-point calibration process accounts for the majority of the DC error seen in a bridge measurement, it does not account for non-linearity or drift. A piecewise calibration can be used to account for these errors, though this requires many measurements across the full input span and temperature range (see Section 5.5). However, these errors are typically small and are often accounted for in the design error budget.

5.5.3 Calibration Example

To better understand how the calibration process works, the following section steps through a weigh scale example using the load cell properties from Table 4-1 and the ADS1235. The example load cell has a nominal bridge sensitivity of 2 mV/V and the weight capacity is 2 kg. Assuming $V_{EXCITATION}$ = 5 V, the ideal full-scale bridge output voltage, $V_{OUT(Ideal)}$, is 2 mV/V • 5 V = 10 mV. This is the expected output from the bridge when a 2-kg weight is placed on the scale. $V_{OUT(Ideal)}$ is also the input voltage, $V_{IN(Ideal)}$, measured by the ADC.

The general formula for an ADC output code is given by Equation 32:

$$\text{ADC output code} = (2^N \bullet \text{Gain} \bullet V_{IN}) / (A \bullet V_{REF}) \quad (32)$$

where:

- N is the ADC resolution
- A is a scaling factor related to the ADC analog voltage range (refer to Section 6.1.5 for more information)

For the ADS1235, N = 24 and A = 2. Using the ADS1235 with a ratiometric reference configuration ($V_{REF} = V_{EXCITATION} = 5$ V) and a PGA setting of 128 V/V, a 10-mV signal yields the ideal ADC output code, ADC_{Ideal}, given by Equation 33:

$$ADC_{Ideal} = (10 \text{ mV} / 78.125 \text{ mV}) \bullet 2^{24} = 2{,}147{,}483 \quad (33)$$

Equation 33 reveals that an error-free system should provide an ADC code value of 2,147,483 when the 2-kg weight is applied and an ADC code value of 0 when the weight is removed ($V_{IN(Ideal)} = 0$ V). Figure 5-15 shows the ideal bridge response using the example parameters.

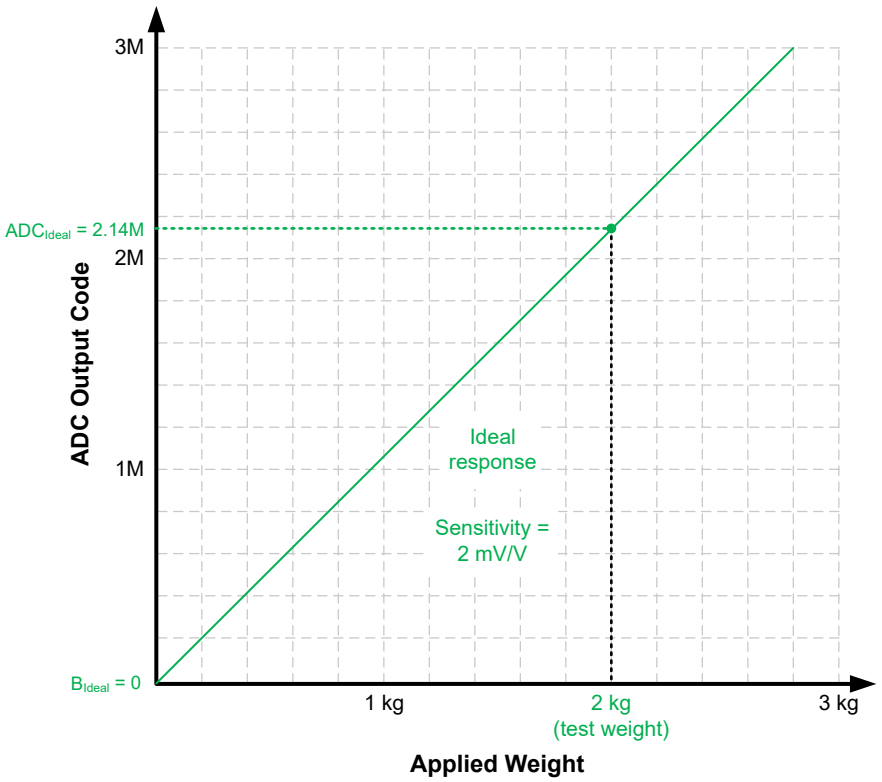

Figure 5-15. Ideal Response for the Example Bridge Measurement System

For this example, the input to the system (x-axis) in Figure 5-15 is the applied weight and the system output is the ADC code (y-axis). The system output used to determine the calibration coefficients should be ADC codes because the calibration process executed by the microcontroller uses an ADC code as an input (see Figure 5-12).

Unfortunately, a real system will always have some errors compared to the ideal response in Figure 5-15, reducing the system accuracy. For example, the ADC and amplification stage have inherent errors, while the choice of bridge connection can introduce a gain error. Even the load cell has an inherent offset (*zero balance*) and gain error (*sensitivity tolerance*), as per Table 4-1. The system-level offset and gain error are the combined error from all of these different sources. Figure 5-16 shows how each system error might impact the green, ideal bridge response from Figure 5-15, resulting in the actual bridge response in red with unknown slope and y-intercept.

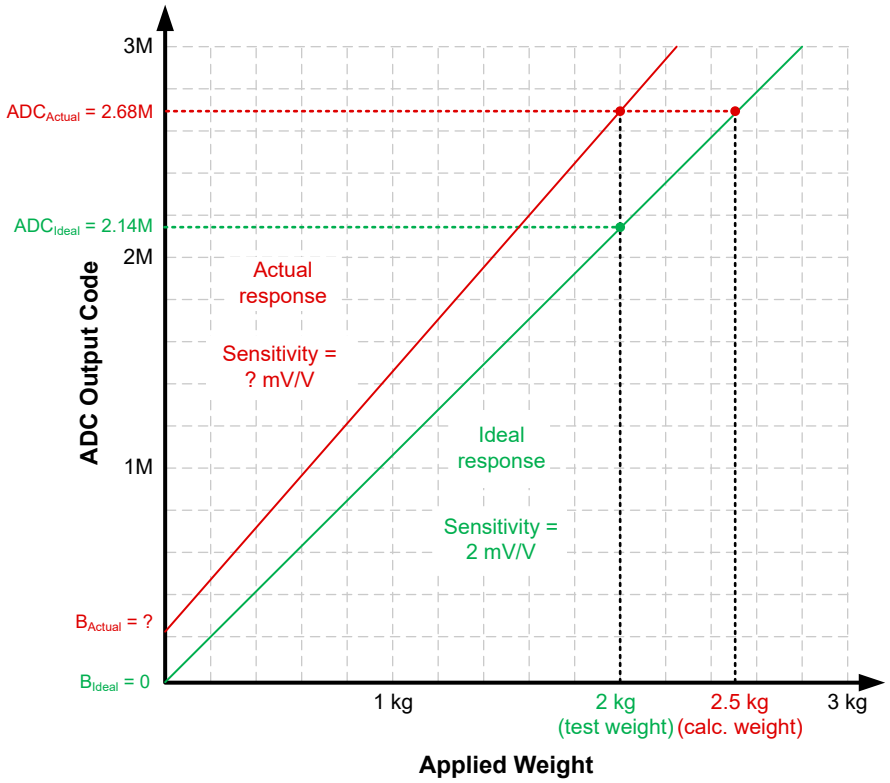

Figure 5-16. Actual vs Ideal Response for the Example Bridge Measurement System

The important takeaway from Figure 5-16 is that there is no way to correlate the measured ADC output code to the actual applied weight without knowing the value of B_{Actual} and the slope of the red bridge response. When the user applies a 2-kg test weight to this example system, the resulting output code, ADC_{Actual}, is 2,684,355. An ADC code of 2,684,355 corresponds to an applied load of 2.5 kg because the user assumes the system follows the green, ideal response. This outcome results in a 25% error at full-scale. Ultimately, calibration is necessary to determine the actual bridge response, reduce these errors, and maintain high-accuracy results.

To calibrate this weigh scale, first perform an offset calibration. In this example, B_{Actual} is measured to be 214,748 codes with no applied weight. Equation 32 can be used to back-calculate that 214,748 codes is approximately 1 mV (or 0.2 kg) when $V_{EXCITATION} = V_{REF} = 5$ V. This value represents the total system offset from all error sources.

The value of B_{Actual} is used to adjust the displayed weight to 0 kg when no load is present on the scale. Figure 5-17 shows how the offset calibration in this example translates the red, uncalibrated bridge response down to the blue, offset-calibrated bridge response. The weigh scale images on the right side of the figure indicate how the scale display changes before (in red) and after (in blue) the offset calibration.

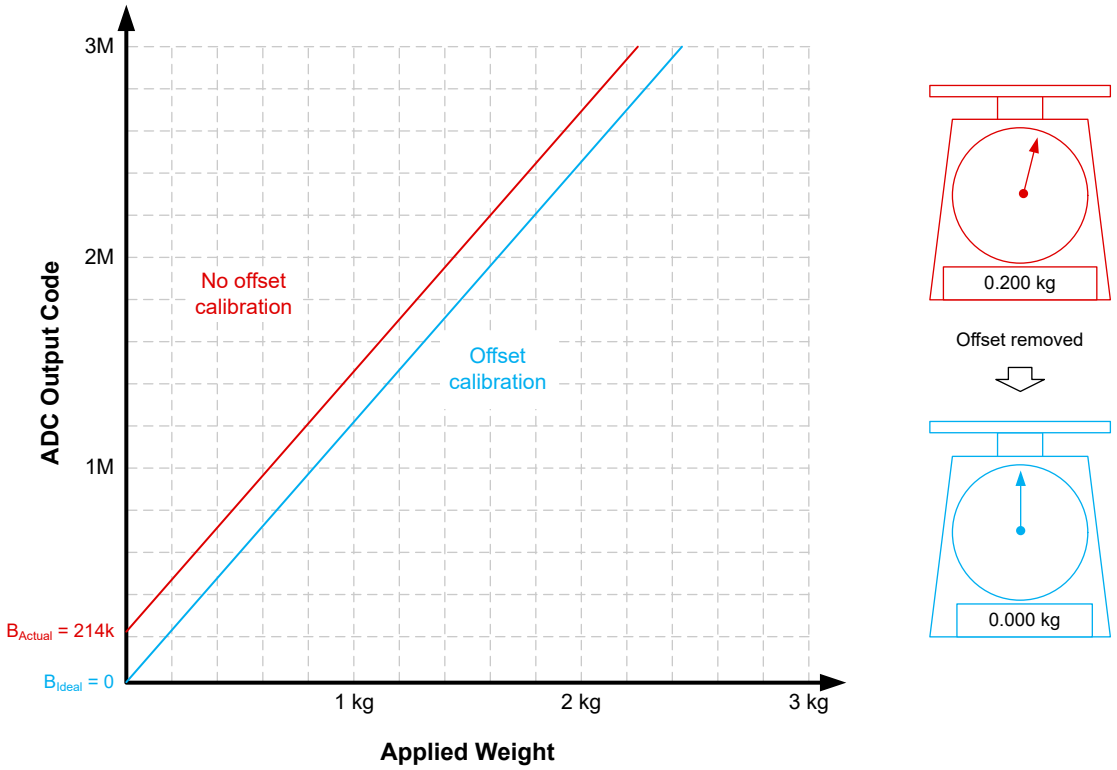

Figure 5-17. Performing an Offset Calibration for the Example Weigh Scale System

The blue response in Figure 5-17 still has a gain error relative to the green, ideal bridge response shown in Figure 5-15. This example corrects that gain error by performing a gain calibration using a calibrated 2-kg test weight, $W_{Calibrated}$. The ADC measures $W_{Calibrated}$ and produces an output code, $ADC_{Calibrated}$, of 2,469,606, which is equal to 2.3 kg. Figure 5-18 compares the ideal response of the 2-kg test weight to the measured response in the offset-free system. The weigh scale images on the right side of the figure indicate how the scale display changes before (in blue) and after (in green) the gain calibration.

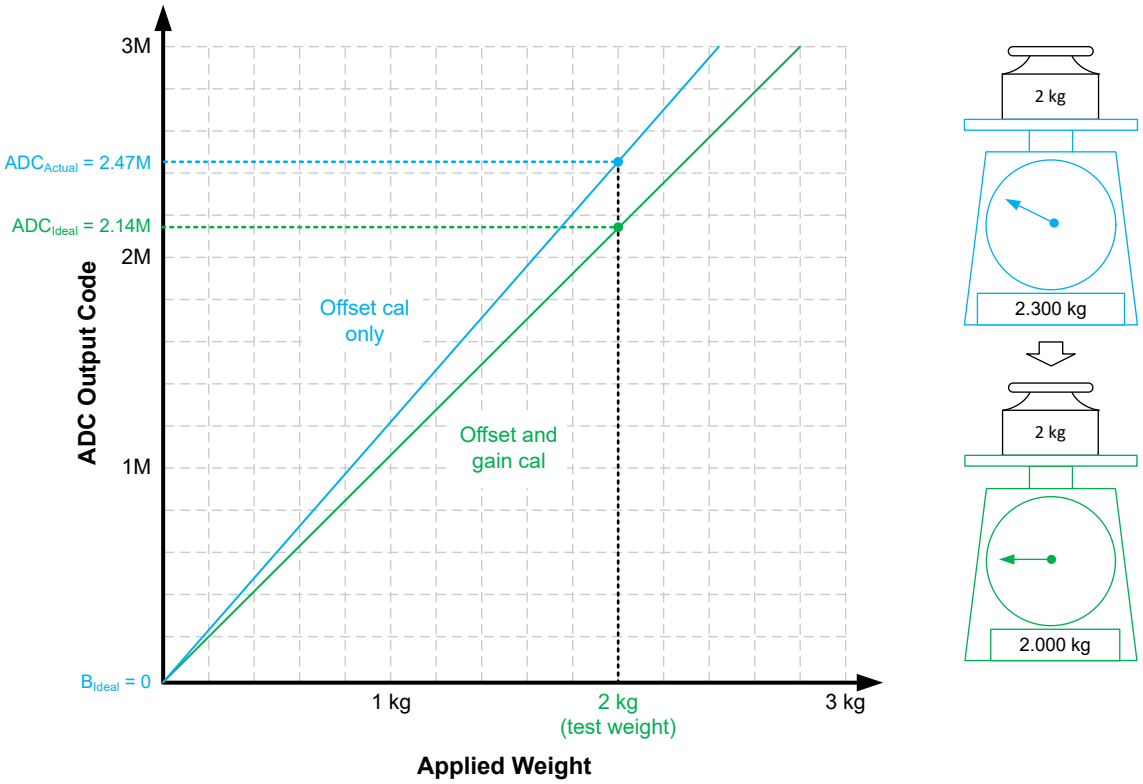

Figure 5-18. Performing a Gain Calibration for the Example Weigh Scale System

As Figure 5-18 shows, the scale displays a value of 2.3 kg even after the offset calibration, resulting in a 15% error at full-scale. This value represents the total system gain error from all error sources. To correct this gain error and accurately display the value of the 2-kg weight, it is necessary to derive the scaling factor, M. Equation 34 shows how to calculate M from the measured parameters:

$$M = W_{Calibrated} / (ADC_{Calibrated} – B_{Actual}) \quad (34)$$

One important takeaway from Equation 34 is that the value of $W_{Calibrated}$ directly impacts the calculation of M and therefore the accuracy of the gain calibration. As a result, ensure that the test load used in the system is calibrated properly and handled with care such that its physical properties are not altered.

Using the values provided in this example yields the result in Equation 35:

$$M = 2 \text{ kg} / (2{,}469{,}606 – 214{,}748) = 2 \text{ kg} / 2{,}254{,}858 = 8.87 \cdot 10^{-7} \text{ kg/code} \quad (35)$$

Equation 36 combines these results to derive the corresponding applied weight, W, from any ADC output code, ADC_{Result}:

$$W = (M \cdot ADC_{Result}) – (M \cdot B_{Actual}) = M \cdot (ADC_{Result} - B_{Actual}) \quad (36)$$

Using the values provided in this example yields the result in Equation 37:

$$W = (8.87 \cdot 10^{-7} \text{ kg/code}) \cdot (ADC_{Result} – 214{,}748) \quad (37)$$

Equation 37 can be used to determine the value of any arbitrary weight applied to the scale in this example. If ADC_{Result} = 1,000,000 for example, then W = 0.697 kg. Figure 5-19 shows how to apply the specific values derived in this example to the calibration block diagram shown in Figure 5-12.

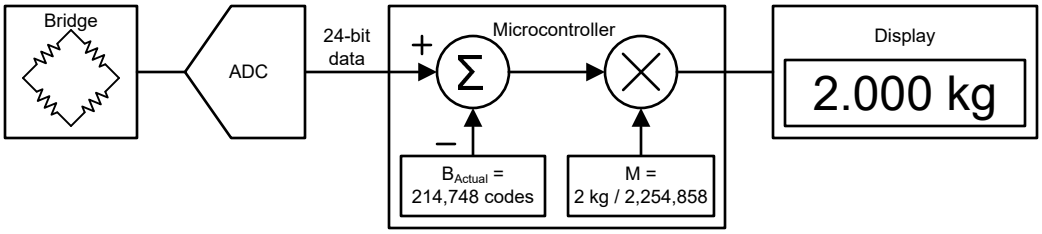

Figure 5-19. Weigh Scale Block Diagram With Example Calibration Coefficients

The values used in this example are theoretical and not meant to represent the behavior of any specific system. It is also important to remember that real systems have multiple sources of offset and gain error that all need to be considered, though it is possible that one error source might dominate. In any case, this calibration process can be applied to any bridge measurement system to remove some of the most common error sources and maintain high-accuracy results.

6 Bridge Measurement Circuits

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

The following sections explore design considerations for different bridge configurations that vary by excitation voltage, bridge connection, excitation source, signal conditioning circuitry, and the number of measured sensors. Each section provides the basic topology with benefits and challenges for the circuit. Important parameters and variables are given for each bridge configuration. A basic theory of operation is provided with notes to guide important design considerations. Each circuit use a single ADC with a multiplexer to measure the bridge.

Conversion results are shown with a generic 24-bit bipolar ADC using the positive full-scale range of the device. Calculate 16-bit ADC conversions using similar methods. Results are shown as functions of the output code as well as the applied load. Each section ends with generic register settings that can be modified for a specific ADC to measure the desired bridge configuration.

Table 6-1 highlights the characteristics of each circuit and provides links to each:

Table 6-1. Summary of Bridge Measurement Circuit Characteristics

Link	Bridge Type	# of Bridges	# of Measurement Channels	Reference Configuration	Excitation Source (Polarity | Voltage)
Circuit #1	4-wire	1	1	Ratiometric	Unipolar | +5 V
Circuit #2	6-wire	1	1	Ratiometric	Unipolar | +5 V
Circuit #3	4-wire	1	1	Pseudo-Ratiometric	Unipolar | +15 V
Circuit #4	4-wire	1	1	Pseudo-Ratiometric	Bipolar | +10V, –5V
Circuit #5	4-wire	1	1	Ratiometric	Current Excitation
Circuit #6	4-wire	2 (series)	2	Pseudo-Ratiometric	Unipolar | +5 V
Circuit #7	4-wire	4 (parallel)	1	Ratiometric	Unipolar | +5 V
Circuit #8	4-wire	4 (parallel)	4	Ratiometric	Unipolar | +5 V

6.1 Four-Wire Resistive Bridge Measurement with a Ratiometric Reference and a Unipolar, Low-Voltage (≤5 V) Excitation Source

A typical four-wire resistive bridge measurement circuit uses a ratiometric reference configuration and a constant voltage to excite the sensor. Figure 6-1 shows a schematic for a bridge measurement using a 5-V supply, an ADC, and a ratiometric reference. The ADC uses the excitation voltage as both the analog supply and differential reference voltage to help eliminate errors due to noise and drift in the excitation source.

6.1.1 Schematic

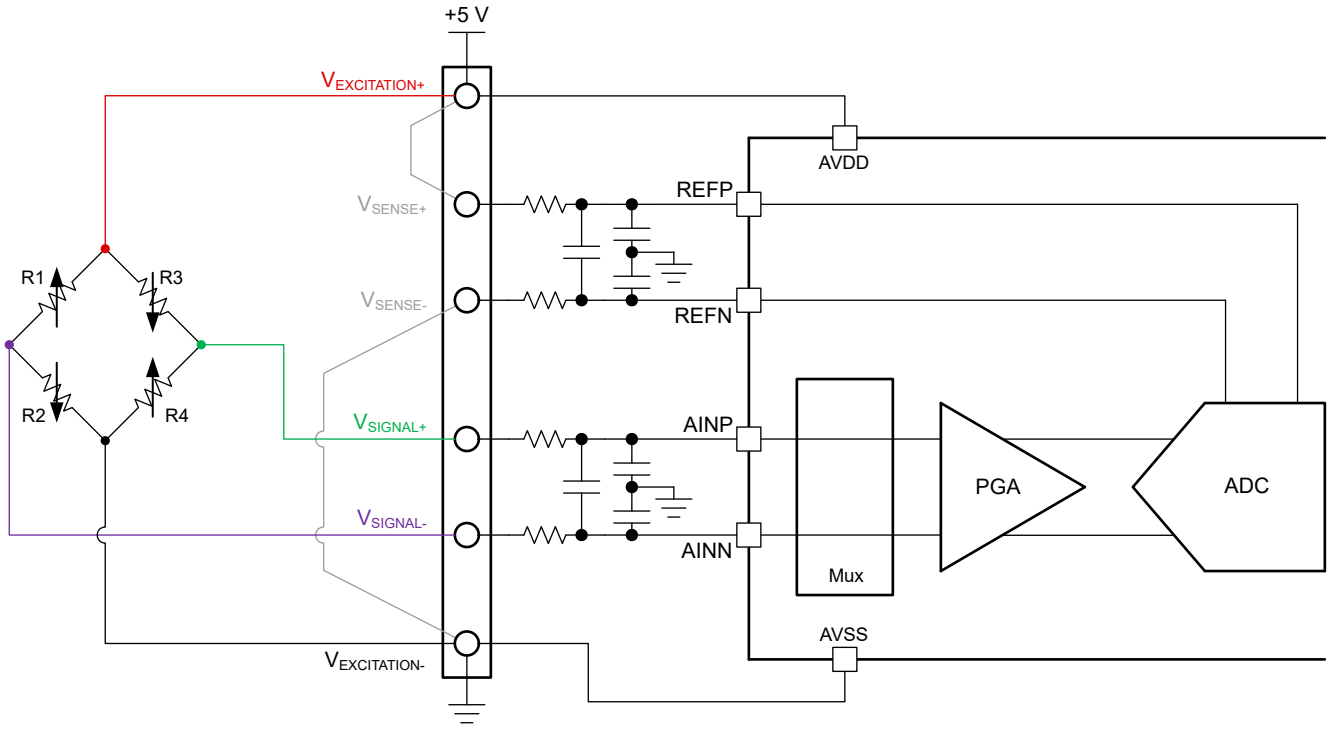

Figure 6-1. Four-Wire Resistive Bridge Measurement with a Ratiometric Reference and a Unipolar, Low-Voltage (≤ 5 V) Excitation Source

6.1.2 Pros and Cons

Pros:

- Simple implementation requiring only a few passive components
- Ratiometric measurement such that excitation source noise and drift are canceled
- Good for local measurements where the wire length is short

Cons:

- Extended-length sensor wires can lead to IR losses such that $V_{EXCITATION} \neq V_{REF}$
- Excitation voltage is limited to ADC V_{REF} range
- Bridge common-mode voltage is limited by ADC analog input range

6.1.3 Parameters and Variables

Table 6-2 defines important parameters and Table 6-3 provides equations for different variables. These parameters and variables are specific to this bridge configuration.

Table 6-2. User-Defined System Parameters

Parameter	Description
$V_{EXCITATION}$	Bridge excitation voltage
Bridge Sensitivity	Change in bridge output voltage relative to excitation voltage
$Load_{(Bridge\ Max)}$	Maximum load that can be applied to the bridge
$Load_{(System\ Max)}$	Maximum load applied to the bridge in the system (can be ≤ $Load_{(Bridge\ Max)}$)
$V_{CM(ADC)}$	Target common-mode voltage for inputs to the ADC (typically AVDD / 2)

Table 6-3. Variable Equations and Definitions

Variable	Equation	Description
$V_{OUT(Bridge\ Max)}$	$V_{EXCITATION}$ • Bridge Sensitivity	Maximum differential output voltage of the bridge
$V_{OUT(System\ Max)}$	($V_{OUT(Bridge\ Max)}$ • $Load_{(System\ Max)}$) / $Load_{(Bridge\ Max)}$	Maximum differential bridge output voltage used in the system (can be ≤ $V_{OUT(System\ Max)}$)
$V_{CM(Bridge)}$	($V_{EXCITATION+}$ + $V_{EXCITATION–}$) / 2	Bridge output common-mode voltage
V_{IN}	$V_{SIGNAL+}$ – $V_{SIGNAL–}$	Differential input voltage to the ADC
V_{REF}	$V_{EXCITATION+}$ – $V_{EXCITATION-}$	Differential reference voltage to the ADC

6.1.4 Design Notes

The unipolar excitation voltage applied to the bridge, $V_{EXCITATION}$, is also used as the ADC supply voltage (AVDD) as well as the ADC reference voltage, V_{REF}. Small variations in the bridge resistance due to tension or compression cause the differential bridge output voltage to change. The PGA integrated into the ADC gains up this low-level signal to reduce system noise and utilize more of the ADC full-scale range (FSR). The ADC samples and converts this amplified voltage against V_{REF}, which is the same voltage used to excite the bridge and therefore ratiometric. The excitation source noise and drift are seen equally in both V_{IN} and V_{REF} in a ratiometric reference configuration, effectively removing these errors from the ADC output code.

A four-wire resistive bridge measurement with a ratiometric reference and a unipolar, low-voltage (≤ 5) supply requires:

- Differential analog inputs (AINP and AINN)
- External reference input (dedicated pin ***or*** use analog supply)
- Low-noise amplifier

First, identify the maximum differential output voltage of the bridge, $V_{OUT(Bridge\ Max)}$, using the equation from Table 6-3 and parameters from Table 6-2. This value provides the maximum output voltage possible from the bridge under normal operating conditions and corresponds to the maximum load that can be applied to the bridge, $Load_{(Bridge\ Max)}$. If the system does not use the entire output range of the bridge, $V_{OUT(System\ Max)}$ defines the maximum differential output signal that is applied to a specific system and $Load_{(System\ Max)}$ is the corresponding maximum load. For example, if $V_{OUT(Bridge\ Max)}$ corresponds to $Load_{(Bridge\ Max)}$ = 5 kg, but the system specifications only require that $Load_{(System\ Max)}$ = 2.5 kg, then $V_{OUT(System\ Max)}$ is given by Equation 38:

$$V_{OUT(System\ Max)} = V_{OUT(Bridge\ Max)} \times (2.5\ kg / 5\ kg) = V_{OUT(Bridge\ Max)} / 2 \quad (38)$$

Note that if $Load_{(System\ Max)} = Load_{(Bridge\ Max)}$, then $V_{OUT(System\ Max)} = V_{OUT(Bridge\ Max)}$.

After $V_{OUT(System\ Max)}$ has been determined, choose the corresponding gain value for the ADC PGA. The amplifier gain should be the largest allowable value that is still less than the ADC FSR. In some cases it is not possible to choose an amplifier gain that uses the entire ADC FSR. While this is often an acceptable tradeoff

between resolution and ease-of-use, care should be taken to ensure that all system requirements are still met when the ADC FSR cannot be maximized.

Next, ensure that the bridge common-mode voltage, $V_{CM(Bridge)}$ (see Table 6-3), is within the common-mode range of the ADC amplifier, $V_{CM(ADC)}$, under a no-load condition (R1 = R2 = R3 = R4). The amplifier common-mode range varies by component, and will be defined in the data sheet based on the gain setting and supply voltage. However, targeting $V_{CM(Bridge)}$ = AVDD / 2 is a good choice as this is typically in the middle of the $V_{CM(ADC)}$ range, enabling the highest gain possible per the previous step. Moreover, the bridge configuration in Figure 6-1 inherently sets $V_{CM(Bridge)}$ to AVDD / 2 under a no-load condition when $V_{EXCITATION}$ = AVDD.

Finally, follow the instructions in Section 5.5 if calibration is required.

6.1.5 Measurement Conversion

To better understand how the output code is determined, it is helpful to know how the least significant bit, or LSB, is calculated as per Equation 39:

$$LSB = FSR / 2^N = (A \cdot V_{REF} / gain) / 2^N \quad (39)$$

where:

- N is the ADC resolution
- A is a scaling factor related to the ADC analog voltage range

The ADC analog input voltage range information is generally found in either the *Electrical Characteristics* or *Recommended Operating Conditions* table in the data sheet. After identifying this range, the scaling factor A can be derived using the following examples:

- A = 4 if FSR = ±2 • V_{REF} / gain
- A = 2 if FSR = ±V_{REF} / gain
- A = 1 if FSR = ±0.5 • V_{REF} / gain
- A = 1 if FSR = 0 to V_{REF} / gain

Note that each FSR equation in the preceding list includes a gain term for completeness even though the scaling factor A is independent of gain. Using this information, the output code is defined by Equation 40 and the applied load, W, can be calculated using Equation 41:

$$Output\ Code = (2^N \cdot Gain \cdot V_{IN}) / (A \cdot V_{REF}) \quad (40)$$

$$W = M \cdot (Output\ Code - B_{Actual}) \quad (41)$$

where:

- M is a calculated scaling factor
- B_{Actual} is the measured offset

Refer to Section 5.5.3 for more information about how Equation 41 is derived.

6.1.6 Generic Register Settings

- Select multiplexer settings for AINP and AINN to measure V_{IN}
- Enable the amplifier and set gain to the desired value as per the instructions in this section
- Select data rate and digital filter settings, as per Section 5.2.1 and Section 5.3
- Select reference input to measure V_{REF} for ratiometric measurement

6.2 Six-Wire Resistive Bridge Measurement With a Ratiometric Reference and a Unipolar, Low-Voltage (≤ 5 V) Excitation Source

A typical six-wire resistive bridge measurement circuit uses a ratiometric reference configuration and a constant voltage to excite the sensor. Figure 6-2 shows a schematic for a bridge measurement using a 5-V supply, an ADC, and a ratiometric reference. The ADC uses the excitation voltage as the analog supply as well as the differential reference voltage to help eliminate errors due to the noise and drift in the excitation source. Moreover, the additional V_{SENSE} lines help eliminate IR losses due to wire resistance in extended-length cables.

6.2.1 Schematic

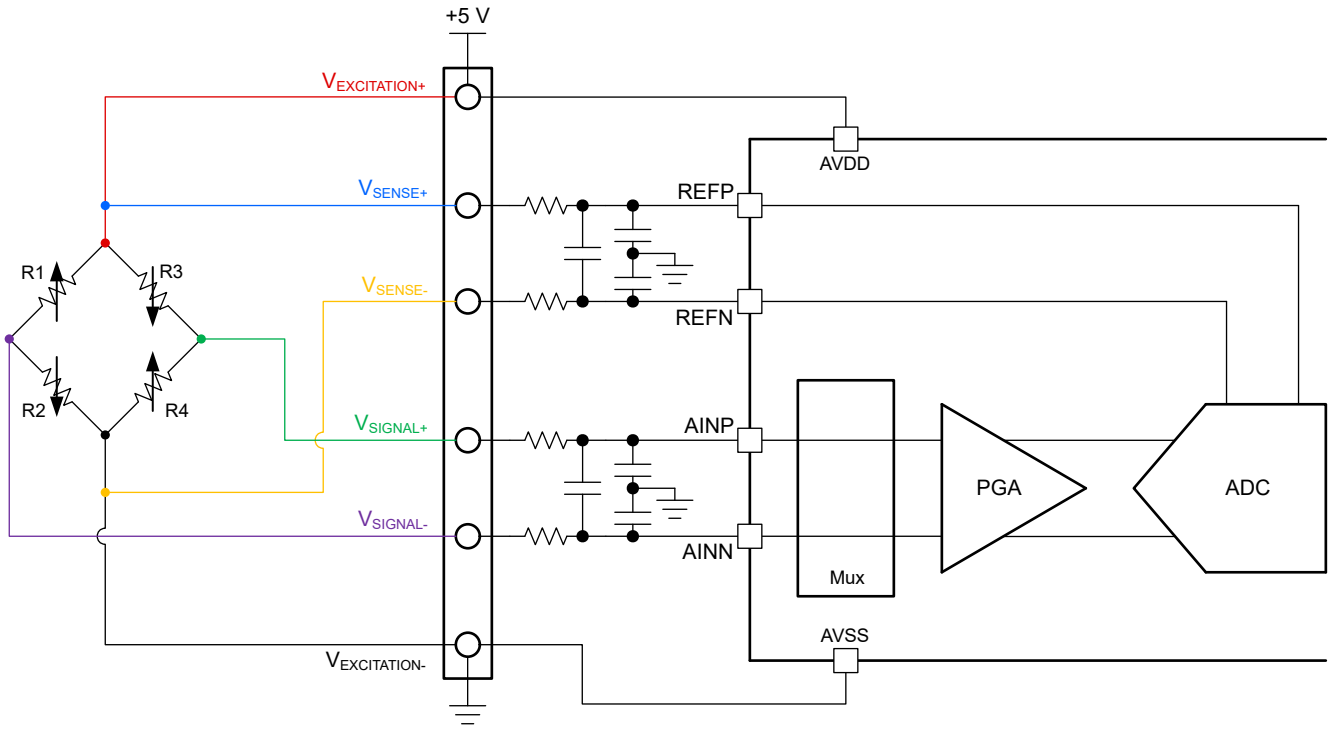

Figure 6-2. Six-Wire Resistive Bridge Measurement With a Ratiometric Reference and a Unipolar, Low-Voltage (≤ 5 V) Excitation Source

6.2.2 Pros and Cons

Pros:

- Additional V_{SENSE} lines reduce IR losses as a result of long leads
- Simple implementation requiring only a few passive components
- Ratiometric measurement such that excitation source noise and drift are canceled

Cons:

- Six-wire sensors are typically more expensive compared to four-wire sensors
- Excitation voltage is limited to ADC V_{REF} range
- Bridge common-mode voltage is limited by ADC analog input range

6.2.3 Parameters and Variables

Table 6-4 defines important parameters and Table 6-5 provides equations for different variables. These parameters and variables are specific to this bridge configuration.

Table 6-4. User-Defined System Parameters

Parameter	Description
$V_{EXCITATION}$	Bridge excitation voltage
Bridge Sensitivity	Change in bridge output voltage relative to excitation voltage
$Load_{(Bridge\ Max)}$	Maximum load that can be applied to the bridge
$Load_{(System\ Max)}$	Maximum load applied to the bridge in the system (can be ≤ $Load_{(Bridge\ Max)}$)
$V_{CM(ADC)}$	Target common-mode voltage for inputs to the ADC (typically AVDD / 2)

Table 6-5. Variable Equations and Definitions

Variable	Equation	Description
$V_{OUT(Bridge\ Max)}$	$V_{EXCITATION}$ • Bridge Sensitivity	Maximum differential output voltage of the bridge
$V_{OUT(System\ Max)}$	($V_{OUT(Bridge\ Max)}$ • $Load_{(System\ Max)}$) / $Load_{(Bridge\ Max)}$	Maximum differential bridge output voltage used in the system (can be ≤ $V_{OUT(System\ Max)}$)
$V_{CM(Bridge)}$	($V_{EXCITATION+}$ + $V_{EXCITATION–}$) / 2	Bridge output common-mode voltage
V_{IN}	$V_{SIGNAL+}$ – $V_{SIGNAL–}$	Differential input voltage to the ADC
V_{REF}	V_{SENSE+} – $V_{SENSE–}$	Differential reference voltage to the ADC

6.2.4 Design Notes

In systems where long lead wires are used to connect the bridge to the terminal block, wire impedance can contribute a small voltage drop between the terminal block and the bridge itself. Under these circumstances, $V_{EXCITATION+} \neq V_{SENSE+}$ and $V_{EXCITATION-} \neq V_{SENSE-}$ in Figure 6-2. Therefore, simply shorting $V_{EXCITATION}$ to V_{REF} similar to Figure 6-1 causes a voltage mismatch between the REFP and REFN pins compared the actual voltage across the bridge, resulting in a gain error. The six-wire resistive bridge accounts for this voltage drop by including two sense lines in addition to the signal and excitation leads. These additional wires route the actual voltage seen at the top and bottom of the bridge to the REFP and REFN pins on the ADC, respectively.

The unipolar excitation voltage applied to the bridge, $V_{EXCITATION}$, is used as the ADC supply voltage (AVDD) but not as the ADC reference voltage, V_{REF}. Instead, the separate sense lines result in $V_{REF} = V_{SENSE+} – V_{SENSE-}$, which is slightly smaller compared to $V_{EXCITATION}$ but still ratiometric to the input voltage, V_{IN}. Small variations in the bridge resistance due to tension or compression cause the differential bridge output voltage to change. The PGA integrated into the ADC gains up this low-level signal to reduce system noise and utilize more of the ADC full-scale range (FSR). The ADC samples and converts this amplified voltage against V_{REF}, which has a ratiometric relationship to $V_{EXCITATION}$. The excitation source noise and drift are seen equally in both V_{IN} and V_{REF} in a ratiometric reference configuration, effectively removing these errors from the ADC output code.

A six-wire resistive bridge measurement with a ratiometric reference and a unipolar, low-voltage (≤ 5 V) supply requires:

- Differential analog inputs (AINP and AINN)
- Differential reference inputs (REFP and REFN)
- Low-noise amplifier

First, identify the maximum differential output voltage of the bridge, $V_{OUT(Bridge\ Max)}$, using the equation from Table 6-5 and parameters from Table 6-4. This value provides the maximum output voltage possible from the bridge under normal operating conditions and corresponds to the maximum load that can be applied to the bridge, $Load_{(Bridge\ Max)}$. If the system does not use the entire output range of the bridge, $V_{OUT(System\ Max)}$ defines the maximum differential output signal that is applied to a specific system and $Load_{(System\ Max)}$ is the corresponding maximum load. For example, if $V_{OUT(Bridge\ Max)}$ corresponds to $Load_{(Bridge\ Max)}$ = 5 kg, but the system specifications only require that $Load_{(System\ Max)}$ = 2.5 kg, then $V_{OUT(System\ Max)}$ is given by Equation 42:

$$V_{OUT(System\ Max)} = V_{OUT(Bridge\ Max)} \bullet (2.5\ kg / 5\ kg) = V_{OUT(Bridge\ Max)} / 2 \quad (42)$$

Note that if $Load_{(System\ Max)} = Load_{(Bridge\ Max)}$, then $V_{OUT(System\ Max)} = V_{OUT(Bridge\ Max)}$.

After $V_{OUT(System\ Max)}$ has been determined, choose the corresponding gain value for the ADC PGA. The amplifier gain should be the largest allowable value that is still less than the ADC FSR. In some cases it is not possible to choose an amplifier gain that uses the entire ADC FSR. While this is often an acceptable tradeoff between resolution and ease-of-use, care should be taken to ensure that all system requirements are still met when the ADC FSR cannot be maximized.

Next, ensure that the bridge common-mode voltage, $V_{CM(Bridge)}$, defined in Table 6-5 is within the common-mode range of the ADC amplifier, $V_{CM(ADC)}$, under a no-load condition (R1 = R2 = R3 = R4). The amplifier common-mode range varies by component, and will be defined in the data sheet based on the gain setting and supply voltage. However, targeting $V_{CM(Bridge)}$ = AVDD / 2 is a good choice as this is typically in the center of the $V_{CM(ADC)}$ range, enabling the highest gain possible per the previous step. Moreover, the bridge configuration in Figure 6-2 inherently sets $V_{CM(Bridge)}$ to AVDD / 2 under a no-load condition when $V_{EXCITATION}$ = AVDD.

Finally, follow the instructions in Section 5.5 if calibration is required.

6.2.5 Measurement Conversion

To better understand how the output code is determined, it is helpful to know how the least significant bit, or LSB, is calculated as per Equation 43:

$$LSB = FSR / 2^N = (A \cdot V_{REF} / gain) / 2^N \quad (43)$$

where:

- N is the ADC resolution
- A is a scaling factor related to the ADC analog voltage range

The ADC analog input voltage range information is generally found in either the *Electrical Characteristics* or *Recommended Operating Conditions* table in the data sheet. After identifying this range, the scaling factor A can be derived using the following examples:

- A = 4 if FSR = ±2 • V_{REF} / gain
- A = 2 if FSR = ±V_{REF} / gain
- A = 1 if FSR = ±0.5 • V_{REF} / gain
- A = 1 if FSR = 0 to V_{REF} / gain

Note that each FSR equation in the preceding list includes a gain term for completeness even though the scaling factor A is independent of gain. Using this information, the output code is defined by Equation 44 and the applied load, W, can be calculated using Equation 45:

$$Output\ Code = (2^N \cdot Gain \cdot V_{IN}) / (A \cdot V_{REF}) \quad (44)$$

$$W = M \cdot (Output\ Code - B_{Actual}) \quad (45)$$

where:

- M is a calculated scaling factor
- B_{Actual} is the measured offset

Refer to Section 5.5.3 for more information about how Equation 45 is derived.

6.2.6 Generic Register Settings

- Select multiplexer settings for AINP and AINN to measure V_{IN}
- Enable the amplifier and set gain to the desired value as per the instructions in this section
- Select data rate and digital filter settings, as per Section 5.2.1 and Section 5.3
- Select reference input to measure V_{REF} for ratiometric measurement

6.3 Four-Wire Resistive Bridge Measurement With a Pseudo-Ratiometric Reference and a Unipolar, High-Voltage (> 5 V) Excitation Source

A variation of the typical four-wire resistive bridge measurement circuit uses a unipolar, high-voltage (> 5 V) supply to excite the sensor. The high-voltage excitation source results in a larger bridge output voltage, which can relax the system noise requirements or improve dynamic range. Figure 6-3 shows a schematic for a voltage-excited bridge measurement using an ADC and a 15-V supply. Note that in this case the excitation voltage must be attenuated before being applied to the differential reference voltage inputs of the ADC, and is therefore considered a pseudo-ratiometric measurement.

6.3.1 Schematic

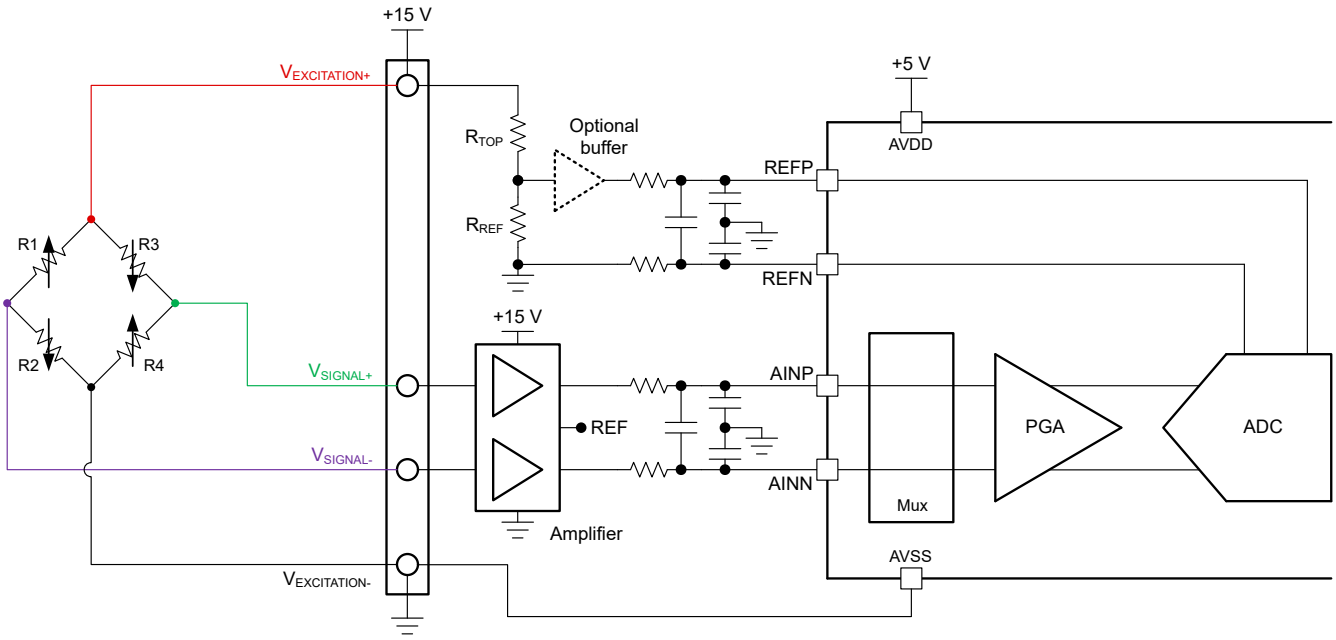

Figure 6-3. Four-Wire Resistive Bridge Measurement With a Pseudo-Ratiometric Reference and a Unipolar, High-Voltage (> 5 V) Excitation Source

6.3.2 Pros and Cons

Pros:

- Larger bridge output signal = relaxed noise requirements ***or*** better dynamic range
- Excitation voltage is not limited by the ADC V_{REF} range
- Bridge common-mode voltage is not limited by the ADC analog input range
- Good for local measurements where the wire length is short

Cons:

- More complex implementation can require signal conditioning on both the signal and reference paths
- Pseudo-ratiometric measurement reduces the overall system performance by introducing error sources between the bridge and the ADC reference and analog inputs
- Additional buffering may add offset, gain, and non-linearity errors
- ADC typically requires a lower-voltage supply (≤ 5 V), resulting in additional voltage rails
- Extended-length sensor wires can lead to IR losses such that $V_{EXCITATION} \neq V_{REF}$
- Can require electrical overstress (EOS) protection between the amplifier and ADC inputs due to high-voltage (> 5 V) supply. In many cases, the anti-aliasing filter resistor at the input of the ADC is sufficient to limit current into the device pins

6.3.3 Parameters and Variables

Table 6-6 defines important parameters and Table 6-7 provides equations for different variables. These parameters and variables are specific to this bridge configuration.

Table 6-6. User-Defined System Parameters

Parameter	Description
$V_{EXCITATION}$	Bridge excitation voltage
$V_{CM(ADC)}$	Target common-mode voltage for inputs to the ADC (typically AVDD / 2)
Bridge Sensitivity	Change in bridge output voltage relative to excitation voltage
$Load_{(Bridge\ Max)}$	Maximum load that can be applied to the bridge
$Load_{(System\ Max)}$	Maximum load applied to the bridge in the system (can be ≤ $Load_{(Bridge\ Max)}$)

Table 6-7. Variable Equations and Definitions

Variable	Equation	Description
$V_{CM(Bridge)}$	$(V_{EXCITATION+} + V_{EXCITATION–}) / 2$	Bridge output common-mode voltage
$R_{RATIO\ (TOP\ /\ REF)}$	$(V_{EXCITATION} / V_{REF}) – 1$	Ratio of resistor R_{TOP} to resistor R_{REF}
$V_{OUT(Bridge\ Max)}$	$V_{EXCITATION}$ • Bridge Sensitivity	Maximum differential output voltage of the bridge
$V_{OUT(System\ Max)}$	$(V_{OUT(Bridge\ Max)} • Load_{(System\ Max)}) / Load_{(Bridge\ Max)}$	Maximum differential bridge output voltage used in the system (can be ≤ $V_{OUT(System\ Max)}$)
V_{IN}	$V_{SIGNAL+} – V_{SIGNAL–}$	Differential input voltage to the ADC
V_{REF}	$V_{EXCITATION} • [R_{REF} / (R_{TOP} + R_{REF})]$	Differential reference voltage to the ADC

6.3.4 Design Notes

In the high-voltage, unipolar supply configuration, the excitation voltage applied to the bridge, $V_{EXCITATION}$, cannot typically be used as the ADC supply voltage. Instead, an additional lower-voltage supply (≤ 5 V) is required to power the ADC. Moreover, the ADC cannot directly use the high-voltage excitation source as the differential reference voltage, V_{REF}, and instead requires an attenuation circuit. A simple resistor divider as shown in Figure 6-3 is typically used, though other options include a difference amplifier or a discrete voltage reference. Using a resistor divider or an amplifier can introduce errors between the bridge and the reference inputs that are not present between the bridge and the ADC inputs, resulting in a pseudo-ratiometric reference configuration. Choosing a discrete voltage reference results in a non-ratiometric configuration. It is also necessary to ensure the higher-voltage bridge output signals are within the lower-voltage input range of the ADC. Solving this design challenge generally requires an amplifier as shown in Figure 6-3. Adding an amplifier between the bridge and the ADC can introduce errors that are not present between the bridge and the reference inputs, further reducing the effectiveness of the pseudo-ratiometric reference configuration.

A four-wire resistive bridge measurement with a pseudo-ratiometric reference and a unipolar, high-voltage (> 5 V) supply requires:

- Differential analog inputs (AINP and AINN)
- External reference input ***or*** integrated voltage reference
- Low-noise amplifier
- High-voltage supplies
- V_{REF} attenuation circuit (resistor divider, difference amplifier, and so forth) ***or*** separate voltage reference
- V_{IN} attenuation circuit (if applicable)

First, identify the maximum differential output voltage of the bridge, $V_{OUT(Bridge\ Max)}$, using the equation from Table 6-7 and parameters from Table 6-6. This value provides the maximum output voltage possible from the bridge under normal operating conditions and corresponds to the maximum load that can be applied to the bridge, $Load_{(Bridge\ Max)}$. If the system does not use the entire output range of the bridge, $V_{OUT(System\ Max)}$ defines the maximum differential output signal that is applied to a specific system and $Load_{(System\ Max)}$ is the corresponding maximum load. For example, if $V_{OUT(Bridge\ Max)}$ corresponds to $Load_{(Bridge\ Max)}$ = 5 kg, but the system specifications only require that $Load_{(System\ Max)}$ = 2.5 kg, then $V_{OUT(System\ Max)}$ is given by Equation 46:

$$V_{OUT(System\ Max)} = V_{OUT(Bridge\ Max)} • (2.5\ kg / 5\ kg) = V_{OUT(Bridge\ Max)} / 2 \quad (46)$$

Note that if $Load_{(System\ Max)} = Load_{(Bridge\ Max)}$, then $V_{OUT(System\ Max)} = V_{OUT(Bridge\ Max)}$.

After $V_{OUT(System\ Max)}$ has been determined, choose the corresponding gain value for the amplifier. For this specific circuit configuration, the gain can be applied by an external or internal amplifier. In either case, the amplifier gain should be the largest allowable value that is still less than the ADC full-scale range (FSR). In some cases it is not possible to choose an amplifier gain that uses the entire ADC FSR, especially when an ADC with an integrated PGA is selected. While this is often an acceptable tradeoff between resolution and ease-of-use, care should be taken to ensure that all system requirements are still met when the ADC FSR cannot be maximized.

Next, consider if the bridge output common-mode voltage, $V_{CM(Bridge)}$, needs to be level-shifted prior to being applied to the ADC. Many ADCs used for bridge measurement applications have support collateral that can aid in this process. Figure 6-4 shows an example of how the *Common-Mode Range Calculator* from the ADS1261 Excel Calculator can be used to determine if $V_{CM(Bridge)}$ is within the input range of the amplifier integrated into the ADS1261.

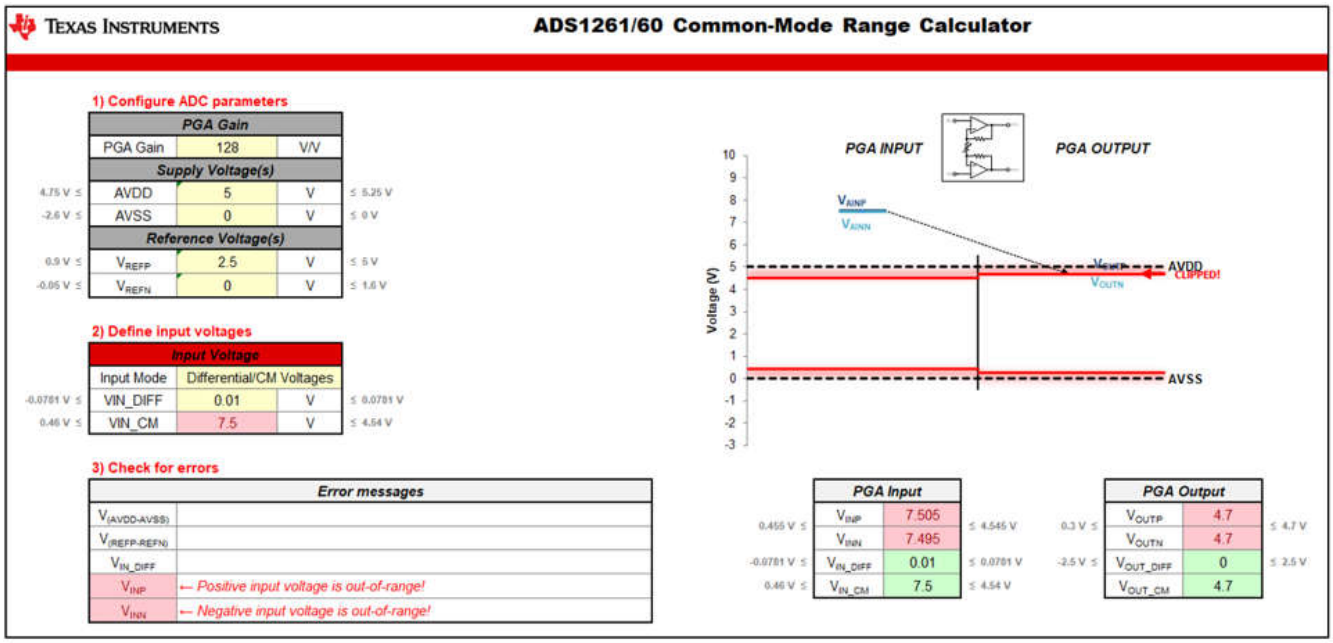

Figure 6-4. Verifying System Requirements Using the ADS1261 VCM Calculator Tool

In Figure 6-4, VIN_CM = 7.5 V, which is $V_{CM(Bridge)}$ in Figure 6-3 under a no-load condition (R1 = R2 = R3 = R4). The tool highlights several errors indicating that this is not a valid input condition. This result is in spite of the fact that the differential input voltage, VIN_DIFF, is well within the ±78-mV input range of the amplifier. It is possible to choose an ADC that can measure high-voltage signals directly, such as the ADS125H02, but most ADCs require an attenuation stage when $V_{EXCITATION}$ > 5 V.

If the ADC cannot directly support higher-voltage input signals, Figure 6-3 shows how an external amplifier can be used to level-shift the bridge output common-mode voltage. There are three options for the amplifier configuration:

1. An instrumentation amplifier with a high gain such as INA849
2. An integrated difference amplifier such as an INA105 with a gain of 1
3. A discrete difference amplifier ***or*** instrumentation amplifier built from multiple op amps and a resistor feedback network

Adding an amplifier between the bridge and the ADC can introduce errors at the ADC input that are not present between the bridge and the V_{REF} inputs, further reducing the effectiveness of the pseudo-ratiometric reference configuration. Choose an appropriate device based on the desired system accuracy and precision, while also factoring in system constraints such as cost, size, and power. Additionally, all amplifier configurations require a reference voltage, REF, to set the amplifier output common-mode voltage to an appropriate level for the ADC.

This voltage is $V_{CM(ADC)}$ in Table 6-6, and is typically set to mid-supply (AVDD / 2). However, Figure 6-4 shows that the ADC amplifier has a $V_{CM(ADC)}$ range of 0.45 V to 4.54 V for this particular set of conditions.

Some ADCs, including the ADS1261 and ADS124S08, integrate a precision reference with an output pin that can be used to bias the amplifier and therefore minimize component count. If this feature is not available on the selected ADC, choose a low-drift, high-accuracy reference source to minimize errors. Moreover, ensure that the entire amplifier circuit is low noise and high accuracy because any error in the input signal conditioning circuitry passes to the ADC output.

After selecting an external amplifier circuit, choose the system reference source. When selecting a discrete voltage reference, ensure this component is high accuracy and low drift for best performance. To maintain a pseudo-ratiometric relationship between $V_{EXCITATION}$ and V_{REF}, choose a resistor divider to attenuate the bridge excitation voltage. The resistor divider shown in Figure 6-3 consists of two resistors, with the reference voltage established across the bottom component, R_{REF}. Since the ADC AVDD is unipolar, V_{REFN} is typically set to 0 V such that the ratio of R_{TOP} to R_{REF} can be expressed using Equation 47:

$$R_{RATIO\ (R\_TOP\ to\ R\_REF)} = (V_{EXCITATION} / V_{REF}) - 1 \quad (47)$$

Equation 48 determines the resistor ratio given the conditions shown in Figure 6-3 where V_{REF} = 5 V and $V_{EXCITATION}$ = 15 V:

$$R_{RATIO\ (R\_TOP\ to\ R\_REF)} = (15\ V / 5\ V) - 1 = 2 \quad (48)$$

Therefore, if the impedance for R_{REF} = R, then R_{TOP} = 2 • R in Figure 6-3.

Select high accuracy (≤ 0.1 %), low temperature-drift (≤ 10 ppm/°C) resistors for the reference path. Keep the nominal resistance value low to limit thermal noise. As an example, a 1-kΩ resistor at 25°C and 1-kHz bandwidth contributes 128 nV_{RMS} of noise. These conditions are important to keep V_{REF} as close as possible to being ratiometric with $V_{EXCITATION}$ and minimize overall measurement error. Additionally, a buffer might be required depending on the impedance of the ADC differential reference inputs. The buffer can also introduce errors and further reduce the ratiometric relationship between V_{IN} and V_{REF}.

Finally, follow the instructions in Section 5.5 if calibration is required.

6.3.5 Measurement Conversion

To better understand how the output code is determined, it is helpful to know how the least significant bit, or LSB, is calculated as per Equation 49:

$$LSB = FSR / 2^N = (A • V_{REF} / gain) / 2^N \quad (49)$$

where:

- N is the ADC resolution
- A is a scaling factor related to the ADC analog voltage range

The ADC analog input voltage range information is generally found in either the *Electrical Characteristics* or *Recommended Operating Conditions* table in the data sheet. After identifying this range, the scaling factor A can be derived using the following examples:

- A = 4 if FSR = ±2 • V_{REF} / gain
- A = 2 if FSR = ±V_{REF} / gain
- A = 1 if FSR = ±0.5 • V_{REF} / gain
- A = 1 if FSR = 0 to V_{REF} / gain

Note that each FSR equation in the preceding list includes a gain term for completeness even though the scaling factor A is independent of gain. Using this information, the output code is defined by Equation 50 and the applied load, W, can be calculated using Equation 51:

$$Output\ Code = (2^N • Gain • V_{IN}) / (A • V_{REF}) \quad (50)$$

$$W = M • (Output\ Code - B_{Actual}) \quad (51)$$

where:

- M is a calculated scaling factor
- B_{Actual} is the measured offset

Refer to Section 5.5.3 for more information about how Equation 51 is derived.

6.3.6 Generic Register Settings

- Select multiplexer settings for AINP and AINN to measure V_{IN}
- Enable the amplifier and set gain to the desired value as per the instructions in this section
- Select data rate and digital filter settings, as per Section 5.2.1 and Section 5.3
- Choose internal or external reference input

6.4 Four-Wire Resistive Bridge Measurement with a Pseudo-Ratiometric Reference and Asymmetric, High-Voltage (> 5 V) Excitation Source

A variation of the typical four-wire resistive bridge measurement circuit uses asymmetric, high-voltage (> 5 V) supplies to excite the sensor. The high-voltage excitation source results in a larger bridge output voltage, which can relax the system noise requirements or improve dynamic range. Figure 6-5 shows a schematic for a voltage-excited bridge measurement using an ADC and an asymmetric bipolar supply of +10 V and –5 V. Note that in this case the excitation voltage must be attenuated before being applied to the differential reference voltage inputs of the ADC, and is therefore considered a pseudo-ratiometric measurement.

6.4.1 Schematic

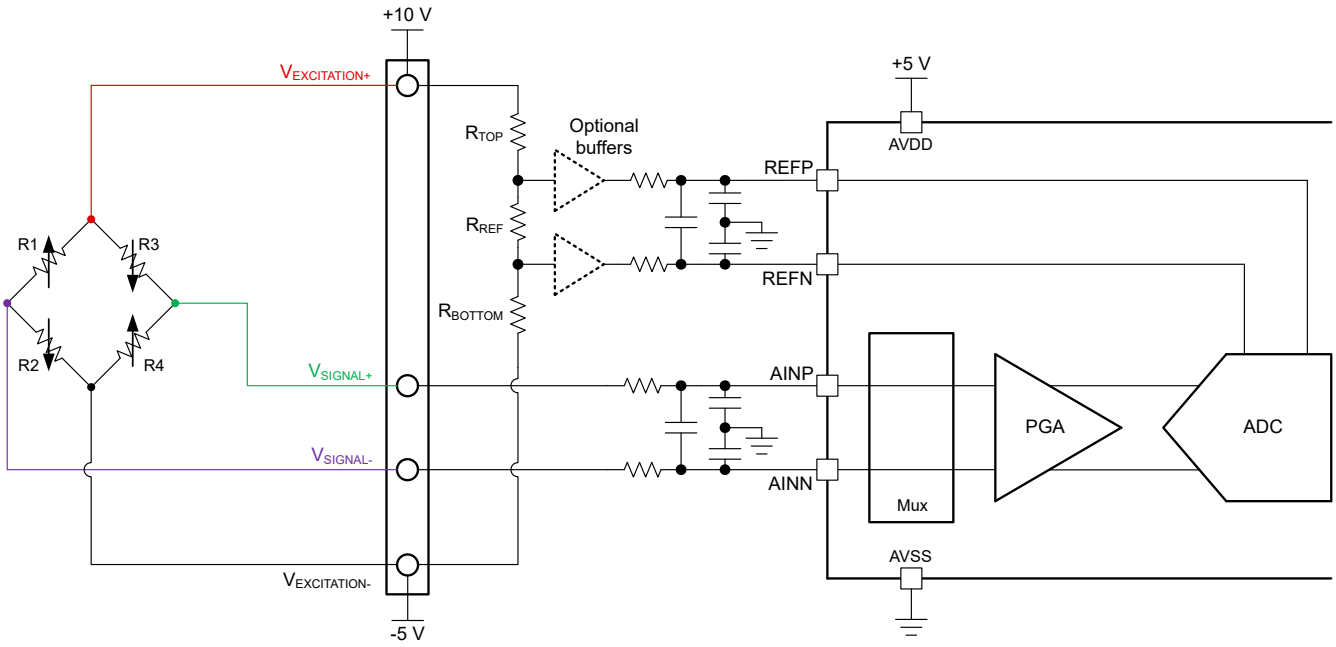

Figure 6-5. Four-Wire Resistive Bridge Measurement With a Pseudo-Ratiometric Reference and Asymmetric, High-Voltage (> 5 V) Excitation Source

6.4.2 Pros and Cons

Pros:

- Larger bridge output signal = relaxed noise requirements ***or*** better dynamic range
- Excitation voltage is not limited by the ADC V_{REF} range
- No input signal conditioning circuitry required because the bridge common-mode voltage is designed to be within the ADC analog input range
- Good for local measurements where the wire length is short

Cons:

- More complex implementation requires attenuation on the reference path
- Pseudo-ratiometric measurement reduces the overall system performance by introducing error sources between the bridge and the ADC reference inputs
- Additional buffering may add offset, gain, and non-linearity errors
- ADC typically requires a lower-voltage supply (≤ 5 V), resulting in additional voltage rails
- Extended-length sensor wires can lead to IR losses such that $V_{EXCITATION} \neq V_{REF}$

6.4.3 Parameters and Variables

Table 6-8 defines important parameters and Table 6-9 provides equations for different variables. These parameters and variables are specific to this bridge configuration.

Table 6-8. User-Defined System Parameters

Parameter	Description
$V_{EXCITATION}$	Bridge excitation voltage
Bridge Sensitivity	Change in bridge output voltage relative to excitation voltage
$V_{CM(ADC)}$	Target common-mode voltage for inputs to the ADC (typically AVDD / 2)
V_{REFN}	Voltage at the ADC REFN pin
$Load_{(Bridge\ Max)}$	Maximum load that can be applied to the bridge
$Load_{(System\ Max)}$	Maximum load applied to the bridge in the system (can be ≤ $Load_{(Bridge\ Max)}$)

Table 6-9. Variable Equations and Definitions

Variable	Equation	Description
$V_{CM(Bridge)}$	$(V_{EXCITATION+} + V_{EXCITATION–}) / 2$	Bridge common-mode voltage (typically equal to $V_{CM(ADC)}$)
$V_{EXCITATION+}$	$V_{CM(ADC)} + (V_{EXCITATION} / 2)$	Positive excitation supply voltage
$V_{EXCITATION-}$	$V_{CM(ADC)} - (V_{EXCITATION} / 2)$	Negative excitation supply voltage
$R_{RATIO\ (TOP\ /\ REF)}$	$[(V_{EXCITATION+} – V_{REFN}) / V_{REF}] – 1$	Ratio of resistor R_{TOP} to resistor R_{REF}
$R_{RATIO\ (BOTTOM\ /\ REF)}$	$(V_{REFN} – V_{EXCITATION–}) / V_{REF}$	Ratio of resistor R_{BOTTOM} to resistor R_{REF}
V_{REF}	$V_{EXCITATION} • [R_{REF} / (R_{TOP} + R_{REF} + R_{BOTTOM})]$	Differential reference voltage to the ADC
$V_{OUT(Bridge\ Max)}$	$V_{EXCITATION}$ • Bridge Sensitivity	Maximum differential output voltage of the bridge
$V_{OUT(System\ Max)}$	$(V_{OUT(Bridge\ Max)} • Load_{(System\ Max)}) / Load_{(Bridge\ Max)}$	Maximum differential bridge output voltage used in the system (can be ≤ $V_{OUT(System\ Max)}$)
V_{IN}	$V_{SIGNAL+} – V_{SIGNAL–}$	Differential input voltage to the ADC

6.4.4 Design Notes

In the asymmetric, high-voltage supply configuration, the excitation voltage applied to the bridge, $V_{EXCITATION}$, cannot typically be used as the ADC supply voltage. Instead, an additional lower-voltage supply (≤ 5 V) is required to power the ADC. Moreover, the ADC cannot directly use the high-voltage excitation source as the differential reference voltage, V_{REF}, and instead requires an attenuation circuit. Typically, a simple resistor divider is used as shown in Figure 6-5, though other options include a difference amplifier or a discrete voltage reference. Using a resistor divider or an amplifier can introduce errors between the bridge and the reference inputs that are not present between the bridge and the ADC inputs, resulting in a pseudo-ratiometric reference configuration. Choosing a discrete voltage reference results in a non-ratiometric configuration. Finally, choose the asymmetric supply voltages such that the bridge output common-mode voltage is within the lower-voltage input range of the ADC. Otherwise, additional input signal conditioning circuitry is necessary.

A four-wire resistive bridge measurement with a pseudo-ratiometric reference and asymmetric, high-voltage (> 5 V) supplies requires:

- Differential analog inputs (AINP and AINN)
- Differential reference inputs (REFP and REFN) ***or*** integrated voltage reference
- Low-noise amplifier
- High-voltage, asymmetric supplies
- V_{REF} attenuation circuit (resistor divider, difference amplifier, and so forth) ***or*** separate voltage reference

First, identify the maximum differential output voltage of the bridge, $V_{OUT(Bridge\ Max)}$, using the equation from Table 6-9 and parameters from Table 6-8. This value provides the maximum output voltage possible from

the bridge under normal operating conditions and corresponds to the maximum load that can be applied to the bridge, $Load_{(Bridge\ Max)}$. If the system does not use the entire output range of the bridge, $V_{OUT(System\ Max)}$ defines the maximum differential output signal that is applied to a specific system and $Load_{(System\ Max)}$ is the corresponding maximum load. For example, if $V_{OUT(Bridge\ Max)}$ corresponds to $Load_{(Bridge\ Max)}$ = 5 kg, but the system specifications only require that $Load_{(System\ Max)}$ = 2.5 kg, then $V_{OUT(System\ Max)}$ is given by Equation 52:

$$V_{OUT(System\ Max)} = V_{OUT(Bridge\ Max)} \bullet (2.5\ kg / 5\ kg) = V_{OUT(Bridge\ Max)} / 2 \quad (52)$$

Note that if $Load_{(System\ Max)} = Load_{(Bridge\ Max)}$, then $V_{OUT(System\ Max)} = V_{OUT(Bridge\ Max)}$.

After $V_{OUT(System\ Max)}$ has been determined, choose the corresponding gain value for the amplifier. The amplifier gain should be the largest allowable value that is still less than the ADC full-scale range (FSR). In some cases it is not possible to choose an amplifier gain that uses the entire ADC FSR, especially when an ADC with an integrated PGA is selected. While this is often an acceptable tradeoff between resolution and ease-of-use, ensure that all system requirements are still met when the ADC FSR cannot be maximized.

Next, choose the values of the asymmetric supplies such that the bridge common-mode voltage, $V_{CM(Bridge)}$, is within the common-mode range of the ADC amplifier under a no-load condition (R1 = R2 = R3 = R4). Typically, the target ADC amplifier common-mode voltage, $V_{CM(ADC)}$, is selected to be at the ADC mid-supply voltage (AVDD / 2), though this is not a requirement. The amplifier common-mode range varies by component, and is defined in the data sheet based on the gain setting and supply voltage.

Using $V_{CM(ADC)}$ and the selected bridge excitation voltage, $V_{EXCITATION}$, the asymmetric excitation voltages $V_{EXCITATION+}$ and $V_{EXCITATION-}$ can be determined using Equation 53 and Equation 54:

$$V_{EXCITATION+} = V_{CM(ADC)} + (V_{EXCITATION} / 2) \quad (53)$$

$$V_{EXCITATION-} = V_{CM(ADC)} – (V_{EXCITATION} / 2) \quad (54)$$

After calculating $V_{EXCITATION+}$ and $V_{EXCITATION-}$, choose the system reference source. When selecting a discrete voltage reference, ensure this component is high accuracy and low-drift for best performance. To maintain a pseudo-ratiometric relationship between $V_{EXCITATION}$ and V_{REF}, choose a resistor divider or a difference amplifier to attenuate the bridge excitation voltage. The resistor-divider method is more commonly-used and is shown in Figure 6-5 as three resistors in series. The reference voltage, V_{REF}, is established across the center component, R_{REF}. Equation 55 and Equation 56 determine the ratio of R_{TOP} and R_{BOTTOM} to R_{REF} using V_{REF}, the previously-determined $V_{EXCITATION±}$ values, and the voltage seen at the REFN pin (V_{REFN}) in Figure 6-5:

$$R_{RATIO\ (TOP\ /\ REF)} = [(V_{EXCITATION+} – V_{REFN}) / V_{REF}] – 1 \quad (55)$$

$$R_{RATIO\ (BOTTOM\ /\ REF)} = (V_{REFN} – V_{EXCITATION-}) / V_{REF} \quad (56)$$

For example, consider a system with the following constraints:

- $V_{EXCITATION}$ = 15 V
- $V_{CM(ADC)} = V_{REF}$ = 2.5 V
- R_{REF} = 4.7 kΩ
- V_{REFN} = 1.25 V

Use Equation 53 through Equation 56 to calculate the remaining system parameters:

- $V_{EXCITATION+}$ = 10 V
- $V_{EXCITATION-}$ = –5 V
- $R_{RATIO\ (TOP\ /\ REF)}$ = 2.5
- $R_{RATIO\ (BOTTOM\ /\ REF)}$ = 2.5

Therefore, $R_{TOP} = R_{BOTTOM}$ = 11.8 kΩ for this specific system. Figure 6-6 shows the various voltages (in blue) and resistor values (in red) that are used in this example.

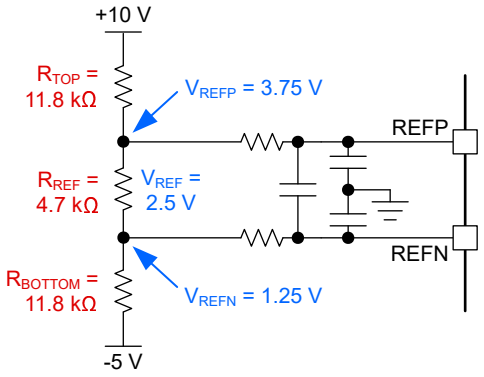

Figure 6-6. Example Resistor and Voltage Values

Note that there are some implied constraints in Equation 55 and Equation 56, including $V_{EXCITATION+} > V_{REFN} > V_{EXCITATION-}$, $V_{EXCITATION+} > V_{EXCITATION-}$, and $V_{EXCITATION} > V_{REF}$. Otherwise, nonsensical results may occur, such as negative resistance values. Ultimately, check that the results of each equation meet all of the final design requirements as well as make physical sense.

It is also important to allow headroom near the maximum absolute and differential reference voltages applied to the ADC. Many systems seek to maximize the ADC dynamic range by maximizing V_{REF}. However, variations in the excitation voltage and resistor impedance may increase V_{REF} beyond the operating range of the ADC, which is typically limited to AVSS on V_{REFN} and AVDD on V_{REFP}. Under these conditions, consider a small reduction in the R_{REF} impedance to allow for system tolerances.

Select high accuracy (≤ 0.1%), low temperature-drift (≤ 10 ppm/°C) resistors for the reference path. Keep the nominal resistance value low to limit thermal noise. As an example, a 1-kΩ resistor at 25°C and 1-kHz bandwidth contributes 128 nV_{RMS} of noise. These conditions are important to keep V_{REF} as close as possible to being ratiometric with $V_{EXCITATION}$ and minimize overall measurement error. Additionally, buffers might be required depending on the impedance of the differential reference inputs of the ADC. The buffer can also introduce errors and further reduce the ratiometric relationship between V_{IN} and V_{REF}.

Finally, follow the instructions in Section 5.5 if calibration is required.

6.4.5 Measurement Conversion

To better understand how the output code is determined, it is helpful to know how the least significant bit, or LSB, is calculated as per Equation 57:

$$LSB = FSR / 2^N = (A \cdot V_{REF} / gain) / 2^N \quad (57)$$

where:

- N is the ADC resolution
- A is a scaling factor related to the ADC analog voltage range

The ADC analog input voltage range information is generally found in either the *Electrical Characteristics* or *Recommended Operating Conditions* table in the data sheet. After identifying this range, the scaling factor A can be derived using the following examples:

- A = 4 if FSR = ±2 • V_{REF} / gain
- A = 2 if FSR = ±V_{REF} / gain
- A = 1 if FSR = ±0.5 • V_{REF} / gain
- A = 1 if FSR = 0 to V_{REF} / gain

Note that each FSR equation in the preceding list includes a gain term for completeness even though the scaling factor A is independent of gain. Using this information, the output code is defined by Equation 58 and the applied load, W, can be calculated using Equation 59:

$$Output\ Code = (2^N \cdot Gain \cdot V_{IN}) / (A \cdot V_{REF}) \quad (58)$$

$$W = M \cdot (Output\ Code - B_{Actual}) \quad (59)$$

where:

- M is a calculated scaling factor
- B_{Actual} is the measured offset

Refer to Section 5.5.3 for more information about how Equation 59 is derived.

6.4.6 Generic Register Settings

- Select multiplexer settings for AINP and AINN to measure V_{IN}
- Enable the amplifier and set gain to the desired value as per the instructions in this section
- Select data rate and digital filter settings, as per Section 5.2.1 and Section 5.3
- Choose internal or external reference input

6.5 Four-Wire Resistive Bridge Measurement With a Ratiometric Reference and Current Excitation

A variation of the typical four-wire resistive bridge measurement circuit uses a constant current source to excite the sensor. Current excitation is useful for certain silicon piezoresistive sensors that exhibit constant sensitivity over temperature when excited by a constant-current source. Additionally, current excitation reduces the non-linearity due to single- or dual-active element bridge topologies. Figure 6-7 shows a schematic for a current-excited bridge measurement using an ADC with an integrated constant-current source (IDAC). The ADC also uses the voltage generated by the current through the resistive bridge as the differential reference voltage. This ratiometric reference configuration helps eliminate errors due to the noise and drift in the excitation source.

6.5.1 Schematic

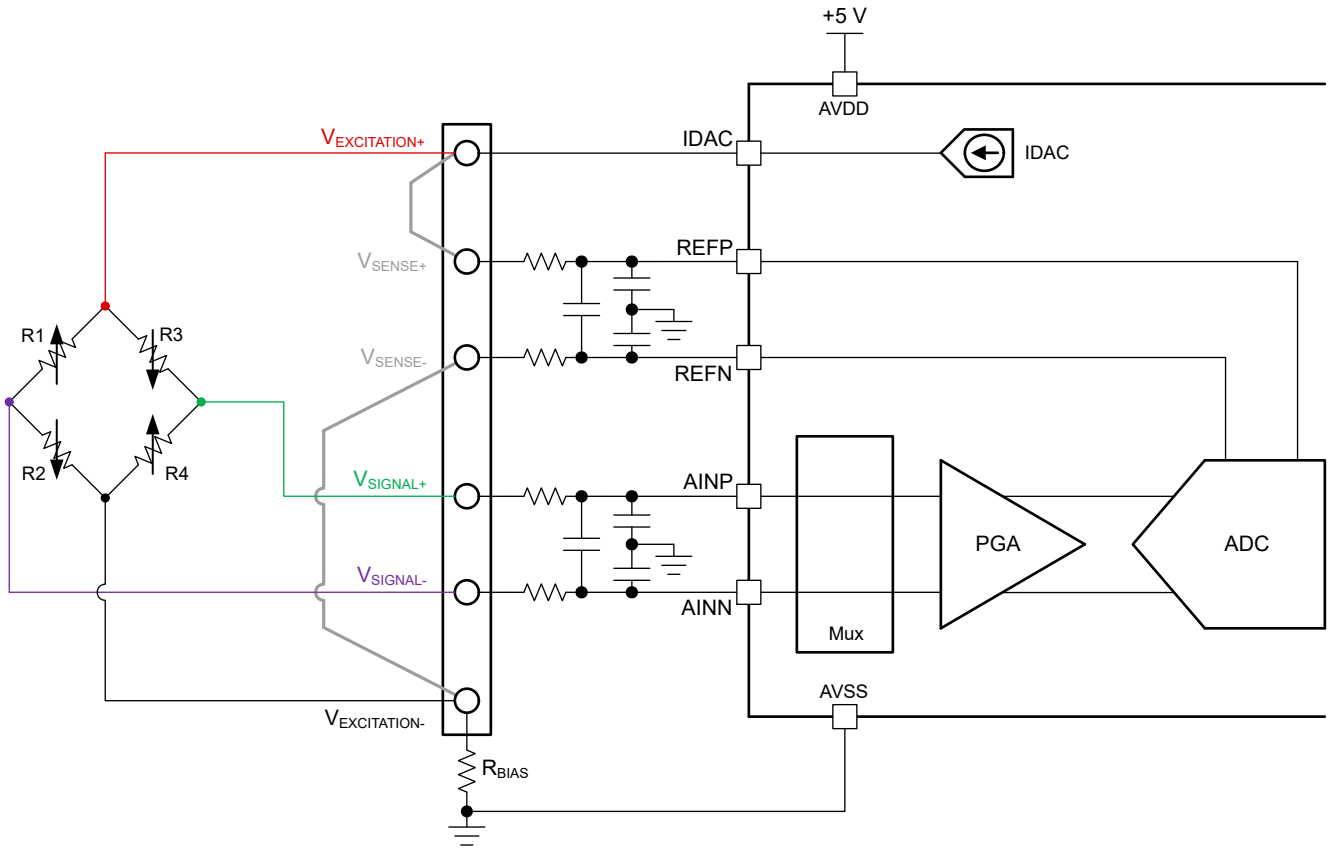

Figure 6-7. Four-Wire Resistive Bridge Measurement With a Ratiometric Reference and Current Excitation

6.5.2 Pros and Cons

Pros:

- Reduces the non-linearity due to single- or dual-active element bridge topologies
- Simple implementation requiring only a few passive components
- Ratiometric measurement such that excitation source noise and drift are canceled
- Good for local measurements where the wire length is short
- Improved temperature sensitivity for certain sensor types

Cons:

- IDAC compliance voltage can reduce the maximum bridge output voltage
- Low-resistance bridges require high current to drive, which can impact self-heating
- Smaller IDAC currents can reduce the bridge output voltage and lead to lower dynamic range
- Excitation voltage is limited to ADC V_{REF} range
- Bias resistor can be required to level-shift the bridge output common-mode voltage

- Bridge common-mode voltage is limited by ADC analog input range
- Extended-length sensor wires can lead to IR losses such that $V_{EXCITATION} \neq V_{REF}$. This can be removed with a six-wire connection as per Section 6.2

6.5.3 Parameters and Variables

Table 6-10 defines important parameters and Table 6-11 provides equations for different variables. These parameters and variables are specific to this bridge configuration.

Table 6-10. User-Defined System Parameters

Parameter	Description
I_{IDAC}	Bridge excitation current
R_{BRIDGE}	Nominal bridge impedance
R_{BIAS}	Bias resistor between the $V_{EXCITATION–}$ and ground (can be removed under certain conditions)
$V_{CM(ADC)}$	Target common-mode voltage for inputs to the ADC (typically AVDD / 2)
Bridge Sensitivity	Change in bridge output voltage relative to excitation voltage
$Load_{(Bridge\ Max)}$	Maximum load that can be applied to the bridge
$Load_{(System\ Max)}$	Maximum load applied to the bridge in the system (can be ≤ $Load_{(Bridge\ Max)}$)

Table 6-11. Variable Equations and Definitions

Variable	Equation	Description
R_{TOTAL}	$R_{BRIDGE} + R_{BIAS}$	Total resistance seen between IDAC pin and ground
V_{BRIDGE}	$I_{IDAC} \cdot R_{BRIDGE}$	Voltage across the bridge
V_{REF}	$V_{EXCITATION+} - V_{EXCITATION–}$	Differential reference voltage to the ADC
$V_{COMPLIANCE}$	$I_{IDAC} \cdot R_{TOTAL}$	Maximum voltage that can be applied to the IDAC pin to maintain constant current
$V_{CM(Bridge)}$	$V_{BRIDGE} / 2 + V_{BIAS}$	Bridge output common-mode voltage
$V_{OUT(Bridge\ Max)}$	V_{BRIDGE} • Bridge Sensitivity	Maximum differential output voltage of the bridge
$V_{OUT(System\ Max)}$	($V_{OUT(Bridge\ Max)} \cdot Load_{(System\ Max)}$) / $Load_{(Bridge\ Max)}$	Maximum differential bridge output voltage used in the system (can be ≤ $V_{OUT(System\ Max)}$)
V_{IN}	$V_{SIGNAL+} – V_{SIGNAL–}$	Differential input voltage to the ADC

6.5.4 Design Notes

The IDAC current, I_{IDAC}, in conjunction with the nominal bridge resistance, R_{BRIDGE}, determine the total voltage across the bridge, V_{BRIDGE}. Assuming zero lead wire resistance, $V_{BRIDGE} = V_{EXCITATION} = V_{EXCITATION+} – V_{EXCITATION-}$, which is also used as the ADC reference voltage, V_{REF}. Unlike the circuit described in Section 6.1 where $V_{EXCITATION}$ is fixed, V_{BRIDGE} varies as R_{BRIDGE} changes. This varying V_{BRIDGE} voltage causes V_{REF} and the input voltage to the ADC to change as well. Additionally, the current source does not inherently center the bridge common-mode voltage, $V_{CM(Bridge)}$, as it does in other bridge measurement circuits. The bias resistor, R_{BIAS}, helps keep $V_{CM(Bridge)}$ within the common-mode range of the ADC analog and voltage reference inputs.

Small variations in R_{BRIDGE} due to tension or compression cause the differential bridge output voltage to change. The PGA integrated into the ADC gains up this low-level signal to reduce system noise and utilize more of the ADC full-scale range (FSR). The ADC samples and converts this amplified voltage against V_{REF}, which is the same voltage used to excite the bridge and therefore ratiometric. The excitation source noise and drift are seen equally in both V_{IN} and V_{REF} in a ratiometric reference configuration, effectively removing these errors from the ADC output code.

A four-wire resistive bridge measurement with a ratiometric reference and current excitation requires:

- Differential analog inputs (AINP and AINN)
- Differential reference inputs (REFP and REFN)
- Low-noise amplifier
- Constant-current source (IDAC)
- Bias resistor (optional in some cases)

Additionally, a four-wire resistive bridge measurement with a ratiometric reference and current excitation requires consideration of several factors, including:

- Absolute (V_{REFP} and V_{REFN}) and differential (V_{REF}) reference voltages
- Bridge excitation current, I_{IDAC}
- IDAC compliance voltage
- Bridge common-mode voltage, $V_{CM(Bridge)}$
- Voltage across the bridge, V_{BRIDGE}
- Bridge resistance, R_{BRIDGE}
- Bias resistor value, R_{BIAS}

All of these factors are inter-related such that selecting one influences the selection of one or more of the others. Several design iterations can be required to determine a final result that meets all of the system specifications.

To reduce the number of possible circuit configurations, it is recommended to begin the design by choosing an ADC with differential V_{REF} inputs, integrated IDACs, and a PGA. The absolute and differential V_{REF} specifications constrain the possible values of V_{BRIDGE}. Integrated IDACs limit the choice of I_{IDAC} to several discrete values and eliminate external circuitry to drive the bridge. The integrated IDACs also have a well-defined compliance voltage that helps determine the maximum values of R_{BRIDGE} and R_{BIAS}. The integrated PGA typically requires a common-mode voltage of half the analog supply voltage (AVDD / 2) to maximize the amplifier gain and keep the PGA output voltage within the linear range of operation. This sets a target $V_{CM(Bridge)}$ of AVDD / 2, which helps determine if an R_{BIAS} resistor is necessary and, if it is, the required value.

For example, the 24-bit ADS1261 integrates all of these necessary features. Figure 6-8 shows the differential and absolute V_{REF} voltage requirements for the ADS1261. Using a unipolar supply such that AVDD = 5 V and AVSS = 0 V, Figure 6-8 shows that V_{REF} must be between 0.9 V and 5 V. This bounds the possible values of V_{BRIDGE}. Additionally, the absolute voltage on V_{REFN} can extend down to AVSS while the absolute voltage on V_{REFP} can extend up to AVDD. This wide absolute V_{REF} voltage range typically does not limit the selection of the other system components, though this should always be verified in each design.

			MIN	NOM	MAX	UNIT
VOLTAGE REFERENCE INPUTS						
V_{REF}	Differential reference voltage	$V_{REF} = V_{(REFPx)} - V_{(REFNx)}$	0.9		AVDD – AVSS	V
$V_{(REFNx)}$	Negative reference voltage		AVSS – 0.05		$V_{(REFPx)}$ – 0.9	V
$V_{(REFPx)}$	Positive reference voltage		$V_{(REFNx)}$ + 0.9		AVDD + 0.05	V

Figure 6-8. ADS1261 V_{REF} Operating Conditions

Figure 6-9 shows the available IDAC current settings and the compliance voltage for the ADS1261. An IDAC integrated into a precision ADC requires some headroom with AVDD to maintain the current magnitude. Since AVDD = 5 V ±5% for the ADS1261, the IDAC compliance voltage = AVDD – 1.1 V = 3.9 V. This value sets an upper bound on R_{BRIDGE} + R_{BIAS} as well as I_{IDAC}.

PARAMETER		MIN	TYP	MAX	UNIT
EXCITATION CURRENT SOURCES (IDACS)					
	Current settings		50, 100, 250, 500, 750, 1000, 1500, 2000, 2500, 3000		µA
	Compliance range	AVSS		AVDD – 1.1	V

Figure 6-9. ADS1261 IDAC Current Settings and Compliance Voltage

To determine if $V_{CM(Bridge)}$ is within the PGA linear region of operation, Section 6.3.4 introduced the ADS1261 Excel Calculator that plots the PGA output to reveal if the input parameters are valid. It is also possible to select a desired target value such as $V_{CM(Bridge)}$ = AVDD / 2 and design the rest of the system around this

common-mode voltage. After the specific ADC operating conditions have been defined, begin selecting the remaining system component values.

For this example, assume that R_{BRIDGE} can be any one of four common bridge resistance values: 120 Ω, 350 Ω, 1 kΩ, or 3.5 kΩ. Then, use the ADS1261 IDAC values given in Figure 6-9 to determine V_{BRIDGE} using the equation in Table 6-11. Table 6-12 calculates V_{BRIDGE} for all possible combinations of I_{IDAC} and R_{BRIDGE}.

Table 6-12. Calculating V_{BRIDGE} for All Combinations of R_{BRIDGE} and I_{IDAC}

R_{BRIDGE} (Ω)	I_{IDAC} (μA)									
	50	**100**	**250**	**500**	**750**	**1000**	**1500**	**2000**	**2500**	**3000**
120	0.006	0.012	0.030	0.060	0.090	0.120	0.180	0.240	0.300	0.360
350	0.018	0.035	0.088	0.175	0.263	0.350	0.525	0.700	0.875	1.050
1000	0.050	0.100	0.250	0.500	0.750	1.000	1.500	2.000	2.500	3.000
3500	0.175	0.350	0.875	1.750	2.625	3.500	5.250	7.000	8.750	10.500

Assuming no lead resistance, $V_{BRIDGE} = V_{REF}$. Therefore, Table 6-12 also highlights in green all possible system combinations where 0.9 V < V_{BRIDGE} < 5 V, as per the ADS1261 requirements. Out of the 40 possible combinations, only nine remain.

Next, determine the possible values of R_{BIAS} for each of the remaining nine combinations by choosing a value for $V_{CM(Bridge)}$. This example uses $V_{CM(Bridge)}$ = AVDD / 2, though other voltages are possible. Always ensure that the PGA common-mode and absolute voltage requirements are met for the target gain value.

As per Table 6-11, $V_{CM(Bridge)} = V_{BRIDGE} / 2 + V_{BIAS}$, $V_{BRIDGE} = I_{IDAC} \cdot R_{BRIDGE}$, and $V_{BIAS} = I_{IDAC} \cdot R_{BIAS}$. Rearranging these equations helps determine R_{BIAS} in terms of I_{IDAC}, R_{BRIDGE}, and AVDD, as per Equation 60:

$$R_{BIAS} = 0.5 \cdot ([AVDD / I_{IDAC}] - R_{BRIDGE}) \quad (60)$$

One important detail about Equation 60 is that R_{BIAS} can be 0 Ω such that the $V_{CM(Bridge)}$ equation simplifies to $V_{CM(Bridge)} = V_{BRIDGE} / 2$. In other words, it is possible to eliminate the R_{BIAS} resistor as long as the ADC and system requirements can still be met. However, this example assumes an R_{BIAS} resistor is necessary. In either case, the next step is to calculate $V_{COMPLIANCE}$ using the equation from Table 6-11. Table 6-13 reports the calculated values of R_{BIAS} and $V_{COMPLIANCE}$ for each of the nine valid combinations in Table 6-12. Additionally, Table 6-13 highlights in green the values of $V_{COMPLIANCE}$ that are within the ADS1261 IDAC compliance voltage of 3.9 V.

Table 6-13. Calculating R_{BIAS} and $V_{COMPLIANCE}$ and for All Combinations of R_{BRIDGE} and I_{IDAC} (AVDD = 5 V)

R_{BRIDGE} (Ω)	I_{IDAC} (μA)	R_{BIAS} (Ω)	$V_{COMPLIANCE}$ (V)
350	**3000**	658	3.025
1000	**1000**	2000	3.000
	1500	1167	3.250
	2000	750	3.500
	2500	500	3.750
	3000	333	4.000
3500	**500**	3250	3.375
	750	1583	3.813
	1000	750	4.250

As Table 6-13 shows, seven of the original nine combinations are within the IDAC 3.9-V compliance voltage specified by the ADS1261. Any of these options could be used in the final design. For example, Figure 6-10 shows a system where R_{BRIDGE} = 1 kΩ, R_{BIAS} = 2 kΩ, and I_{IDAC} = 1 mA. The IDAC current path is highlighted in red and the resulting system voltages are highlighted in blue.

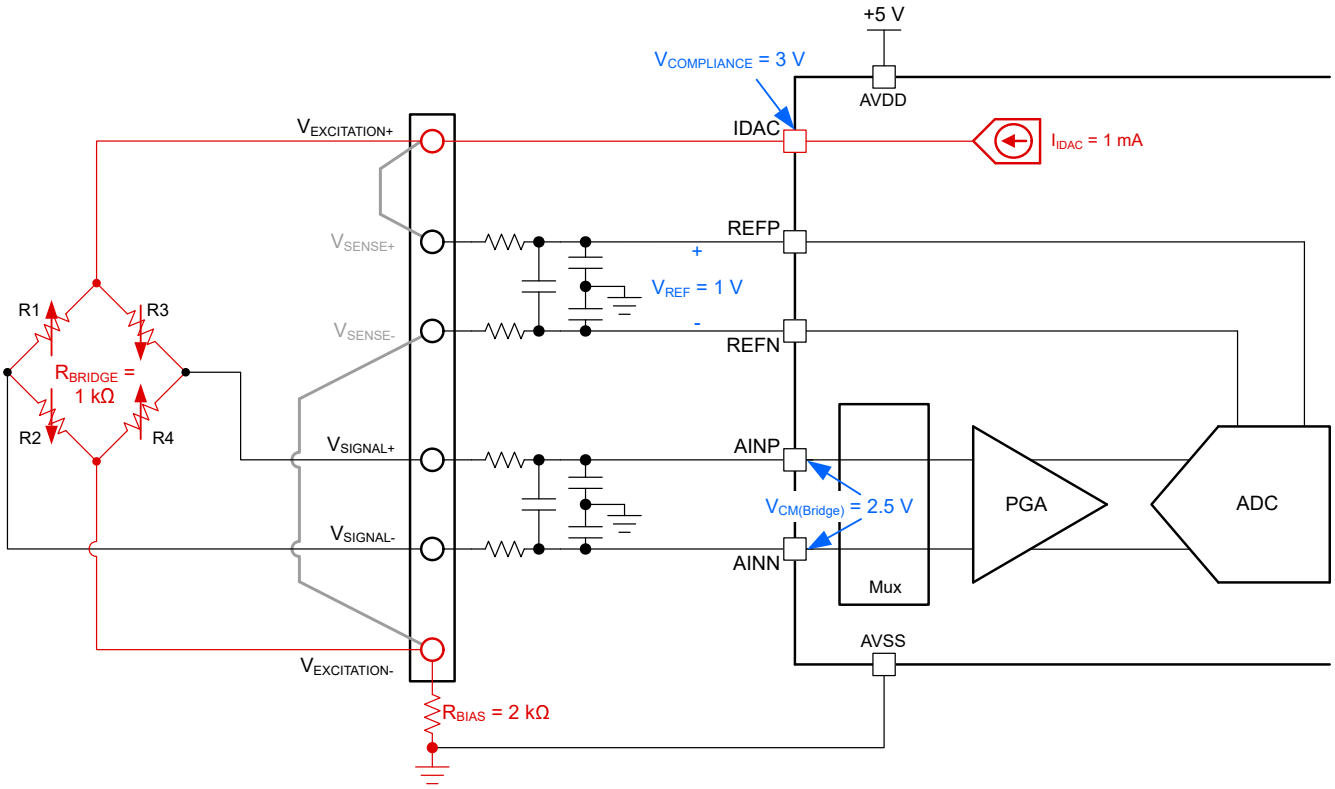

Figure 6-10. Current-Excited Bridge Measurement Using R_{BRIDGE} = 1 kΩ, R_{BIAS} = 2 kΩ, and I_{IDAC} = 1 mA

One important result from Figure 6-10 that was not previously-discussed is that $V_{BRIDGE} = V_{REF}$ = 1 V. In other words, the current-excited system has $V_{EXCITATION}$ = 1 V, while a voltage-excited system typically has $V_{EXCITATION} \geq 5$ V. Assuming each bridge has the same sensitivity, the output voltage from the current-excited bridge is 20% compared to the voltage-excited bridge. This can reduce the dynamic range of the system to an unacceptable level given the system noise targets. In this case, repeat the design process using a different ADC, a discrete current source, or a wider range of R_{BRIDGE} values.

After the system configuration has been selected, identify the maximum differential output voltage of the bridge, $V_{OUT(Bridge\ Max)}$, using the equation from Table 6-11 and parameters from Table 6-10. This value provides the maximum output voltage possible from the bridge under normal operating conditions and corresponds to the maximum load that can be applied to the bridge, $Load_{(Bridge\ Max)}$. If the system does not use the entire output range of the bridge, $V_{OUT(System\ Max)}$ defines the maximum differential output signal that is applied to a specific system and $Load_{(System\ Max)}$ is the corresponding maximum load. For example, if $V_{OUT(Bridge\ Max)}$ corresponds to $Load_{(Bridge\ Max)}$ = 5 kg, but the system specifications only require that $Load_{(System\ Max)}$ = 2.5 kg, then $V_{OUT(System\ Max)}$ is given by Equation 61:

$$V_{OUT(System\ Max)} = V_{OUT(Bridge\ Max)} \bullet (2.5\ kg / 5\ kg) = V_{OUT(Bridge\ Max)} / 2 \quad (61)$$

Note that if $Load_{(System\ Max)} = Load_{(Bridge\ Max)}$, then $V_{OUT(System\ Max)} = V_{OUT(Bridge\ Max)}$.

After $V_{OUT(System\ Max)}$ has been determined, choose the corresponding gain value for the ADC PGA. The maximum gain value is limited by the previously-selected value of $V_{CM(Bridge)}$ and the ADC FSR. The amplifier gain should be the largest allowable value that keeps the PGA output voltage within the linear range of operation given the $V_{CM(Bridge)}$ voltage *and* is less than the ADC FSR. In some cases it is not possible to choose an amplifier gain that uses the entire ADC FSR. While this is often an acceptable tradeoff between resolution and ease-of-use, care should be taken to ensure that all system requirements are still met when the ADC FSR cannot be maximized.

Finally, follow the instructions in Section 5.5 if calibration is required.

6.5.5 Measurement Conversion

To better understand how the output code is determined, it is helpful to know how the least significant bit, or LSB, is calculated as per Equation 62:

$$LSB = FSR / 2^N = (A \cdot V_{REF} / gain) / 2^N \quad (62)$$

where:

- N is the ADC resolution
- A is a scaling factor related to the ADC analog voltage range

The ADC analog input voltage range information is generally found in either the *Electrical Characteristics* or *Recommended Operating Conditions* table in the data sheet. After identifying this range, the scaling factor A can be derived using the following examples:

- A = 4 if FSR = $\pm 2 \cdot V_{REF}$ / gain
- A = 2 if FSR = $\pm V_{REF}$ / gain
- A = 1 if FSR = $\pm 0.5 \cdot V_{REF}$ / gain
- A = 1 if FSR = 0 to V_{REF} / gain

Note that each FSR equation in the preceding list includes a gain term for completeness even though the scaling factor A is independent of gain. Using this information, the output code is defined by Equation 63 and the applied load, W, can be calculated using Equation 64:

$$\text{Output Code} = (2^N \cdot \text{Gain} \cdot V_{IN}) / (A \cdot V_{REF}) \quad (63)$$

$$W = M \cdot (\text{Output Code} - B_{Actual}) \quad (64)$$

where:

- M is a calculated scaling factor
- B_{Actual} is the measured offset

Refer to Section 5.5.3 for more information about how Equation 64 is derived.

6.5.6 Generic Register Settings

- Select multiplexer settings for AINP and AINN to measure V_{IN}
- Enable the amplifier and set gain to the desired value as per the instructions in this section
- Select data rate and digital filter settings, as per Section 5.2.1 and Section 5.3
- Select the external reference input
- Select IDAC output current and IDAC output channel

6.6 Measuring Multiple Four-Wire Resistive Bridges in Series with a Pseudo-Ratiometric Reference and a Unipolar, Low-Voltage (≤5V) Excitation Source

It is possible to measure multiple four-wire resistive bridges using a single pseudo-ratiometric reference and a constant voltage to excite the sensor. Figure 6-11 shows a schematic for a measuring two bridge sensors in series using a 5-V supply, an ADC, and a pseudo-ratiometric reference configuration. The output voltage of Bridge A can change depending on the properties of Bridge B (and vice versa). As a result, the output voltage from either bridge is never truly ratiometric to the excitation voltage, and is therefore pseudo-ratiometric.

6.6.1 Schematic

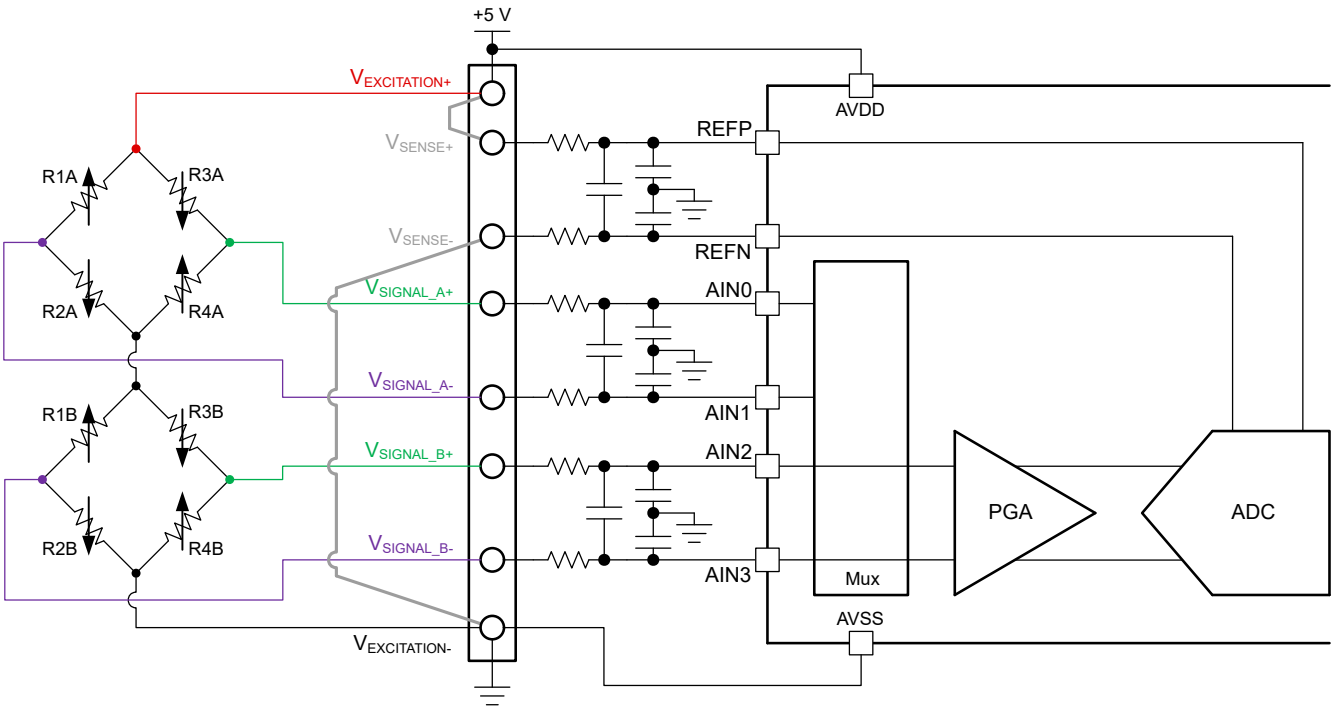

Figure 6-11. Measuring Multiple Four-Wire Resistive Bridges in Series With a Pseudo-Ratiometric Reference and a Unipolar, Low-Voltage (≤ 5 V) Excitation Source

6.6.2 Pros and Cons

Pros:

- Simple implementation requiring only a few passive components
- Good for local measurements where the wire length is short
- Reduced current through each bridge compared to measuring multiple bridges in parallel also reduces power consumption and thermal effects due to sensor self-heating

Cons:

- Excitation voltage is limited to ADC V_{REF} range
- Bridge common-mode voltage is limited by ADC analog input range
- Signal conditioning required ***or*** the ADC must support wider common-mode voltage range
- Pseudo-ratiometric measurement reduces the overall system performance by introducing error sources between the bridge and the ADC reference inputs. This can be improved by using dedicated voltage reference inputs for each bridge
- Wire break for one sensor eliminates the excitation path for both sensors
- Excitation voltage for each bridge is reduced compared to measuring multiple bridges in parallel, which reduces output signal range. This can be improved by using dedicated voltage reference inputs for each bridge
- Extended-length sensor wires can lead to IR losses such that $V_{EXCITATION} \neq V_{REF}$. This can be removed with a six-wire connection per Section 6.2

6.6.3 Parameters and Variables

Table 6-14 defines important parameters and Table 6-15 provides equations for different variables. These parameters and variables are specific to this bridge configuration.

Table 6-14. User-Defined System Parameters

Parameter	Description
$V_{EXCITATION}$	Excitation voltage applied to the series combination of Bridge A and Bridge B
R_{BRIDGE} (1)	Nominal impedance of each bridge
Bridge Sensitivity (1)	Change in bridge output voltage relative to excitation voltage
$Load_{(Bridge\ Max)}$ (1)	Maximum load that can be applied to the bridge
$Load_{(System\ Max)}$	Maximum load applied to the bridge in the system (can be ≤ $Load_{(Bridge\ Max)}$)
$V_{CM(ADC)\_RANGE}$	Target common-mode voltage range allowed by the ADC amplifier

(1) Should be the same for each bridge

Table 6-15. Variable Equations and Definitions

Variable	Equation	Description
$V_{CM(Bridge\_A)}$	$V_{EXCITATION}$ • (3 / 4)	Common-mode voltage for Bridge A
$V_{CM(Bridge\_B)}$	$V_{EXCITATION}$ • (1 / 4)	Common-mode voltage for Bridge B
$V_{OUT(Bridge\ Max)}$	$V_{EXCITATION}$ • Bridge Sensitivity	Maximum differential output voltage of the bridge
$V_{OUT(System\ Max)}$	($V_{OUT(Bridge\ Max)}$ • $Load_{(System\ Max)}$) / $Load_{(Bridge\ Max)}$	Maximum differential bridge output voltage used in the system (can be ≤ $V_{OUT(System\ Max)}$)
V_{IN_A}	$V_{SIGNAL\_A+} – V_{SIGNAL\_A–}$	Differential input voltage to the ADC from Bridge A
V_{IN_B}	$V_{SIGNAL\_B+} – V_{SIGNAL\_B–}$	Differential input voltage to the ADC from Bridge B
V_{REF}	$V_{EXCITATION+} – V_{EXCITATION–}$	Differential reference voltage to the ADC

6.6.4 Design Notes

The unipolar excitation voltage, $V_{EXCITATION}$, is used as the ADC supply voltage (AVDD) as well as the ADC reference voltage, V_{REF}. Small variations in the bridge resistance due to tension or compression cause the differential output voltage for each bridge to change. The bridge output voltage is reduced compared to a single bridge measurement because $V_{EXCITATION}$ is divided between Bridge A and Bridge B. The PGA integrated into the ADC gains up the low-level bridge output signal to reduce system noise and utilize more of the ADC full-scale range (FSR). The ADC samples and converts this amplified voltage against V_{REF}. This measurement is not ratiometric because the output voltage of Bridge A can change depending on the properties of Bridge B (and vice versa). This dependence occurs even in the absence of a change in the applied load, resulting in a pseudo-ratiometric reference configuration. This challenge can be removed by using a dedicated set of reference inputs per bridge, assuming the ADC has multiple differential reference inputs.

Measuring multiple four-wire resistive bridges in series using a pseudo-ratiometric reference and a unipolar, low-voltage (≤ 5 V) supply requires:

- Multiple differential analog inputs (AINP*x* and AINN*x*) ***or*** external multiplexer
- External reference input (dedicated pin ***or*** use analog supply)
- Low-noise amplifier

When implementing a circuit with multiple bridges in series, it is important to use sensors with similar parameters (should be the same for each bridge) as mentioned in Table 6-14. Following this guideline simplifies how the common-mode voltage for each bridge is determined. Additionally, using bridges with different nominal resistances can introduce gain errors as well as make it more challenging to determine the load weight. This

latter challenge can be removed by using a dedicated set of reference inputs per bridge, assuming the ADC has multiple differential reference inputs.

To begin a design, start by using the equations in Table 6-15 to calculate the bridge output common-mode voltage, $V_{CM(Bridge\_A)}$ and $V_{CM(Bridge\_B)}$, under a no-load condition (R1 = R2 = R3 = R4). For example, if R_{BRIDGE} = 1 kΩ and $V_{EXCITATION}$ = 5 V, Equation 65 and Equation 66 yield the following results:

$$V_{CM(Bridge\_A)} = 5\ V \bullet (3 / 4) = 3.75\ V \quad (65)$$

$$V_{CM(Bridge\_B)} = 5\ V \bullet (1 / 4) = 1.25\ V \quad (66)$$

Figure 6-12 shows the voltage level at each input of the ADC multiplexer and how each will be applied to the same amplifier.

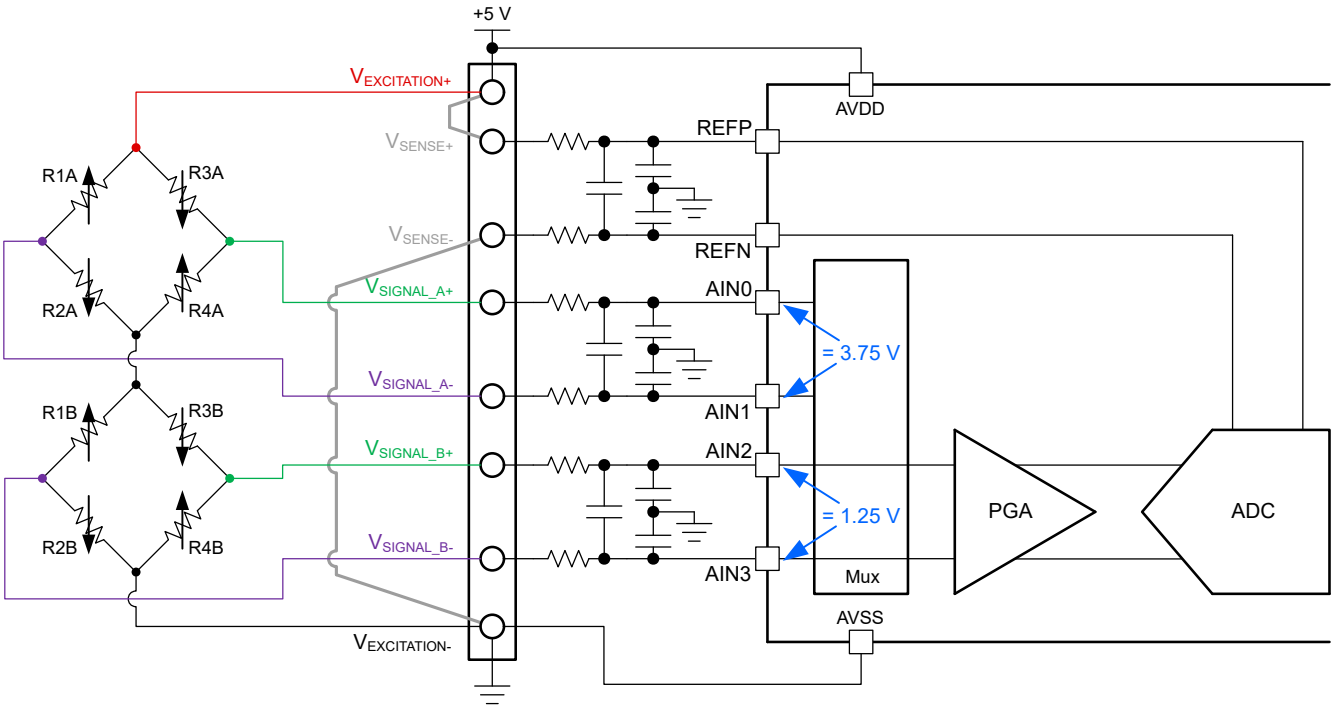

Figure 6-12. Common-Mode Voltage for Two Bridges in a Series Configuration

Unlike the previous examples where one of the system parameters was a specific ADC amplifier common-mode voltage target, a series combination of bridges requires identifying the ADC amplifier common-mode voltage *range*, $V_{CM(ADC)\_RANGE}$. This range helps accommodate a potentially wide variance between $V_{CM(Bridge\_A)}$ and $V_{CM(Bridge\_B)}$, which is the case in Figure 6-12. As described in Section 6.3.4, many ADCs used for bridge measurement applications have support collateral that can help identify the ADC amplifier common-mode range for a particular set of input conditions.

Figure 6-13 shows an example of how the *Common-Mode Range Calculator* from the ADS1261 Excel Calculator can be used to determine if $V_{CM(Bridge\_A)}$ and $V_{CM(Bridge\_B)}$ are within the input range of the amplifier integrated into the ADS1261.

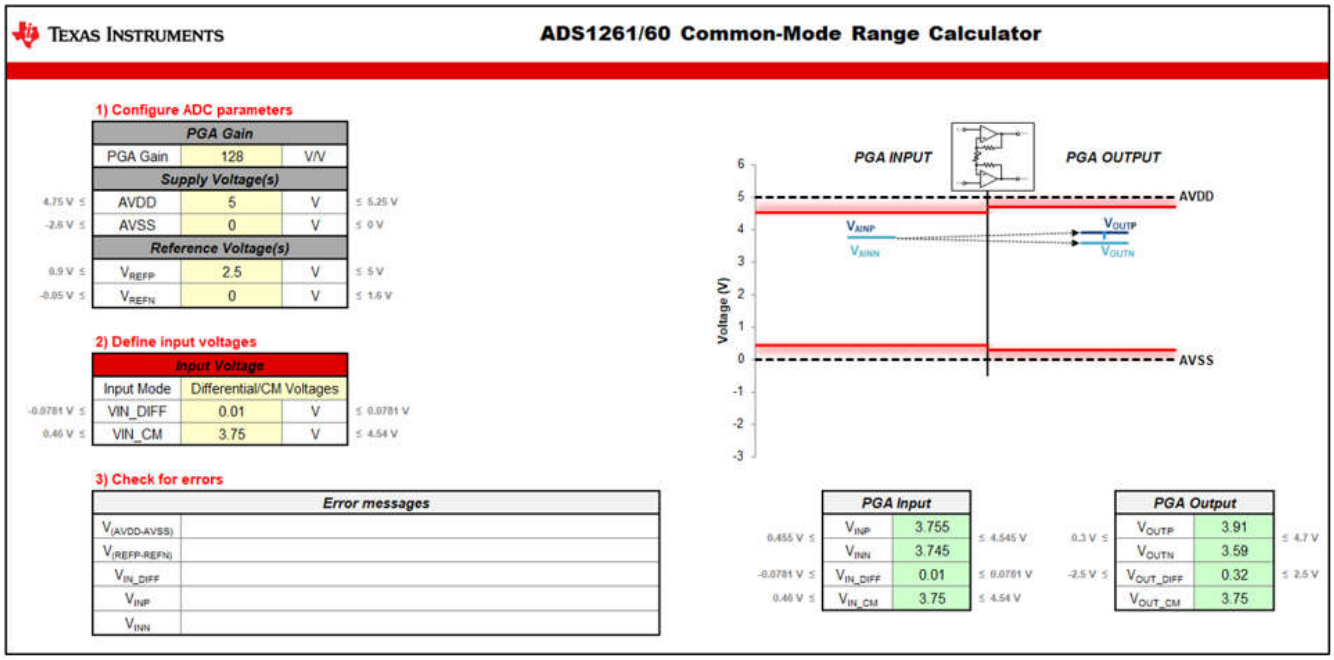

Figure 6-13. Verifying System Requirements Using the ADS1261 VCM Calculator Tool

In Figure 6-13, VIN_CM = 3.75 V to check if the ADC amplifier can accept $V_{CM(Bridge\_A)}$. The tool shows no errors for an input signal with this common-mode voltage, indicating that this is a valid input condition when gain = 128, AVDD = 5 V, and VIN_DIFF = 10 mV (though not shown, VIN_CM = 1.25 V is also a valid input condition). Moreover, the tool shows that for these specific settings, $V_{CM(ADC)\_RANGE}$ extends from 0.45 V to 4.54 V, indicating that the ADC amplifier can accept both $V_{CM(Bridge\_A)}$ and $V_{CM(Bridge\_B)}$.

Note that $V_{CM(ADC)\_RANGE}$ depends on the PGA gain in this example. Therefore, the PGA gain for each bridge must be selected in conjunction with confirming that $V_{CM(Bridge\_A)}$ and $V_{CM(Bridge\_B)}$ are within $V_{CM(ADC)\_RANGE}$. The PGA gain should be the largest allowable value that is still less than the ADC FSR. In some cases it is not possible to choose an amplifier gain that uses the entire ADC FSR. While this is often an acceptable tradeoff between resolution and ease-of-use, care should be taken to ensure that all system requirements are still met when the ADC FSR cannot be maximized.

Next, identify the maximum differential output voltage of each bridge, $V_{OUT(Bridge\ Max)}$, using the equation from Table 6-15 and parameters from Table 6-14. This value provides the maximum output voltage possible from the bridge under normal operating conditions and corresponds to the maximum load that can be applied to the bridge, $Load_{(Bridge\ Max)}$. If the system does not use the entire bridge output range, $V_{OUT(System\ Max)}$ defines the maximum differential output signal that is applied to a specific system and $Load_{(System\ Max)}$ is the corresponding maximum load. For example, if $V_{OUT(Bridge\ Max)}$ corresponds to $Load_{(Bridge\ Max)}$ = 5 kg, but the system specifications only require that Load(System Max) = 2.5 kg, then $V_{OUT(System\ Max)}$ is given by Equation 67:

$$V_{OUT(System\ Max)} = V_{OUT(Bridge\ Max)} \bullet (2.5\ kg / 5\ kg) = V_{OUT(Bridge\ Max)} / 2 \quad (67)$$

Note that if $Load_{(System\ Max)} = Load_{(Bridge\ Max)}$, then $V_{OUT(System\ Max)} = V_{OUT(Bridge\ Max)}$.

Finally, follow the instructions in Section 5.5 if calibration is required. Note that each bridge in Figure 6-11 must be calibrated separately, requiring the host processor to calculate and store multiple sets of calibration coefficients.

6.6.5 Measurement Conversion

To better understand how the output code is determined, it is helpful to know how the least significant bit, or LSB, is calculated as per Equation 68:

$$LSB = FSR / 2^N = (A \cdot V_{REF} / gain) / 2^N \quad (68)$$

where:

- N is the ADC resolution
- A is a scaling factor related to the ADC analog voltage range

The ADC analog input voltage range information is generally found in either the *Electrical Characteristics* or *Recommended Operating Conditions* table in the data sheet. After identifying this range, the scaling factor A can be derived using the following examples:

- A = 4 if FSR = $\pm 2 \cdot V_{REF}$ / gain
- A = 2 if FSR = $\pm V_{REF}$ / gain
- A = 1 if FSR = $\pm 0.5 \cdot V_{REF}$ / gain
- A = 1 if FSR = 0 to V_{REF} / gain

Note that each FSR equation in the preceding list includes a gain term for completeness even though the scaling factor A is independent of gain. Using this information, the output code is defined by Equation 69 and the applied load, W, can be calculated using Equation 70:

$$\text{Output Code} = (2^N \cdot \text{Gain} \cdot V_{IN}) / (A \cdot V_{REF}) \quad (69)$$

$$W = M \cdot (\text{Output Code} - B_{Actual}) \quad (70)$$

where:

- M is a calculated scaling factor
- B_{Actual} is the measured offset

Refer to Section 5.5.3 for more information about how Equation 70 is derived.

6.6.6 Generic Register Settings

To measure Bridge_A:

- Select multiplexer settings for AINP and AINN to measure V_{IN} of Bridge_A. In Figure 6-11, this corresponds to AIN0 and AIN1, respectively
- Enable the amplifier and set gain to the desired value as per the instructions in this section
- Select data rate and digital filter settings, as per Section 5.2.1 and Section 5.3
- Select the external reference input

To measure Bridge_B:

- Select multiplexer settings for AINP and AINN to measure V_{IN} of Bridge_B. In Figure 6-11, this corresponds to AIN2 and AIN3, respectively
- Enable the amplifier and set gain to the desired value (if different from Bridge_A)
- Select data rate and digital filter settings (if different from Bridge_A)

6.7 Measuring Multiple Four-Wire Resistive Bridges in Parallel Using a Single-Channel ADC With a Ratiometric Reference and a Unipolar, Low-Voltage (≤ 5 V) Excitation Source

It is possible to measure multiple four-wire resistive bridges using a single-channel ADC, a single ratiometric reference, and a constant voltage to excite the sensor. Figure 6-14 shows a schematic for measuring four bridge circuits in parallel using a 5-V supply, a single-channel ADC, and a ratiometric reference configuration. The ADC uses the excitation voltage as the analog supply and differential reference voltage to help eliminate errors due to the noise and drift in the excitation source.

6.7.1 Schematic

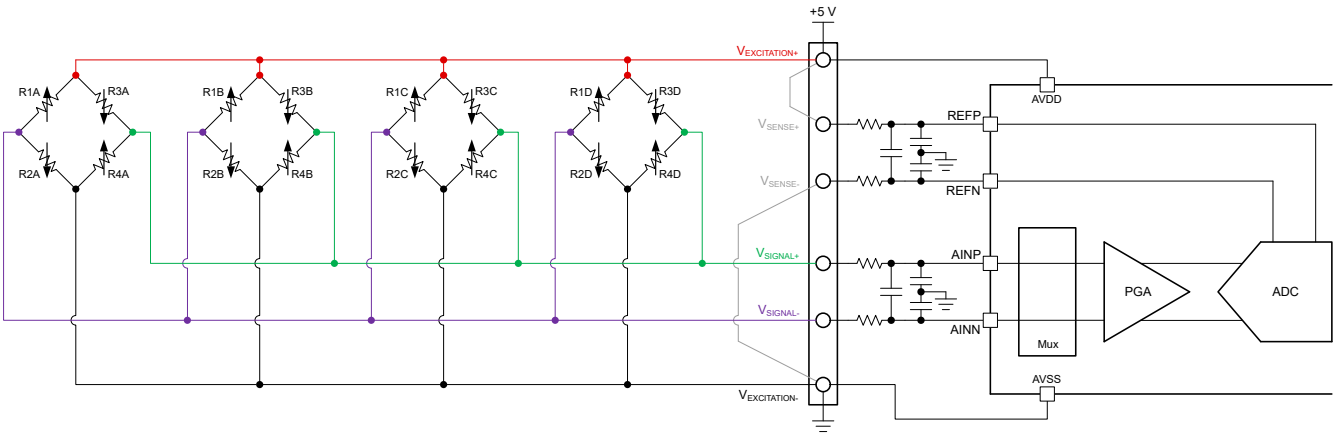

Figure 6-14. Measuring Multiple Four-Wire Resistive Bridges in Parallel Using a Single-Channel ADC With a Ratiometric Reference and a Unipolar, Low-Voltage (≤ 5 V) Excitation Source

6.7.2 Pros and Cons

Pros:

- Simple implementation requiring only a few passive components
- Ratiometric measurement, excitation source noise and drift are canceled
- Good for local measurements where the wire length is short
- Wire breaks for one bridge do not disturb the output for the other bridges
- Smaller ADC amplifier common-mode range required, especially if bridges have equivalent nominal impedance
- One measurement for all bridges increases throughput

Cons:

- Differences in bridge performance or specifications can cause inaccuracy that is not easily calibrated – requires external summing box or well-matched sensors
- Increased current through each bridge compared to measuring multiple bridges in series – increases power consumption and thermal effects due to sensor self-heating
- Excitation voltage is limited to ADC V_{REF} range
- Bridge common-mode voltage is limited by ADC analog input range
- Extended-length sensor wires can lead to IR losses such that $V_{EXCITATION} \neq V_{REF}$. This can be removed with a six-wire connection as per Section 6.2

6.7.3 Parameters and Variables

Table 6-16 defines important parameters and Table 6-17 provides equations for different variables. These parameters and variables are specific to this bridge configuration.

Table 6-16. User-Defined System Parameters

Parameter	Description
$V_{EXCITATION}$	Excitation voltage applied to the parallel combination of all bridges
R_{BRIDGE} (1)	Nominal impedance of each bridge
Bridge Sensitivity (1)	Change in bridge output voltage relative to excitation voltage
$Load_{(Bridge\ Max)}$ (1)	Maximum load that can be applied to the bridge

(1) Should be the same for each bridge

Table 6-17. Variable Equations and Definitions

Variable	Equation	Description
$V_{CM(Bridge)}$	$(V_{EXCITATION+} – V_{EXCITATION–}) / 2$	Output common-mode voltage for all bridges
$Load_{(System\ Max)}$	# of bridges • $Load_{(Bridge\ Max)}$	Maximum load applied to the bridge in the system (can be > $Load_{(Bridge\ Max)}$)
$V_{OUT(Bridge\ Max)}$	$V_{EXCITATION}$ • Bridge Sensitivity	Maximum differential output voltage of each bridge
$V_{OUT(Max)}$	# of bridges • $V_{OUT(Bridge\ Max)}$	Maximum combined differential voltage for all bridges
V_{IN}	$V_{SIGNAL+} – V_{SIGNAL–}$	Differential input voltage to the ADC
V_{REF}	$V_{EXCITATION+} – V_{EXCITATION–}$	Differential reference voltage to the ADC

6.7.4 Design Notes

The unipolar excitation voltage, $V_{EXCITATION}$, is used as the ADC supply voltage (AVDD) as well as the ADC reference voltage, V_{REF}. Small variations in the bridge resistance due to tension or compression change the differential output voltage for each bridge. The circuit configuration combines and averages the output of each bridge to generate a voltage that is proportional to the applied load. The PGA integrated into the ADC gains up this low-level signal to reduce system noise and utilize more of the ADC full-scale range (FSR). The ADC samples and converts this amplified voltage against V_{REF}, which is the same voltage used to excite each bridge and therefore ratiometric. The excitation source noise and drift are seen equally in both V_{IN} and V_{REF} in a ratiometric reference configuration, effectively removing these errors from the ADC output code.

Measuring multiple four-wire resistive bridges in parallel using a single-channel ADC, a ratiometric reference, and a unipolar, low-voltage (≤ 5 V) supply requires:

- Differential analog inputs (AINP and AINN)
- External reference input (dedicated pin ***or*** use analog supply)
- Low-noise amplifier

When measuring multiple bridges in parallel using a multichannel ADC, the ADC measures each bridge individually and the host processor sums these values together to determine the applied load. When measuring multiple bridges in parallel using a single-channel ADC, this *summation* occurs before the input signal is applied to the ADC. To understand how the bridge circuit in Figure 6-14 yields a voltage proportional to the applied load, it is helpful to convert each bridge into its Thevenin equivalent.

Figure 6-15 derives the Thevenin equivalent of the standard bridge circuit using the assumption that R >> ΔR.

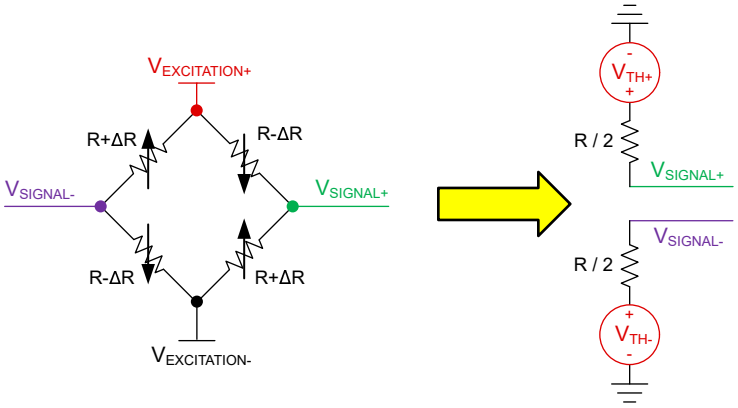

Figure 6-15. Thevenin Equivalent of a Single Bridge Circuit

In Figure 6-15, V_{TH+} and $V_{TH–}$ can be calculated using Equation 71 and Equation 72, respectively:

$$V_{TH+} = \frac{V_{EXCITATION}}{2} + \frac{V_{EXCITATION}}{2} \cdot \left(\frac{\Delta R}{R}\right) = \frac{V_{EXCITATION}}{2} \cdot \left(1 + \frac{\Delta R}{R}\right) \quad (71)$$

$$V_{TH-} = \frac{V_{EXCITATION}}{2} - \frac{V_{EXCITATION}}{2} \cdot \left(\frac{\Delta R}{R}\right) = \frac{V_{EXCITATION}}{2} \cdot \left(1 - \frac{\Delta R}{R}\right) \quad (72)$$

Figure 6-16 applies the result from Figure 6-15 to show the Thevenin equivalent circuit for all four bridges in Figure 6-14 (Bridge A, B, C, and D). This result helps determine how the complete bridge circuit yields an output voltage proportional to the applied load.

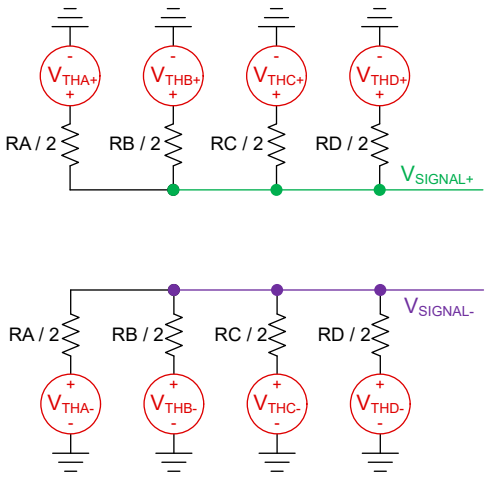

Figure 6-16. Thevenin Equivalent of Four Bridge Circuits in Parallel

Equation 73 defines the differential bridge output voltage at $V_{SIGNAL±}$ that is applied to the ADC inputs, V_{IN}, in Figure 6-14:

$$V_{IN} = V_{SIGNAL+} - V_{SIGNAL-} = V_{EXCITATION} \cdot \left(\frac{\Delta RA + \Delta RB + \Delta RC + \Delta RD}{RA + RB + RC + RD}\right) \quad (73)$$

Assuming RA = RB = RC = RD = R such that all nominal bridge resistances are identical, Equation 73 reduces to Equation 74:

$$V_{IN} = V_{SIGNAL+} - V_{SIGNAL-} = V_{EXCITATION} \cdot \left(\frac{\Delta RA + \Delta RB + \Delta RC + \Delta RD}{4 \cdot R}\right) \quad (74)$$

Ultimately, V_{IN} is proportional to $V_{EXCITATION}$ scaled by the average value of the change in each bridge resistance.

To understand how the result in Equation 74 translates to a real system, one common application for measuring multiple resistive bridges in parallel using a single-channel ADC is determining the weight of a load on a platform. The bridges are placed at specific points around the platform, and the weight of the load is determined by the methodology described in this section. This is especially useful when the load is not centered on the platform because the weight measured by each bridge scales relative to the distance from the load. A red, centered load is shown in Figure 6-17 (left) while a non-centered load is shown in Figure 6-17 (right). Each platform in Figure 6-17 has four bridges (in blue), similar to the circuit shown in Figure 6-14.

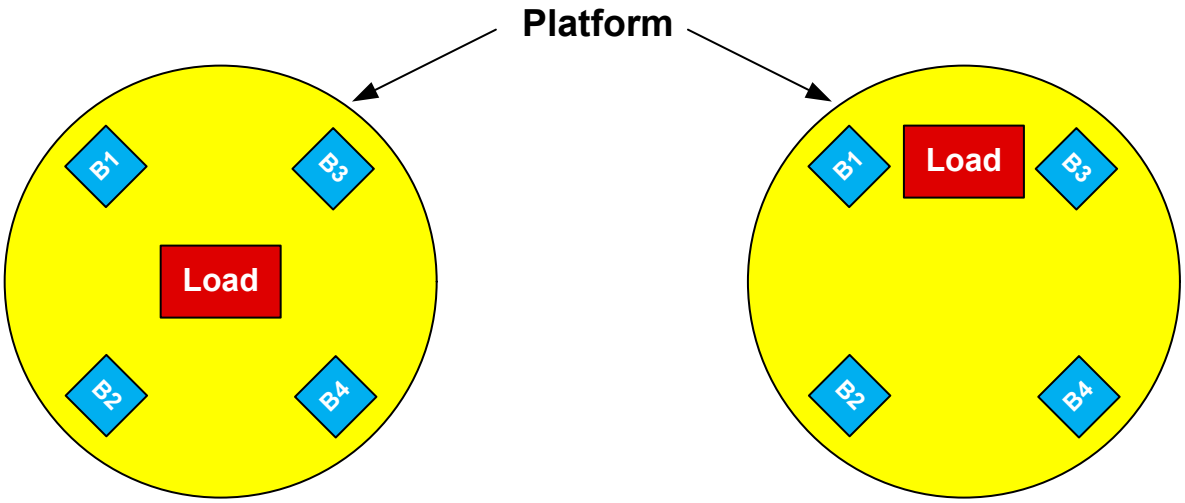

Figure 6-17. Measuring a Load on a Platform Using Multiple Bridges in Parallel: Centered Load (left) and Non-Centered Load (right)

In Figure 6-17 (left), each bridge ideally measures 1/4 of the overall load when the load is centered on the platform. When the load is not centered, as shown in Figure 6-17 (right), Bridge 1 (B1) and Bridge 3 (B3) measure a larger percentage of the overall load compared to Bridge 2 (B2) and Bridge 4 (B4). For example, B1 and B3 might each measure 45% of the total load, while B2 and B4 only measure 5% each. As a result, it is important to use bridges with similar parameters (Should be the same for each bridge) as mentioned in Table 6-16. Using the same component for each bridge in a parallel configuration with a single-channel ADC helps simplify the calculations that determine the total load.

Specifically, the total load, $Load_{(System\ Max)}$, in this parallel bridge configuration is equal to the sum of the maximum load that can be applied to each bridge, $Load_{(Bridge\ Max)}$. Assuming the table note for Table 6-16 is respected such that $Load_{(Bridge\ Max)}$ is the same for all bridges, then $Load_{(System\ Max)}$ = # of bridges • $Load_{(Bridge\ Max)}$. For example, if $Load_{(Bridge\ Max)}$ = 5 kg for each bridge in Figure 6-14, then $Load_{(System\ Max)}$ = 4 • 5 kg = 20 kg. Therefore, it is possible that each bridge can deliver the maximum differential output voltage, $V_{OUT(Bridge\ Max)}$, at any time. Since this specific circuit configuration combines the output voltage of each bridge to create $V_{SIGNAL±}$, it is also necessary to determine the maximum signal that can be applied to the ADC, $V_{OUT(Max)}$, as per Table 6-17.

After $V_{OUT(Max)}$ has been determined, choose the corresponding gain value for the ADC PGA. The amplifier gain should be the largest allowable value that is still less than the ADC FSR. In some cases it is not possible to choose an amplifier gain that uses the entire ADC FSR. While this is often an acceptable tradeoff between resolution and ease-of-use, care should be taken to ensure that all system requirements are still met when the ADC FSR cannot be maximized.

Next, ensure that the bridge output common-mode voltage, $V_{CM(Bridge)}$, defined in Table 6-17 is within the common-mode range of the ADC amplifier, $V_{CM(ADC)}$, under a no-load condition (R1 = R2 = R3 = R4). The amplifier common-mode range varies by component, and is defined in the data sheet based on the gain setting and supply voltage. However, targeting $V_{CM(Bridge)}$ = AVDD / 2 is a good choice as this is typically in the center of

the $V_{CM(ADC)}$ range, enabling the highest gain possible per the previous step. Moreover, the bridge configuration in Figure 6-14 inherently sets $V_{CM(Bridge)}$ to AVDD / 2 under a no-load condition when $V_{EXCITATION}$ = AVDD.

Finally, the circuit in Figure 6-14 introduces an additional challenge in that there is no easy way to calibrate each bridge because they all share the $V_{SIGNAL±}$ leads. This is dissimilar from a circuit with multiple bridges in parallel using a multichannel ADC because each bridge is measured independently in that case. That circuit configuration allows the host processor to derive specific calibration coefficients for each bridge and remove the measurement error before summation. Comparatively, the system in Figure 6-14 combines all of the bridge errors together. This results in a single set of calibration coefficients that are only applicable to the specific settings used during the calibration procedure.

To demonstrate why this issue occurs, Figure 6-18 plots hypothetical bridge responses for a weight-measurement system similar to Figure 6-17. In this example, V_{REF} = $V_{EXCITATION}$ = 5 V, while each bridge has a sensitivity of 2 mV/V and $Load_{(Bridge\ Max)}$ = 2 kg. This system also has an applied load, W, of 2 kg.

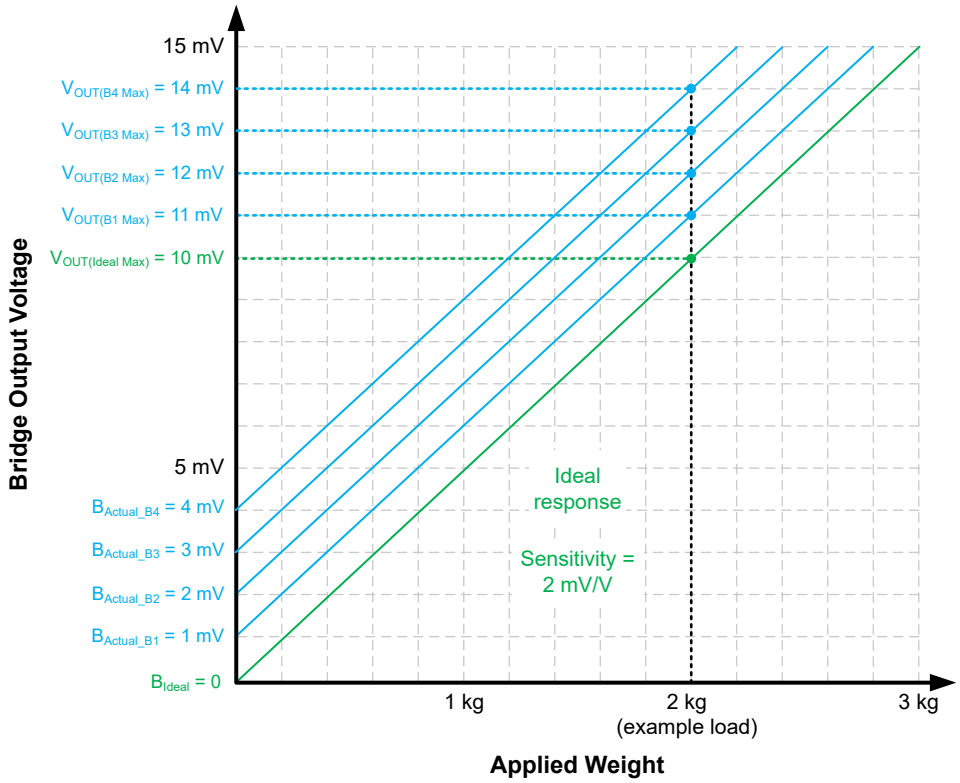

Figure 6-18. Calibrating a Weigh Scale System Using Four Bridges in Parallel With a Single-Channel ADC

Each of the four bridges in this example would have $V_{OUT(Bridge\ Max)}$ = $V_{OUT(Ideal\ Max)}$ = 10 mV if they all followed the green, ideal response in Figure 6-18. However, this example assumes each sensor has some offset value. As shown in the blue plots in Figure 6-18, B1 has an offset of 1 mV (B_{Actual_B1} = 1 mV), B_{Actual_B2} = 2 mV, B_{Actual_B3} = 3 mV, and B_{Actual_B4} = 4 mV. The offset-affected bridge response changes $V_{OUT(Bridge\ Max)}$ for each bridge ($V_{OUT(Bx\ Max)}$). The output voltage, V_B, for a single bridge in this example is given by Equation 75:

$$V_B = P_{Bridge} \cdot V_{OUT(Bridge\ Max)} \cdot (W / Load_{(Bridge\ Max)}) \quad (75)$$

In Equation 75, the scaling factor P_{Bridge} is the percentage of the total load measured by that specific bridge. Assuming a centered load as per Figure 6-17 (left), all four bridges in Figure 6-18 have P_{Bridge} = 1/4 = 25%. This is true whether they are ideal (green plot) or offset-affected (blue plots).

When P_{Bridge} = 25%, W = 2 kg, and $Load_{(Bridge\ Max)}$ = 2 kg, each of the four bridges represented by the green, ideal plot have an output voltage of 2.5 mV. This results in a total output voltage at $V_{SIGNAL±}$ of 4 · 2.5 mV = 10 mV. Comparatively, applying Equation 75 to the four blue, offset-affected bridge responses in Figure 6-18 yields the results in Equation 76 through Equation 79:

$$V_{B1} = 0.25 \cdot 11\ mV \cdot (2\ kg / 2\ kg) = 2.75\ mV \quad (76)$$

$$V_{B2} = 0.25 \cdot 12\ mV \cdot (2\ kg / 2\ kg) = 3.00\ mV \quad (77)$$

$$V_{B3} = 0.25 \cdot 13\ mV \cdot (2\ kg / 2\ kg) = 3.25\ mV \quad (78)$$

$$V_{B4} = 0.25 \cdot 14\ mV \cdot (2\ kg / 2\ kg) = 3.50\ mV \quad (79)$$

The total output voltage applied to $V_{SIGNAL±}$ is the sum of the results in Equation 76 through Equation 79, or 12.5 mV. This value includes an error of 2.5 mV compared to the ideal voltage of 10 mV. This error voltage is stored in the host processor as the offset calibration coefficient and removed from each subsequent measurement.

Next, assume the load is moved between B1 and B3 as shown in Figure 6-17 (right). In this case, the portion of the load measured by each bridge is unequal, which changes the output voltage from each bridge. Using the same distribution given earlier in this section (P_{B1} = P_{B3} = 45 %, P_{B2} = P_{B4} = 5%), the resulting output voltage from each bridge is given by Equation 80 through Equation 83:

$$V_{B1} = 0.45 \cdot 11\ mV \cdot (2\ kg / 2\ kg) = 4.95\ mV \quad (80)$$

$$V_{B2} = 0.05 \cdot 12\ mV \cdot (2\ kg / 2\ kg) = 0.60\ mV \quad (81)$$

$$V_{B3} = 0.45 \cdot 13\ mV \cdot (2\ kg / 2\ kg) = 5.85\ mV \quad (82)$$

$$V_{B4} = 0.05 \cdot 14\ mV \cdot (2\ kg / 2\ kg) = 0.70\ mV \quad (83)$$

Similar to the centered-load case, the total output voltage applied to $V_{SIGNAL±}$ is the sum of all V_{Bx}, or 12.1 mV. Subtracting the previously determined offset error value of 2.5 mV gives a calibrated voltage of 9.6 mV, resulting in a 4% error compared to the ideal value (10 mV). This outcome occurs despite the fact that the only difference between the first and second scenario is the location of the load on the scale. Accounting for other common errors such as sensitivity tolerance, ADC errors, gain error from the lead resistance, and variation in the nominal bridge resistances could further reduce the system accuracy.

Ultimately, systems that measure multiple bridges in parallel using a single-channel ADC require well-matched bridge sensors with similar specifications to maintain high performance results. Another option is to use an external summing box that calibrates any differences among the bridge sensors before the summation occurs. Finally, some low-accuracy systems may find the level of performance of this circuit acceptable compared to the increased throughput and ease-of-design.

6.7.5 Measurement Conversion

To better understand how the output code is determined, it is helpful to know how the least significant bit, or LSB, is calculated as per Equation 84:

$$LSB = FSR / 2^N = (A \bullet V_{REF} / gain) / 2^N \quad (84)$$

where:

- N is the ADC resolution
- A is a scaling factor related to the ADC analog voltage range

The ADC analog input voltage range information is generally found in either the *Electrical Characteristics* or *Recommended Operating Conditions* table in the data sheet. After identifying this range, the scaling factor A can be derived using the following examples:

- A = 4 if FSR = ±2 • V_{REF} / gain
- A = 2 if FSR = ±V_{REF} / gain

- A = 1 if FSR = ±0.5 • V_{REF} / gain
- A = 1 if FSR = 0 to V_{REF} / gain

Note that each FSR equation in the preceding list includes a gain term for completeness even though the scaling factor A is independent of gain. Using this information, the output code is defined by Equation 85 and the applied load, W, can be calculated using Equation 86:

$$\text{Output Code} = (2^N \bullet \text{Gain} \bullet V_{IN}) / (A \bullet V_{REF}) \quad (85)$$

$$W = M \bullet (\text{Output Code} - B_{Actual}) \quad (86)$$

where:

- M is a calculated scaling factor
- B_{Actual} is the measured offset

Refer to Section 5.5.3 for more information about how Equation 86 is derived.

6.7.6 Generic Register Settings

- Select multiplexer settings for AINP and AINN to measure V_{IN}
- Enable the amplifier and set gain to the desired value as per the instructions in this section
- Select data rate and digital filter settings, as per Section 5.2.1 and Section 5.3
- Select the external reference input

6.8 Measuring Multiple Four-Wire Resistive Bridges in Parallel Using a Multichannel ADC With a Ratiometric Reference and a Unipolar, Low-Voltage (≤ 5 V) Excitation Source

It is possible to measure multiple four-wire resistive bridges using a multichannel ADC, a single ratiometric reference, and a constant voltage to excite the sensor. Figure 6-19 shows a schematic for a measuring four bridge circuits in parallel using a 5-V supply, a multichannel ADC, and a ratiometric reference configuration. The ADC uses the excitation voltage as the analog supply and differential reference voltage to help eliminate errors due to the noise and drift in the excitation source.

6.8.1 Schematic

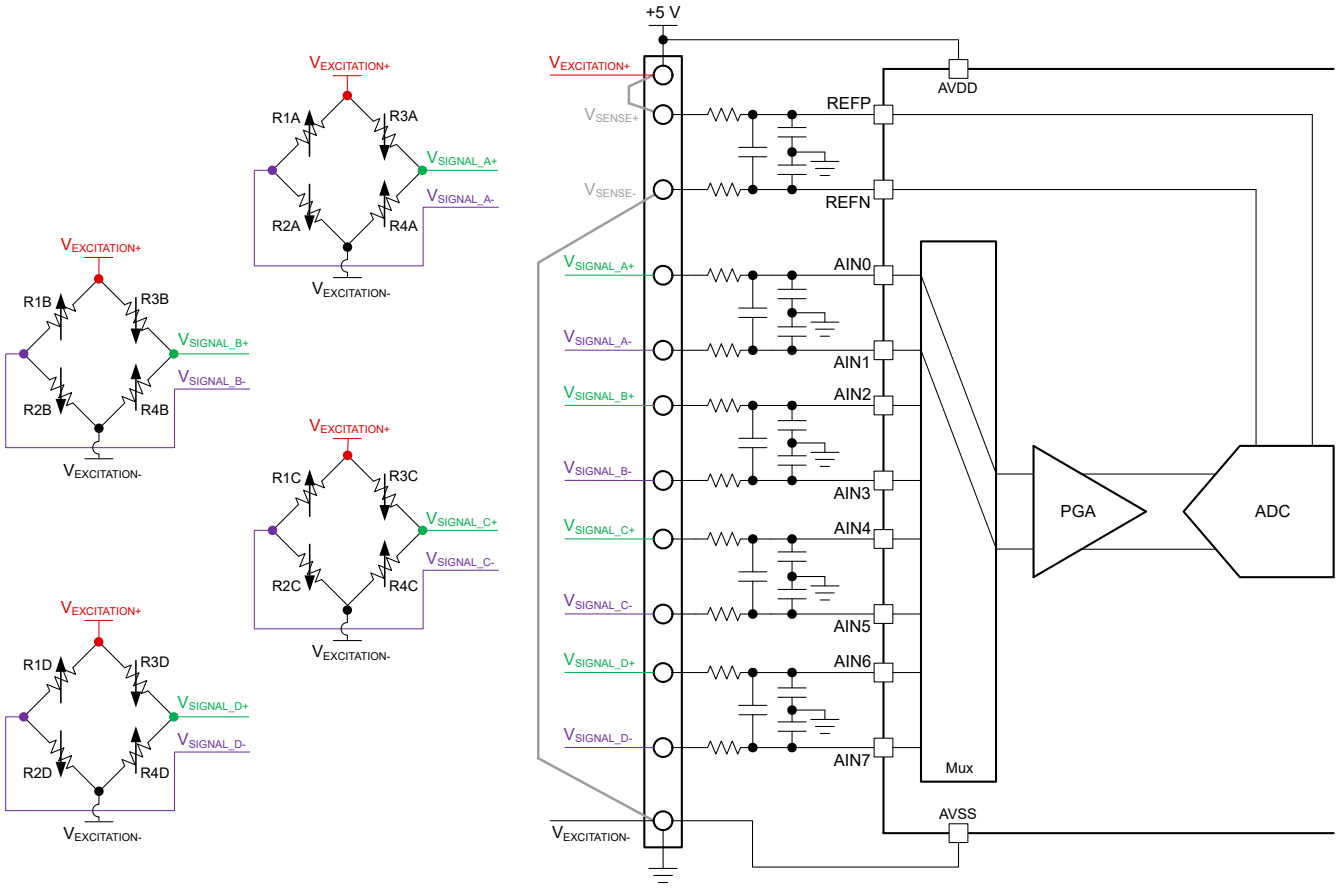

Figure 6-19. Measuring Multiple Four-Wire Resistive Bridges in Parallel Using a Multichannel ADC With a Ratiometric Reference and a Unipolar, Low-Voltage (≤ 5 V) Excitation Source

6.8.2 Pros and Cons

Pros:

- Simple implementation requiring only a few passive components
- Ratiometric measurement such that excitation source noise and drift are canceled
- Good for local measurements where the wire length is short
- Wire breaks for one bridge do not disturb the output for the other bridges
- Smaller ADC amplifier common-mode range required, especially if bridges have equivalent nominal impedance

Cons:

- Each bridge requires a discrete measurement to calculate the applied load, resulting in reduced throughput for multiplexed systems or requiring simultaneous sampling
- Increased current through each bridge compared to measuring multiple bridges in series – increases power consumption and thermal effects due to sensor self-heating

- Excitation voltage is limited to ADC V_{REF} range
- Bridge common-mode voltage is limited by ADC analog input range
- Extended-length sensor wires can lead to IR losses such that $V_{EXCITATION} \neq V_{REF}$. This can be removed with a six-wire connection as per Section 6.2

6.8.3 Parameters and Variables

Table 6-18 defines important parameters and Table 6-19 provides equations for different variables. These parameters and variables are specific to this bridge configuration.

Table 6-18. User-Defined System Parameters

Parameter	Description
$V_{EXCITATION}$	Excitation voltage applied to the parallel combination of all bridges
R_{BRIDGE} (1)	Nominal impedance of each bridge
Bridge Sensitivity (1)	Change in bridge output voltage relative to excitation voltage
$Load_{(Bridge\ Max)}$ (1)	Maximum load that can be applied to the bridge

(1) Should be the same for each bridge.

Table 6-19. Variable Equations and Definitions

Variable	Equation	Description
$V_{CM(Bridge)}$	$(V_{EXCITATION+} - V_{EXCITATION-}) / 2$	Output common-mode voltage for all bridges
$Load_{(System\ Max)}$	# of bridges • $Load_{(Bridge\ Max)}$	Maximum load applied to the bridge in the system (can be > $Load_{(Bridge\ Max)}$)
$V_{OUT(Bridge\ Max)}$	$V_{EXCITATION}$ • Bridge Sensitivity	Maximum differential output voltage of the bridge
V_{IN_A}	$V_{SIGNAL\_A+} - V_{SIGNAL\_A-}$	Differential input voltage to the ADC from Bridge A
V_{IN_B}	$V_{SIGNAL\_B+} - V_{SIGNAL\_B-}$	Differential input voltage to the ADC from Bridge B
V_{IN_C}	$V_{SIGNAL\_C+} - V_{SIGNAL\_C-}$	Differential input voltage to the ADC from Bridge C
V_{IN_D}	$V_{SIGNAL\_D+} - V_{SIGNAL\_D-}$	Differential input voltage to the ADC from Bridge D
V_{REF}	$V_{EXCITATION+} - V_{EXCITATION-}$	Differential reference voltage to the ADC

6.8.4 Design Notes

The unipolar excitation voltage, $V_{EXCITATION}$, is used as the ADC supply voltage (AVDD) as well as the ADC reference voltage, V_{REF}. Small variations in the bridge resistance due to tension or compression change the differential output voltage for each bridge. The system measures each bridge output and the PGA integrated into the ADC gains up the low-level signal to reduce system noise and utilize more of the ADC full-scale range (FSR). The ADC samples and converts this amplified voltage against V_{REF}, which is the same voltage used to excite each bridge and therefore ratiometric. The excitation source noise and drift are seen equally in both V_{IN} and V_{REF} in a ratiometric reference configuration, effectively removing these errors from the ADC output code. The host processor sums the ADC output from each bridge to determine the value of the applied load.

Measuring multiple four-wire resistive bridges in parallel using a multichannel ADC, a ratiometric reference, and a unipolar, low-voltage (≤ 5 V) supply requires:

- Multiple differential analog inputs (AINP*x* and AINN*x*) ***or*** external multiplexer
- External reference input (dedicated pin ***or*** use analog supply)
- Low-noise amplifier

Similar to the previous bridge circuit, a common application for measuring multiple resistive bridges in parallel using a multichannel ADC is determining the weight of a load on a platform. The bridges are placed at specific points around the platform and each bridge is measured by the ADC. The host processor sums these individual measurements together to determine the weight of the load. This is especially useful when the load is not centered on the platform, since the weight measured by each bridge scales relative to the distance from the load. A red, centered load is shown in Figure 6-20 (left) while a non-centered load is shown in Figure 6-20 (right). Each platform in Figure 6-20 has four bridges (in blue), similar to the system shown in Figure 6-19.

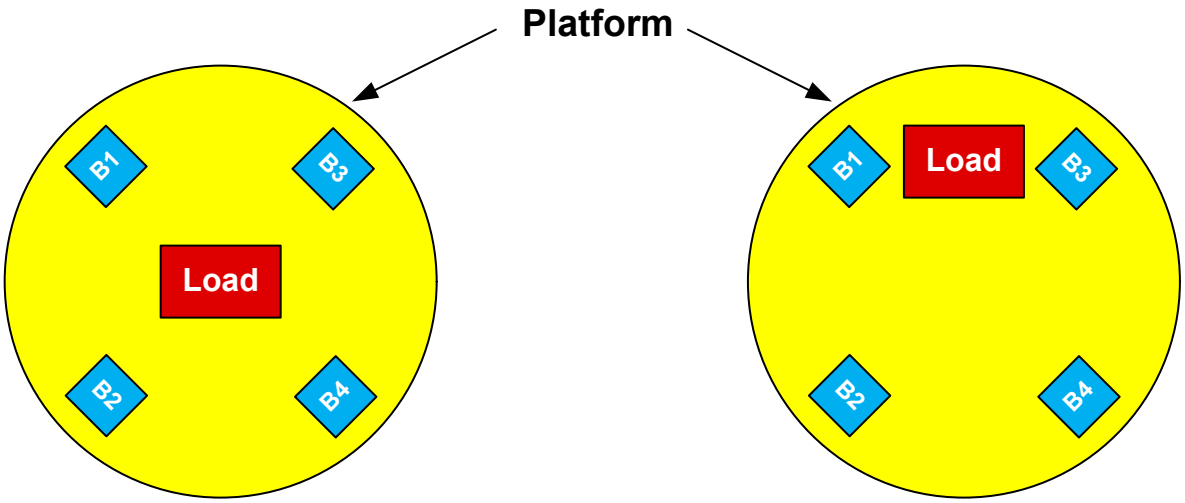

Figure 6-20. Measuring a Load on a Platform Using Multiple Bridges in Parallel: Centered Load (left) and Non-Centered Load (right)

In Figure 6-20 (left), each bridge ideally measures 1/4 of the overall load when the load is centered on the platform. When the load is not centered, as shown in Figure 6-20 (right), Bridge 1 (B1) and Bridge 3 (B3) measure a larger percentage of the overall load compared to Bridge 2 (B2) and Bridge 4 (B4). For example, B1 and B3 might each measure 45% of the total load, while B2 and B4 only measure 5% each. As a result, it is important to use bridges with similar parameters (should be the same for each bridge) as mentioned in Table 6-18 because this helps simplify how the total load weight is determined.

Specifically, the total load, $Load_{(System\ Max)}$, in a parallel bridge configuration is equal to the sum of the maximum load that can be applied to each bridge, $Load_{(Bridge\ Max)}$. Assuming the table note for Table 6-18 is respected such that $Load_{(Bridge\ Max)}$ is the same for all bridges, then $Load_{(System\ Max)}$ = # of bridges • $Load_{(Bridge\ Max)}$. For example, if $Load_{(Bridge\ Max)}$ = 5 kg for each bridge in Figure 6-19, then $Load_{(System\ Max)}$ = 4 • 5 kg = 20 kg. Therefore, it must be assumed that any bridge can deliver the maximum differential output voltage, $V_{OUT(Bridge\ Max)}$, at any time. $V_{OUT(Bridge\ Max)}$ should be the same for all bridges, and the equation is shown in Table 6-19.

After $V_{OUT(System\ Max)}$ has been determined, choose the corresponding gain value for the ADC PGA. The amplifier gain should be the largest allowable value that is still less than the ADC FSR. In some cases it is not possible to choose an amplifier gain that uses the entire ADC FSR. While this is often an acceptable tradeoff between resolution and ease-of-use, take care to ensure that all system requirements are still met when the ADC FSR cannot be maximized.

Next, ensure that the bridge output common-mode voltage, $V_{CM(Bridge)}$, defined in Table 6-19 is within the common-mode range of the ADC amplifier, $V_{CM(ADC)}$, under a no-load condition (R1 = R2 = R3 = R4). The amplifier common-mode range varies by component, and is defined in the data sheet based on the gain setting and supply voltage. However, targeting $V_{CM(Bridge)}$ = AVDD / 2 is a good choice as this is typically in the center of the $V_{CM(ADC)}$ range, enabling the highest gain possible per the previous step. Moreover, the bridge configuration in Figure 6-19 inherently sets $V_{CM(Bridge)}$ to AVDD / 2 under a no-load condition when $V_{EXCITATION}$ = AVDD.

Then, follow the instructions in Section 5.5 if calibration is required. Note that each bridge in Figure 6-19 must be calibrated separately, requiring the host processor to calculate and store multiple sets of calibration coefficients.

Finally, the host processor needs to convert the ADC output code from each bridge measurement to a voltage and then sum these values together to determine the value of the applied load.

6.8.5 Measurement Conversion

To better understand how the output code is determined, it is helpful to know how the least significant bit, or LSB, is calculated as per Equation 87:

$$LSB = FSR / 2^N = (A \cdot V_{REF} / gain) / 2^N \quad (87)$$

where:

- N is the ADC resolution
- A is a scaling factor related to the ADC analog voltage range

The ADC analog input voltage range information is generally found in either the *Electrical Characteristics* or *Recommended Operating Conditions* table in the data sheet. After identifying this range, the scaling factor A can be derived using the following examples:

- A = 4 if FSR = ±2 • V_{REF} / gain
- A = 2 if FSR = ±V_{REF} / gain
- A = 1 if FSR = ±0.5 • V_{REF} / gain
- A = 1 if FSR = 0 to V_{REF} / gain

Note that each FSR equation in the preceding list includes a gain term for completeness even though the scaling factor A is independent of gain. Using this information, the output code is defined by Equation 88 and the applied load, W, can be calculated using Equation 89:

$$\text{Output Code} = (2^N \cdot \text{Gain} \cdot V_{IN}) / (A \cdot V_{REF}) \quad (88)$$

$$W = M \cdot (\text{Output Code} - B_{Actual}) \quad (89)$$

where:

- M is a calculated scaling factor
- B_{Actual} is the measured offset

Refer to Section 5.5.3 for more information about how Equation 89 is derived.

6.8.6 Generic Register Settings

To measure Bridge_A:

- Select multiplexer settings for AINP and AINN to measure V_{IN} of Bridge_A. In Figure 6-19, this corresponds to AIN0 and AIN1, respectively
- Enable the amplifier and set gain to the desired value as per the instructions in this section
- Select data rate and digital filter settings, as per Section 5.2.1 and Section 5.3
- Select the external reference input

To measure Bridge_B:

- Select multiplexer settings for AINP and AINN to measure V_{IN} of Bridge_B. In Figure 6-19, this corresponds to AIN2 and AIN3, respectively
- Enable the amplifier and set gain to the desired value (if different from Bridge_A)
- Select data rate and digital filter settings (if different from Bridge_A)

To measure Bridge_C:

- Select multiplexer settings for AINP and AINN to measure V_{IN} of Bridge_C. In Figure 6-19, this corresponds to AIN4 and AIN5, respectively
- Enable the amplifier and set gain to the desired value (if different from Bridge_B)
- Select data rate and digital filter settings (if different from Bridge_B)

To measure Bridge_D:

- Select multiplexer settings for AINP and AINN to measure V_{IN} of Bridge_D. In Figure 6-19, this corresponds to AIN6 and AIN7, respectively
- Enable the amplifier and set gain to the desired value (if different from Bridge_C)
- Select data rate and digital filter settings (if different from Bridge_C)

7 Summary

Resistive bridge circuits are a versatile and commonly-used sensor type in industrial applications, measuring signals such as weight, pressure, temperature, and flow. Achieving the most accurate bridge measurements with precision ADCs requires a detailed understanding of how these sensors work, how they are calibrated, how they connect to an ADC, and how the ADC is configured.

This application note presents an overview of the bridge circuit, how bridges are used to measure different forces, how the ADC measurement is configured, and what errors may arise in the measurement. This application note starts with an overview of bridge circuit basics, how they are constructed, and what parameters are important when designing a bridge measurement system. Circuits are presented showing connections to precision ADCs.

The circuits shown in this application note are an introduction to bridge measurement systems, and are not meant to be all-inclusive. Instead, these circuits represent basic topologies that can be modified or combined to fit specific systems requirements.

8 Revision History

Changes from Revision * (February 2022) to Revision A (March 2024)	Page
• Updated the numbering format for tables, figures, and cross-references throughout the document	1
• Updated equation 10.	8

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