Application Note

Understanding and Using SAR ADC SPICE Micromodel

Arthur Kay *Precision ADC*

ABSTRACT

This application note provides an overview of the internal topology of the Texas Instruments flexible SAR ADC model. The document also shows how to use this model to help optimize the SAR ADC input amplifier design, and reference settling circuit. Furthermore, the model can be used to predict analog performance of the circuit including noise, gain error, and offset error.

Table of Contents

Trademarks

PSpice® is a registered trademark of Cadence Design Systems, Inc..
All trademarks are the property of their respective owners.

1 Introduction

This document describes the operation and design of a flexible Successive Approximation Register (SAR) Analog to Digital Converter (ADC) model. The model was developed to be easily modifiable using SPICE parameters so that it can be used for simulating the behavior of many different SAR ADCs. By adjusting the parameters, this behavioral model can be modified to cover many different models of SAR ADCs. This document defines each parameter and shows how the parameter value can be determined from the device data sheet. Thus, if a model for a particular device is not available, the general model can be modified to cover most ADCs. Figure 1-1 shows the spice model with its associated parameter list. Various performance criteria such as input switching transients, noise, and offset can be modified by adjusting the model parameters. The first part of this document covers the internal operation of the model and how the external parameters can be set using data sheet criteria. The second part of this document covers ADC design optimization using the model. The final part of this document covers design performance verification using the model.

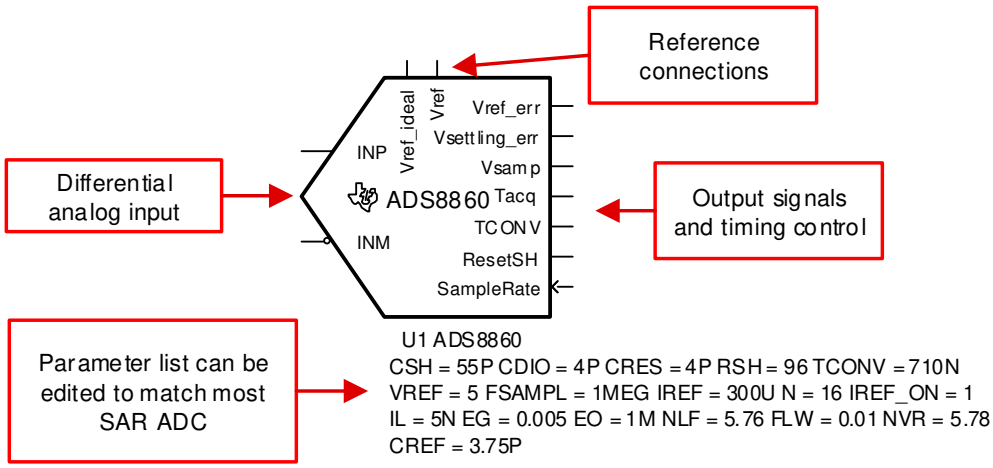

Figure 1-1. ADC Model With Parameters

2 Internal Topology of SAR ADC Model

This section provides a simplified description of the internal operation of the model. Also, the meaning of the external parameters and selection of values based on data sheet criteria are covered.

2.1 Sample and Hold

A SAR ADC operates by sampling the input signal during the acquisition period and holding the signal during the conversion period. The sampling action is performed during the acquisition period by closing switch SW1 and allowing sampling Csh to charge via resistor Rsh. At the end of the acquisition period, the switch is opened and the input voltage is held for conversion. To achieve minimal distortion, the capacitor Csh needs to be fully settled at the end of the acquisition phase to properly measure the externally applied signal. The settling is dependent on amplifier bandwidth, the external RC filter, the internal sampling circuit, and the ADC timing. The model has a Vsamp output that shows the sampling behavior, and a Vsettling_error output that displays the difference between the sampled value and the steady state input signal. This settling analysis can be used to facilitate the selection of the amplifier and optimization of the external RC circuit. An input drive circuit optimization is covered in detail in Section 3.1. Figure 2-1 illustrates the ADC system design with the internal sample and hold circuit. Note that Rsh and Csh are parameters that can be adjusted according to the ADC data sheet. Most SAR ADC data sheets provide an input sampling stage equivalent circuit. This circuit provides values for Rsh and Csh.

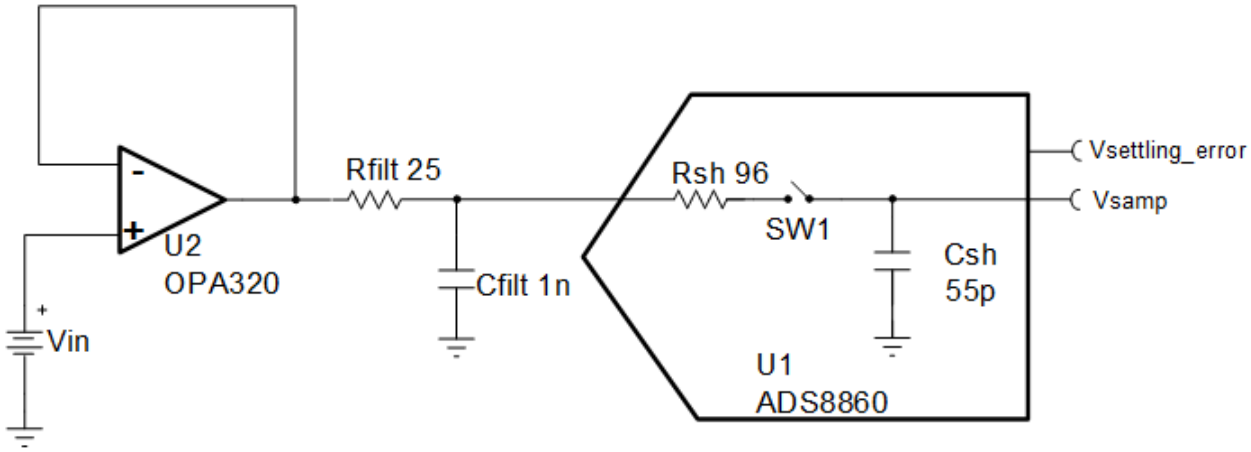

Figure 2-1. ADC System Showing External Drive Circuit and Internal Sample and Hold

2.2 Sample and Hold Timing

As previously mentioned, the conversion cycle is broken into an acquisition phase where the sample and hold switch is closed and a conversion phase where the switch is opened and the sampled signal is held. The conversion period is a fixed amount of time set by an internal oscillator or external clock signal. Most converters transition to the acquisition period whenever the ADC is not converting. For example, assume the converter has a conversion phase (TCONV) that lasts for 710 ns. If the device sampling rate is 1 Msps, or 1 sample/µs, then the acquisition period can be calculated by subtracting the conversion phase from the device throughput (tacq = throughput – TCONV= 1 µs – 710 ns = 290 ns). Furthermore, if the sampling rate is reduced to 100 ksps, the conversion period remains the same and the acquisition period naturally gets longer (tacq = 10 µs – 710 ns = 9.29 µs).

The model includes a parameter to set TCONV, and uses an external square wave to set the sampling rate. The external square wave triggers an internal one-shot timer that initiates the conversion phase. The conversion phase lasts for a time specified by the parameter TCONV. Inside the model the parameter TCONVis used to set the timing capacitor for the one-shot. Whenever the device is not converting it is acquiring, so the tacq signal is the inversion of TCONV.

The TCONVand tacq signals are used to control the timing of the sample and hold circuit. The sample and hold switch is closed throughout the tacq period and open during the TCONV period. At the end of the TCONVperiod a small reset sample and hold signal is generated. This signal connects Csh in parallel with a reset capacitor. The reset capacitor initially charged to 0 V, so when it is connected in parallel with Csh it causes the voltage on Csh to droop. This droop emulates the real-world behavior of a sample and hold circuit. The droop happens as a result of the conversion process and typically it is about 10% of the held voltage. Thus, Creset is typically sized to be 10% of Csh. Figure 2-2 below shows the sample and hold timing control.

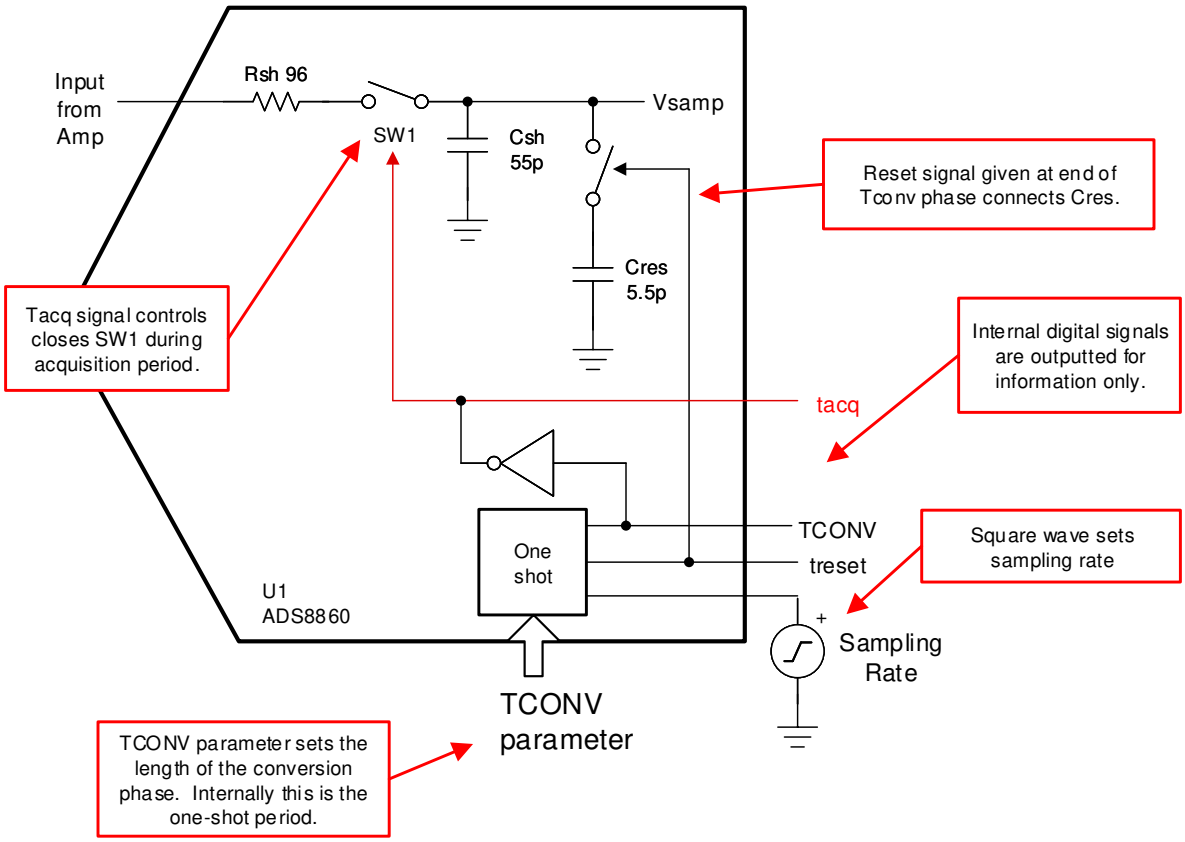

Figure 2-2. Sample and Hold Timing Control

2.3 Reference Transients

The reference input to many SAR ADCs is not a high impedance. This input has a switched capacitor input that can have multiple large transient currents over a short duration of time. In fact, the number of transients is typically equal to the device resolution, and these transients are spread equally across the conversion phase. So, a 16-bit converter with a 710-ns conversion phase has 16 transient pulses across the 710-ns conversion (710 ns / 16 = 44.375 ns between pulses). The average current for all these current pulses is generally provided in the data sheet. For each conversion phase, the magnitude of the current pulses starts large then diminishes throughout the conversion cycle. This model has parameters for the average reference current (Iref), the number of pulses (N), the reference value (Vref), and the sampling rate (Fsampl). All these parameters are used to generate the transient current waveform on the reference input. For example, the ADS8860 is a 16-bit converter with a 5-V reference that draws an average reference current of 300 µA at a sampling rate of 1 Msps so the parameters are set as follows: Iref = 300 µA, N = 16, Fsampl = 1 MHz, and Vref = 5 V. These parameters are applied to modeling equations that select the appropriate switching capacitor which generates the current transient waveform. The model uses timing control circuits to charge the Cref capacitor and to connect and disconnect the capacitor N number of times. In between each connection, the capacitor is reset to the appropriate voltage to generate the average current. Note that this exponential decay of the transient level approximates what happens in the real-world circuit. The real-world circuit transient level diminishes as shown in the simulation but also has some dependency on the input signal. Nevertheless, from a practical perspective the exponential decay of the transients is sufficient for accurate simulation results.

Figure 2-3 illustrates a simplified version of this circuit, and Figure 2-4 shows an example of the reference current for ADS8860.

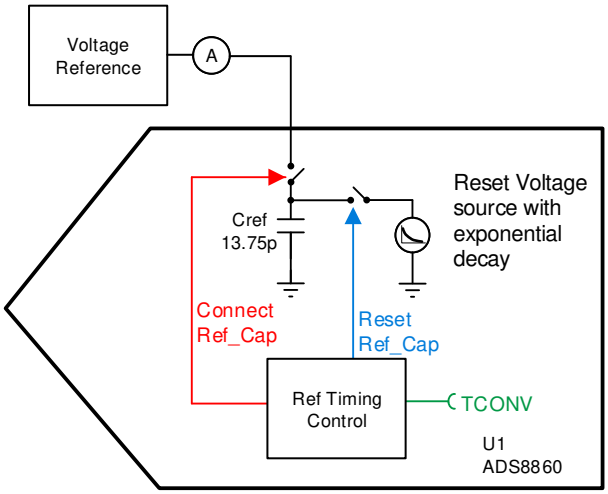

Figure 2-3. Reference Transient Current Block Diagram

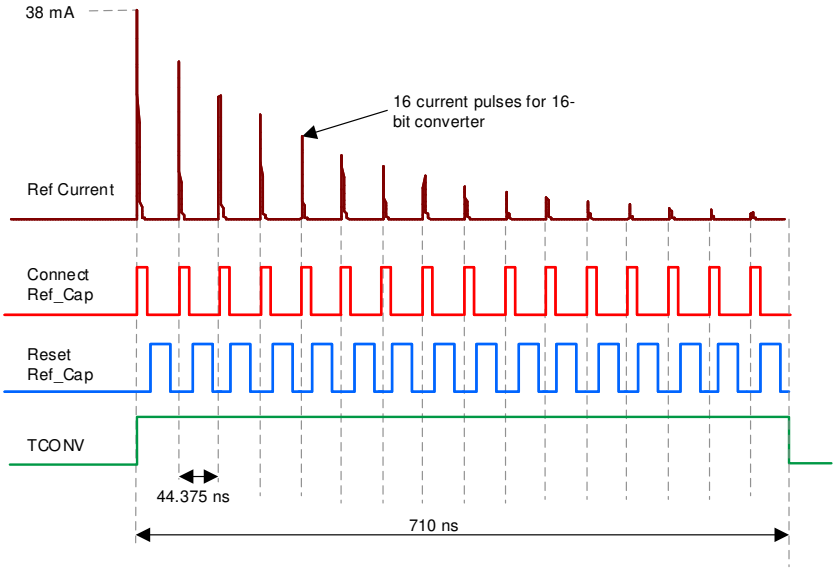

Figure 2-4. Reference Current Waveform for ADS8860

2.4 Bandwidth Modeling

The bandwidth of the input circuit depends mainly on the sample and hold circuit. The input resistor Rsh and input capacitor Csh can be used to calculate the bandwidth. Some SAR ADC data sheets show a specified bandwidth that is slightly different from the bandwidth set by the input Rsh × Csh filter, but typically this difference is very small and can be neglected. The bandwidth of the ADC is very important in noise simulations as proper bandwidth modeling allows calculation of total noise. Figure 2-5 illustrates how the internal bandwidth is set by the sample and hold circuit.

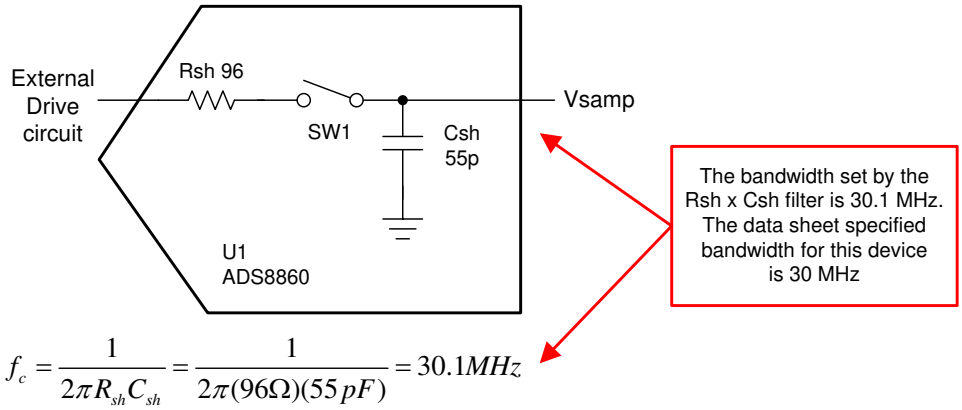

Figure 2-5. Bandwidth of ADC

2.5 Noise Modeling

The noise for the ADC is primarily from the switch resistance in the sample and hold circuit Rsh. However, there are secondary noise sources that are not accounted for by Rsh which can make a significant difference in the total noise simulation. To model noise as accurately as possible, noise is defined by a noise source and internal resistors are all noiseless. The noise signal source is adjustable via the external parameter list. Noise parameters are: NLF, FLW, and NVR. NLF is the noise in the flicker region. FLW is the frequency that the flicker noise is specified at. NVR is the noise in the broadband region. For most ADC models the flicker noise is not specified, so NLF and NVR are set to the same value and FLW is set to an arbitrary low value such as 0.01. NLF and NVR are given in nV/$\sqrt{\text{Hz}}$. For example, setting NLF = 10, NVR = 10, and FLW = 0.01 indicates that noise density is flat and is equal to 10 nV/$\sqrt{\text{Hz}}$. Figure 2-6 shows the noise model for the ADC.

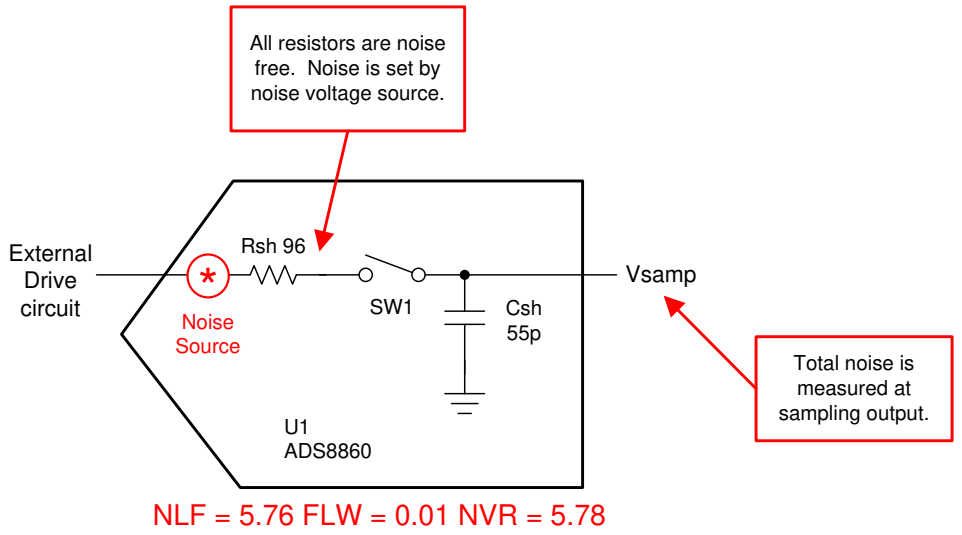

Figure 2-6. ADC Noise Model

Typically, the ADC data sheet specifies noise as a total RMS noise. This may be done directly as a transition noise, or indirectly in the SNR specification. To choose the correct value for the noise parameters, convert the total RMS noise into a noise density. Figure 2-7 shows that calculation. Note that the models in the TI library already have this parameter adjusted as needed. This procedure is only needed when a new model is being developed. Review Calculating ADC Noise Video for details on the calculations.

$$f_c = \frac{1}{2\pi R_{sh} C_{sh}} = \frac{1}{2\pi(96\ \Omega)(55\ pF)} = 30.1\ MHz$$

$$BW_n = 1.57 f_c = 1.57(30.1\ MHz) = 47.3\ MHz$$

$$Translating\ transition\ noise\ to\ a\ voltage\ for\ ADS8860$$

$$E_{n\_rms} = transition\_noise = 0.5\,LSB = 0.5\left(\frac{5\ V}{2^{16}}\right) = 38\ \mu V\text{rms}$$

$$e_n = \frac{E_{n\_rms}}{\sqrt{BW_n}} = \frac{38\ \mu V}{\sqrt{47.3\ MHz}} = 5.5\ nV/\sqrt{Hz}$$

$$NLF = 5.5,\ \text{NVR} = 5.5,\ \text{and FLW} = 0.01$$

Figure 2-7. Selecting the Noise Parameters

2.6 Reference Droop and Reference Noise Errors

Some of the noise applied to the reference input of a SAR ADC is in the digitized output signal. The reference noise detects the bandwidth restrictions from a filter formed by the reference capacitor CREF and input switch resistance RSH. The reference capacitor value is typically one-fourth the sample and hold capacitor. In this example CSH is 55 pF so the reference capacitor is 55 pF / 4 = 13.75 pF.

Reference noise is also impacted by the input signal level. For a 0-V input signal, no reference noise appears at the output and for a full-scale signal, all the reference noise appears at the output. Figure 2-8 illustrates the noise scaling inside the model.

Another aspect of the data converter voltage reference input is that droop in the ideal reference voltage causes a gain error on the ADC. For example, if the ideal reference voltage is 5 V and the actual reference droops to 4.99 V this introduces a 0.2% error in the measured output signal (100 × (4.99 V – 5 V) / 5 V = 0.2%). The reference circuit shown in Figure 2-8 also models this behavior. Note that the input called *Vref_ideal* is used to set the ideal reference value. This input floats to the VREF parameter if it is not connected. If a different Vref_ideal is desired, the pin can be driven as needed.

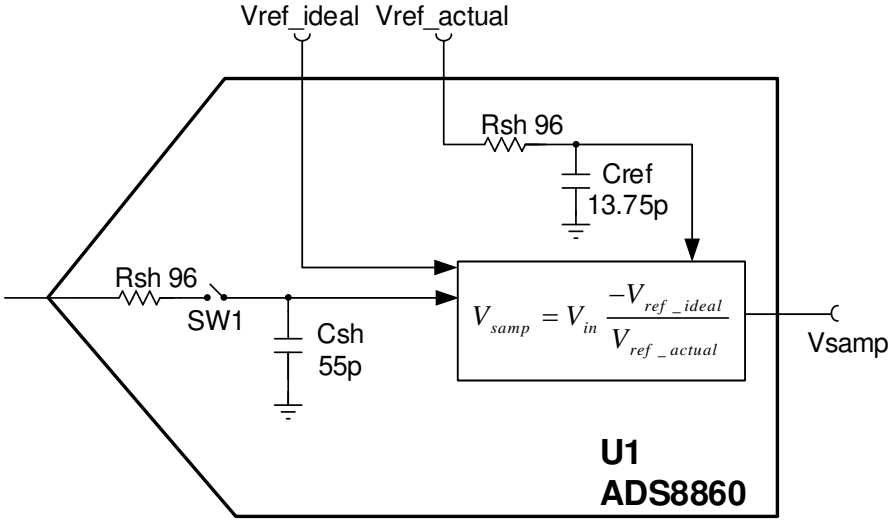

Figure 2-8. Reference Noise Scaling Model

2.7 Gain, Offset, and Input Leakage Modeling

The input voltage offset is modeled by placing a DC voltage source in series with the input. The leakage currents are modeled as DC current sources on each input. Gain error is modeled as a voltage-controlled voltage source with a gain that includes the error (GAIN = 1 + EG / 100). Figure 2-9 illustrates the gain, offset, and leakage modeling.

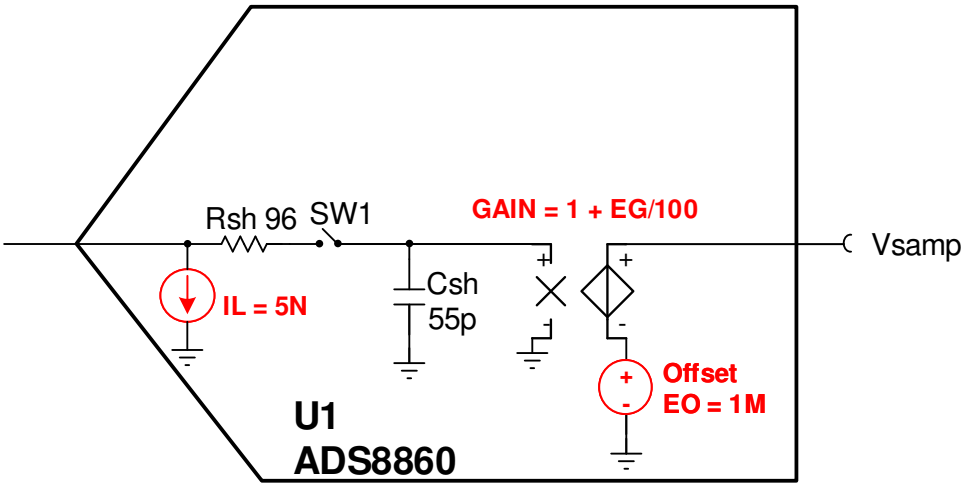

Figure 2-9. Reference Noise Scaling Model

2.8 Differential input behavior

The figures shown in this application note use a single-ended configuration for simplicity. The actual model implementation uses a differential configuration. The differential configuration simply mirrors many of the key elements such as sample and hold resistors and capacitors. The output of the differential input is converted to single ended using a voltage-controlled voltage source. Figure 2-10 illustrates the differential sample and hold configuration.

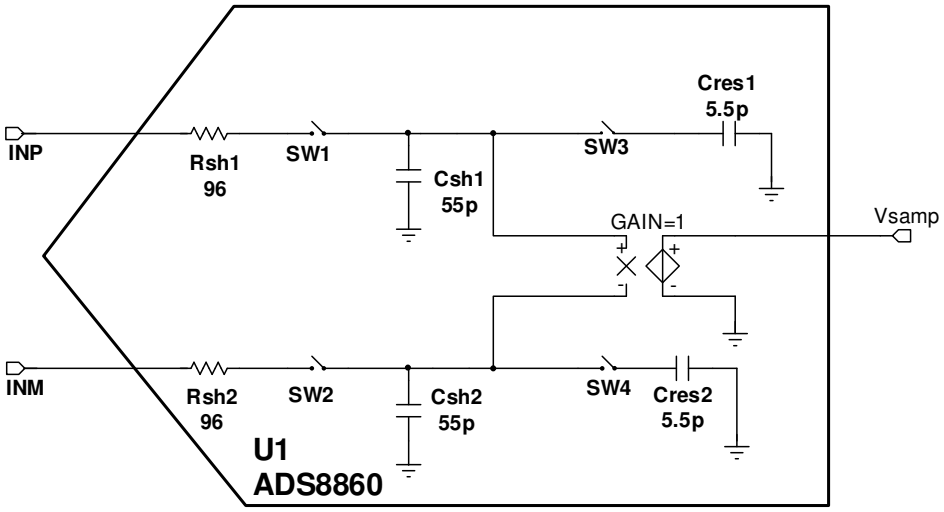

Figure 2-10. Differential Sample and Hold

2.9 ESD Protection Diodes and Parasitic Capacitance

The analog inputs on SAR ADCs are normally protected with ESD diodes. The ESD diodes have parasitic capacitance associated with them. Figure 2-11 illustrates the connection of the ESD diodes.

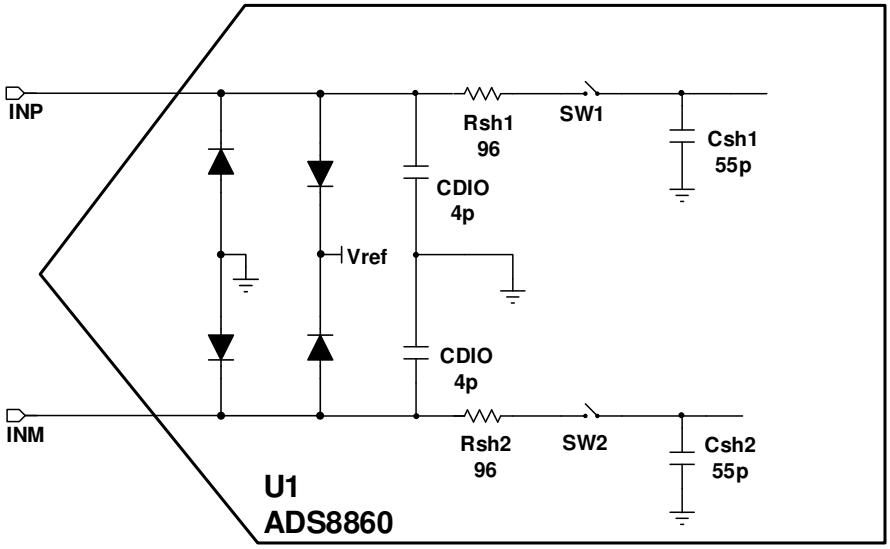

Figure 2-11. ESD Protection Diodes

2.10 Summary of Parameters

Table 2-1 lists a short summary for each parameter. For more details on the parameters and internal model schematics see the previous sections of this application report.

Table 2-1. Parameter Summary

Parameter	Definition
CSH	Sample and hold input capacitor. Typically, this internal capacitor is found in the ***Input Sampling Stage Equivalent Circuit*** section of the data sheet and also may be listed in the data sheet table. Typical values for this capacitor range from 5 pF to 100 pF.
RSH	Parasitic resistance of sample and hold switch. Typically, this internal resistor is found in the ***Input Sampling Stage Equivalent Circuit*** section of the data sheet and also may be listed in the data sheet table. Typical values for this resistor range from 10 Ω to 200 Ω.
CDIO	Parasitic capacitance of ESD diodes which is often in the ***Input Sampling Stage Equivalent Circuit*** section of the data sheet. This capacitance is typically 4 pF.
CRES	Sample and hold reset capacitance. This capacitor is used to reset the sample and hold capacitor at the end of the conversion phase and it emulates the droop seen at the end of the conversion phase. Typically, this is set to 10% of the sample and hold capacitor.
TCONV	Conversion phase time is the amount of time it takes for the internal conversion to complete. This parameter is found in the data sheet table. Always use the largest time for this parameter as this gives a worst case for the acquisition period.
VREF	The ideal value for the voltage reference. If the Vref_ideal pin is not connected, it will float to this value. This parameter is also the specified reference voltage at which the IREF average current is defined.
FSAMPL	The sampling rate at which the IREF average is defined.
N	The resolution of the device which is used to generate N current transient pulses on the reference during the conversion cycle.
IREF	The average value of the reference current. Typically, this value is in the hundreds of microamps, whereas the transient amplitude is in milliamps. This parameter works in conjunction with VREF, FSAMPL, and N to set the reference transients. For example, the ADS8860 is a 16-bit device with A 5-V reference that draws an average of 300 µA at 1 MHz. Its parameters are: IREF = 300U, N = 16, FSAMP = 1 Meg, and VREF = 5 V.
IREF_ON	IREF_ON turns on or off the voltage reference transients. IREF_ON = 1 turns on the transients, and IREF_OFF turns off the transients.
IL	The input leakage current of the ADC analog input pins. This parameter is found in the data sheet table. Typical values for this current range from 1 pA to 1 µA.
EG	The gain error specification as a percentage of full-scale range.
EO	The offset error specification in volts. Typical values range from microvolts to millivolts.
NLF	The flicker noise density in nV/$\sqrt{\text{Hz}}$ specified as frequency FLW. If the device does not have a specification for flicker noise, set this number equal to NVR and set FLW to a low value (0.01 Hz).
NVR	The broadband noise density nV/$\sqrt{\text{Hz}}$. Derive this value based on the SNR or transition noise of the device (see section Section 2.5).
FLW	The frequency that the flicker noise density (NLF) is defined at in Hertz.
CREF	The reference capacitance. This capacitance sets the cutoff of the filter that the reference noise is applied to. Typically, this value is set to 0.25 CSH.

2.11 Summary of Model Pins

Table 2-2 lists a short summary of the model pin. For more details on the pins and internal model schematics, see the previous sections of this application report.

Table 2-2. Model Pin Summary

Pin Name	Pin Function
INN	Negative analog input pin for the device.
INP	Positive analog input pin for the device
Vref	External reference input pin for the device. Connect the external Vref here.
SampleRate	This pin controls the sampling rate of the ADC. Connect a ±5-V square wave here. Set the frequency of that square wave to the sampling rate at which the device must operate. So, for a 1 Msps device, apply a 1-MHz, ±5-V square wave.
Vref_ideal	Connect this pin to the ideal value of the voltage reference. If left unconnected it floats to the value of the VREF parameter in the parameter list. So, for example, the ADS8860 has the VREF parameter set to 5 V. If using a nominal 5-V reference, do not connect this pin. This pin calculates the effects of reference droop and reference error in the output signals.
Vref_err	This is an output pin used to show the reference error. If this output is 0 V there is no error on the output. If the output is 1 mV, the reference has a 1-mV error.
Vsettling error	This is an output pin used to show the effects of sample and hold settling. This pin compares the steady state ideal input to the ADC to the sample and hold value captured for Vref. If Vsettling_error = 1 mV, than the settling error is 1 mV. Note settling is tested with a DC input signal. This output is not meaningful for AC inputs.
Vsamp	Shows the output of the sample and hold.
Tacq	This is an internal signal that shows when the ADC is acquiring (sampling).
TCONV	This is an internal signal that shows when the ADC is converting (holding).
ResetSH	This is an internal signal that illustrates when the internal sample and hold is reset.

3 Downloading and Using PSpice® Example Projects From Web

The SAR ADC SPICE macromodel was used to develop multiple PSpice® models and example circuits on the web. For example, the ADS8860 has the example projects for the model under Design and Development. Download the ZIP file containing the ADS8860 PSpice Model. Extract the zip file and click on ADS8860.OPJ to open the PSpice project. After the PSpice project loads, you can access the example circuits and simulation profiles. Figure 3-1 shows the example project and emphasizes where important elements reside.

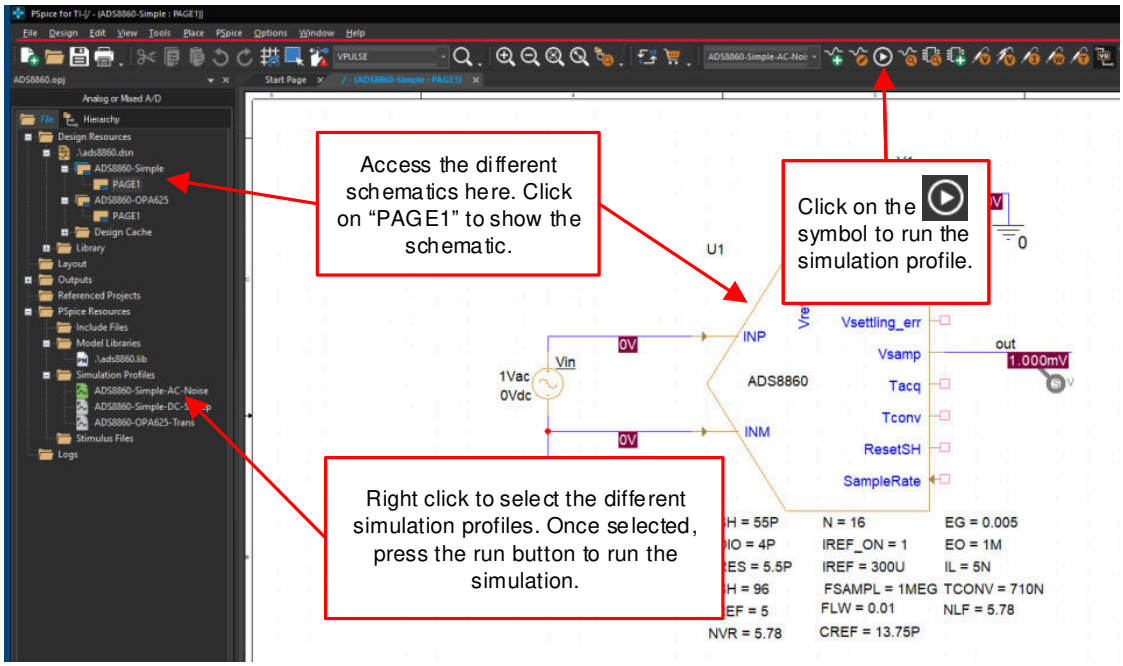

Figure 3-1. PSpice® Example Project

3.1 Selecting the Amplifier and Optimizing the RC Circuit

To get low distortion data acquisition, it is important to select an amplifier with sufficient bandwidth and an external RC circuit that settles quickly. A series of Precision Labs Videos covers this process in great detail. This document quickly summarizes the process. For more information on the subject, see SAR Drive Optimization Video Series.

The first step in designing the drive circuit is selecting the amplifier and choosing a range of values for the RC circuit. The Analog engineer's calculator is a software tool that contains many different utilities to solve common electrical engineering problems. Use the SAR ADC drive tool to determine the amplifier bandwidth and RC filter range for optimal settling on the ADC. Figure 3-2 shows an example using the ADS8860 SAR ADC. The resolution, sample and hold capacitor, full-scale range and acquisition time is entered into the calculator. The calculator output is the minimum amplifier gain bandwidth required, the filter capacitor, and a range of filter resistors. A parameter step operation is used next to find the optimal filter resistor. In this example the bandwidth of the amplifier must be greater than 17.8 MHz, the filter capacitor Cfilt is 1.1 nF, and the filter resistor range is from 8.1 Ω to 65 Ω. There are many amplifiers with a bandwidth exceeding 17.8 MHz. For this example, use the OPA322 which has a bandwidth of 20 MHz. Choosing the amplifier for your application involves looking at all the DC and AC error sources such as offset, bias current, and noise. These tradeoffs are covered in greater detail in the Amplifier Precision Labs video series.

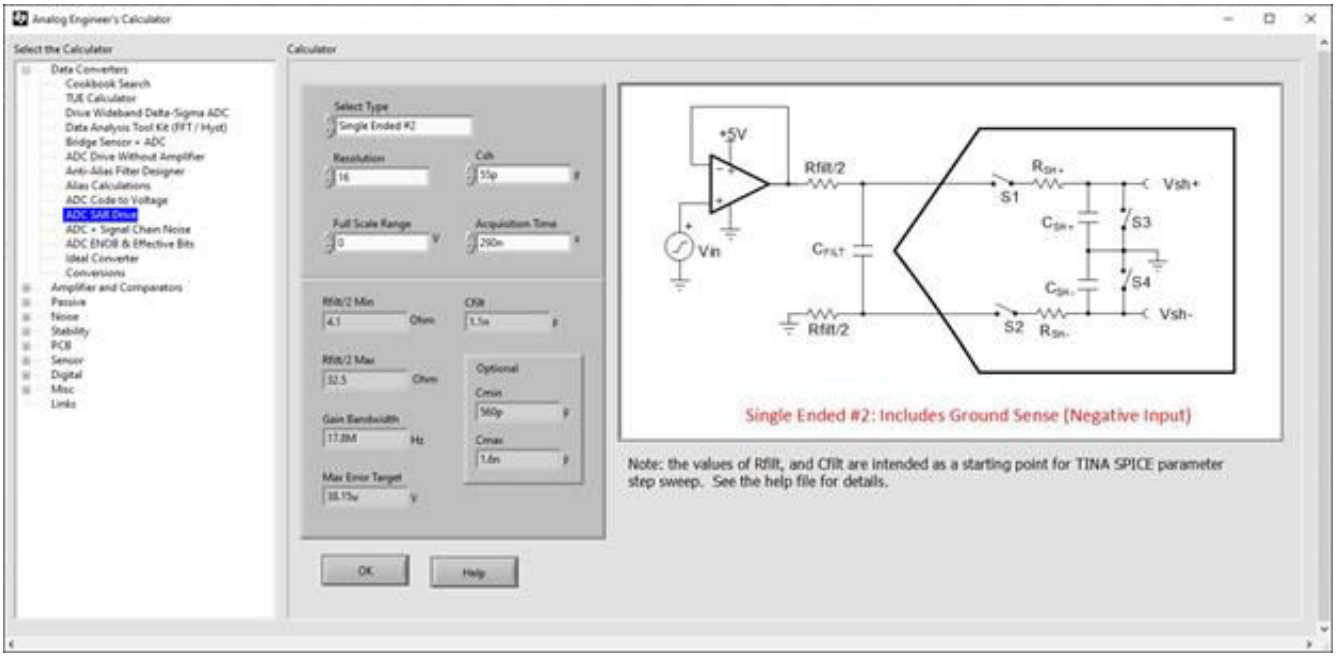

Figure 3-2. Analog Engineer's Calculator

Next, the filter resistors need to be *Parameter Stepped* to find the optimal value. There are a number of steps required to do parameter stepping in PSpice. First, place a PARAMETER element. Do this by selecting Place>PSpice Component...>Search from the PSpice menu. Search for PARAM in the search window and place it (See Figure 3-3). Place the PARAMETER element on the schematic near the element you are controlling.

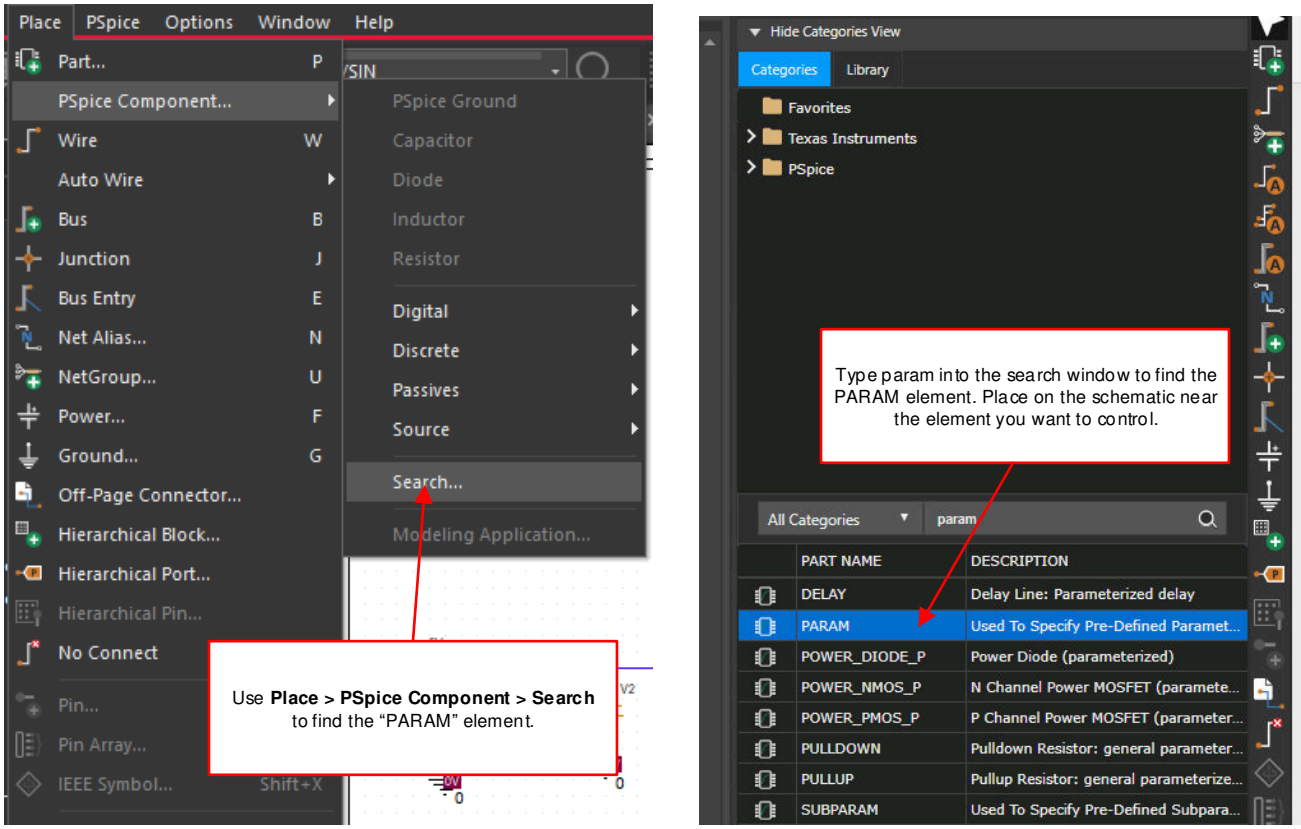

Figure 3-3. Find and Place the PARAMETER Element

Next, click on the PARAMETER element you just placed to edit it. Press the *New Property* button. Enter the name for the element you want to control. For example, R_Val to control a resistor. Choose a good value for this element such as 10 for 10 Ω (see Figure 3-4).

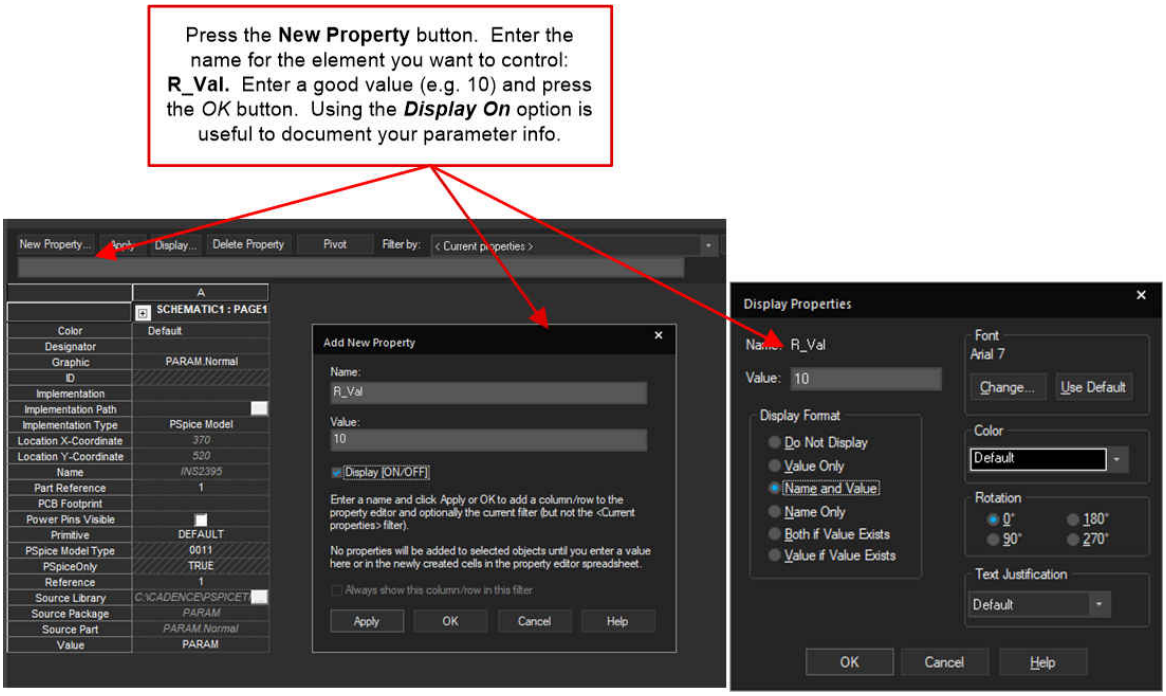

Figure 3-4. Add Property to PARAMETER Element

Next, click on the component you want to edit and change the value to match the value entered in the PARAMETER element. Use braces around the value: {R_Val}. Note that in this example both R4 and R5 are controlled with the same value (see Figure 3-5).

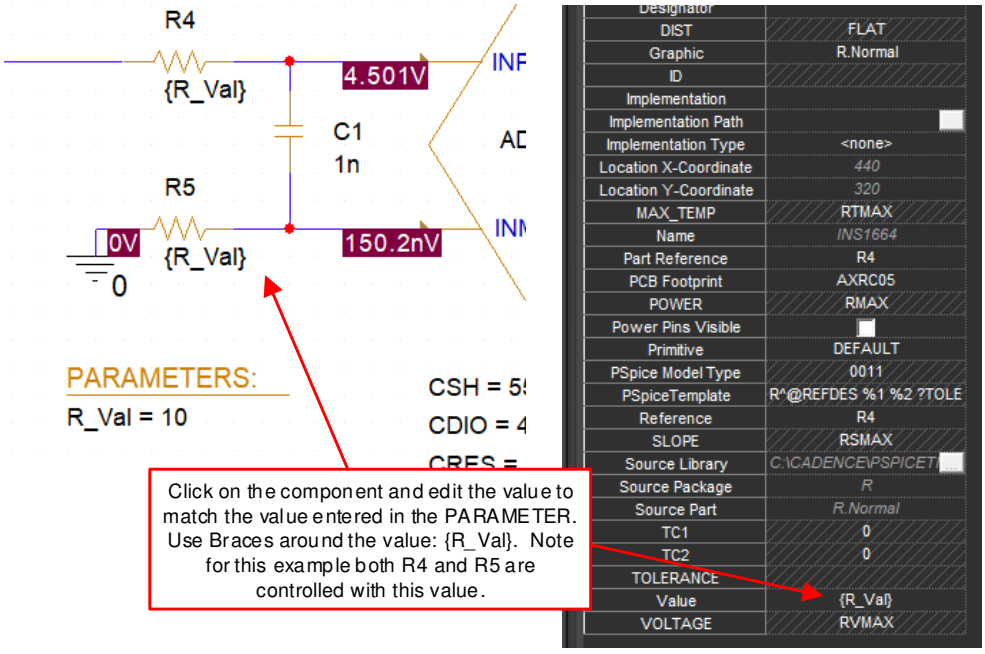

Figure 3-5. Edit the Component Value for Parameter Stepping

The last step before simulating is to set up the simulation profile. In this case the general settings are set for transient analysis, and the parametric step is set to adjust the filter resistor from 5 Ω to 30 Ω in steps of 5 Ω (see Figure 3-6).

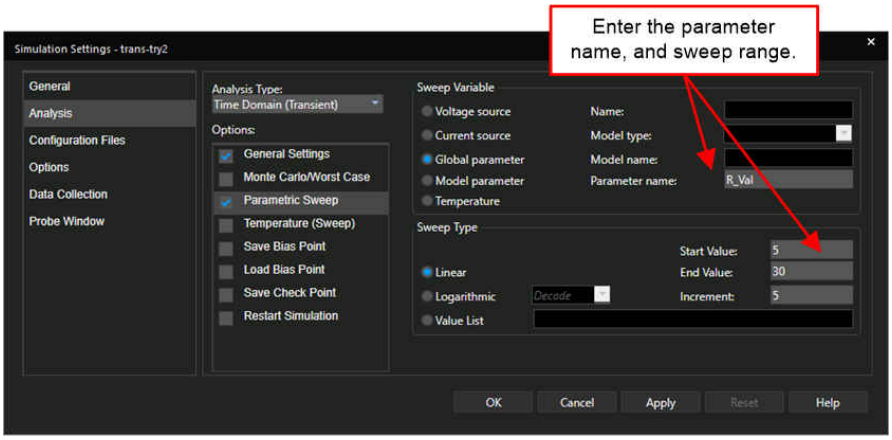

Figure 3-6. Simulation Profile for Parameter Stepping

Figure 3-7 shows the settling results. Notice that multiple output curves are present for each measurement. The different curves are all measured with different filter resistor values ranging from 5 Ω to 30 Ω as was selected in the simulation profile. Notice that the settling output response ranges from large overshoot (underdamped) to slow rise time (overdamped). The ideal settling happens with the fastest rise time that does not overshoot (critically damped). Note that for transient simulations, the offset voltage, leakage current, gain, and noise errors are disconnected. Thus, ideally the final settling error is 0 V as the DC error sources are not used in the transient simulation.

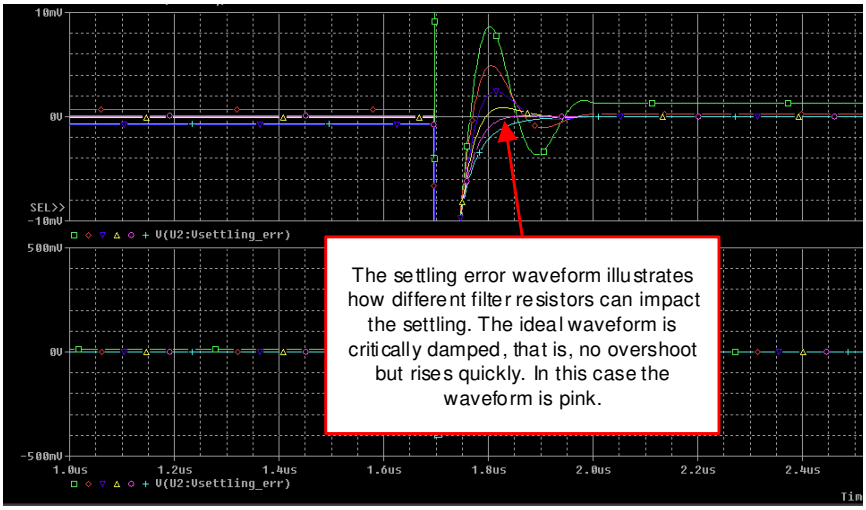

Figure 3-7. Simulation Results for Parameter Stepping

Figure 3-8 illustrates how you can determine the parameter value that corresponds to the optimal curve. Select the curve, right click, and choose ***Trace Information***. For this example simulation, the optimal settling happened with a 25-Ω filter resistor. It may be useful to first run the parameter step with course limits and then re-run with refined limits for better accuracy.

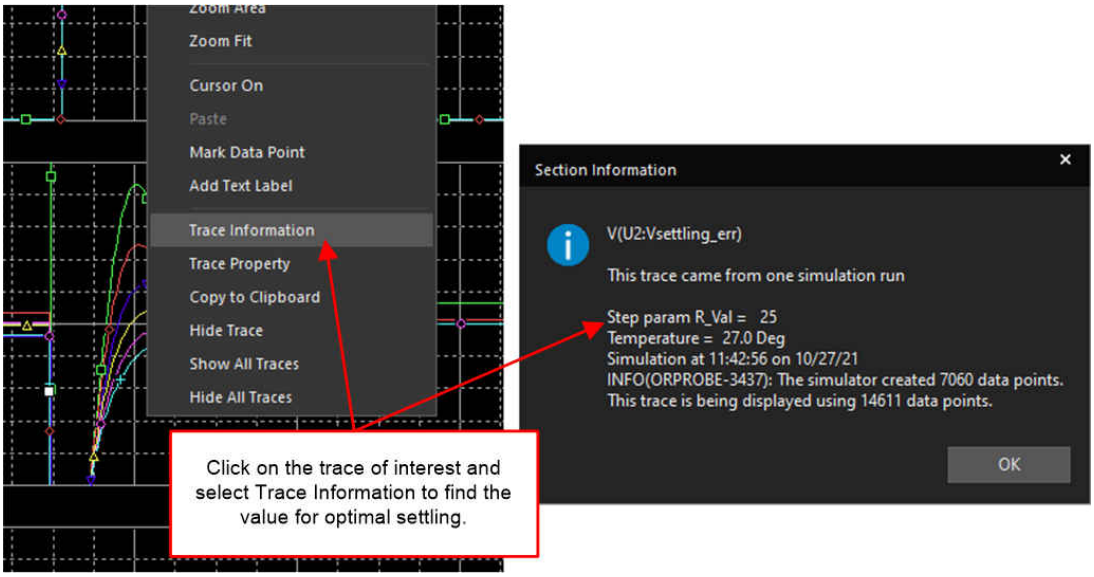

Figure 3-8. Trace Information for Parameter Stepping

3.2 Worst-Case Settling by Adjusting the Reset Capacitor

As mentioned in Section 2.2, the internal sample and hold is reset at the end of the sample and hold period using the reset capacitor Cres. This capacitor is typically set to 10% of the sample and hold value so that the voltage droop at the end of the conversion (hold) period is approximately 10% of the hold value. For example, if Csh is 55 pF, than Cres is typically set to 5.5 pF. In this case if the held voltage is 5 V it will be reset to 4.5 V at the end conversion period. This circuit models the real-world behavior of many modern SAR ADCs. For some legacy devices the held signal is fully reset to zero at the end of the conversion period. Also, it may be useful to fully reset this capacitor as a worst-case to emulate the behavior of an input signal step. To achieve this full reset to 0 V, simply adjust Cres to a value that is larger compared to the sample and hold capacitor. For example, replacing the Cres with 55 nF makes Cres a thousand times greater than Csh (1000 × 55 pF = 55 nF). Figure 3-9 compares the output settling with Cres = 5.5 pF and 55 nF.

Figure 3-9. Output Settling With Cres = 5.5 pF and 55 nF

3.3 Verification of Reference Droop

Real-world voltage references have a finite output impedance and bandwidth. These limitations can cause the output voltage of the voltage reference to droop when it is loaded by the transient currents from the ADC reference input pin. Figure 3-10 shows a typical circuit where the impact of the voltage reference limitations can be monitored. The best way to judge the reference settling error is to look at the Vref_err pin. This pin compares the steady state reference input to the transient reference input. The Vsettling_err pin also shows effects of reference droop as it is the total settling error from the sample and hold and reference.

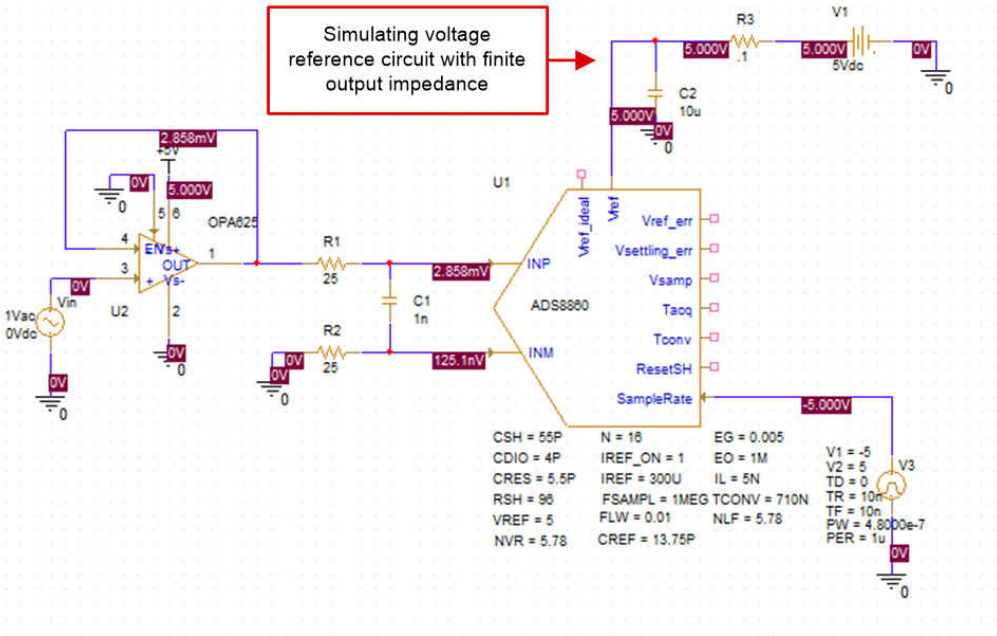

Figure 3-10. Monitoring Voltage Reference Settling

Figure 3-11 shows the transient simulation results for the voltage reference input on ADS8860. Notice the reference input has transient behavior related to the current transients.

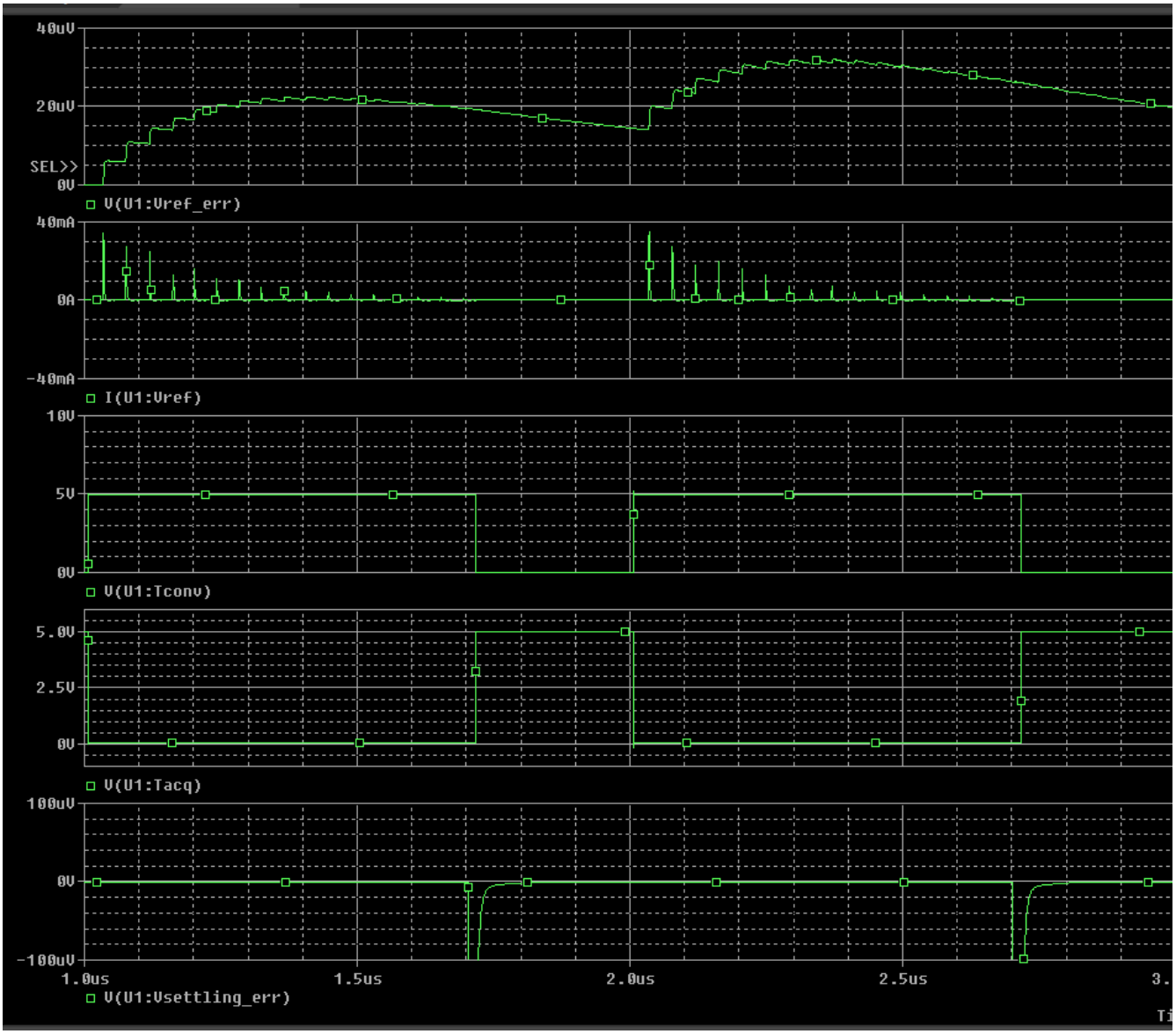

Figure 3-11. Reference Transient Simulation

3.4 System Noise Verification

The noise and bandwidth simulations are very useful to determine the overall error of a system due to noise. This simulation includes the noise of the ADC as well as noise from all external components. The noise modeling does not have any impact on the transient simulation and is only measured during an AC-Noise simulation. The total noise for the system is always measured at the Vsamp output on the ADC. Also, this output must be given a *Net Alias* as the simulation profile uses this to reference the output node. Figure 3-12 shows the simulation profile for the Noise AC-Noise analysis. Figure 3-13 shows the simulation results.

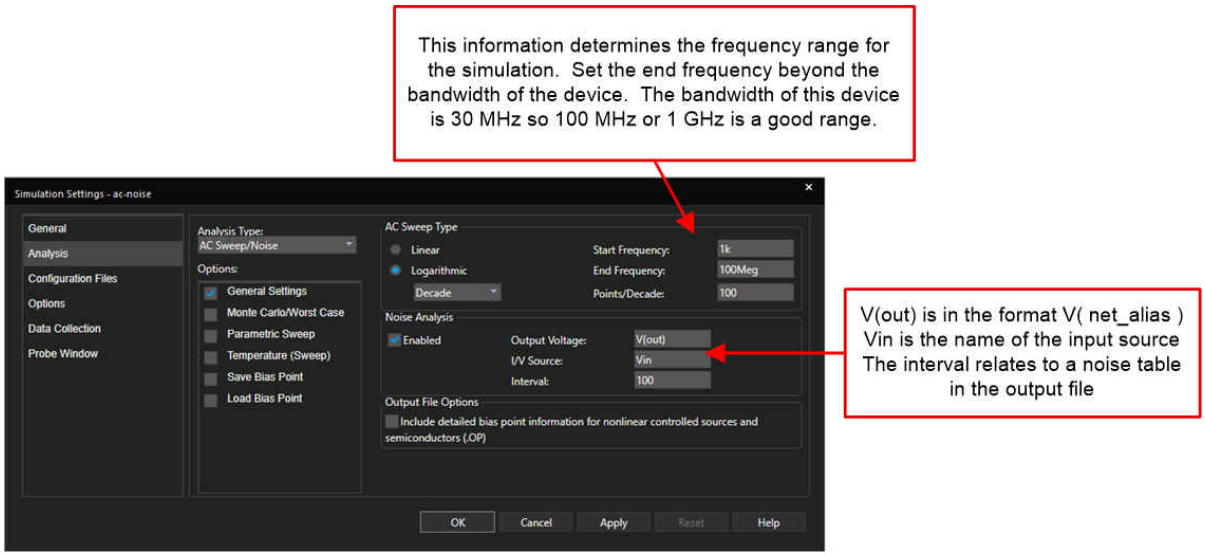

Figure 3-12. Noise Simulation Profile

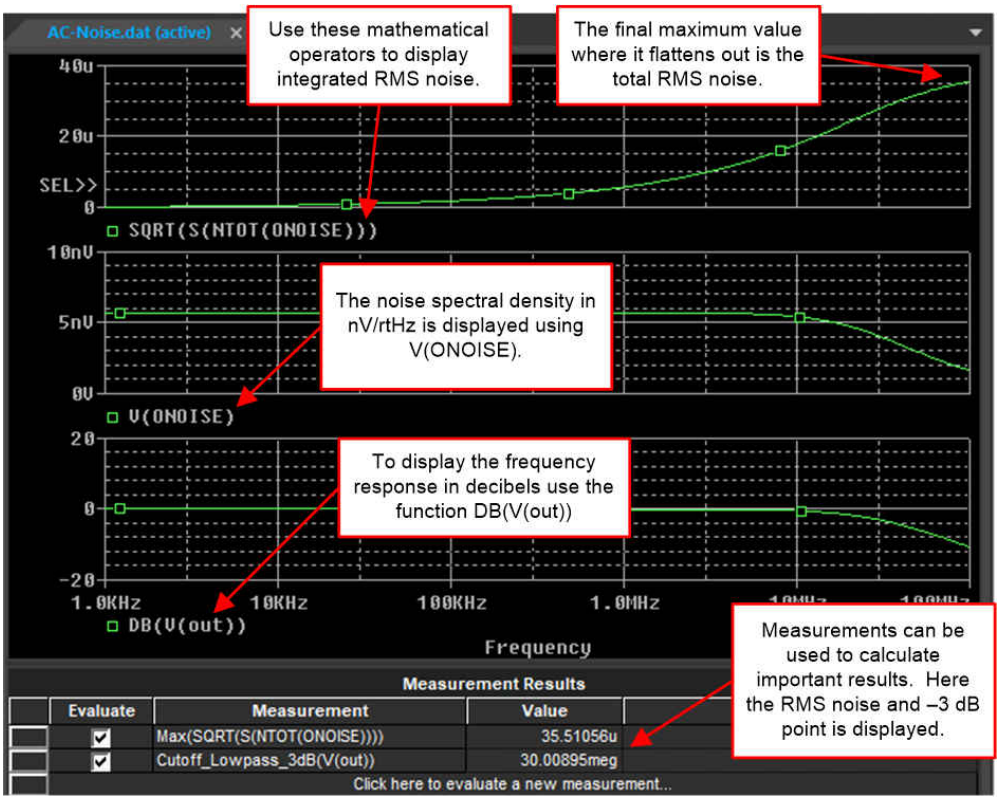

Figure 3-13. Noise Simulation Results

3.5 Gain, Offset, and Input Leakage Verification

The best way to see the impact of gain error, offset error, and input leakage current is with a DC sweep simulation. The DC sweep generates an input vs output voltage plot. The simulation profile is simple and only requires the input source and range to be specified (see Figure 3-14). Figure 3-15 shows the gain error plot and the output transfer function.

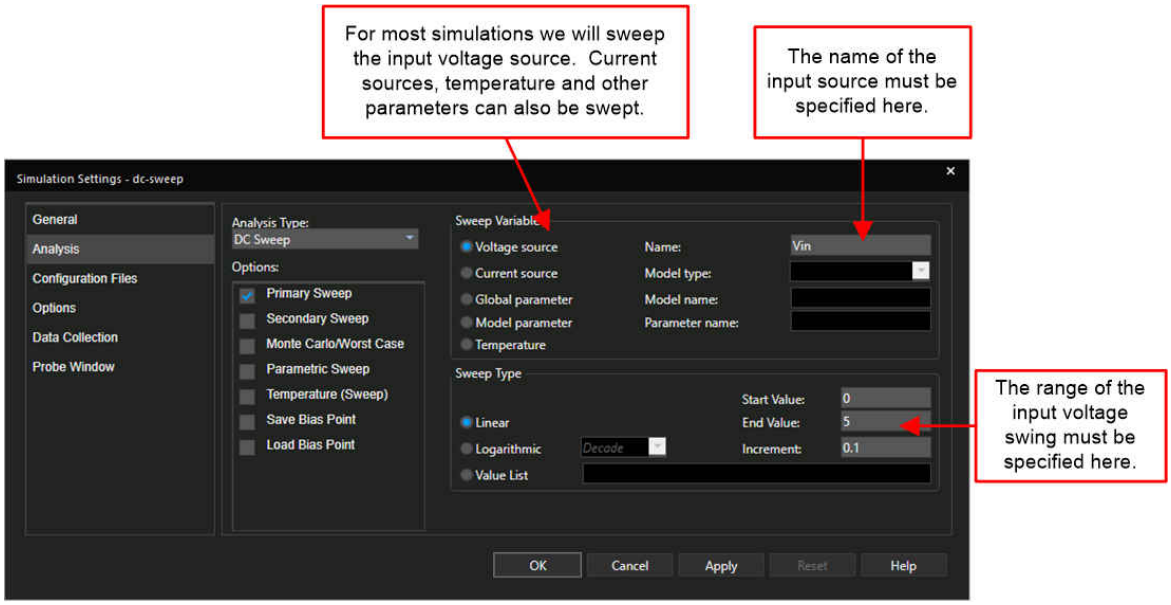

Figure 3-14. DC Sweep Simulation Profile

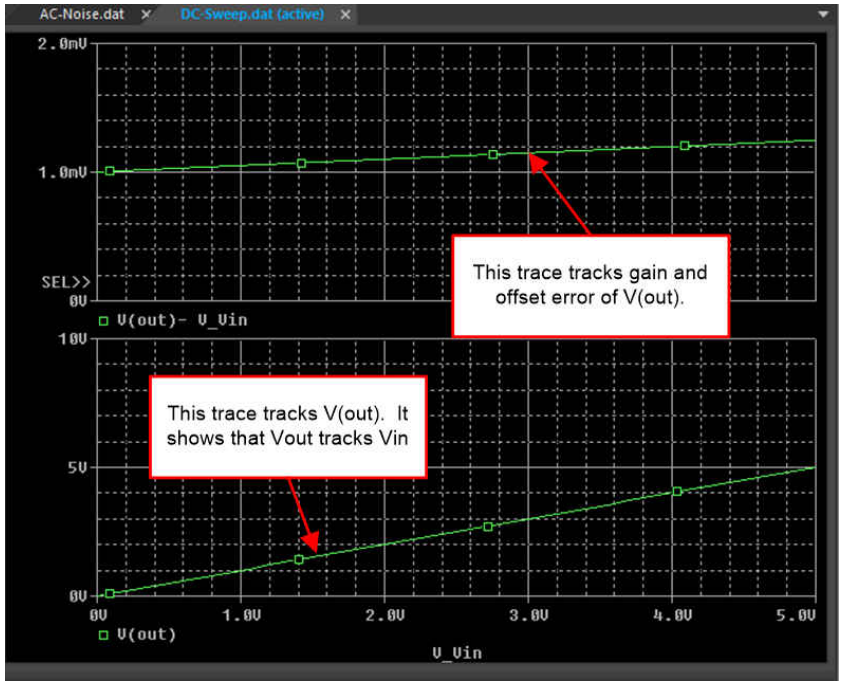

Figure 3-15. DC Sweep Results

4 Summary

This document gives an overview of the features and operation of the SAR ADC model. The model covers the analog and transient behavior of many SAR ADCs. The model allows the use of PSpice parameters to adjust its behavior. Texas Instruments includes models with the parameters prepopulated for popular ADC devices. The models are found in the PSpice for TI library and on TI.com.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265