Application Brief

Space-Grade, 100-krad, Programmable Voltage Source Circuit With Remote Sense FB

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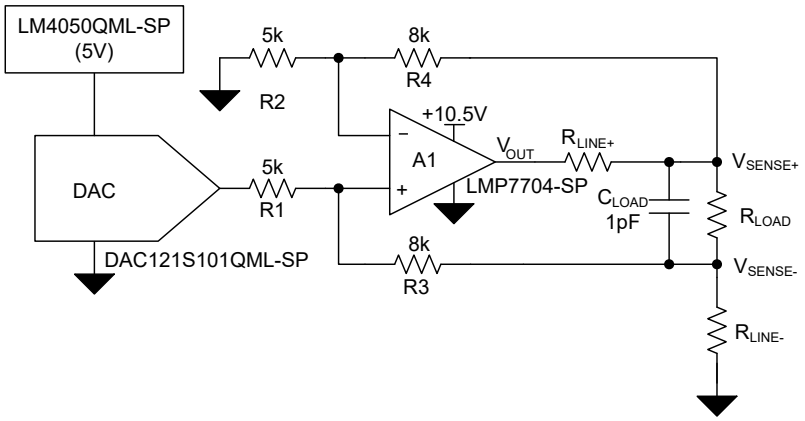
Design Goals

Parameter	Output
DAC Output Voltage	0V–5V
Output Voltage V_{LOAD}	0V–8V
Minimum Load Resistance R_{LOAD}	800Ω
Maximum Line Resistance Compensation	+28% of R_{LOAD}
Total Ionizing Dose (TID)	100 krad(Si)
Single-Event Latch-up (SEL) Immunity	85 MeV·cm^2/mg

Design Description

The programmable voltage output with sense connections circuit provides a precise voltage across a load, compensating for parasitic series resistance. The amplifier A1 uses feedback from the high-side and low-side of the attached load to accurately regulate the voltage between V_{SENSE+} and $V_{SENSE–}$. The digital-to-analog converter (DAC) output and discrete resistors set the voltage across the load. This circuit is used in applications where additional line resistance may be present and must be compensated for by increasing the output voltage to deliver the correct voltage to the load.



Design Notes

1. The LMP7704-SP supply voltage of 10.5V was selected according the derating specifications provided by the National Aeronautics and Space Administration (NASA) in document EEE-INST-002 (April 2008) and the European Cooperation for Space Standardization (ECSS) in document ECSS-Q-ST-30-11C Rev.1 (4 October 2011). The documents specify an 80% and 90% derating of the absolute maximum supply voltage for linear ICs, respectively.
2. Select a DAC with low total unadjusted error (TUE) and with the required resolution for the application. Use a DAC like the DAC121S10QML-SP device (which uses the supply as a reference) to minimize components and solution size.
3. Choose a high-voltage amplifier, with rail-to-rail output to ensure sufficient output swing to drive the load and line resistance. The amplifier should have low offset voltage and offset voltage drift so it does not significantly contribute to output error.
4. Resistor mismatch directly contributes to gain error at the output. Use resistors with 0.05% tolerance or better and low thermal drift.
5. For correct compensation of additional line resistance, the ratio of R2:R4 must match the ratio of R3:R1 as closely as possible.
6. The amplifier supply voltage is chosen based on the required output voltage, additional line resistance, and amplifier output swing at maximum load current.
7. To reduce error at zero-scale, supply a negative voltage to the amplifier.

Design Steps

1. The transfer function for V_{OUT} based on DAC voltage and resistor values is:

$$V_{LOAD} = \frac{R3}{R1} \times V_{DAC}; \frac{R3}{R1} = \frac{R4}{R2}$$

2. An 8-kΩ resistance is chosen for R3. R1 is then calculated:

$$R1 = \frac{V_{DAC,FS}}{V_{LOAD,FS}} \times R3 = \frac{5V}{8V} \times 8k\Omega = 5k\Omega$$

3. R4 and R2 are chosen equal to R3 and R1, respectively.
4. Calculate the maximum load current based on the minimum load resistance and full scale V_{LOAD}. The maximum load current impacts the amplifier output voltage swing and the additional line resistance the circuit can compensate.

$$I_{LOAD,max} = \frac{V_{LOAD,FS}}{R_{LOAD,FS}} \times R3 = \frac{8V}{800\Omega} = 10mA$$

The required V_{CC} voltage is calculated to drive 28% additional load resistance and still maintain voltage regulation across R_{LOAD}. $V_{O,rail}$ is the approximate amplifier output swing from V+ at a 10-mA load current.

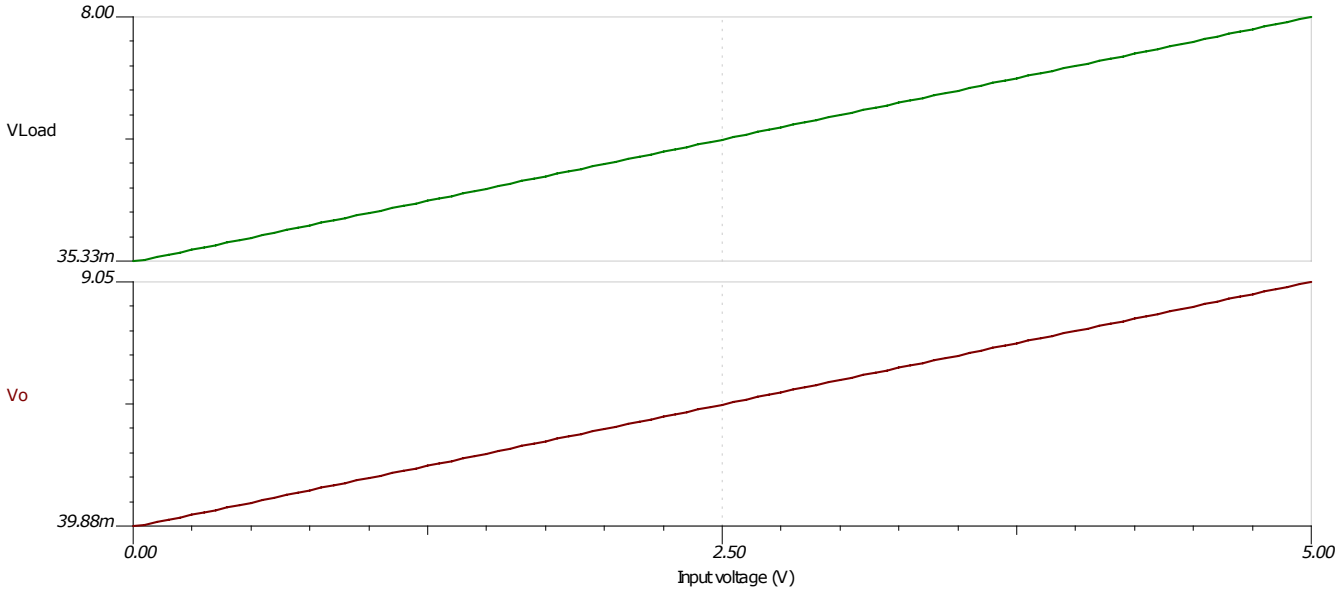
$$V_{CC,min} = C_{O,rail} + 0.28 \times R_{LOAD,min} \times I_{LOAD,max} + V_{LOAD,FS} = 200mV + 0.28 \times 800\Omega \times 10mA + 8V = 10.44V$$

Derating the LMP7704-SP maximum supply by 80% gives a 10.5-V maximum supply.

Design Simulations

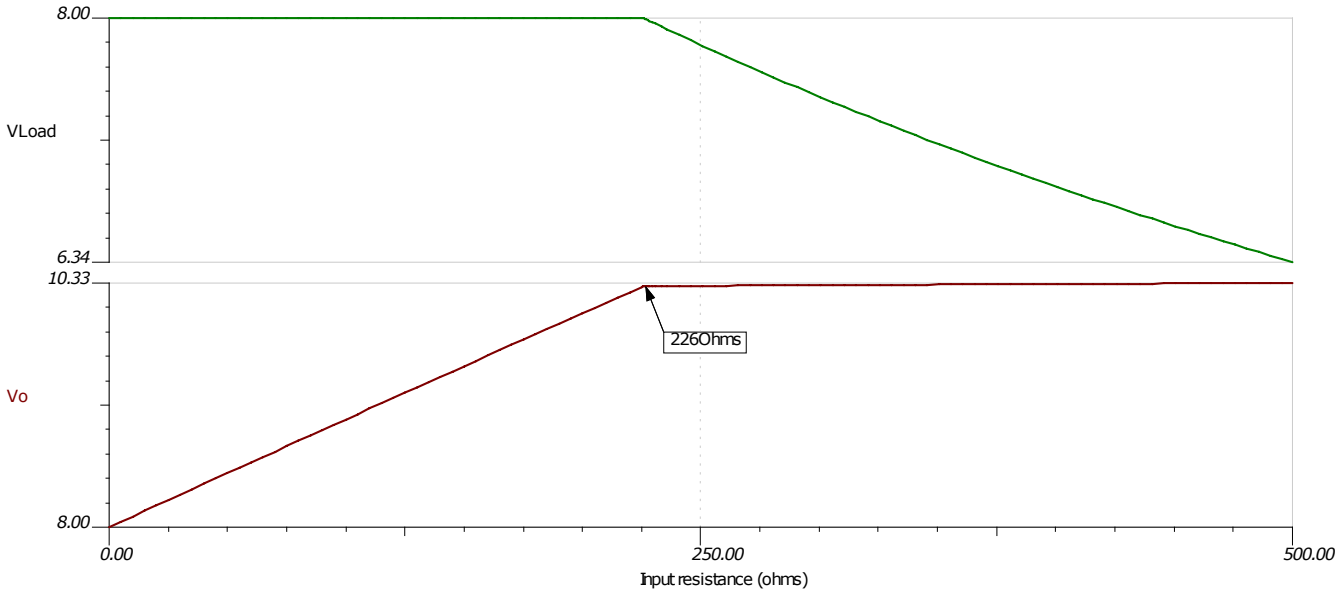
DC Transfer Characteristic

The following simulation shows the output transfer function of the circuit with 100Ω of additional line resistance.



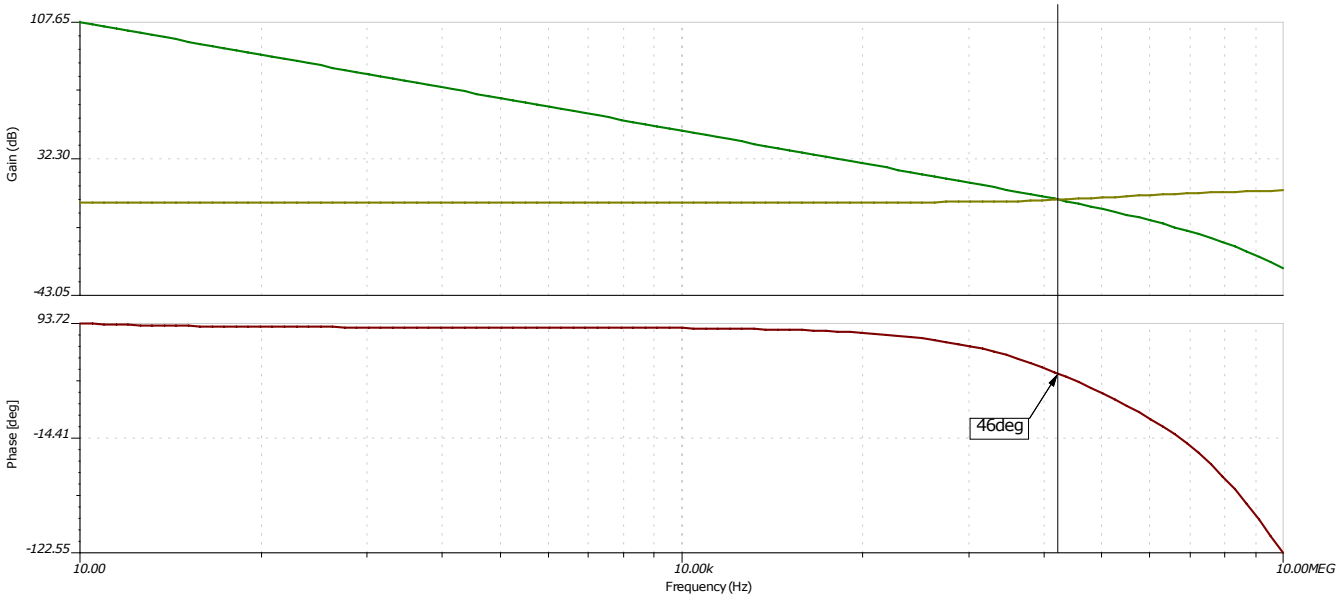
Maximum Additional Line Resistance

This simulation shows the maximum load voltage of 8V being regulated with up to 226Ω of extra line resistance.



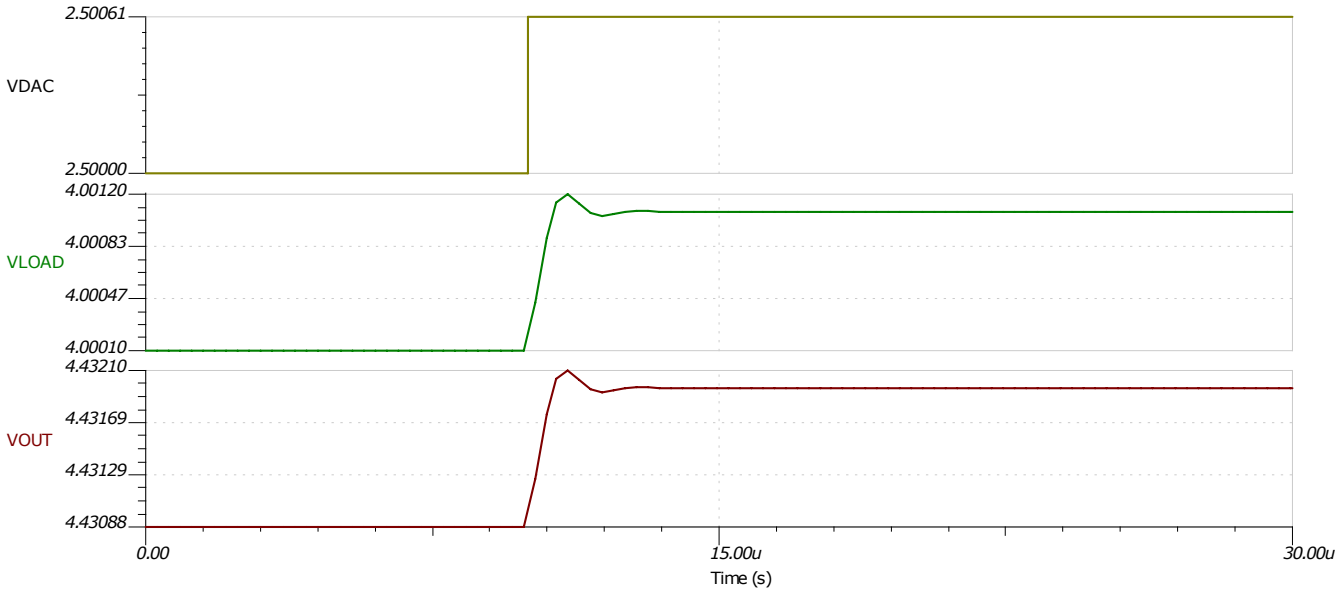
Stability

The following figure displays a stability simulation of the circuit with a 1-pF load on the output. The phase margin is 46°.



Small-Step Response

The following figure displays an LSB step response of the circuit with 1-pF load on the output.



Design References

Programmable voltage output with sense connections circuit

Additional Resources:

- Learn more about using precision DACs at our Precision DAC Learning Center.
- Learn about TI's precision DAC portfolio and find more technical content.

For direct support from TI Engineers use the E2E community: e2e.ti.com.

Design Featured Devices

Device	Key Features	Link
DAC121S101QML-SP	Radiation-hardened, 12-bit micro power digital-to-analog converter with rail-to-rail output	https://www.ti.com/product/DAC121S101QML-SP
LMP7704-SP	Low-power, high-precision, low-noise, rail-to-rail output, operational amplifier	https://www.ti.com/product/LMP7704-SP
LM4050QML-SP	Radiation-hardness-assured (RHA) 2.5-V or 5-V shunt voltage reference	https://www.ti.com/product/LM4050QML-SP

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