Analog Engineer's Circuit

Circuit for detecting input floating on ADS8681 ADC

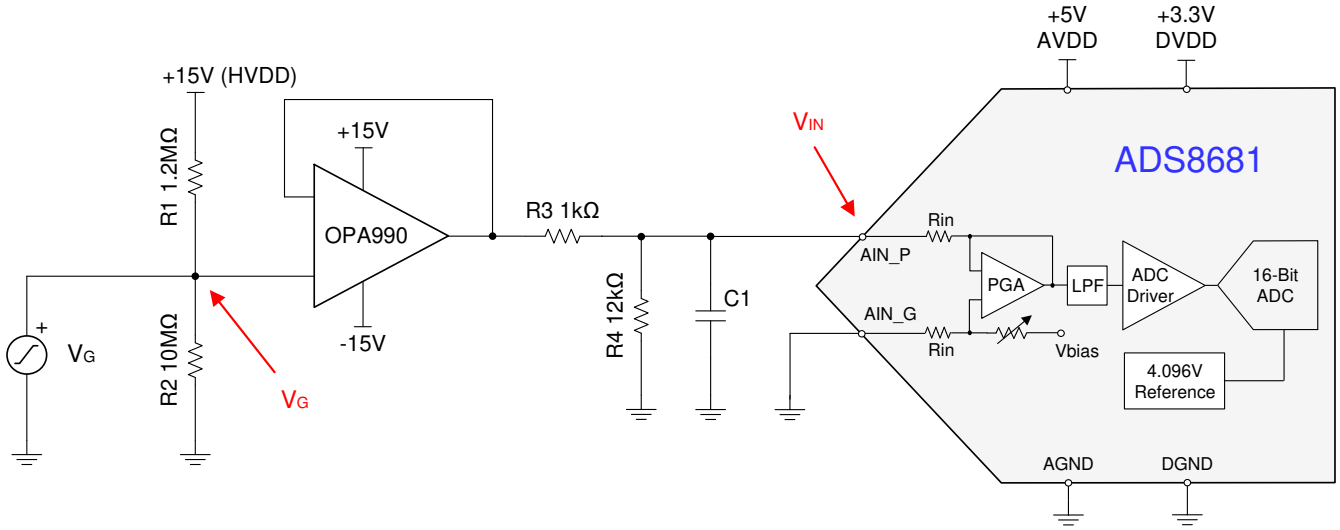
Data Converters *Dale Li*

Normal Bipolar Input Signal Range		Bipolar Input Range on ADS8681		Supply and Voltage Reference		
V_{G_Min}	V_{G_Max}	V_{ADC_Min}	V_{ADC_Max}	AVDD	DVDD	V_{REF}
–12.88V	+12.88V	–12.88V	+12.88V	+5V	+3.3V	4.096V

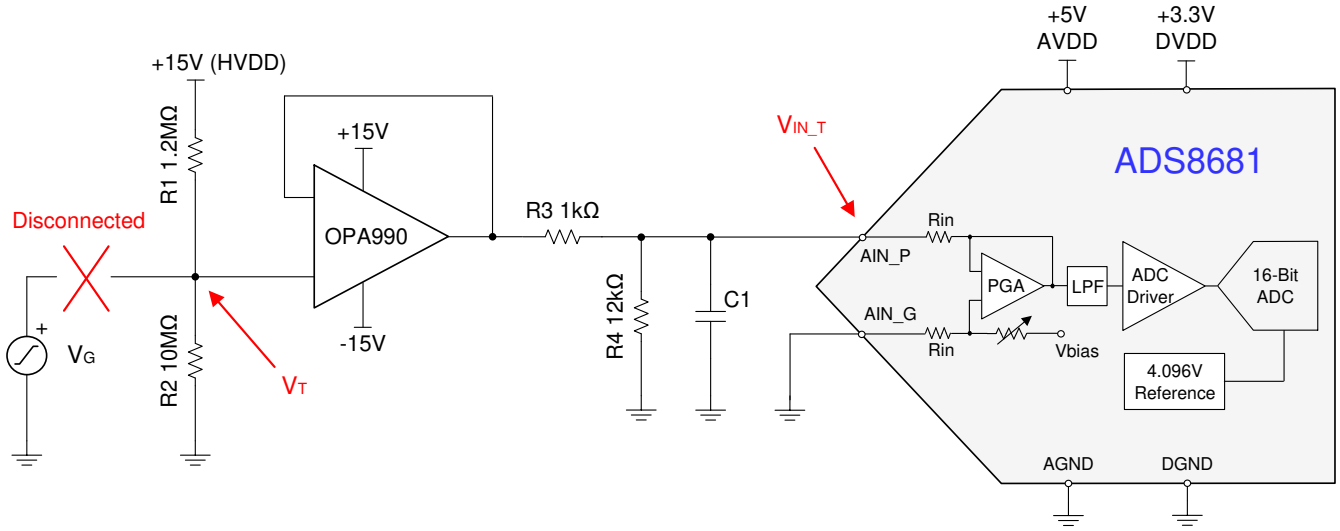
Design Description

This circuit shows a solution to detect if the ADS8681 successive approximation register (SAR) analog-to-digital converter (ADC) input is floating. The ADS8681 device features a significant amount of signal chain integration, including high resistive input impedance, a programmable gain amplifier (PGA), and an ADC input driver. These features eliminate the requirement for driving the ADC inputs with a high-bandwidth amplifier. Therefore, a low-bandwidth, low-cost amplifier in a non-inverting unity gain configuration can be used in a solution for detecting a floating input. This solution has a minimal impact on the system performance metrics including signal-to-noise ratio (SNR) and total harmonic distortion (THD). This circuit is useful in end equipment such as: Analog input module, Servo drive functional safety module, Motor drives, and Factory automation and control.

Normal Operation:



Input Floating:



Specifications

Specification	Goal	Calculated and Simulated Value
Noise	< 10μV	Calculated: 4.3μV Simulated: 4.38μV
Phase Margin	> 45°	64°

Design Notes

1. The resistors (R1 and R2) divide the power supply (HVDD) to create a biasing voltage, V_T, that is outside of the expected input voltage range which is used to detect whether the V_G input is floating.
2. The amplifier (OPA990) is configured as a non-inverting unity gain buffer to offer a high input impedance for the signal source (V_G).
3. The resistors (R3 and R4) are used to scale down the input signal for a margin to detect if the input is floating.
4. Select 0.1% or better accuracy resistors for R3 and R4 to minimize the gain error.
5. Select C0G type capacitor for C1 in the front-end RC filter to minimize the distortion.

Component Selection

1. The normal input signal range (V_G) is ±12.88V. V_G is scaled down by the resistor divider (R3 and R4) to provide margin above the normal input voltage range for the floating input detection voltage. The following table lists the input range on the ADS8681 in this design, the input voltage range (V_G), and the expected normal voltage (V_{IN}) on the ADC input for 1-V margin.

	Input Signal Voltage (V_G)	ADS8681 Input Range (V_{ADC})	Expected Normal Voltage on ADC Input (V_{IN})	Expected Voltage on ADC Input for Float (V_{IN_T})
Maximum	+12.88V	+12.88V	+11.88V	+12.38V
Minimum	–12.88V	–12.88V	–11.88V	+12.38V

R3 is selected as 1kΩ for a small gain and offset error. Therefore, R4 is determined by the following equation:

$$V_{IN} = \frac{R_4}{R_3 + R_4} \times V_G$$

$$R_4 = \frac{V_{IN}}{V_G + V_{IN}} \times R_3 = \frac{11.88V}{12.88V - 11.88V} \times 1k\Omega = 11.88k\Omega$$

A 12-kΩ and 0.1% tolerance resistor is finally selected for R4. The resistor value can be adjusted according to the noise and margin required in the system.

2. The objective of this step is to select the ADC input voltage under which a float is detected (called V_{IN_T}). This voltage is selected to be 0.5V higher than the highest normal operating input voltage (+11.88V) for margin to prevent a false detection of a float condition. Therefore, the V_{IN_T} can be calculated from the equation:

$$V_{IN\_T} = V_{IN} + 0.5V = 11.88V + 0.5V = 12.38V$$

3. The objective of this step is to select a voltage divider on the input of the amplifier (OPA990) that will set the float voltage at the input of the ADC as selected in step 2. V_{IN_T} is the divided input down threshold voltage (V_T) during a floating input condition. Use the following equations to calculate the required VT voltage to achieve the desired V_{IN_T}:

$$V_{IN\_T} = \frac{R_4}{R_3 + R_4} \times V_T$$

$$V_T = \frac{R_3 + R_4}{R_4} \times V_{IN\_T} = \frac{1k\Omega + 12k\Omega}{12k\Omega} \times 12.38V = 13.4V$$

R1 and R2 are selected to create the VT voltage during floating inputs. To achieve higher input impedance, R2 is selected as 10MΩ. R1 is determined by the following equation:

$$V_T = \frac{R_2}{R_1 + R_2} \times HVDD$$

$$R_1 = \frac{HVDD - V_T}{V_T} \times R_2 = \frac{15V - 13.4V}{13.4V} \times 10M\Omega = 1.194M\Omega$$

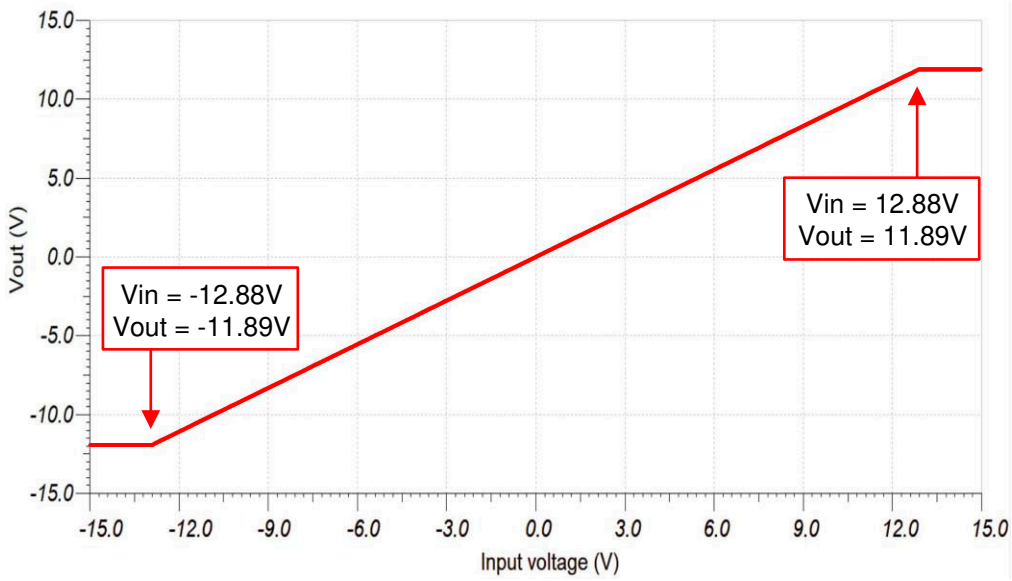
R1 is selected as 1.2MΩ which is a standard resistor value. Note that the tolerance on these resistors only impacts the float voltage accuracy.

4. The capacitor C1 in parallel with R3||R4 is used to filter the noise from the front-end circuit. The equation for the cutoff frequency based on the input resistors and capacitors follows. The exact value may not be critical so we use a standard value of 10nF in this design.

$$f_C = \frac{R_3 + R_4}{2\pi \times R_3 \times R_4 \times C_1} = \frac{1k\Omega + 12k\Omega}{2\pi \times 1k\Omega \times 12k\Omega \times 10nF} = 17.2kHz$$

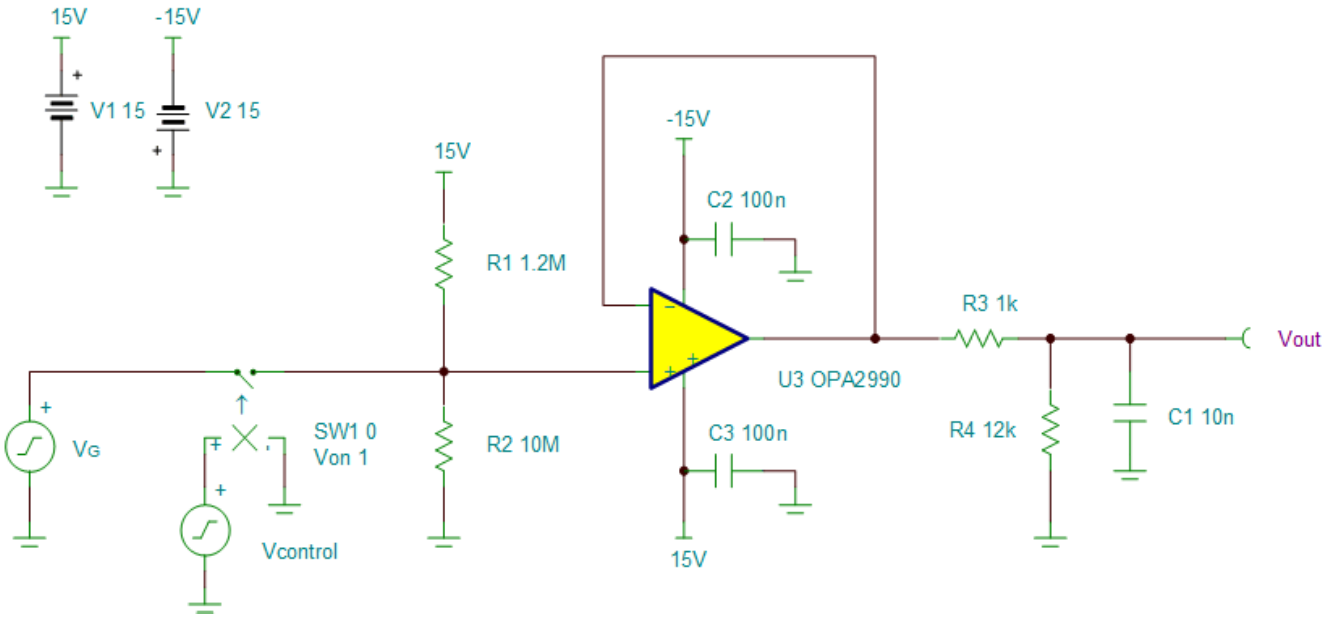
DC Transfer Characteristics

The following graph shows a linear output response of the front-end circuit for input from single-ended –12.88V to +12.88V. See Determining a SAR ADC's Linear Range when using Instrumentation Amplifiers for detailed theory on this subject. The full-scale range (FSR) of the ADC falls within the linear range of the amplifier (OPA990).

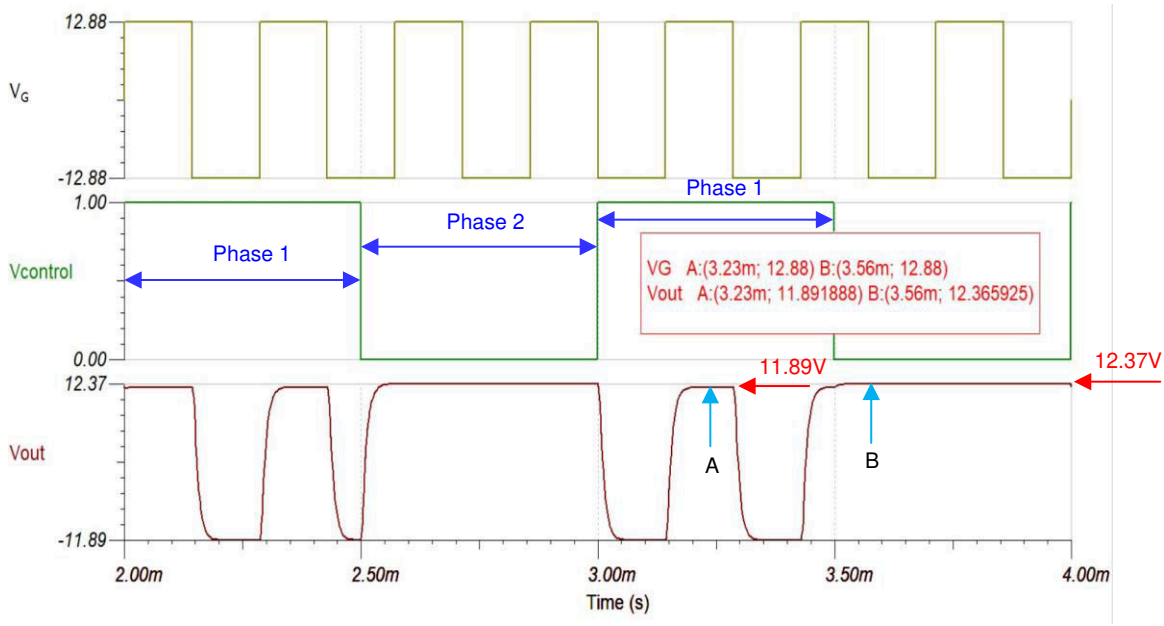


Simulation Verification for Floating Input

The following circuit is used in TINA-TI to simulate and verify if the output voltage is correct as expected when the input of amplifier is floating. A voltage-controlled switch (SW1) is intentionally added to simulate the connection and disconnection status. The switch (SW1) is controlled by a periodic voltage signal (Vcontrol) for open and close.



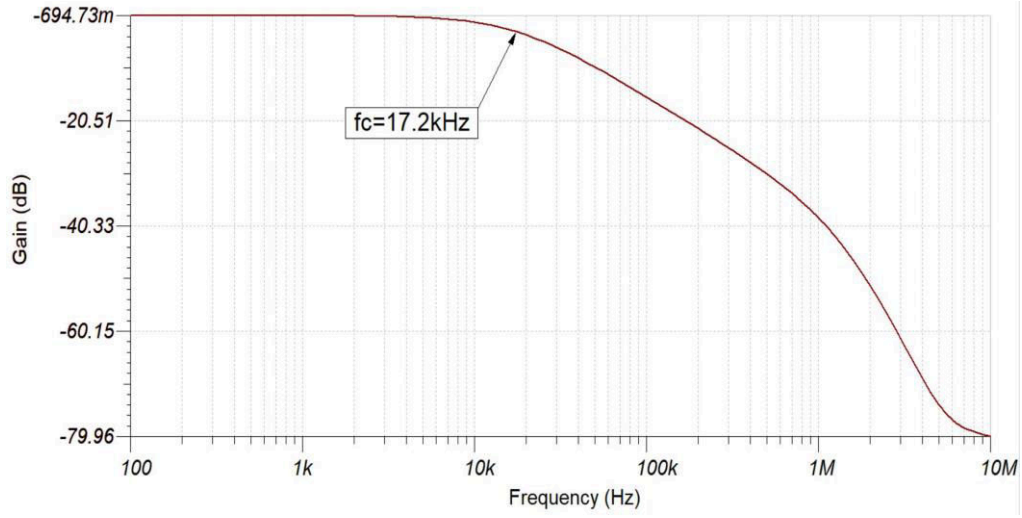
The simulated result is shown in the following graph. The continuous input signal (V_G) sweeps within the normal voltage range of ±12.88V. The control signal (Vcontrol) forces the switch (SW1) to turn on for a connected state in phase 1. The simulation shows a ±11.89-V output signal (Vout) in phase 1. The control signal (Vcontrol) forces the switch (SW1) to turn off for a floating state in phase 2. The simulation shows a 12.37-V output signal (Vout) in phase 2. Note that the simulated value and calculated value (12.38V) match well.



AC Transfer Characteristics

The bandwidth for this circuit is limited by the RC filter (R3||R4 and C1). The hand calculation and the simulated results compare well (hand calculation f_C = 17.2kHz, simulated f_C = 17.2kHz). See the Op Amp Bandwidth video series for more details on this subject. Note that the internal 2nd-order low pass filter of the ADS8681 has a 15-kHz bandwidth. The bandwidth for this circuit is mainly dominated by the low-pass filter of the ADC.

$$f_C = \frac{R_3 + R_4}{2\pi \times R_3 \times R_4 \times C_1} = \frac{1k\Omega + 12k\Omega}{2\pi \times 1k\Omega \times 12k\Omega \times 10nF} = 17.2kHz$$



Noise Simulation

This section walks through a simplified noise calculation for the front-end circuit, providing an estimate to compare with simulated results in TI-TINA. In this circuit example, the resistor noise from the large resistance (R_1 and R_2) is a significant portion of the overall noise of the system. However, the output impedance (R_S) of the signal source (V_G) is usually low so the noise from the combination of R_S, R_1, and R_2 is small. See the following equation for noise calculation with R_S = 100Ω.

Thermal noise from the resistors (R_S, R_1, and R_2):

$$R_{eq1} = R_S \parallel R_1 \parallel R_2 = \frac{R_S \times R_1 \times R_2}{(R_S \times R_1) + (R_S \times R_2) + (R_1 \times R_2)} = \frac{100\Omega \times 1.2M\Omega \times 10M\Omega}{(100\Omega \times 1.2M\Omega) + (100\Omega \times 10M\Omega) + (1.2M\Omega \times 10M\Omega)} = 99.99\Omega$$

$$e_{n\_Req1} = \sqrt{4 \times k_n \times T_n \times R_{eq1}} = \sqrt{4 \times (1.38 \times 10^{-23}) \times 298 \times 99.99\Omega} = 1.282nV / \sqrt{Hz}$$

$$E_{n\_Req1\_RTI} = e_{n\_Req1} \times \sqrt{K_n \times f_C} = (1.282nV / \sqrt{Hz}) \times \sqrt{1.57 \times 17.2kHz} = 0.21uV_{rms}$$

$$E_{n\_Req1\_RTO} = E_{n\_Req1\_RTI} \times \frac{R_4}{R_3 + R_4} = (0.21uV_{rms}) \times \frac{12k\Omega}{1k\Omega + 12k\Omega} = 0.194uV_{rms}$$

Thermal noise from the resistors (R_3 and R_4):

$$R_{eq2} = R_3 \parallel R_4 = \frac{R_3 \times R_4}{R_3 + R_4} = \frac{1k\Omega \times 12k\Omega}{1k\Omega + 12k\Omega} = 0.923k\Omega$$

$$e_{n\_Req2} = \sqrt{4 \times k_n \times T_n \times R_{eq2}} = \sqrt{4 \times (1.38 \times 10^{-23}) \times 298 \times 0.923k\Omega} = 3.89nV / \sqrt{Hz}$$

$$E_{n\_Req2} = e_{n\_Req2} \times \sqrt{K_n \times f_C} = (3.89nV / \sqrt{Hz}) \times \sqrt{1.57 \times 17.2kHz} = 0.64uV_{rms}$$

Noise from OPA990 amplifier:

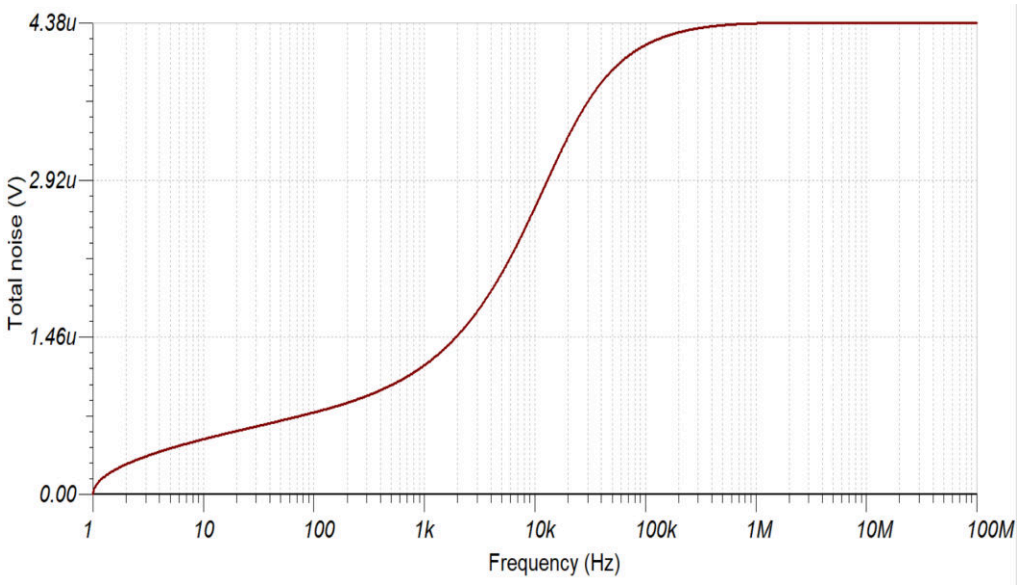
$$E_{n\_OPA\_RTI} = e_{n\_OPA} \times \sqrt{K_n \times f_C} = (28nV / \sqrt{Hz}) \times \sqrt{1.57 \times 17.2kHz} = 4.6uV_{rms}$$

$$E_{n\_OPA\_RTO} = E_{n\_OPA\_RTI} \times \frac{R_4}{R_3 + R_4} = (4.6uV_{rms}) \times \frac{12k\Omega}{1k\Omega + 12k\Omega} = 4.25uV_{rms}$$

Total noise applied to input of the ADC:

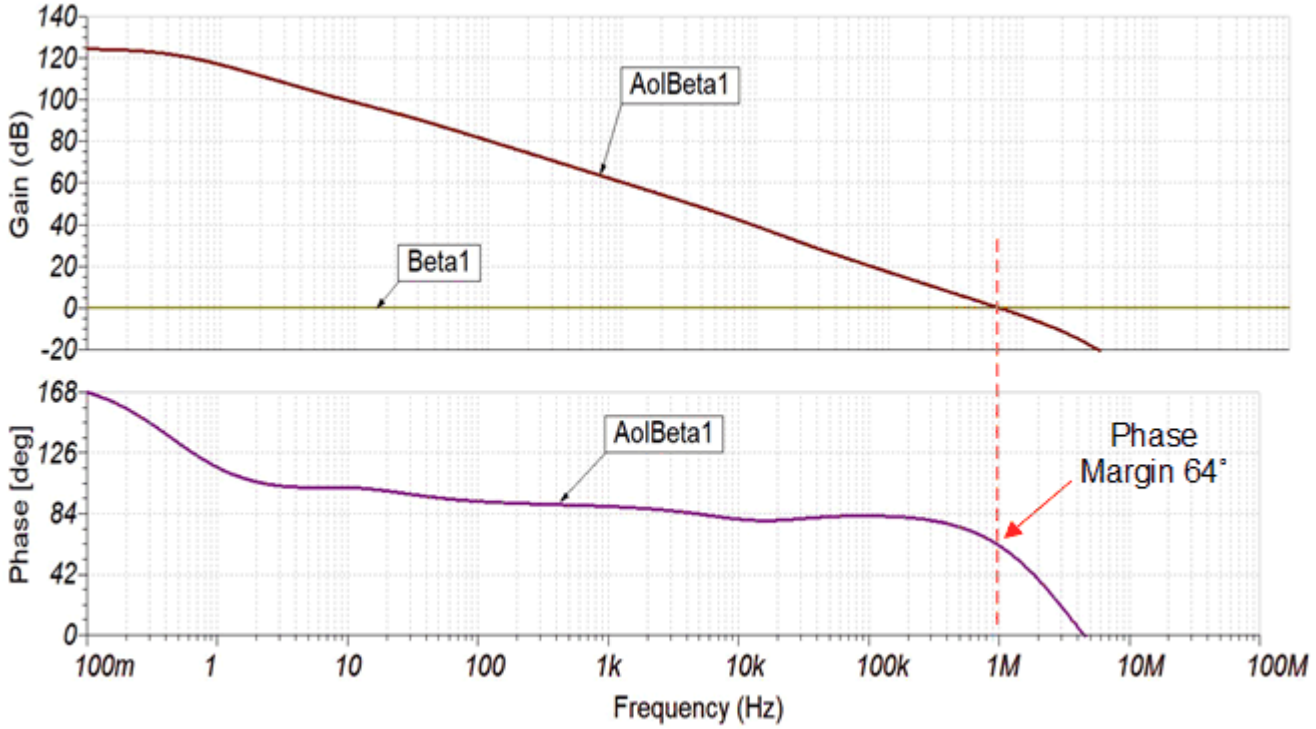
$$E_{n\_total} = \sqrt{E_{n\_Req1\_RTO}^2 + E_{n\_Req2}^2 + E_{n\_OPA\_RTO}^2} = \sqrt{0.194uV_{rms}^2 + 0.64uV_{rms}^2 + 4.25uV_{rms}^2} = 4.3uV_{rms}$$

The calculated and simulated noise match well (calculated noise = 4.3μV_{rms} and simulated = 4.38μV_{rms} as in the following graph). See TI Precision Labs - Op Amps: Noise 4 for detailed theory on amplifier noise calculations, Amplifier Noise Simulations (Op Amps: Noise 5) for detailed theory on amplifier noise simulations, and Calculating the Total Noise for ADC Systems for data converter noise.



Stability Simulation

The following simulation shows a stability check for the solution previously shown. This design has 64 degrees of phase margin which indicates that the circuit is stable. Generally, the circuit which has more than 45 degrees of phase margin is considered to be stable. For more information on stability analysis checks, see the Op Amps: Stability video series.



Design References

See the Analog Engineer's Circuit Cookbooks for TI's comprehensive circuit library.

See TINA-TI simulation software.

Design Featured Devices

Device	Key Features	Link	Other Possible Devices
ADS8681	16-bit, 1-MSPS, single-channel, single supply with bipolar inputs SAR ADC	http://www.ti.com/product/ADS8681	http://www.ti.com/adcs
ADS8688	16-bit, 500-kSPS, 8-channel non-simultaneous-sampling, single supply with bipolar inputs SAR ADC	http://www.ti.com/product/ADS8688	http://www.ti.com/adcs
ADS8686	16-bit, 1MSPS, 16-channel, dual simultaneous-sampling, single supply with bipolar inputs SAR ADC	http://www.ti.com/product/ADS8686S	http://www.ti.com/adcs

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