Application Note

Using the Automatic Gain Controller in TLV320ADCx120 and PCMx120-Q1 Family

ABSTRACT

The TLV320ADCx120 and PCMx120-Q1 family of devices (TLV320ADC3120, TLV320ADC5120, TLV320ADC6120, PCM3120-Q1, PCM5120-Q1, and PCM6120-Q1) are dual-channel, high-performance, analog-to-digital converters for audio applications. This family of devices has an extensive set of features that includes the following:

- Programmable channel gain (PGA)
- Digital volume control
- A programmable microphone bias voltage
- A phase-locked loop (PLL)
- A programmable high pass filter (HPF)
- Automatic Gain Control (AGC)
- Dynamic Range Enhancer (DRE) support in the TLV320ADC5120, TLV320ADC6120, PCM5120-Q1, and PCM6120-Q1
- Linear phase or low-latency filter modes for sample-rates up to 768 kHz

This application note describes how to configure the automatic gain control (AGC) feature in TLV320ADCx120 and PCMx120-Q1 devices.

Table of Contents

List of Figures

List of Tables

Trademarks

1 Introduction

Automatic Gain Control (AGC) is an algorithm that dynamically controls the gain of a signal to maintain a nominally constant output level. A typical example application for AGC occurs while recording speech signals when the speaker is changing his or her distance from the microphone while speaking. Sound pressure levels at the microphone vary inversely with distance to the sound source. Therefore, microphone output levels are weak for the farther sound sources, and loud for the closer sound sources. Without AGC and just a fixed-gain PGA, output levels vary from soft to loud as the person moves closer to the microphone. With AGC enabled, the input level variation can be maintained at a constant level. Thus, AGC automatically responds to changes in the input signal to maintain a fixed level to meet target application requirements. Figure 1-1 shows how the AGC responds to a tone whose level falls below the target level and then rises above it.

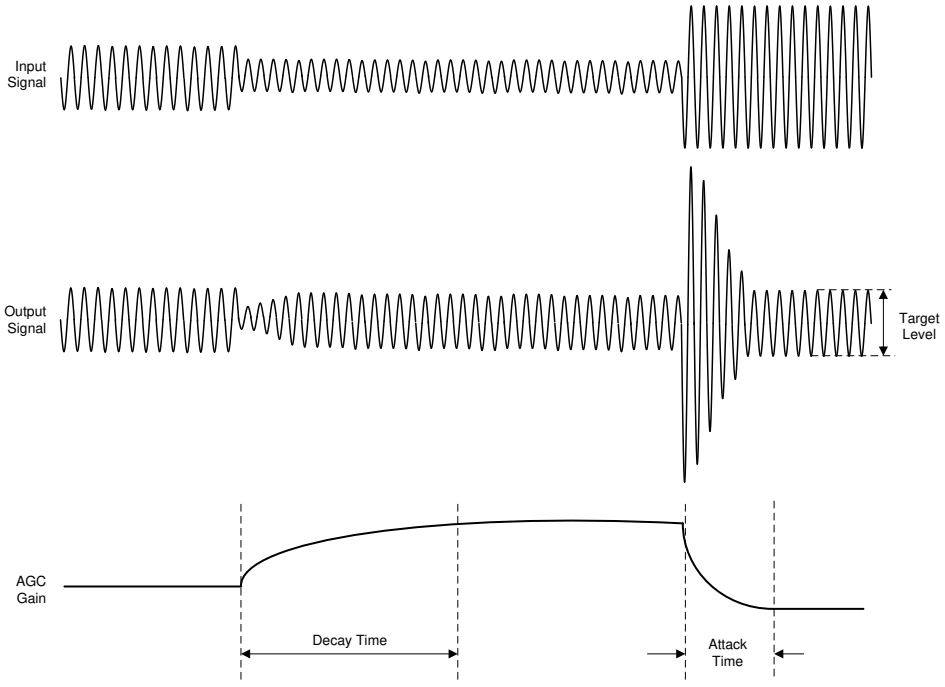

Figure 1-1. AGC Example

Automatic Gain Control (AGC) is supported on all ADC channels of the TLV320ADCx120 and PCMx120-Q1 device family. This application note describes the operation of the AGC, the tunable parameters, and the device configurations required to support AGC.

2 Automatic Gain Control

The AGC algorithm is a mixed-signal solution, where the analog programmable gain amplifier (PGA) of a channel is controlled by a closed-loop control digital algorithm. Figure 2-1 shows the signal processing chain for the device.

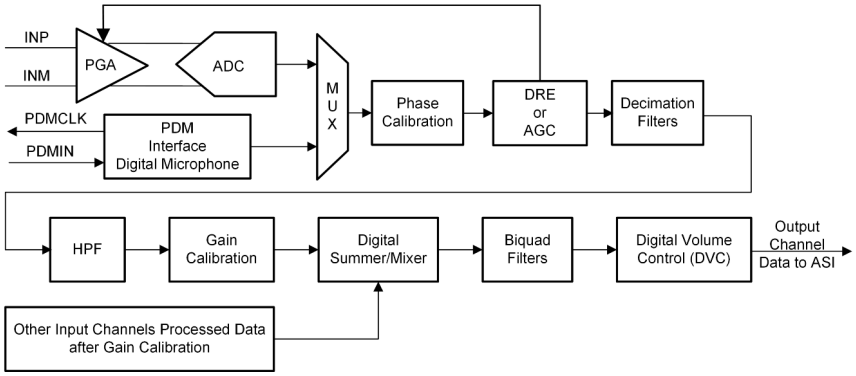

Figure 2-1. AGC Block Diagram

To respond to changes in the input signal, the AGC algorithm monitors the digitized signal from the ADC and adjusts the PGA to maintain a constant target level. If the signal is below the target level, the AGC increases the PGA gain. If the signal is above the target level, the AGC decreases the PGA gain. Using the analog circuitry of the PGA to change the input signal provides optimal noise performance, since it avoids gain adjustments in the digital circuitry that increases the quantization noise. Moreover, the AGC algorithm uses a small step size during PGA changes to reduce distortions in the input signal.

The TLV320ADCx120 and PCMx120-Q1 family supports up to two analog external input channels, with all input channels supporting AGC. The devices support differential or single-ended signals from an analog microphone source or auxiliary line input. The analog microphone inputs supports electret condensers and micro-electro-mechanical (MEMS) microphones. Even though the devices also support digital pulse density modulated (PDM) digital microphones, the AGC does not support digital channels, since the analog gain of the digital microphone cannot be controlled.

The TLV320ADC5120, TLV320ADC6120, PCM5120-Q1, and PCM6120-Q1 also support a Dynamic Range Enhancer (DRE) algorithm on the analog channels to augment the dynamic range. The DRE algorithm controls the PGA to reduce the noise floor for low-level signals. DRE and AGC algorithms cannot be used simultaneously, since both the algorithms control the PGA. As shown in Table 2-1, DRE or AGC selection is done using the DRE_AGC_SEL bit of DSP_CFG1 register (page = 0x00, address = 0x6C). AGC or DRE can be independently enabled or disabled for each channel using the CH1_DREEN (P0_R60_D0), CH2_DREEN (P0_R65_D0), CH3_DREEN (P0_R70_D0), and CH4_DREEN (P0_R75_D0) register bits.

Table 2-1. DRE or AGC Selection Using DSP_CFG1 Register

BIT	FIELD	TYPE	RESET	DESCRIPTION
3	DRE_AGC_SEL	R/W	0h	DRE or AGC selection when is enabled for any channel. 0d = DRE is selected. 1d = AGC is selected.

2.1 High Pass Filter

To remove any DC offset that leads to incorrect input level estimates, the AGC algorithm processes the input signal through a high-pass filter. This HPF is exclusive to the AGC, and is different from the second-order HPF filters used by the decimation filters.

The transfer function implemented by the high-pass filter is given by Equation 1.

$$H(z) = \frac{N0 + N1 \times z^{-1}}{1 + D1 \times z^{-1}} \quad (1)$$

The HPF is a first-order filter implemented using three coefficients: AGC_HPF_B0, AGC_HPF_B1, and AGC_HPF_A1. The transfer function parameters (N0, N1, and D1) are converted to coefficients using Equation 2, Equation 3, and Equation 4.

$$AGC\_HPF\_B0 = round(2^{31} \times N0) \quad (2)$$

$$AGC\_HPF\_B1 = round(2^{31} \times N1) \quad (3)$$

$$AGC\_HPF\_A1 = round(2^{31} \times D1) \quad (4)$$

These coefficients are user-programmable to set a different cutoff frequency from the default cutoff (-3 dB) of 100 Hz for a 48 kHz sample rate. Increasing the cutoff frequency results in faster settling of signal-level estimates, while decreasing the cutoff frequency improves the accuracy of the signal-level estimate. The default filter coefficients provide a good balance between speed and accuracy, and are suitable for most applications. Table 2-2 shows the coefficient registers. The coefficients are represented in 2s-complement, 32-bit format.

Table 2-2. Programmable Coefficient Registers for High Pass Filter

COEFFICIENT	PAGE	REGISTER	RESET VALUE	DESCRIPTION
AGC_HPF_B0	0x06	0x78	0x7F	AGC_HPF_B0 Byte[31:24]
	0x06	0x79	0x7F	AGC_HPF_B0 Byte[23:16]
	0x06	0x7A	0xD2	AGC_HPF_B0 Byte[15:8]
	0x06	0x7B	0xB4	AGC_HPF_B0 Byte[7:0]
AGC_HPF_B1	0x06	0x7C	0x80	AGC_HPF_B1 Byte[31:24]
	0x06	0x7D	0x80	AGC_HPF_B1 Byte[23:16]
	0x06	0x7E	0x2D	AGC_HPF_B1 Byte[15:8]
	0x06	0x7F	0x4C	AGC_HPF_B1 Byte[7:0]
AGC_HPF_A1	0x07	0x08	0x7E	AGC_HPF_A1 Byte[31:24]
	0x07	0x09	0xFF	AGC_HPF_A1 Byte[23:16]
	0x07	0x0A	0xA5	AGC_HPF_A1 Byte[15:8]
	0x07	0x0B	0x68	AGC_HPF_A1 Byte[7:0]

2.2 AGC Parameters

Table 2-3 shows the parameters of the AGC algorithm. The first two parameters (AGC Target Level and Maximum Gain) are controlled by writing to the device registers. The other parameters reside in the 32-bit wide coefficient memory (Book 0, Page 5, Page 6, and Page 7) of the device. During warmboot device takes the default values for the parameters in Book 0: page 5, page 6 and page 7, for overriding these parameters with the user values we need to set the bit "DRE_AGC_CFG_DEF_OVR = 1" in DSP_CFG1 register (P0_R108_D2).

Table 2-3. List of AGC Parameters

AGC PARAMETER	Function/Description
AGC Target Level (dB)	The AGC target level represents the nominal level at which the AGC attempts to maintain its output signal.
Maximum Gain (dB)	Upper limit of gain in dB applied by the AGC for signals below target level.
Noise Threshold (dB)	The threshold level the AGC utilizes to distinguish noise from weak signals. Signals lower than this threshold are classified as noise and not amplified by the AGC.
Release Time Constant (seconds)	How fast the AGC circuitry responds with a PGA gain increase when the input signal falls below the target level.
Attack Time Constant (seconds)	How fast the AGC circuitry responds with a PGA gain decrease when input signal rises above the target level.
Release Hysteresis (dB)	Amount of signal level decrease in dB past the Target Level that forces the AGC to increase gain and start a release.
Attack Hysteresis (dB)	Amount of signal level increase in dB past the Target Level that forces the AGC to decrease gain and start an attack.
Noise Hysteresis (dB)	Amount of signal level change past the Noise Threshold that causes the AGC to decide between noise or signal.
Release Debounce (samples)	The number of consecutive input samples that falls below Target Level after an attack event before the AGC starts releasing and increasing PGA gain.
Attack Debounce (samples)	The number of consecutive input samples that rises above Target Level after a release event before the AGC starts attacking and decreasing PGA gain.
Noise Debounce (samples)	The number of consecutive samples for the input to fall below Noise Threshold for the signal to be considered as noise.

AGC Target Level: The AGC target level represents the nominal level at which the AGC attempts to maintain the output signal. The target level is expressed relative to full scale (dBFS) of the ADC output. Table 2-4 lists the AGC Target Level configuration settings. The default is -34 dB. Setting a high target level increases the converted output level. However, large target level settings can lead to clipping the input signal with a sudden increase in the signal level. Therefore, set the target level with enough margin so as to prevent clipping when loud sounds occur.

Table 2-4. AGC Target Level Programmable Settings

P0_R112_D[7:4] : AGC_LVL[3:0]	AGC TARGET LEVEL FOR OUTPUT
0000	The AGC target level is the –6 dB output signal level
0001	The AGC target level is the –8 dB output signal level
0010	The AGC target level is the –10 dB output signal level
…	…
1110 (default)	The AGC target level is the –34 dB output signal level
1111	The AGC target level is the –36 dB output signal level

Maximum Gain: The maximum gain represents the upper limit of gain applied by the AGC for signals below the target level. Table 2-5 lists the Maximum Gain configuration settings. The default value is 24 dB. It can be programmed from 3 dB to 42 dB with steps of 3 dB.

Table 2-5. AGC Maximum Gain Programmable Settings

P0_R112_D[3:0] : AGC_MAXGAIN[3:0]	AGC MAXIMUM GAIN ALLOWED
0000	The AGC maximum gain allowed is 3 dB
0001	The AGC maximum gain allowed is 6 dB
0010	The AGC maximum gain allowed is 9 dB
…	…
0111 (default)	The AGC maximum gain allowed is 24 dB
…	…
1110	The AGC maximum gain allowed is 39 dB
1111	The AGC maximum gain allowed is 42 dB

Noise Threshold: The threshold level used by the AGC to distinguish noise from weak signals. Signals lower than this threshold are classified as noise and not amplified by the AGC. Noise Threshold is set by writing to the AGC_NOISE coefficient. Equation 5 shows the computation of the AGC_NOISE parameter.

$$AGC\_NOISE = \text{round}(2^8 \times NT) \tag{5}$$

where

- NT is the Noise Threshold in dB

The default value (0xFFFFA600) corresponds to -90 dB. Table 2-6 shows the registers that control the AGC_NOISE parameter.

Table 2-6. Programmable Coefficient Registers for Noise Threshold

COEFFICIENT	PAGE	REGISTER	RESET VALUE	DESCRIPTION
AGC_NOISE	0x06	0x20	0xFF	AGC_NOISE Byte[31:24]
	0x06	0x21	0xFF	AGC_NOISE Byte[23:16]
	0x06	0x22	0xA6	AGC_NOISE Byte[15:8]
	0x06	0x23	0x00	AGC_NOISE Byte[7:0]\

Release Time Constant: How fast the AGC circuitry responds with a PGA gain increase when the input signal falls below the target level. The Release Time Constant is controlled by two coefficients: AGC_REL_ALPHA and AGC_REL_BETA. Equation 6 and Equation 7 show how to compute the AGC_REL_ALPHA and AGC_REL_BETA parameters from the following time constant:

$$AGC\_REL\_ALPHA = \text{round}(2^{31} \times e^{-\ln(9)/48000 \times RT}) \tag{6}$$

$$AGC\_REL\_BETA = 2^{31} - \text{round}(2^{31} \times e^{-\ln(9)/48000 \times RT}) \tag{7}$$

where

- RT is the Release Time Constant in seconds

Table 2-7 shows the registers that control AGC_REL_ALPHA and AGC_REL_BETA parameters. These parameters are written in 2s-complement representation. The default values for AGC_REL_ALPHA and AGC_REL_BETA corresponds to a time constant of 20 milliseconds.

Table 2-7. Programmable Registers for Release Time Constant

COEFFICIENT	PAGE	REGISTER	RESET VALUE	DESCRIPTION
AGC_REL_ALPHA	0x05	0x7C	0x7F	AGC_REL_ALPHA Byte[31:24]
	0x05	0x7D	0xB5	AGC_REL_ALPHA Byte[23:16]
	0x05	0x7E	0x16	AGC_REL_ALPHA Byte[15:8]
	0x05	0x7F	0x50	AGC_REL_ALPHA Byte[7:0]
AGC_REL_BETA	0x06	0x08	0x00	AGC_REL_BETA Byte[31:24]
	0x06	0x09	0x4A	AGC_REL_BETA Byte[23:16]
	0x06	0x0A	0xE9	AGC_REL_BETA Byte[15:8]
	0x06	0x0B	0xB0	AGC_REL_BETA Byte[7:0]

Attack Time Constant: How fast the AGC circuitry responds with a PGA gain decrease when the input signal rises above the target level. Equation 8 and Equation 9 show the computation of the Attack Time Constant Parameters AGC_ATT_ALPHA and AGC_ATT_BETA.

$$AGC\_ATT\_ALPHA = \text{round}(2^{31} \times e^{-\ln(9)/48000 \times AT}) \quad (8)$$

$$AGC\_ATT\_BETA = \text{round}(2^{31} \times e^{-\ln(9)/48000 \times AT}) \quad (9)$$

where

- AT is the Attack Time Constant in seconds

AGC_ATT_ALPHA and AGC_ATT_BETA parameters are each 32-bit wide, 2s-complement representations, and are controlled by registers shown in Table 2-8. The default values for AGC_ATT_ALPHA and AGC_ATT_BETA corresponds to a time constant of 0.1 milliseconds.

Table 2-8. Programmable Registers for Attack Time Constant

COEFFICIENT	PAGE	REGISTER	RESET VALUE	DESCRIPTION
AGC_ATT_ALPHA	0x06	0x0C	0x50	AGC_ATT_ALPHA Byte[31:24]
	0x06	0x0D	0xFC	AGC_ATT_ALPHA Byte[23:16]
	0x06	0x0E	0x64	AGC_ATT_ALPHA Byte[15:8]
	0x06	0x0F	0x5C	AGC_ATT_ALPHA Byte[7:0]
AGC_ATT_BETA	0x06	0x10	0x2F	AGC_ATT_BETA Byte[31:24]
	0x06	0x11	0x03	AGC_ATT_BETA Byte[23:16]
	0x06	0x12	0x9B	AGC_ATT_BETA Byte[15:8]
	0x06	0x13	0xA4	AGC_ATT_BETA Byte[7:0]

Release Hysteresis: Amount of signal level decrease past Target Level that forces the AGC to increase gain and start a release. Release Hysteresis is specified in dB. Equation 10 shows the computation of the AGC_REL_HYST parameter.

$$AGC\_REL\_HIST = \text{round}(2^{8} \times RH) \quad (10)$$

where

- RH (>= 0) is the Release Hysteresis in dB

The default value of AGC_REL_HYST is 0x00000300, which corresponds to a hysteresis of 3 dB. Table 2-9 list the registers corresponding to AGC_REL_HYST.

Table 2-9. Programmable Registers for Release Hysteresis

COEFFICIENT	PAGE	REGISTER	RESET VALUE	DESCRIPTION
AGC_REL_HYST	0x06	0x34	0x00	AGC_REL_HYST Byte[31:24]
	0x06	0x35	0x00	AGC_REL_HYST Byte[23:16]
	0x06	0x36	0x03	AGC_REL_HYST Byte[15:8]
	0x06	0x37	0x00	AGC_REL_HYST Byte[7:0]

Attack Hysteresis: Amount of signal level increase past Target Level that forces the AGC to decrease the gina and start an attack. Attack Hysteresis is specified in dB. Equation 11 shows the computation of the AGC_ATT_HYST parameter.

$$AGC\_ATT\_HYST = \text{round}(2^8 \times AH) \tag{11}$$

where

- AH (>= 0) is the Attack Hysteresis in dB

The default value of Attack Hysteresis is 1 dB. Table 2-10 shows the registers that control the AGC_ATT_HYST parameter.

Table 2-10. Programmable Coefficient Registers for Attack Hysteresis

COEFFICIENT	PAGE	REGISTER	RESET VALUE	DESCRIPTION
AGC_ATT_HYST	0x06	0x3C	0x00	AGC_ATT_HYST Byte[31:24]
	0x06	0x3D	0x00	AGC_ATT_HYST Byte[23:16]
	0x06	0x3E	0x01	AGC_ATT_HYST Byte[15:8]
	0x06	0x3F	0x00	AGC_ATT_HYST Byte[7:0]

Noise Hysteresis: (AGC_NOISE_HYST): Amount of signal level change around the Noise Threshold that causes the AGC to decide between noise and signal. A rising signal has to rise above the Noise Hysteresis level to be amplified to the Target Level. A decreasing signal has to fall below the Noise Hysteresis level to be considered as noise. Noise Hysteresis is specified in dB. Equation 12 shows the computation of the AGC_NOISE_HYST parameters.

$$AGC\_NOISE\_HYST = \text{round}(2^8 \times NH) \tag{12}$$

where

- NH (>= 0) is the Noise Hysteresis in dB

The default value of AGC_NOISE_HYST is 0x00000600, which corresponds to a hysteresis of 6 dB. Table 2-10 shows the registers controlling the AGC_NOISE_HYST parameter.

Table 2-11. Programmable Registers for Noise Hysteresis

COEFFICIENT	PAGE	REGISTER	RESET VALUE	DESCRIPTION
AGC_NOISE_HYST	0x06	0x54	0x00	AGC_NOISE_HYST Byte[31:24]
	0x06	0x55	0x00	AGC_NOISE_HYST Byte[23:16]
	0x06	0x56	0x06	AGC_NOISE_HYST Byte[15:8]
	0x06	0x57	0x00	AGC_NOISE_HYST Byte[7:0]

Attack Debounce: The number of consecutive input samples that rises above the target level after a release event before the AGC starts attack and decreases the PGA. Equation 13 shows the computation of the AGC_ATT_CNT parameter.

$$AGC\_ATT\_CNT = round(2^8 \times 48000 \times AD) \quad (13)$$

where

- AD (>= 0) is specified in seconds

Table 2-12 shows the registers controlling the AGC_ATT_CNT parameter.

Table 2-12. Programmable Registers for Attack Debounce

COEFFICIENT	PAGE	REGISTER	RESET VALUE	DESCRIPTION
AGC_ATT_CNT	0x06	0x18	0x00	AGC_ATT_CNT Byte[31:24]
	0x06	0x19	0x00	AGC_ATT_CNT Byte[23:16]
	0x06	0x1A	0x02	AGC_ATT_CNT Byte[15:8]
	0x06	0x1B	0x00	AGC_ATT_CNT Byte[7:0]

Release Debounce: The number of consecutive input samples that falls below Target Level after an attack event before the AGC starts releasing and increasing the PGA gain. The default value of Release Debounce is 25 milliseconds at 48 kHz. Equation 14 shows the computation of the AGC_REL_CNT parameter.

$$AGC\_REL\_CNT = round(2^8 \times 48000 \times RD) \quad (14)$$

where

- RD (>= 0) is the Release Debounce specified in seconds

Table 2-13 shows the registers controlling the AGC_REL_CNT parameter.

Table 2-13. Programmable Registers for Release Debounce

COEFFICIENT	PAGE	REGISTER	RESET VALUE	DESCRIPTION
AGC_REL_CNT	0x06	0x1C	0x00	AGC_REL_CNT Byte[31:24]
	0x06	0x1D	0x04	AGC_REL_CNT Byte[23:16]
	0x06	0x1E	0xB0	AGC_REL_CNT Byte[15:8]
	0x06	0x1F	0x00	AGC_REL_CNT Byte[7:0]

Noise Debounce: The number of consecutive samples for the input to fall below Noise Threshold for the signal to be considered noise. Equation 15 shows the computation of the AGC_NOISE_CNT parameter.

$$AGC\_NOISE\_CNT = round(2^8 \times 48000 \times ND) \quad (15)$$

where

- ND (>= 0) is the Noise Debounce time specified in seconds

The default value of AGC_NOISE_CNT is 0x0004B000, which corresponds to a debounce time of 25 milliseconds at 48 kHz. Table 2-14 shows the registers controlling the AGC_NOISE_CNT parameter.

Table 2-14. Programmable Registers for Noise Debounce

COEFFICIENT	PAGE	REGISTER	RESET VALUE	DESCRIPTION
AGC_NOISE_CNT	0x06	0x44	0x00	AGC_NOISE_CNT Byte[31:24]
	0x06	0x45	0x04	AGC_NOISE_CNT Byte[23:16]
	0x06	0x46	0xB0	AGC_NOISE_CNT Byte[15:8]
	0x06	0x47	0x00	AGC_NOISE_CNT Byte[7:0]

3 AGC Results

This section discusses the AGC results for Normal AGC mode and Enhanced AGC mode. Output level vs Input level and THDN vs. Input level plots are included for the following cases

- Backward sweep (High input (0 dB for example, 2 VRms) to low input (-130 dB for example, 0.64 uVRms))
- Forward sweep (Low input (-130 dB for example, 0.64 uVRms) to High input (0 dB for example, 2 VRms))
- AGC disabled

Different configuration values for these plots are

Recommended setting for Noise Threshold when using AGC at different sampling frequencies are -85 dB for 16 KHz to 48 KHz, -70 dB for 96 KHz, -65 dB for 192 KHz.

- Target Level = -34 dB
- Maximum Gain = 24 dB
- Attack Hysteresis = 1 dB
- Release Hysteresis = 3 dB
- Noise Hysteresis = 4 dB

3.1 Normal AGC Mode

AGC curves (output level vs. input level and THDN vs. input level) for different sampling rates, 48 KHz in Figure 3-1 and Figure 3-2, 16 KHz in Figure 3-3 and Figure 3-4 and 96 KHz in Figure 3-5 and Figure 3-6 for normal AGC mode.

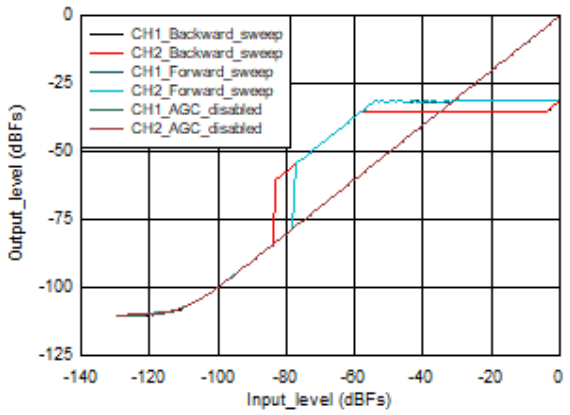

Figure 3-1. Output Level vs. Input Level 48 KHz

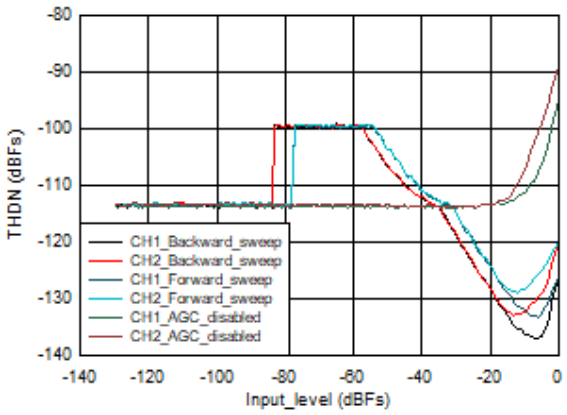

Figure 3-2. THDN vs. Input_Level 48 KHz

Forward sweep: When the input level is swept in the forward direction starting from -130 db, as the input level is less than the noise threshold AGC does not amplify the signal and output level tracks input level as the AGC disabled case, it waits for the input level to cross the noise threshold, also we have noise hysteresis of 4 dB , hence AGC should start applying gain when input level crosses -81 dB, but output level estimation of AGC can have an error in the range of ~1.5 dB to 2 dB, this could vary from device to device, hence AGC starts applying gain when input is at -79 dB. When input is at -79 dB, AGC applies its maximum gain possible trying to achieve the target level. Maximum gain of 24dB is applied by AGC from input level -79 dB to -55 dB (actual should have been -58 dB , but because of output level estimation error of 2 dB and attack hysteresis of 1 dB , AGC applies maximum gain till -55 dB), now as the input increases further AGC starts attacking by decreasing the PGA gain and maintaining the output at -31 dB level (Output maintained = Target programmed (-34 dB) + attack hysteresis (1 dB) + output level estimation error (2 dB)). For further increase in the input level from -54 dB to -1 dB, AGC decreases the PGA gain accordingly and maintains the output at -31 dB level. For full scale input (0dB) AGC output level drops by 2 dB and output is held at -33 dB. To get rid of this full scale input issue , user should use Enhanced AGC mode.

Backward sweep: When the input level is swept in the backward direction starting from 0db , as the input level is suddenly full scale (for example, 2 VRms) , AGC cannot maintaining the output level constant to the target level instantaneously. Now as the input level goes down AGC starts responding and output level is maintained at -35 dB when input reaches around -4 dB (Output maintained = Target programmed (-34 dB) - release hysteresis (3 dB) + output level estimation error (2 dB)). As the input signal level decreases further, output level is maintained constant at -35 dB by increasing the PGA gain till input level of -58 dB. As the input level goes down further AGC applies its maximum gain possible (24 dB) and the output level = input level + maximum gain , this continues till the input signal level reaches noise threshold of -85 dB. For further reduction in input, AGC stops working and output level tracks input level as in AGC disabled case.

AGC disabled: When AGC is disabled , output level tracks input level (channel gain programmed to 0 dB), when input is swept from High input (0 dB for example, 2 VRms) to low input (-130 dB for example, 0.64 uVRms) or Low input (-130 dB for example, 0.64 uVRms) to High input (0 dB for example, 2 VRms), till noise floor is reached.

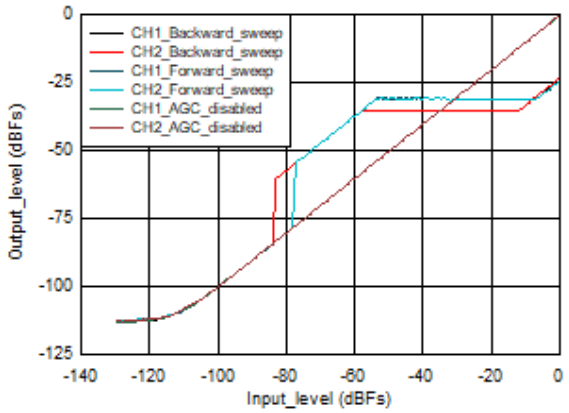

Figure 3-3. Output Level vs. Input Level 16 KHz

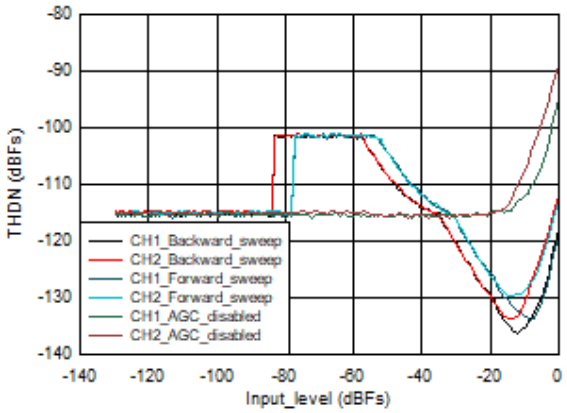

Figure 3-4. THDN vs. Input_Level 16 KHz

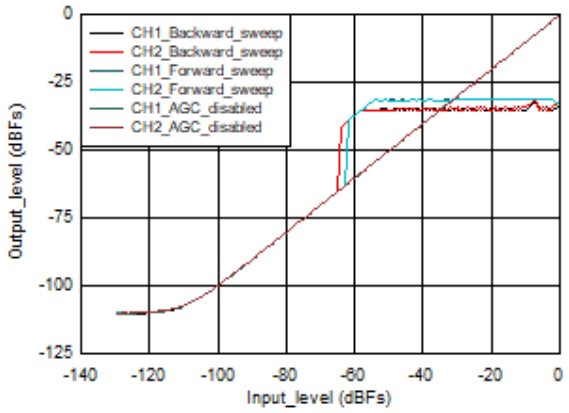

Figure 3-5. Output Level vs. Input Level 96 KHz

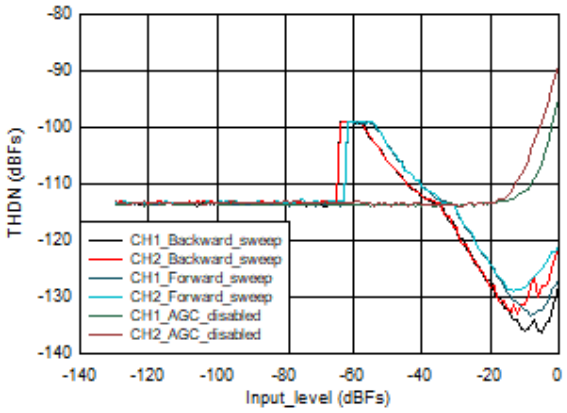

Figure 3-6. THDN vs. Input_Level 96 KHz

3.2 Enhanced AGC mode

AGC curves (output level vs. input level and THDN vs. input level) for different sampling rates, 48 KHz in Figure 3-7 and Figure 3-8, 16 KHz in Figure 3-9 and Figure 3-10 and 96 KHz in Figure 3-11 and Figure 3-12 for enhanced AGC mode.

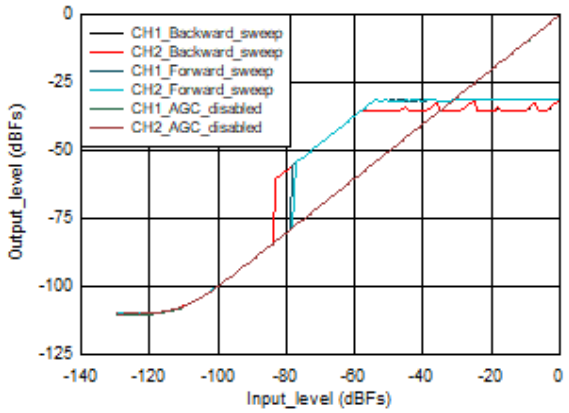

Figure 3-7. Output Level vs. Input Level 48 KHz (Enhanced mode)

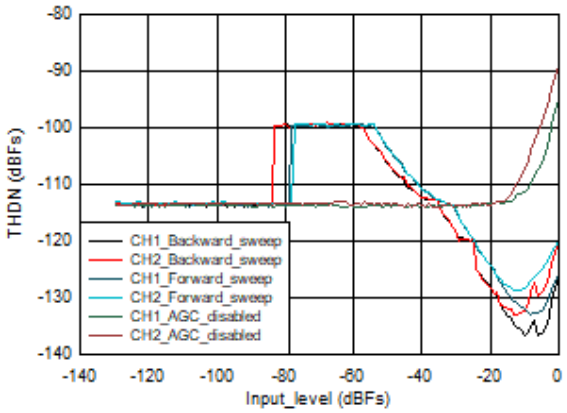

Figure 3-8. THDN vs. Input_Level 48 KHz (Enhanced Mode)

Forward sweep: Enhanced mode behavior is same as normal mode behavior for input level sweep in the forward direction from -130 dB to -1 dB. For full scale input (0dB) also AGC output level is held at -31 dB when we are in Enhanced AGC mode.

Backward sweep: Enhanced mode behavior is same as normal mode behavior for input level sweep in the backward direction from 0 dB to -130 dB.

AGC disabled: Enhanced mode behavior is same as normal mode behavior when AGC is disabled.

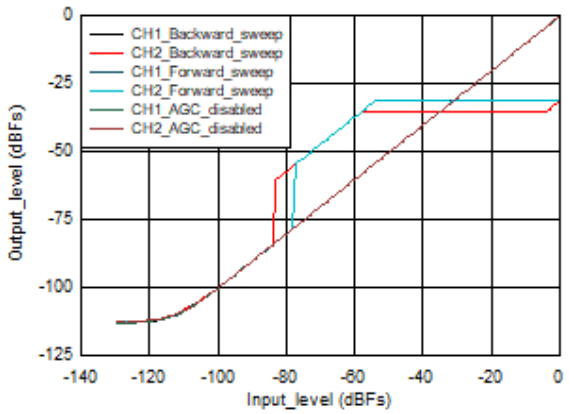

Figure 3-9. Output Level vs. Input Level 16 KHz (Enhanced Mode)

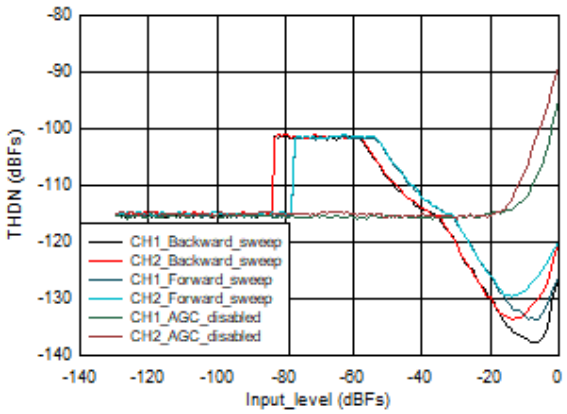

Figure 3-10. THDN vs. Input_Level 16 KHz (Enhanced Mode)

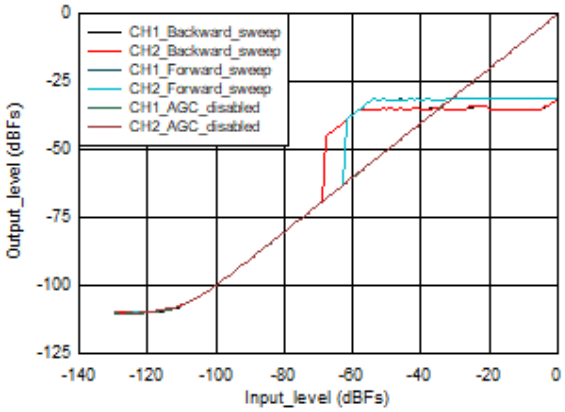

Figure 3-11. Output Level vs. Input Level 96 KHz (Enhanced Mode)

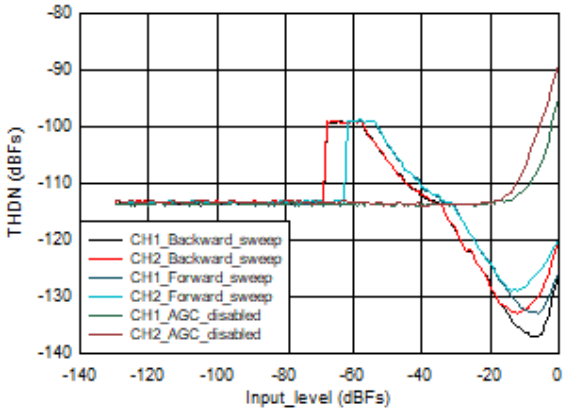

Figure 3-12. THDN vs. Input_Level 96 KHz (Enhanced Mode)

4 Examples

Two examples are presented below for configuring the AGC for two different target applications at sampling frequency of 48KHz. Example 1 is for scenarios when the noise is much lower than the input signal. Example 2 is for scenarios where the noise is significantly larger than the desired signal.

Example 1: When noise is significantly smaller in amplitude compared to signal, the AGC can easily distinguish between noise and signal by setting the Noise Threshold higher than the noise floor, but lower than the weakest possible signal. When such clear demarcations are possible, higher maximum gain can be used, since there is low possibility of gaining up the noise. The following values can be used for this application.

- Target Level = -36 dB
- Maximum Gain = 24 dB
- Noise Threshold = -85 dB
- Attack Time = 0.1 ms
- Release Time = 20 ms
- Attack Hold = 0.0417 ms
- Release Hold = 20 ms
- Attack Hysteresis = 1 dB
- Release Hysteresis = 3 dB
- Noise Hysteresis = 4 dB

```
# Key: w 9C XX YY ==> write to I2C address 0x98, to register 0xXX, data 0xYY
#               # ==> comment delimiter
#
# The following list gives an example sequence of items that must be executed in the time
# between powering the device up and reading data from the device. Note that there are
# other valid sequences depending on which features are used.
#
# See the corresponding EVM user guide for jumper settings and audio connections.
#
# Differential 2-channel : INP1/INM1 - Ch1, INP2/INM2 - Ch2
# FSYNC = 48 kHz (Output Data Sample Rate), BCLK = 11.2896 MHz (BCLK/FSYNC = 256)
#################################################################
#
#
# Power up IOVDD and AVDD power supplies
# Wait for 1ms.
#
w 9C 00 00 # Goto Page 0
w 9C 02 81 # Wake-up device by I2C write into P0_R2 using internal AREG
w 9C 02 81 # Exit Sleep mode
d 10       # Wait for 16 ms
w 9c 6C 4C # Enable AGC in DSP_CFG1 and Override AGC parameters with user values
w 9C 3C 01 # Select AGC on Ch. 1 using CH1_CFG0
w 9C 41 01 # Select AGC on Ch. 2 using CH2_CFG0
w 9C 70 E7 # AGC LVL = -36 dB, AGC GAIN = 24 dB
w 9C 00 05          # Goto Page 5
w 9C 7C 7F B5 16 50 # AGC Release Time Alpha
w 9C 00 05          # Goto Page 6
w 9C 08 00 4A E9 B0 # AGC Release Time Beta
w 9C 0C 50 FC 64 5C # AGC Attack Time Alpha
w 9C 10 2F 03 9B A4 # AGC Attack Time Beta
w 9C 18 00 00 02 00 # AGC Attack Debounce
w 9C 1C 00 04 B0 00 # AGC Release Debounce
w 9C 20 FF FF AB 00 # AGC Noise Threshold : -85 dB
w 9C 44 00 04 B0 00 # AGC Noise Debounce
w 9C 3C 00 00 01 00 # AGC Attack Hysteresis
w 9C 34 00 00 03 00 # AGC Release Hysteresis
w 9C 54 00 00 04 00 # AGC Noise Hysteresis : 4 dB
w 9C 78 7F 7F D2 B4 # AGC HPF B0
w 9c 7C 80 80 2D 4C # AGC HPF B1
w 9C 00 06          # Goto Page 6
w 9c 54 7E FF A5 68 # AGC HPF A1

w 9C 00 00 # Goto Page 0
w 9c 07 30 # TDM Mode with 32 Bits/Channel
w 9C 73 C0 # Enable Ch.1 - Ch.2
w 9C 74 C0 # Enable ASI Output channels
w 9c 75 E0 # Power up ADC
```

Example 2: When noise is significantly high and not easily distinguishable from a weak signal, it is not recommended to use a high maximum gain. The Noise Threshold has to be set closer to the expected noise floor. The following values can be used for this application.

- Target Level = -36 dB
- Maximum Gain = 18 dB
- Noise Threshold = -80 dB
- Attack Time = 0.1 ms
- Release Time = 20 ms
- Attack Hold = 0.0417 ms
- Release Hold = 20 ms
- Attack Hysteresis = 1 dB
- Release Hysteresis = 3 dB
- Noise Hysteresis = 4 dB

```
# Key: w 9C XX YY ==> write to I2C address 0x98, to register 0xXX, data 0xYY
#               # ==> comment delimiter
#
# The following list gives an example sequence of items that must be executed in the time
# between powering the device up and reading data from the device. Note that there are
# other valid sequences depending on which features are used.
#
# See the corresponding EVM user guide for jumper settings and audio connections.
#
# Differential 2-channel : INP1/INM1 - Ch1, INP2/INM2 - Ch2
# FSYNC = 48 kHz (Output Data Sample Rate), BCLK = 11.2896 MHz (BCLK/FSYNC = 256)
##################################################################
#
#
# Power up IOVDD and AVDD power supplies
# Wait for 1ms.
#
w 9C 00 00 # Goto Page 0
w 9C 02 81 # Wake-up device by I2C write into P0_R2 using internal AREG
w 9C 02 81 # Exit Sleep mode
d 10       # Wait for 16 ms
w 9c 6C 4C # Enable AGC in DSP_CFG1 and Override AGC parameters with user values
w 9C 3C 01 # Select AGC on Ch. 1 using CH1_CFG0
w 9C 41 01 # Select AGC on Ch. 2 using CH2_CFG0
w 9C 70 E5 # AGC LVL = -36 dB, AGC GAIN = 18 dB
w 9C 00 05          # Goto Page 5
w 9C 7C 7F B5 16 50 # AGC Release Time Alpha
w 9C 00 05          # Goto Page 6
w 9C 08 00 4A E9 B0 # AGC Release Time Beta
w 9C 0C 50 FC 64 5C # AGC Attack Time Alpha
w 9C 10 2F 03 9B A4 # AGC Attack Time Beta
w 9C 18 00 00 02 00 # AGC Attack Debounce
w 9C 1C 00 04 B0 00 # AGC Release Debounce
w 9C 20 FF FF B0 00 # AGC Noise Threshold : -80 dB
w 9C 44 00 04 B0 00 # AGC Noise Debounce
w 9C 3C 00 00 01 00 # AGC Attack Hysteresis
w 9C 34 00 00 03 00 # AGC Release Hysteresis
w 9C 54 00 00 04 00 # AGC Noise Hysteresis : 4 dB
w 9C 78 7F 7F D2 B4 # AGC HPF B0
w 9C 7C 80 80 2D 4C # AGC HPF B1
w 9C 00 06          # Goto Page 6
w 9C 54 7E FF A5 68 # AGC HPF A1

w 9C 00 00 # Goto Page 0
w 9C 07 30 # TDM Mode with 32 Bits/Channel
w 9C 73 c0 # Enable Ch.1 - Ch.2
w 9C 74 c0 # Enable ASI Output channels
w 9C 75 e0 # Power up ADC
```

5 Related Documentation

For related documentation see the following:

- PCM6120-Q1
  - Texas Instruments, *PCM6120-Q1 2-Channel, 768-kHz, Burr-Brown Audio ADC data sheet*
- PCM5120-Q1
  - Texas Instruments, *PCM5120-Q1 2-Channel, 768-kHz, Burr-Brown Audio ADC data sheet*
- PCM3120-Q1
  - Texas Instruments, *PCM3120-Q1 2-Channel, 768-kHz, Burr-Brown Audio ADC data sheet*
- TLV320ADC6120
  - Texas Instruments, *TLV320ADC6120 2-Channel, 768-kHz, Burr-Brown™ Audio ADC data sheet*
  - Texas Instruments, *TLV320ADC6120 stereo-channel, 768-kHz, Burr-Brown™ audio ADC with 106-dB SNR evaluation module*
- TLV320ADC5120
  - Texas Instruments, *TLV320ADC5120 2-Channel, 768-kHz, Burr-Brown™ Audio ADC data sheet*
  - Texas Instruments, *TLV320ADC5120 stereo-channel, 768-kHz, Burr-Brown™ audio ADC with 106-dB SNR evaluation module*
- TLV320ADC3120
  - Texas Instruments, *TLV320ADC3120 2-Channel, 768-kHz, Burr-Brown™ Audio ADC data sheet*
  - Texas Instruments, *TLV320ADC3120 stereo-channel, 768-kHz, Burr-Brown™ audio ADC with 106-dB SNR evaluation module*
- Texas Instruments, *ADCx120EVM-PDK User's Guide*
- Texas Instruments, *PurePath™ Console*

A Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (September 2021) to Revision A (April 2022)	Page
• Added PCMx120-Q1 devices	1

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265