Application Note

Dynamic Range Enhancer and Compressor in TLV320ADCx120 and PCMx120-Q1

Gaurav Rana *Diljith Thodhi*

ABSTRACT

TLV320ADC5120/PCM5120-Q1 and TLV320ADC6120/PCM6120-Q1 devices are dual-channel, high-performance, audio analog-to-digital converters that have an extensive set of features that includes the following:

- Programmable Gain Amplifier (PGA)
- Digital volume control
- A programmable microphone bias voltage
- A phase-locked loop (PLL)
- A programmable high pass filter (HPF)
- Automatic Gain Control (AGC)
- Dynamic Range Enhancer (DRE)
- Dynamic Range Compressor (DRC)
- Linear phase or low-latency filter modes for sample rates up-to 768 kHz

This application note describes how to configure the dynamic range enhancer (DRE) and dynamic range compressor (DRC) feature in TLV320ADC5120/PCM5120-Q1 and TLV320ADC6120/PCM6120-Q1 devices.

Table of Contents

List of Figures

List of Tables

Trademarks

All trademarks are the property of their respective owners.

1 Introduction

TLV320ADC5120/PCM5120-Q1 and TLV320AD6120/PCM6120-Q1 devices from TI's Audio ADC portfolio features an algorithm called Dynamic Range Enhancer (DRE) that can be used to improve the far-field recording performance by improving the dynamic range of the ADC channel at low signal levels. The DRE is a digitally-assisted algorithm that dynamically adjusts the front-end programmable gain amplifier (PGA) to improve the signal-to-noise ratio of low-level signals while preventing high-level signals from saturating the PGA and ADC. Far-field recording performance can also be improved by using a high PGA gain, but it can degrade near-field recording performance since a dynamic change to high-input levels combined with a high fixed-gain PGA can saturate the PGA and ADC. The DRE provides the ability to improve the far-field recording performance without degrading the near-field recording performance. Figure 1-1 shows the improvements in channel performance with DRE. With DRE, the ADC channel performance is not limited by the ADC noise floor and improves the recording performance even for signals below the noise floor of the ADC. Every 6 dB improvement in dynamic range increases the far-field recording distance by a factor of two.

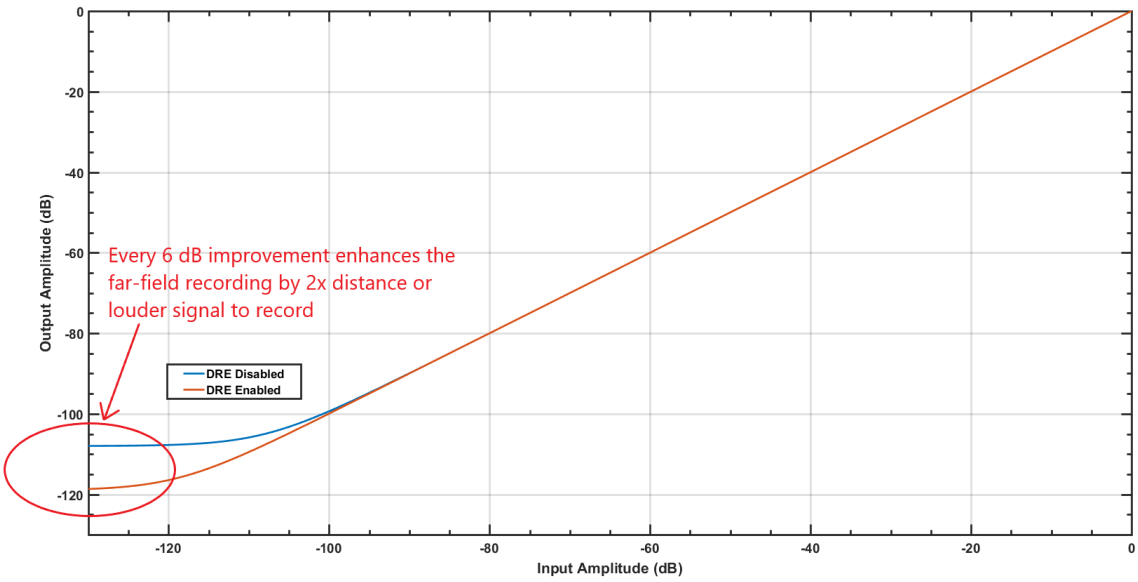

Figure 1-1. DRE Performance

Dynamic Range Compression (DRC) is an algorithm that dynamically adjusts the PGA gain of the ADC channel to expand the signal level over a region of the audio range. A typical example application for DRC occurs while recording speech signals when the speaker is changing his or her distance from the microphone while speaking. Sound pressure levels at the microphone vary inversely with distance to the sound source. Therefore, microphone output levels are weak for the farther sound sources. Without DRC and just a fixed-gain PGA, output levels vary from soft to loud as the person moves closer to the microphone. With DRC enabled, the input level variation below a certain threshold can be maintained at a constant level. Hence, the speech signals which are below a certain threshold are gained up to maintain a constant output so that the weaker speech signals can be recorded properly. Thus, DRC automatically responds to changes in the input signal below a certain threshold to maintain a fixed level to meet target application requirements. Figure 2 shows output vs input plot when the DRC disabled as well as enabled.

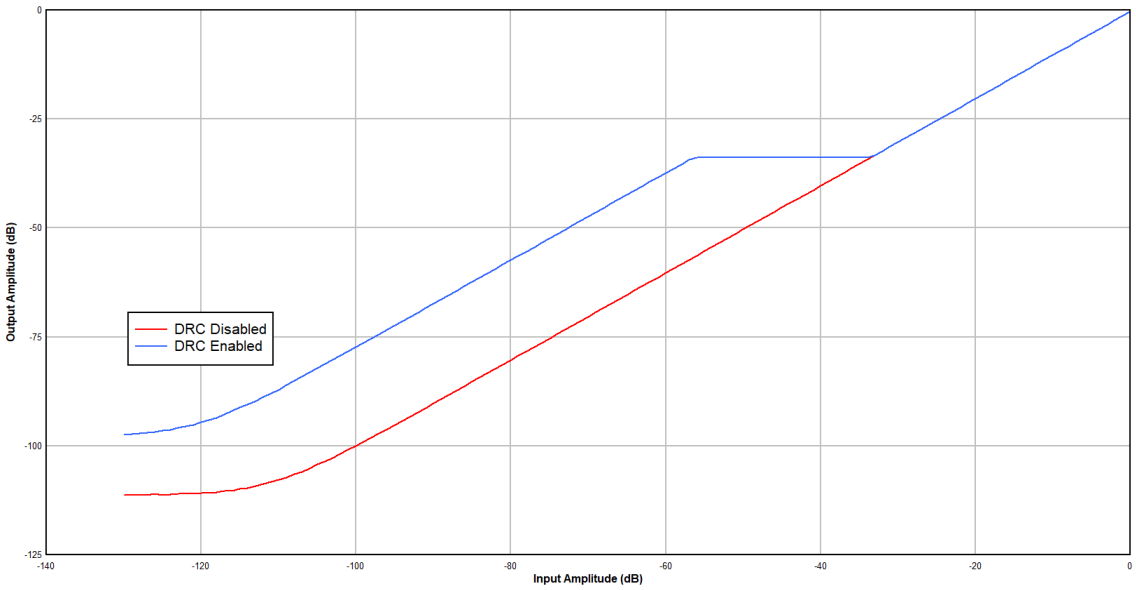

Figure 1-2. DRC Performance

DRE and DRC is supported on all ADC channels of TLV320ADC5120/PCM5120-Q1 and TLV320ADC6120/PCM6120-Q1 devices. This application note describes the operation of the DRE and DRC, the tunable parameters, and the device configurations required to use DRE/DRC.

2 Dynamic Range Enhancer

Figure 2-1 shows the signal processing chain for TLV320ADC5120/PCM5120-Q1 and TLV320ADC6120/PCM6120-Q1 devices. The dynamic range performance of the front-end PGA in TLV320ADC5120/PCM5120-Q1 and TLV320ADC6120/PCM6120-Q1 devices are 120 dB and 122 dB respectively. The subsequent delta-sigma ADC has 108 dB dynamic range for the TLV320ADC5120 /PCM3120-Q1 and 113 dB dynamic range for the TLV320ADC6120/PCM6120-Q1 .Without the DRE, the ultra-low noise performance of the PGA is limited by the ADC performance and the overall channel dynamic range is determined by the dynamic range of the ADC. With the DRE, the overall channel dynamic range can be improved beyond the dynamic range of the ADC and is limited more by the dynamic range of the PGA.

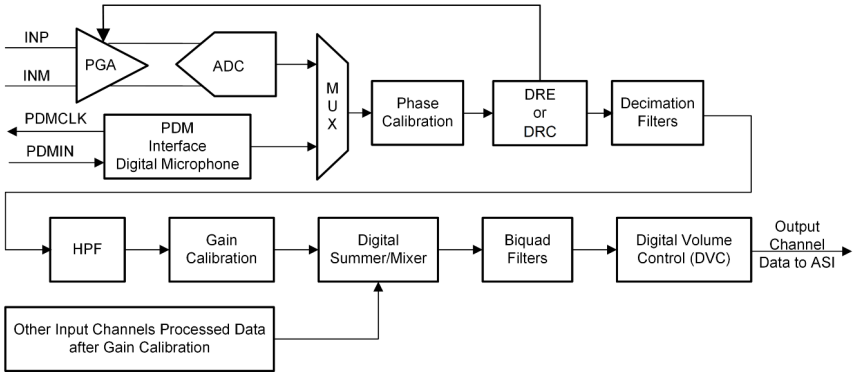

Figure 2-1. Signal Processing Block Diagram

The DRE algorithm monitors the input signal and increases the gain of the analog PGA for signal levels below a threshold. At the same time, the DRE algorithm creates a corresponding reciprocal attenuation in the digital circuits so the net effect of the analog PGA gain and digital attenuation cancel each other out. Thus the DRE improves the dynamic range without increasing the overall channel gain. The DRE does not gain signals above the threshold. Boosting the low-level signals in analog keeps the input to the ADC significantly above its noise floor and thus prevents the ADC performance from being the limiting factor. Subsequent processing is done using a high-performance, 32-bit, digital signal processor with very low quantization noise, and, therefore, the PGA performance becomes the limiting factor in the overall channel performance. TLV320ADC5120 /PCM5120-Q1 and TLV320ADC6120/PCM6120-Q1 devices support up to four analog input channels. All analog input channels support DRE. The devices support differential or single-ended signals from an analog microphone source or auxiliary line input. The analog microphone inputs support electret condenser and microelectrical-mechanical (MEMS) microphones. Even though the devices also support digital pulse density modulated (PDM) digital microphones, the DRE/DRC does not support the digital channels as the analog gain of the digital microphone cannot be controlled. The TLV320ADCx120/PCMx120-Q1 family of devices also support an automatic gain control (AGC) algorithm on the analog channels to maintain a constant nominal output level. AGC, DRE and DRC algorithms cannot be used simultaneously since all these algorithms control the PGA. DRE or AGC selection is done using AGC_DRE_SEL field of DSP_CFG1 register (page = 0x00, address = 0x6C) as shown inTable 2-1.

Table 2-1. DRE Selection Using DSP_CFG1 Register

BIT	FIELD	TYPE	RESET	DESCRIPTION
3	DRE_AGC_SEL	R/W	0h	DRE or DRE selection when is enabled for any channel. 0d = DRE is selected. 1d = DRE is selected.

3 Dynamic Range Compressor

The DRC algorithm is a mixed-signal solution, where the analog programmable gain amplifier (PGA) of a channel is controlled by a closed-loop control digital algorithm. Figure 2-1 shows the signal processing chain for the device. To respond to changes in the input signal, the DRC algorithm monitors the digitized signal from the ADC and adjusts the PGA to maintain a constant target level below a certain threshold. If the signal is below the threshold level, the DRC increases the PGA gain. If the signal is above the threshold level, the DRC keeps the default PGA gain. Using the analog circuitry of the PGA to change the input signal provides optimal noise performance, since it avoids gain adjustments in the digital circuitry that increases the quantization noise. Moreover, the DRC algorithm uses a small step size during PGA changes to reduce distortions in the input signal. As shown in DRC Selection Using DSP_CFG1 Register, DRC selection is done using the DRE_AGC_SEL and DRC_EN bits of DSP_CFG1 register (page = 0x00, address = 0x6C).

Table 3-1. DRC Selection Using DSP_CFG1 Register

BIT	FIELD	TYPE	RESET	DESCRIPTION
3	DRE_AGC_SEL	R/W	0b	DRE or DRE selection when is enabled for any channel. 0d = DRE is selected. 1d = DRE is selected.
1	DRC_EN	R/W	0b	Dynamic range compression (DRC) same as DRE without gain compesnation in digital 0d = DRC disabled. Device can be in DRE or AGC mode depending on DRE_AGC_SEL bit. 1d = DRC enabled. Device cannot be in DRE or AGC mode.

DRE/DRC can be independently enabled or disabled for each channel using the following register bits:

- CH1_DREEN (P0_R60_D0)
- CH2_DREEN (P0_R65_D0)
- CH3_DREEN (P0_R70_D0)
- CH4_DREEN (P0_R75_D0)

4 PGA Anti-Saturation

The DRE and DRC algorithms have a feature to prevent saturation of the PGA for bounded input signals. The input signal level is compressed to avoid clipping when channel gain (PGA gain) is greater than 0 dB. This feature can be enabled using the EN_AVOID_CLIP bit of DSP_CFG1 register (page = 0x00, address = 0x6C).

Table 4-1. PGA Anti-Saturation Selection Using DSP_CFG1 Register

BIT	FIELD	TYPE	RESET	DESCRIPTION
0	EN_AVOID_CLIP	R/W	0b	Anti clippler when channel gain > 0 dB and either of DRE, DRC or AGC mode enabled. 0d = Channel gain is maintained as per user programmed value. 1d = Signal level is compressed to avoid clipping when channel gain > 0 dB and signal level crosses programmed threshold setting set in page-4.

A typical example application for PGA anti-saturation feature occurs when some constant analog programmable gain (C0 dB) is configured along with DRE or DRC. Increasing the input signal level beyond a certain level (-C0 dB) causes the output of the PGA to saturate which is detrimental to the performance of the analog circuitry. With PGA anti-saturation feature enabled, the PGA output does not saturate even if input signal level increases beyond – C0 dB level because the PGA gain is reduced and the residual gain is applied on the digital side. The overall channel gain remains unchanged.

5 High Pass Filter

To remove any DC offset that leads to incorrect input level estimates, the DRE/DRC algorithm processes the input signal through a high-pass filter (HPF). This HPF is exclusive to the DRE/DRC and is different from the second-order HPF filters used by the decimation filters.

The transfer function implemented by the HPF is given by Equation 1.

$$H(z) = \frac{N0 + N1 \times z^{-1}}{1 + D1 \times z^{-1}} \quad (1)$$

The HPF is a first order filter implemented using three coefficients: DRE_HPF_B0, DRE_HPF_B1, and DRE_HPF_A1. The transfer function parameters (N0, N1, and D1) are converted to coefficients using Equation 2, Equation 3, and Equation 4.

$$DRE\_HPF\_BO = round(2^8 * N0) \quad (2)$$

$$DRE\_HPF\_B1 = round(2^8 * N1) \quad (3)$$

$$DRE\_HPF\_A1 = round(2^8 * D1) \quad (4)$$

These coefficients are user-programmable to set a different cutoff frequency from the default cutoff (3 dB point) frequency of 10 Hz for a 48 kHz operation. Increasing the cutoff frequency results in faster settling of signal-level estimates. Decreasing the cutoff frequency improves the accuracy of the signal-level estimate. The default filter coefficients provide a good balance between speed and accuracy and are suitable for most applications. Table 5-1 shows the coefficient registers of the HPF. The coefficients are represented in 2s-complement, 32-bit format.

Table 5-1. Programmable Registers for High Pass Filter Coefficients

COEFFICIENT	PAGE	REGISTER	RESET VALUE	DESCRIPTION
DRE_HPF_B0	0x06	0x6C	0x7F	DRE_HPF_B0 Byte[31:24]
	0x06	0x6D	0xFF	DRE_HPF_B0 Byte[23:16]
	0x06	0x6E	0xFF	DRE_HPF_B0 Byte[15:8]
	0x06	0x6F	0xFF	DRE_HPF_B0 Byte[7:0]
DRE_HPF_B1	0x06	0x70	0x80	DRE_HPF_B1 Byte[31:24]
	0x06	0x71	0x00	DRE_HPF_B1 Byte[23:16]
	0x06	0x72	0x00	DRE_HPF_B1 Byte[15:8]
	0x06	0x73	0x01	DRE_HPF_B1 Byte[7:0]
DRE_HPF_A1	0x06	0x74	0x7E	DRE_HPF_A1 Byte[31:24]
	0x06	0x75	0xEE	DRE_HPF_A1 Byte[23:16]
	0x06	0x76	0xD8	DRE_HPF_A1 Byte[15:8]
	0x06	0x77	0xE2	DRE_HPF_A1 Byte[7:0]

6 DRE/DRC Parameters

Table 6-1 show the parameters of the DRE/DRC algorithm. Two of the parameters are controlled by writing to the device registers. The other parameters reside in the 32-bits wide coefficient memory (Book 0, Page 5, Page 6, and Page 7) of the device. During warm boot device takes the default values for the parameters in Book 0: page 5, page 6 and page 7, for overriding these parameters with the user values we need to set the bit *DRE_AGC_CFG_DEF_OVR = 1* in DSP_CFG1 register (P0_R108_D2).

Table 6-1. List of DRE Parameters

DRE PARAMETER	FUNCTION/DESCRIPTION
DRE/DRC threshold (dB)	The signal level above which the DRE/DRC is inactive.
Maximum Gain (dB)	Upper limit of gain applied by DRE/DRC.
Release Time Constant (seconds)	How fast the DRE/DRC circuitry responds with a PGA gain increase when the input signal falls below DRE/DRC threshold.
Attack Time Constant (seconds)	How fast the DRE/DRC circuitry responds with a PGA gain decrease when the input signal rises above DRE/DRC threshold.
Release Hysteresis (dB)	Amount of signal-level decrease in dB past the DRE/DRC threshold that forces the DRE/DRC to increase gain and start a release.
Attack Hysteresis (dB)	Amount of signal-level increase in dB past the DRE/DRC threshold that forces the DRE/DRC to decrease gain and start an attack.
Release Debounce (samples)	The number of consecutive input samples that falls below the DRE threshold after an attack event before the DRE/DRC starts a release and increases the PGA gain.
Attack Debounce (samples)	The number of consecutive input samples that rises above the DRE threshold after a release event before the DRE/DRC starts an attack and decreases the PGA gain.

DRE/DRC threshold: The signal level above which the DRE/DRC stops modifying the PGA and sets it to unity gain. The threshold level is expressed relative to full scale (dBFS) of the ADC output. Table 6-2 lists the DRE/DRC threshold configuration settings. The default is -54 dB. Setting a high threshold level reduces the headroom available for the DRE/DRC to react when there is a sudden increase in the signal level and can result in digital clipping and PGA saturation. Therefore, the DRE/DRC threshold has to be set with enough margin to prevent clipping with large dynamic changes in input levels.

Table 6-2. DRE/DRC Trigger Threshold Level Programmable Settings

P0_R109_D[7:4] : DRE_LVL[3:0]	DRE TRIGGER THRESHOLD LEVEL
0000	The DRE/DRC target threshold is the –12 dB output signal level.
0001	The DRE/DRC target threshold is the –18 dB output signal level.
0010	The DRE/DRC target threshold is the –24 dB output signal level.
…	…
0111 (default)	The DRE/DRC target threshold is the –54 dB output signal level.
…	…
1001	The DRE/DRC target threshold is the –66 dB output signal level.
1010 to 1111	Reserved (do no use these settings)

Maximum Gain: The maximum gain represents the upper limit of gain applied by the DRE/DRC for signals below the DRE/DRC threshold. Table 6-3 lists the Maximum Gain configuration settings. The default value is 24 dB. It can be programmed from 2 dB to 30 dB with steps of 2 dB.

Table 6-3. DRE/DRC Maximum Gain Programmable Settings

P0_R109_D[3:0] : DRE_MAXGAIN[3:0]	DRE/DRC MAXIMUM GAIN ALLOWED
0000	The DRE/DRC maximum gain allowed is 2 dB.
0001	The DRE/DRC maximum gain allowed is 4 dB.
0010	The DRE/DRC maximum gain allowed is 6 dB.
…	…
1011 (default)	The DRE/DRC maximum gain allowed is 24 dB.
…	…

Table 6-3. DRE/DRC Maximum Gain Programmable Settings (continued)

P0_R109_D[3:0] : DRE_MAXGAIN[3:0]	DRE/DRC MAXIMUM GAIN ALLOWED
1110	The DRE/DRC maximum gain allowed is 30 dB.
1111	Reserved (do not use this setting)

Release Time Constant: How fast the DRE/DRC circuitry increases the PGA gain when the input signal falls below the DRE/DRC threshold. The Release Time Constant is controlled by two coefficients:DRE_REL_ALPHA and DRE_REL_BETA. Equation 5 and Equation 6 show how to compute the DRE_REL_ALPHA and DRE_REL_BETA parameters from the following time constant.

$$DRE\_REL\_ALPHA = round(2^{31} * e^{-ln(9) / 48000*RT}) \quad (5)$$

$$DRE\_REL\_BETA = (2^{31} - round(2^{31} * e^{-ln(9) / 48000*RT}) \quad (6)$$

where

- RT is the Release Time Constant in seconds
- FSYNC is the sample rate of the ADC in Hz

Table 6-4 shows the registers that control the DRE_REL_ALPHA and DRE_REL_BETA parameters. Theses parameters are each 32-bits wide, and have to be written in 2s-complement representation. The default values for DRE_REL_ALPHA and DRE_REL_BETA corresponds to a time constant of 20 milliseconds.

Table 6-4. Programmable Registers for Release Time Constant Parameter

COEFFICIENT	PAGE	REGISTER	RESET VALUE	DESCRIPTION
DRE_REL_ALPHA	0x05	0x7C	0x7F	DRE_REL_ALPHA Byte[31:24]
	0x05	0x7D	0xB5	DRE_REL_ALPHA Byte[23:16]
	0x05	0x7E	0x16	DRE_REL_ALPHA Byte[15:8]
	0x05	0x7F	0x50	DRE_REL_ALPHA Byte[7:0]
DRE_REL_BETA	0x06	0x08	0x00	DRE_REL_BETA Byte[31:24]
	0x06	0x09	0x4A	DRE_REL_BETA Byte[23:16]
	0x06	0x0A	0xE9	DRE_REL_BETA Byte[15:8]
	0x06	0x0B	0xB0	DRE_REL_BETA Byte[7:0]

Attack Time Constant: How fast the DRE/DRC circuitry decreases the PGA gain when input signal rises above the DRE/DRC threshold. The Attack Time Constant is controlled by two coefficients: DRE_ATT_ALPHA and DRE_ATT_BETA. Equation 7 and Equation 8 show how to compute the DRE_ATT_ALPHA and DRE_ATT_BETA parameters from the following time constant.

$$DRE\_ATT\_ALPHA = round(2^{31} * e^{-ln(9) / 48000*AT}) \quad (7)$$

$$DRE\_ATT\_BETA = (2^{31} - round(2^{31} * e^{-ln(9) / 48000*AT}) \quad (8)$$

where

- AT is the Attack Time Constant in seconds
- FSYNC is the sample rate of the ADC in Hz

DRE_ATT_ALPHA and DRE_ATT_BETA coefficients are each 32-bits wide, 2s-complement representations. Table 6-5 shows the registers that control DRE_ATT_ALPHA and DRE_ATT_BETA parameters. The default values for DRE_ATT_ALPHA and DRE_ATT_BETA corresponds to a time constant of 0.1 milliseconds.

Table 6-5. Programmable Registers for Attack Time Constant Parameter

COEFFICIENT	PAGE	REGISTER	RESET VALUE	DESCRIPTION
DRE_ATT_ALPHA	0x06	0x0C	0x50	DRE_ATT_ALPHA Byte[31:24]
	0x06	0x0D	0xFC	DRE_ATT_ALPHA Byte[23:16]
	0x06	0x0E	0x64	DRE_ATT_ALPHA Byte[15:8]
	0x06	0x0F	0x5C	DRE_ATT_ALPHA Byte[7:0]
DRE_ATT_BETA	0x06	0x10	0x2F	DRE_ATT_BETA Byte[31:24]
	0x06	0x11	0x03	DRE_ATT_BETA Byte[23:16]
	0x06	0x12	0x9B	DRE_ATT_BETA Byte[15:8]
	0x06	0x13	0xA4	DRE_ATT_BETA Byte[7:0]

Release Hysteresis: Amount of signal-level decrease past the DRE/DRC threshold that forces the DRE/DRC to increase gain and start a release. Release Hysteresis is specified in dB. Equation 9 shows the computation of the DRE_REL_HYST parameter.

$$DRE\_REL\_HYST = round(2^8 * RH) \quad (9)$$

where

- RH (>= 0) is the Release Hysteresis in dB

The default value of DRE_REL_HYST is 0x00000300, which corresponds to a hysteresis of 3 dB. Table 6-6 shows the registers that control the DRE_REL_HYST parameter.

Table 6-6. Programmable Registers for Release Hysteresis Parameter

COEFFICIENT	PAGE	REGISTER	RESET VALUE	DESCRIPTION
DRE_REL_HYST	0x06	0x34	0x00	DRE_REL_HYST Byte[31:24]
	0x06	0x35	0x00	DRE_REL_HYST Byte[23:16]
	0x06	0x36	0x03	DRE_REL_HYST Byte[15:8]
	0x06	0x37	0x00	DRE_REL_HYST Byte[7:0]

Attack Hysteresis: Amount of signal-level increase past DRE threshold that forces the DRE/DRC to decrease the gain and start an attack. Equation 10 shows the computation of the DRE_ATT_HYST parameter.

$$DRE\_ATT\_HYST = round(2^8 * AH) \quad (10)$$

where

- AH (>= 0) is the Attack Hysteresis in dB

The default value of Attack Hysteresis is 1 dB. The default can be changed by writing to the registers listed in Table 6-7.

Table 6-7. Programmable Registers for Attack Hysteresis Parameter

COEFFICIENT	PAGE	REGISTER	RESET VALUE	DESCRIPTION
DRE_ATT_HYST	0x06	0x3C	0x00	DRE_ATT_HYST Byte[31:24]
	0x06	0x3D	0x00	DRE_ATT_HYST Byte[23:16]
	0x06	0x3E	0x01	DRE_ATT_HYST Byte[15:8]
	0x06	0x3F	0x00	DRE_ATT_HYST Byte[7:0]

Attack Debounce: The number of consecutive input samples that rises above the DRE/DRC threshold after a release event before the DRE/DRC starts attack and decreases the PGA. The default value of this parameter is 2 samples at 48 kHz (0.01 milliseconds). Equation 11 shows the computation of DRE_ATT_CNT parameter.

$$DRE\_ATT\_CNT = round(2^8 * FSYNC * AD) \quad (11)$$

where

- AD (>= 0) is specified in seconds
- FSYNC is the sample rate of the ADC in Hz

Table 6-8 shows the registers controlling the DRE_ATT_CNT parameter.

Table 6-8. Programmable Registers for Attack Debounce Parameter

COEFFICIENT	PAGE	REGISTER	RESET VALUE	DESCRIPTION
DRE_ATT_CNT	0x06	0x18	0x00	DRE_ATT_CNT Byte[31:24]
	0x06	0x19	0x00	DRE_ATT_CNT Byte[23:16]
	0x06	0x1A	0x02	DRE_ATT_CNT Byte[15:8]
	0x06	0x1B	0x00	DRE_ATT_CNT Byte[7:0]

Release Debounce: The number of consecutive input samples that falls below DRE/DRC threshold after an attack event before the DRE/DRC starts releasing and increasing the PGA. The default value of Release Debounce is 25 milliseconds at 48 kHz. Equation 12 shows the computation of the DRE_REL_CNT parameter.

$$DRE\_REL\_CNT = round(2^8 * FSYNC * RD) \quad (12)$$

where

- RD (>= 0) is the Release Debounce specified in seconds
- FSYNC is the sample rate of the ADC in Hz

Table 6-9 lists the registers controlling the DRE_REL_CNT parameter.

Table 6-9. Programmable Registers for Release Debounce Parameter

COEFFICIENT	PAGE	REGISTER	RESET VALUE	DESCRIPTION
DRE_REL_CNT	0x06	0x1C	0x00	DRE_REL_CNT Byte[31:24]
	0x06	0x1D	0x04	DRE_REL_CNT Byte[23:16]
	0x06	0x1E	0xB0	DRE_REL_CNT Byte[15:8]
	0x06	0x1F	0x00	DRE_REL_CNT Byte[7:0]

7 Sample Rate Support

The DRE/DRC algorithm does not support all sampling rates and all channel combinations. Table 7-1 shows the sample rates and the corresponding number of channels supported at that sample rate by the DRE/DRC algorithm. For sample rates from 16 or 14.7 kHz to 96 or 88.2 kHz, the DRE/DRC algorithm supports all two analog channels. At a 192 or 176.4 kHz sample rate, DRE/DRC is restricted to just one channel.

Table 7-1. Sample Rates Supported by DRE Algorithm

SAMPLE RATE (kHz)	NUMBER OF CHANNELS
16/14.7	2
24/22.05	2
32/29.4	2
48/44.1	2
96/88.2	2
192/176.4	1

8 Example

The DRE default parameters work well for most applications. The default DRE trigger threshold is -54 dB. This provides sufficient headroom for the DRE to react in a timely manner to a sudden loud signal. Increasing the DRE trigger threshold improves the small-signal performance, but it decreases the headroom available before switching to an attack cycle. This can be mitigated by decreasing the attack time. This section shows an example where a higher DRE trigger threshold is set and time constants adjusted to make the DRE respond faster.

- Target Level = -54 dB
- Maximum Gain = 24 dB
- Attack Time = 0.01 ms
- Release Time = 20 ms
- Attack Hold = 0.0417 ms
- Release Hold = 20 ms
- Attack Hysteresis = 1 dB
- Release Hysteresis = 3 dB

```
# Key: w 9C XX YY ==> write to I2C address 0x9c, to register 0xXX, data 0xYY
#               # ==> comment delimiter
#
# The following list gives an example sequence of items that must be executed in the time
# between powering the device up and reading data from the device. Note that there are
# other valid sequences depending on which features are used.
#
# See the corresponding EVM user guide for jumper settings and audio connections.
#
# Differential 2-channel : INP1/INM1 - Ch1, INP2/INM2 - Ch2
# FSYNC = 48 kHz (Output Data Sample Rate), BCLK = 11.2896 MHz (BCLK/FSYNC = 256)
################################################################
#
#
# Power up IOVDD and AVDD power supplies
# Wait for IOVDD and AVDD power supplies to settle to steady state operating voltage range.
# Wait for 1ms.
#
w 9C 00 00 # Goto Page 0
w 9C 02 81 # Exit Sleep mode
d 10       # Wait for 16 ms
w 9C 01 01 # Reset
w 9C 6C 44 # Enable DRE in DSP_CFG1 and Override DRE parameters with user values
w 9C 3C 01 # Select DRE on Ch. 1 using CH1_CFG0
w 9C 41 01 # Select DRE on Ch. 2 using CH2_CFG0
w 9C 6D 4B # DRE LVL = -36 dB, DRE GAIN = 24 dB
w 9C 00 05          # Goto Page 5
w 9C 7C 7F B5 16 50 # DRE Release Time Alpha
w 9C 00 05          # Goto Page 6
w 9C 08 00 4A E9 B0 # DRE Release Time Beta
w 9C 0C 01 50 DB 39 # DRE Attack Time Alpha
w 9C 10 7E B5 16 50 # DRE Attack Time Beta
w 9C 18 00 00 02 00 # DRE Attack Debounce
w 9C 1C 00 04 B0 00 # DRE Release Debounce
w 9C 3C 00 00 01 00 # DRE Attack Hysteresis
w 9C 34 00 00 03 00 # DRE Release Hysteresis

w 9C 00 00 # Goto Page 0
w 9C 07 30 # TDM Mode with 32 Bits/Channel
w 9C 73 c0 # Enable Ch.1 - Ch.2
w 9C 74 f0 # Enable ASI Output channels
w 9C 75 e0 # Power up ADC
```

To enable the DRC algorithm instead of DRE algorithm with the same parameter set as above, set DSP_CFG1 (Page 0, Register 0x6c) with a value 0x46 (instead of 0x44 for DRE).

9 References

For related documentation see the following:

- TLV320ADC6120
  - Texas Instruments, *TLV320ADC6120 2-Channel, 768-kHz, Burr-Brown™ Audio ADC* data sheet.
  - Texas Instruments, *TLV320ADC6120 stereo-channel, 768-kHz, Burr-Brown™ audio ADC with 106-dB SNR evaluation module*.
- TLV320ADC5120
  - Texas Instruments, *TLV320ADC5120 2-Channel, 768-kHz, Burr-Brown™ Audio ADC* data sheet.
  - Texas Instruments, *TLV320ADC5120 stereo-channel, 768-kHz, Burr-Brown™ audio ADC with 106-dB SNR evaluation module*.
- TLV320ADC3120
  - Texas Instruments, *TLV320ADC3120 2-Channel, 768-kHz, Burr-Brown™ Audio ADC* data sheet.
  - Texas Instruments, *TLV320ADC3120 stereo-channel, 768-kHz, Burr-Brown™ audio ADC with 106-dB SNR evaluation module*
- Texas Instruments, *ADCx120EVM-PDK User's Guide*
- Texas Instruments, *PurePath™ Console*
- Texas Instruments, *PCM6120-Q1 2-Channel, 768-kHz, Burr-Brown™ Audio ADC* data sheet.
- Texas Instruments, *PCM5120-Q1 2-Channel, 768-kHz, Burr-Brown™ Audio ADC* data sheet.
- Texas Instruments, *PCM3120-Q1 2-Channel, 768-kHz, Burr-Brown™ Audio ADC* data sheet.

10 Revision History

Changes from Revision * (November 2021) to Revision A (April 2022)	Page
• Added PCM5120-Q1 and PCM6120-Q1 throughout the publication	1

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265