Functional Safety Information

ADS7142-Q1
Functional Safety FIT Rate, FMD and Pin FMA

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Trademarks

1 Overview

This document contains information for ADS7142-Q1 (WSON package) to aid in a functional safety system design. Information provided are:

- Functional Safety Failure In Time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and their distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (Pin FMA)

Figure 1-1 shows the device functional block diagram for reference.

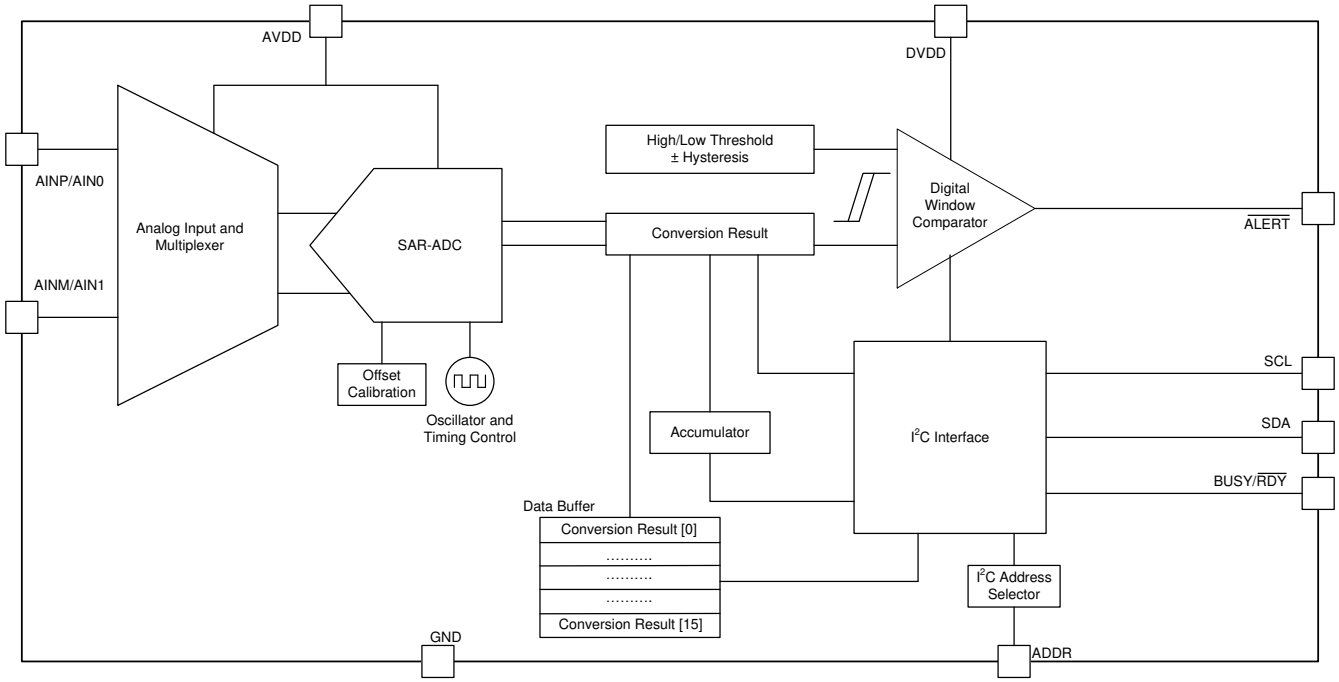

Figure 1-1. Functional Block Diagram

ADS7142-Q1 was developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

2 Functional Safety Failure In Time (FIT) Rates

This section provides Functional Safety Failure In Time (FIT) rates for ADS7142-Q1 based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total Component FIT Rate	5
Die FIT Rate	2
Package FIT Rate	3

The failure rate and mission profile information in Table 2-1 comes from the Reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission Profile: Motor Control from Table 11
- Power dissipation: 3.6 mW
- Climate type: World-wide Table 8
- Package factor (lambda 3): Table 17b
- Substrate Material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS, BICMOS Digital, analog / mixed	60 FIT	70°C

The Reference FIT Rate and Reference Virtual T_J (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for ADS7142-Q1 in Table 3-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures due to misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
Incorrect channel selected	10%
Channel-channel short	10%
ADC output code bit error	15%
ADC gain error out of specification	20%
ADC offset error out of specification	20%
Communication error	20%
Digital Window Comparator/$\overline{\text{ALERT}}$ output fails to trip or false trip	5%

4 Pin Failure Mode Analysis (Pin FMA)

This section provides a Failure Mode Analysis (FMA) for the pins of the ADS7142-Q1. The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to Ground (see Table 4-2)
- Pin open-circuited (see Table 4-3)
- Pin short-circuited to an adjacent pin (see Table 4-4)
- Pin short-circuited to supply (see Table 4-5)

Table 4-2 through Table 4-5 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1.

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality
B	No device damage, but loss of functionality
C	No device damage, but performance degradation
D	No device damage, no impact to functionality or performance

Figure 4-1 shows the ADS7142-Q1 pin diagram. For a detailed description of the device pins please refer to the *Pin Configuration and Functions* section in the ADS7142-Q1 data sheet.

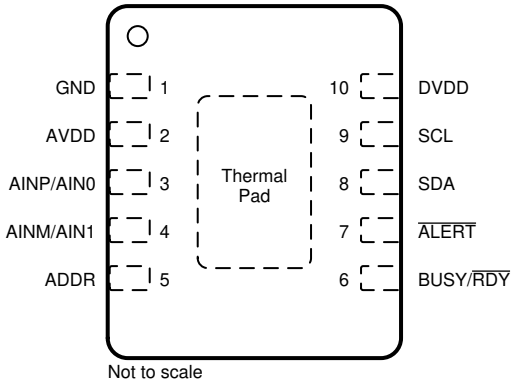

Figure 4-1. Pin Diagram

Following are the assumptions of use and the device configuration assumed for the pin FMA in this section:

- AVDD and DVDD use the same supply voltage.
- Short circuit to Power means short to AVDD = DVDD.
- RC filters on every analog input, AINx. Series resistors are sized to limit the input currents into the analog inputs to < 10 mA in all circumstances, including when the device is unpowered and an input signal is applied.
- Device is the only slave on the I^2C bus.
- The device thermal pad is connected to Ground.

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
GND	1	No effect. Normal operation.	D
AVDD	2	Device not powered up because AVDD = GND. Observe that the absolute maximum ratings for all pins of the device are met, otherwise device damage may be plausible.	A
AINP/AIN0	3	Single-ended configuration: Conversion result for AIN0 will be close to 0x000.	B
		Pseudo-differential configuration: Conversion result will be close to 0x000.	B
AINM/AIN1	4	Single-ended configuration: Conversion result for AIN1 will be close to 0x000.	B
		Pseudo-differential configuration: Conversion result will be incorrect as AINM voltage is out of range. Conversion result will be lower than expected by a factor of AVDD/2; ADC accuracy will be lower.	B
ADDR	5	I^2C address will be 0x18. If the device is supposed to be configured for a different I^2C address, then there will be no I^2C communication with device possible.	B
		I^2C address will be 0x18. If the device is supposed to be configured for I^2C address 0x18, then normal operation.	D
BUSY/$\overline{\text{RDY}}$	6	BUSY/$\overline{\text{RDY}}$ stuck low. No busy/data ready indication possible. Increase in supply current when BUSY/$\overline{\text{RDY}}$ tries to drive high. Device damage plausible if BUSY/$\overline{\text{RDY}}$ drives high for extended period of time.	A
$\overline{\text{ALERT}}$	7	$\overline{\text{ALERT}}$ stuck low. No alert indication possible. Other than that normal operation.	B
SDA	8	SDA stuck low. No I^2C communication with device possible.	B
SCL	9	SCL stuck low. No I^2C communication with device possible.	B
DVDD	10	Digital interface not powered up. No I^2C communication with device possible.	B
Thermal Pad	—	No effect. Normal operation.	D

Table 4-3. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
GND	1	Device functionality undetermined. Device may be unpowered or connect to ground internally through alternate pin ESD diode and power up.	B
AVDD	2	Device functionality undetermined. Device unpowered and not functional if all external analog pins are held low. Device may power up through internal ESD diodes to AVDD if voltages above the device's power-on reset threshold are present on any of the analog pins.	B
AINP/AIN0	3	Single-ended configuration: Conversion result for AIN0 will be undetermined.	B
		Pseudo-differential configuration: Conversion result will be undetermined.	B
AINM/AIN1	4	Single-ended configuration: Conversion result for AIN1 will be undetermined.	B
		Pseudo-differential configuration: Conversion result will be undetermined.	B
ADDR	5	I^2C address will be 0x18. If the device is supposed to be configured for a different I^2C address, then there will be no I^2C communication with device possible.	B
		I^2C address will be 0x18. If the device is supposed to be configured for I^2C address 0x18, then normal operation.	D
BUSY/$\overline{\text{RDY}}$	6	No busy/data ready indication possible. Other than that normal operation.	B
$\overline{\text{ALERT}}$	7	No alert indication possible. Other than that normal operation.	B
SDA	8	No I^2C communication with device possible.	B
SCL	9	No I^2C communication with device possible.	B
DVDD	10	Digital interface not powered up if all external digital pins are held low. No I^2C communication with device possible. Digital interface may power up through internal ESD diodes to DVDD if voltages above the device's power-on reset threshold are present on any of the digital pins.	B
Thermal Pad	—	No effect. Normal operation.	D

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effect(s)	Failure Effect Class
GND	1	AVDD	Device not powered up because AVDD = GND. Observe that the absolute maximum ratings for all pins of the device are met, otherwise device damage may be plausible.	A
AVDD	2	AINP/AIN0	Single-ended configuration: Conversion result for AIN0 will be close to 0xFFF.	B
			Pseudo-differential configuration: Conversion result will be close to 0xFFF.	B
AINP/AIN0	3	AINM/AIN1	Single-ended configuration: Conversion result for AIN0 and AIN1 will be the same. Depending on the external circuits driving AIN0 and AIN1, the conversion result may be incorrect.	B
			Pseudo-differential configuration: Conversion result will be close to 0x000.	B
AINM/AIN1	4	ADDR	Single-ended configuration: Conversion result for AIN1 will depend on the voltage on ADDR pin. If AIN1 overdrives ADDR pin, the I^2C address may change. In that case no I^2C communication with device possible.	B
			Pseudo-differential configuration: Conversion result may be incorrect if the voltage on ADDR pin is not according to the analog input specification. If AIN1 overdrives ADDR pin, the I^2C address may change. In that case no I^2C communication with device possible.	B
ADDR	5	—	Not considered. Corner pin.	—
BUSY/$\overline{\text{RDY}}$	6	$\overline{\text{ALERT}}$	Busy/data ready and alert indication corrupted. Increase in supply current possible when BUSY/$\overline{\text{RDY}}$ (push-pull output) tries to drive high while $\overline{\text{ALERT}}$ (open drain output) drives low. Device damage plausible if this condition exists for extended period of time.	A
$\overline{\text{ALERT}}$	7	SDA	Digital window comparator is enabled: I^2C communication corrupted when $\overline{\text{ALERT}}$ pin asserted.	B
			Digital window comparator is disabled: Normal operation when $\overline{\text{ALERT}}$ pin is Hi-Z.	D
SDA	8	SCL	I^2C communication corrupted. No I^2C communication with device possible.	B
SCL	9	DVDD	No I^2C communication with device possible. Increase in supply current when SCL tries to drive low. Device damage plausible if SCL drives low for extended period of time.	A
DVDD	10	—	Not considered. Corner pin.	—
Thermal Pad	—	—	Refer to Short Circuit to Ground condition for respective device pins.	—

Table 4-5. Pin FMA for Device Pins Short-Circuited to supply

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
GND	1	Device not powered up because AVDD = GND. Observe that the absolute maximum ratings for all pins of the device are met, otherwise device damage may be plausible.	A
AVDD	2	No effect. Normal operation.	D
AINP/AIN0	3	Single-ended configuration: Conversion result for AIN0 will be close to 0xFFF.	B
		Pseudo-differential configuration: Conversion result will be close to 0xFFF.	B
AINM/AIN1	4	Single-ended configuration: Conversion result for AIN1 will be close to 0xFFF.	B
		Pseudo-differential configuration: Conversion result will be incorrect as AINM voltage is out of range. Conversion result will be higher than expected by a factor of AVDD/2; ADC accuracy will be lower.	B
ADDR	5	I^2C address will be 0x1F. If the device is supposed to be configured for a different I^2C address, then there will be no I^2C communication with device possible.	B
		I^2C address will be 0x1F. If the device is supposed to be configured for I^2C address 0x1F, then normal operation.	D
BUSY/$\overline{\text{RDY}}$	6	No busy/data ready indication possible. Increase in supply current when BUSY/$\overline{\text{RDY}}$ tries to drive low. Device damage plausible if BUSY/$\overline{\text{RDY}}$ drives low for extended period of time.	A
$\overline{\text{ALERT}}$	7	No alert indication possible. Increase in supply current when $\overline{\text{ALERT}}$ tries to drive low. Device damage plausible if $\overline{\text{ALERT}}$ drives low for extended period of time.	A
SDA	8	No I^2C communication with device not possible. Increase in supply current when SDA tries to drive low. Device damage plausible if SDA drives low for extended period of time.	A
SCL	9	No I^2C communication with device possible. Increase in supply current when SCL tries to drive low. Device damage plausible if SCL drives low for extended period of time.	A
DVDD	10	No effect. Normal operation.	D
Thermal Pad	—	Device unpowered. Device not functional. Observe that the absolute maximum ratings for all pins of the device are met, otherwise device damage may be plausible.	A

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Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265