Application Report

High Speed SAR ADC: Data Rate, Performance, and Pin Count Optimization

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ABSTRACT

Size, cost, and performance are key considerations for many high-speed (+ 10 MSPS) SAR ADC applications. Whether it is because of a size and or weight constrained environment, or an effort to reduce the cost of an existing design, there are a few ways to reduce board space and data rates while also improving performance in your application. Using the low latency 14-bit, 65 MSPS ADC3643, and 10 MSPS ADC3541, this application note outlines various methods for optimizing ADC component count, data rates, and performance.

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1 Introduction

High Speed SAR ADCs incorporate precision features (for example, excellent DC linearity and AC performance) while also allowing for sampling rates above 10 MSPS at ultra-low power consumption. With higher sampling speeds comes higher output data rates, so FPGA's are typically used to handle these higher speed CMOS and LVDS interfaces. However, there are trade-offs that can be made to reduce data rates and pin count while maintaining (or improving) the performance your application demands which can open the door for lower cost ADC data capture solutions (micro controllers and low cost FPGAs).

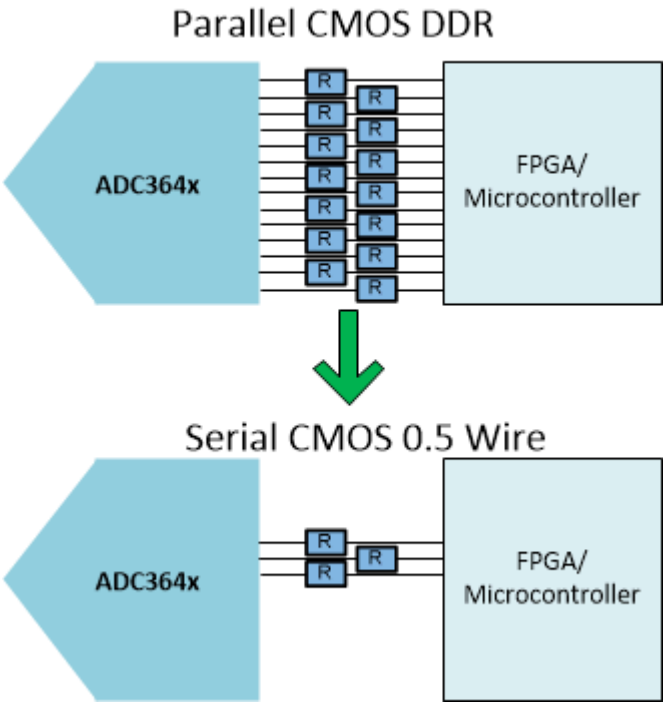

Figure 1-1. ADC3643 2CH CMOS Interfaces

2 Reduce Data Rates: Optimize Pin Count and Data Rate

The CMOS interface is very common for high-speed data converters, and we typically see a maximum rate of 250 Mbps for CMOS interface. While the ADC36XX family also offers LVDS output data (see ADC3683 and ADC3663), this section focuses primarily on the CMOS interface of the ADC3643 and ADC3541, and trade-offs to consider when optimizing your application.

The ADC3643 and ADC3541 can be configured in a parallel or serial CMOS mode. Both of these modes have unique features, so it is important to understand both accordingly.

2.1 Parallel CMOS

Parallel CMOS output is the most common method of implementation for high-speed CMOS ADCs. However, there are different Parallel CMOS implementations, like SDR (Single Data Rate) and DDR (Dual Data Rate), and both have implications on either data rate or pin count. Due to the nature of the CMOS output, a series resistance is needed to control the current output and ensure signal integrity, so reducing the number of output pins will correspondingly reduce the amount of series resistors.

2.1.1 Parallel SDR

In SDR mode, each data bit corresponds to one CMOS output pin on the ADC. For a 14-bit ADC, there will be 14 resistors at each output pin, and one resistor for the data clock (DCLK) for a total of 15 pins and or resistors.

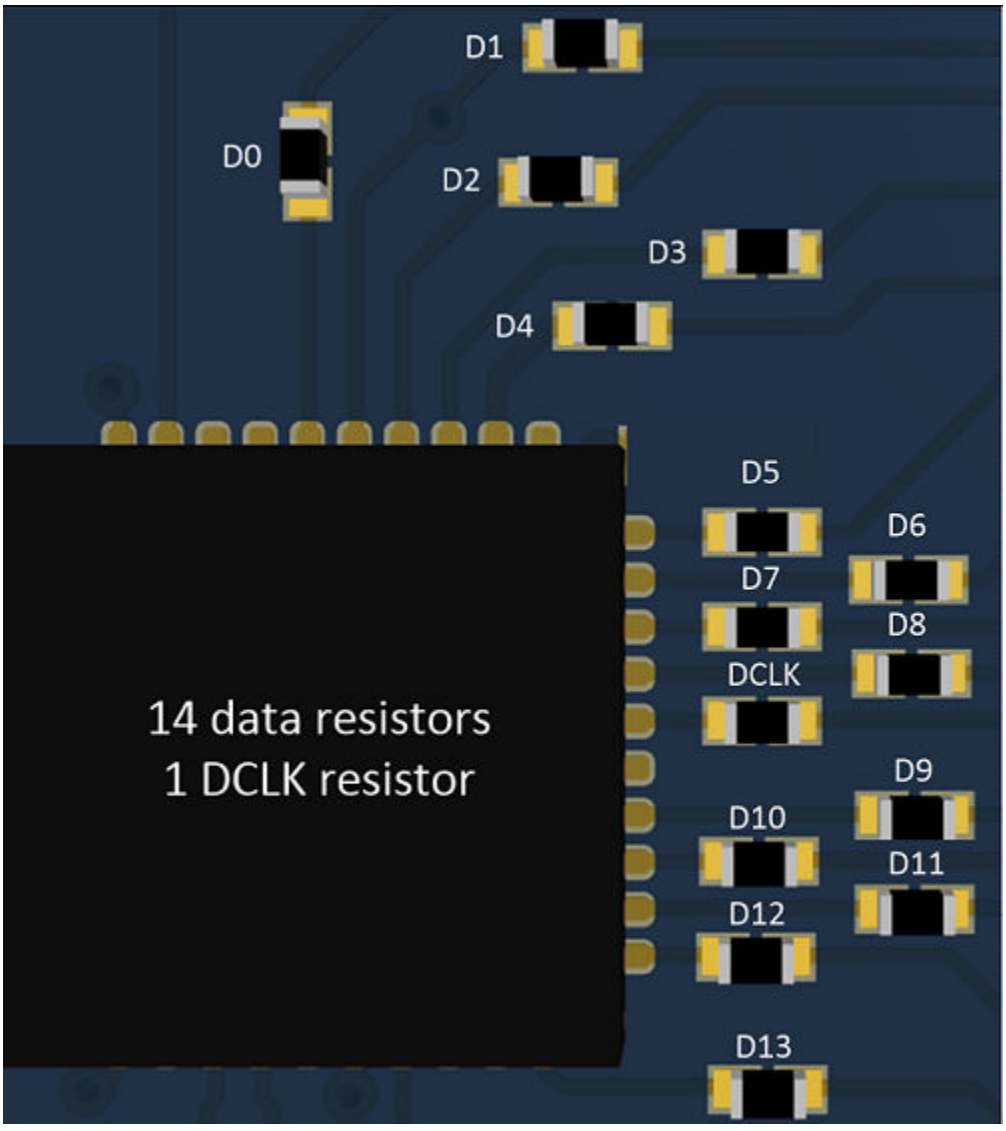

Figure 2-1. Parallel CMOS: 14 bit SDR Resistors

Also, the DCLK will latch the data on only the rising edge of the DCLK. This means that the data bits and the data clock are toggling at the same rate. For example, if the ADC3541 is sampling at 10 MSPS, the data bits and DCLK are toggling at a frequency of 10 MHz. This is actually the lowest data rate we can achieve without utilizing the on-chip digital decimation features 0f the ADC3541.

Table 2-1. Parallel SDR CMOS Mode

Parallel Interface	Max Sampling Rate (MSPS)	Data Rate (Mbps)	Data Pins/Resistors
SDR	65	65	15

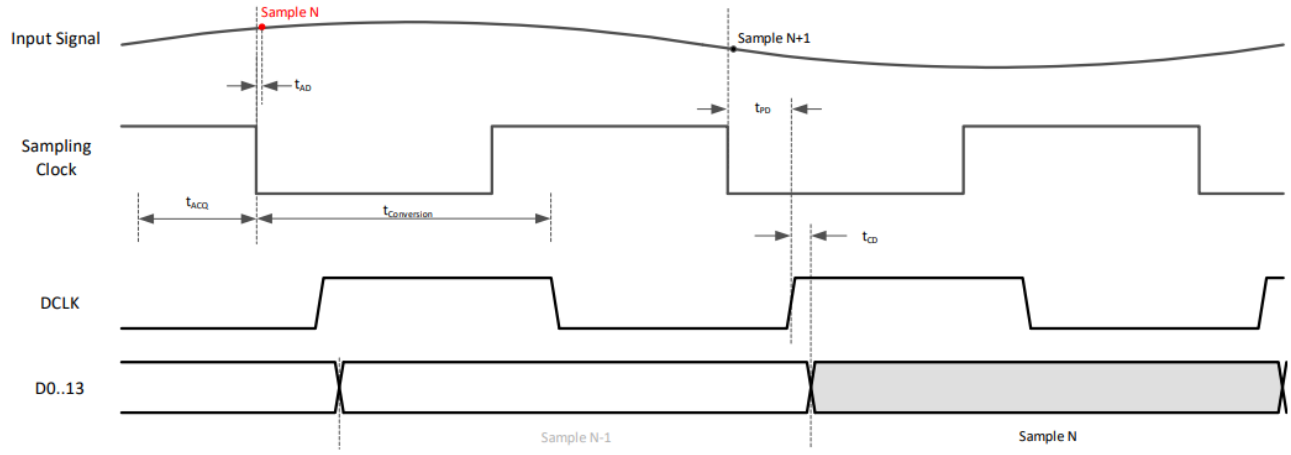

Figure 2-2. Parallel CMOS SDR Timing Diagram

2.1.2 Parallel DDR

In DDR mode, two data bits correspond to one CMOS output pin on the ADC. Considering the same 14 bit ADC, only 7 data output pins (plus the DCLK) are required, halving our resistor count to 8 resistors.

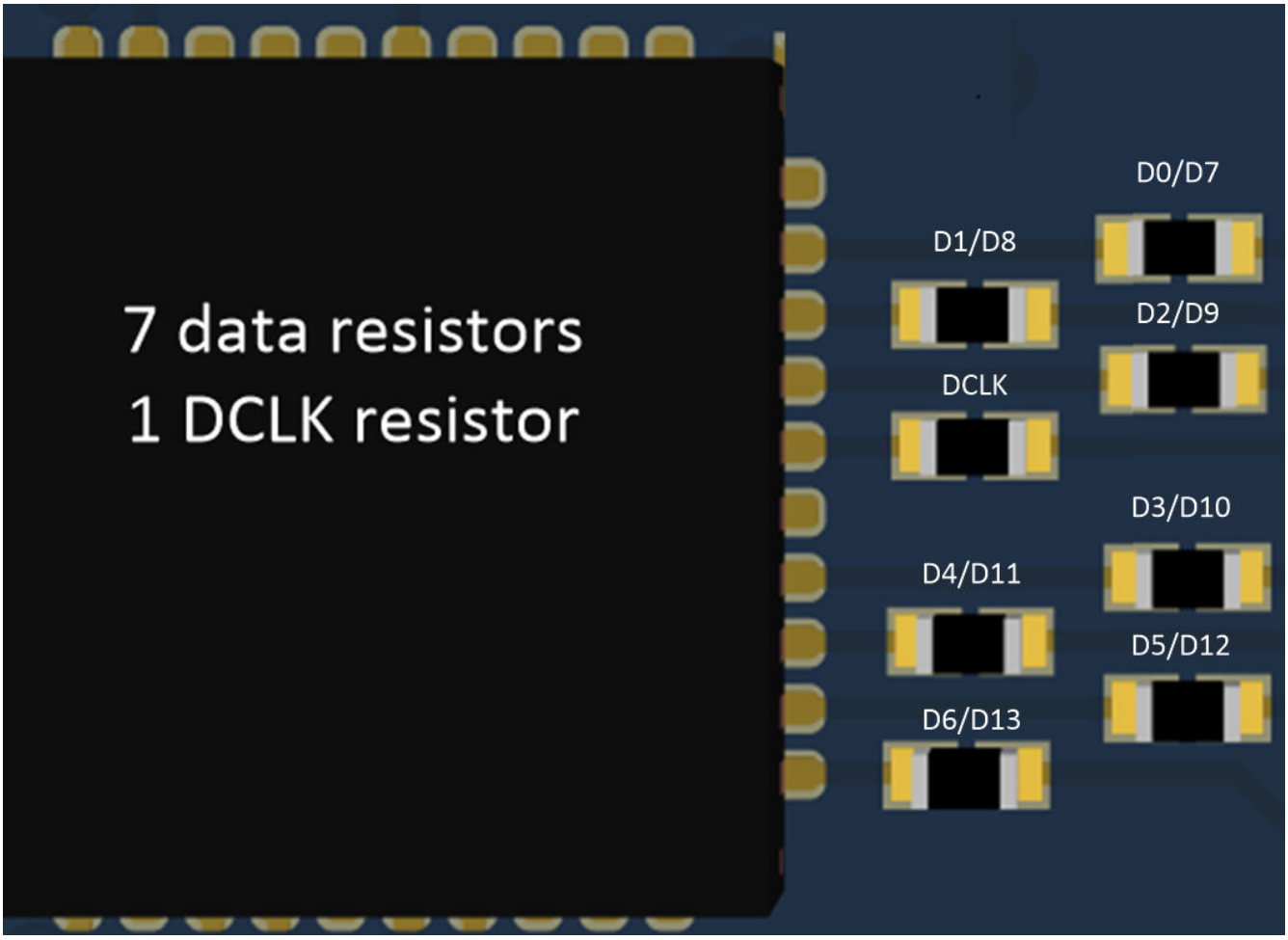

Figure 2-3. Parallel CMOS: 14 bit DDR resistors

Also the DCLK will latch the data on the rising and falling edge of the DCLK. This means that the data bits are toggling twice as fast as the DCLK. For example, if the ADC3541 is sampling at 10 MSPS, the data bits are toggling at a frequency of 20 MHz, and the DCLK is toggling at a frequency of 10 MHz.

Table 2-2. Parallel DDR CMOS Mode

Parallel Interface	Max Sampling Rate (MSPS)	Data Rate (Mbps)	Data Pins/Resistors
DDR	65	130	8

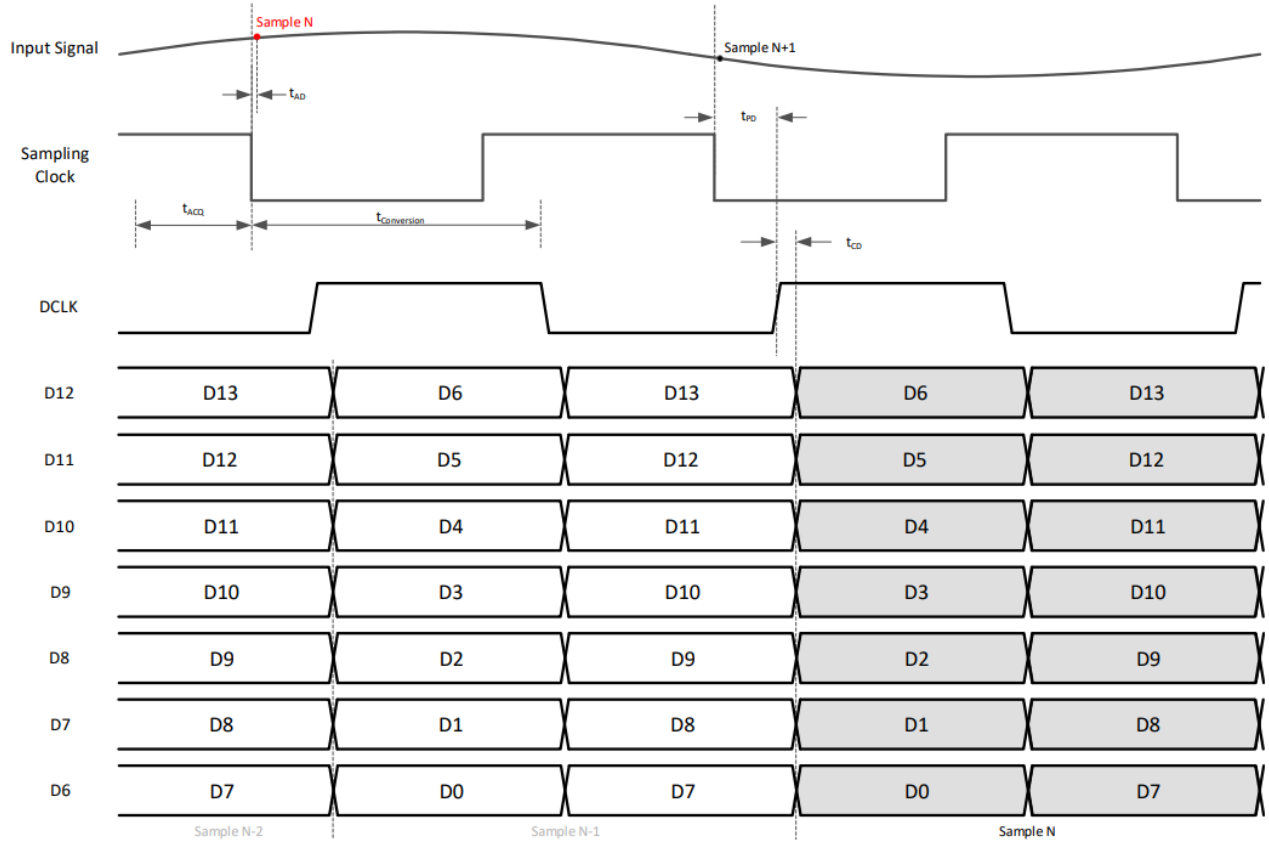

Figure 2-4. Parallel CMOS DDR Timing Diagram

In summary of the parallel interfaces, we can see that, while SDR mode offers the lowest data rate, it also requires the highest number of data output pins (resistors), and will then have a greater size/cost impact in terms of components and FPGA/uC resources. DDR mode, on the other hand, reduces the number of data output pins (resistors), but increases the data rate by a factor of 2.

Table 2-3. Parallel CMOS Modes Summary

Parallel Interface	Max Sampling Rate (MSPS)	Data Rate (Mbps)	Data Outputs/Resistors
SDR	65	65	15
DDR	65	130	8

2.2 Serial CMOS

If reducing the CMOS data output resistor count (or pin count) is even more critical in your system, then using a serialized CMOS interface (DDR) may be an attractive choice. Similar to parallel CMOS, there are a few options to consider when using a serial CMOS interface.

To transmit all 14 bits within the time period of the sampling rate, the ADC output data must be transmitted at a faster rate (serialized), and we must provide this serialization frequency as an input to the ADC. Also, a frame clock is now generated by the ADC to encapsulate each 14 bit sample, so that we will know the beginning and end of each sample.

2.2.1 2 Wire

In 2 Wire mode, all 14 bits of one channel are being transmitted on two wires, 7 bits per wire. In a 2CH ADC (ADC3643), there are a total of 6 data outputs/resistors: 4 data resistors (2 per channel), 1 Data Clock and 1 Frame Clock.

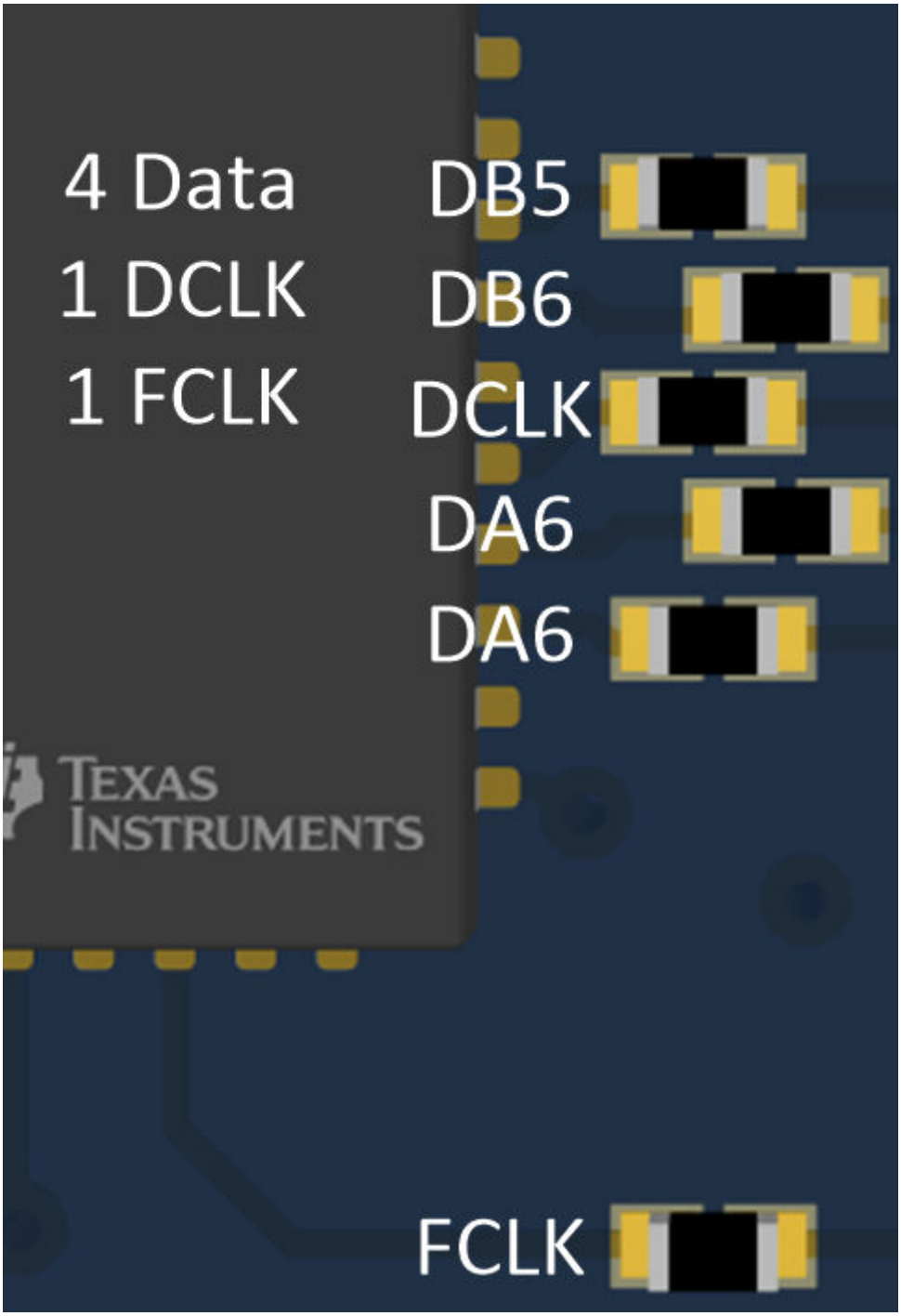

Figure 2-5. ADC3643 Serial CMOS: 2 Wire Resistors

A total of 7 bits per wire will be transmitted over one frame clock period. The serialization rate is 7x times the sampling rate. The data rate is limited to ~250 due to the CMOS interface, so the max sampling rate in this mode is 35 MSPS. Higher sampling rates can be used when decimation is used.

Table 2-4. 2 Wire Serial CMOS (No Decimation)

Mode	Max Sampling Rate (MSPS)	Serialization Rate	Data Rate (Mbps)	Data Outputs/ Resistors
2 Wire	35	7	250	6

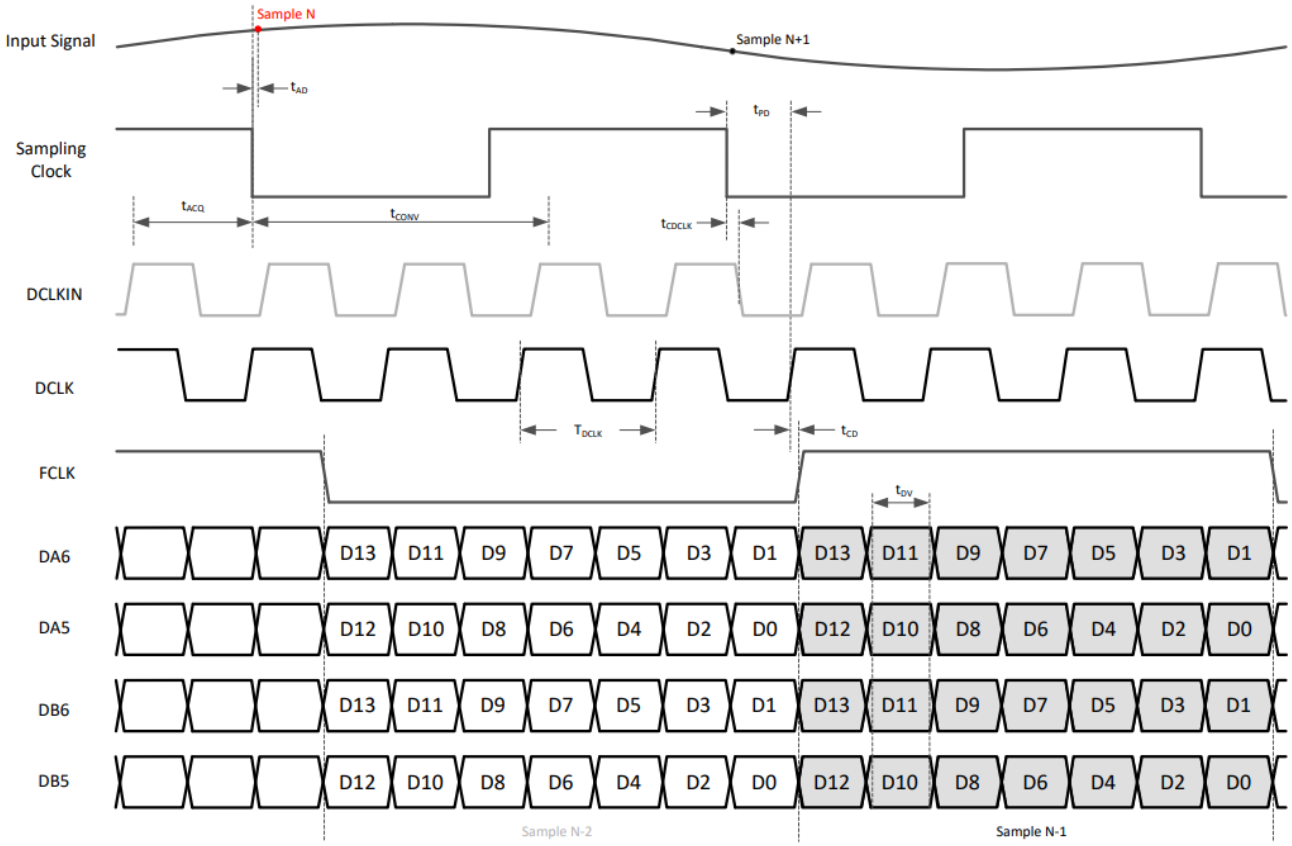

Figure 2-6. Serial CMOS 2W Timing Diagram

2.2.2 1 Wire

In 1 Wire mode, all 14 bits of one channel are being transmitted on one wire. With the DCLK and FCLK, this is a total of 4 output pins/resistors.

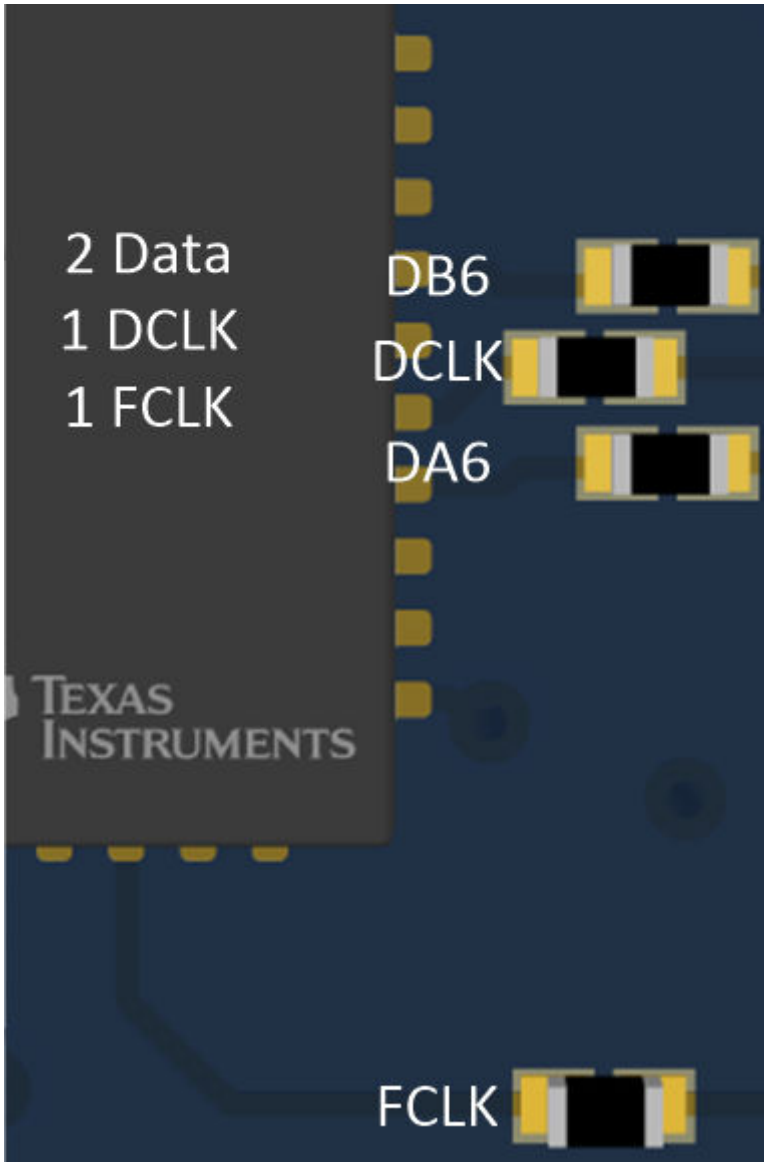

Figure 2-7. ADC3643 Serial CMOS: 1 Wire Resistors

A total of 14 bits on one wire will be transmitted over one frame clock period, so the serialization rate is 14x times the sampling rate. The data rate is limited to ~250 Mbps due to the CMOS interface, so the max sampling rate in this mode is 35 MSPS. Higher sampling rates can be used when decimation is used.

Table 2-5. 1 Wire Serial CMOS (No Decimation)

Mode	Max Sampling Rate (MSPS)	Serialization Rate	Data Rate (Mbps)	Data Outputs/ Resistors
1 Wire	17.8	14	250	4

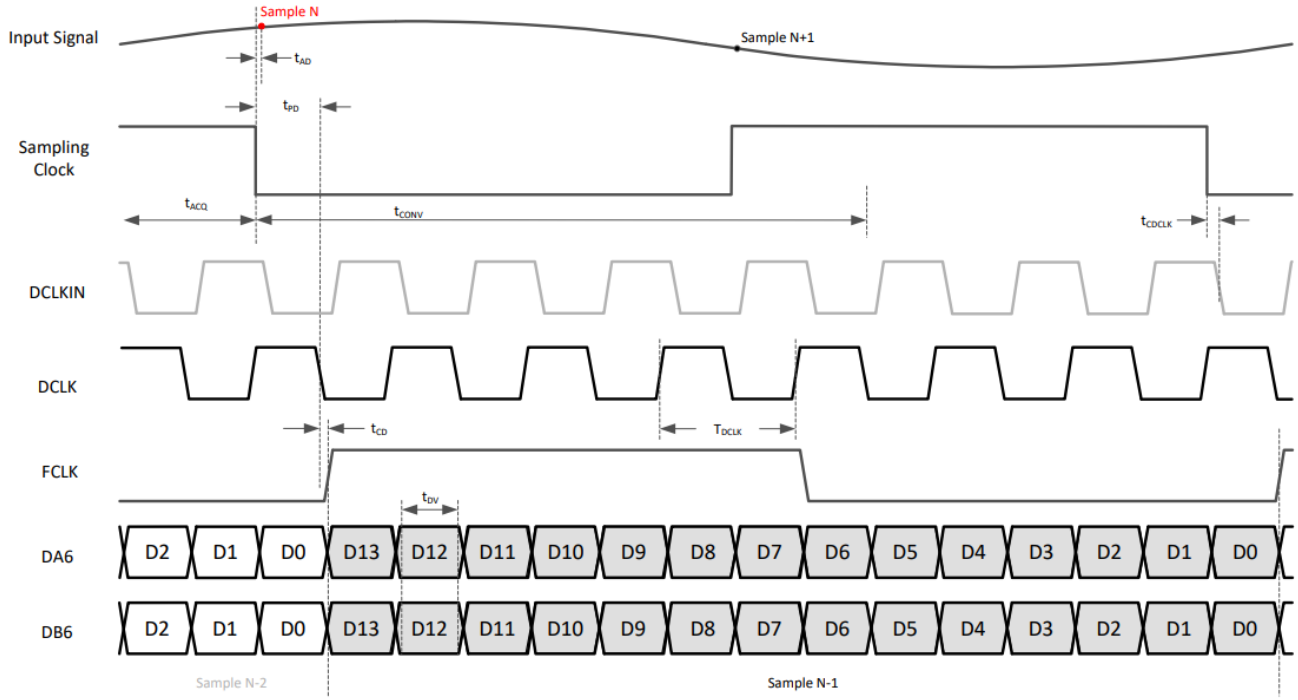

Figure 2-8. Serial CMOS 1W Timing Diagram

2.2.3 0.5 Wire

In 1/2 Wire mode (only applicable to 2CH ADCs), all 14 bits of two channels are being transmitted on one wire. With the DCLK and FCLK, there is a total of 3 output pins/resistors.

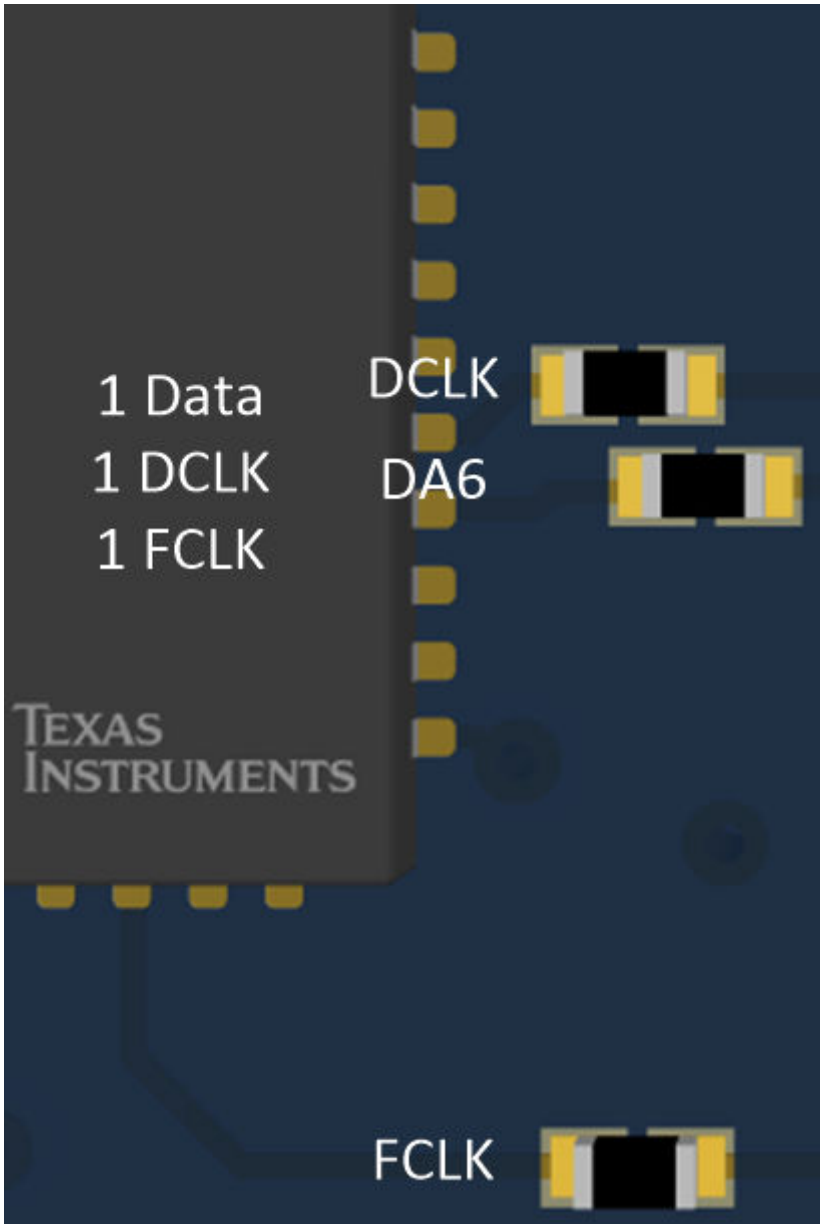

Figure 2-9. ADC3643 Serial CMOS: 0.5 Wire Resistors

A total of 28 bits (14 bits from CHA and 14 bits from CHB) are being transmitted on one wire over one frame clock period, so the serialization rate is 28x. The data rate is limited to ~250 due to the CMOS interface, so the max sampling rate in this mode is 8.9 MSPS. Higher sampling rates can be used when decimation is utilized.

Table 2-6. 0.5 Wire Serial CMOS (No Decimation)

Mode	Max Sampling Rate (MSPS)	Serialization Rate	Data Rate (Mbps)	Data Outputs/ Resistors
1 Wire	8.9	28	250	4

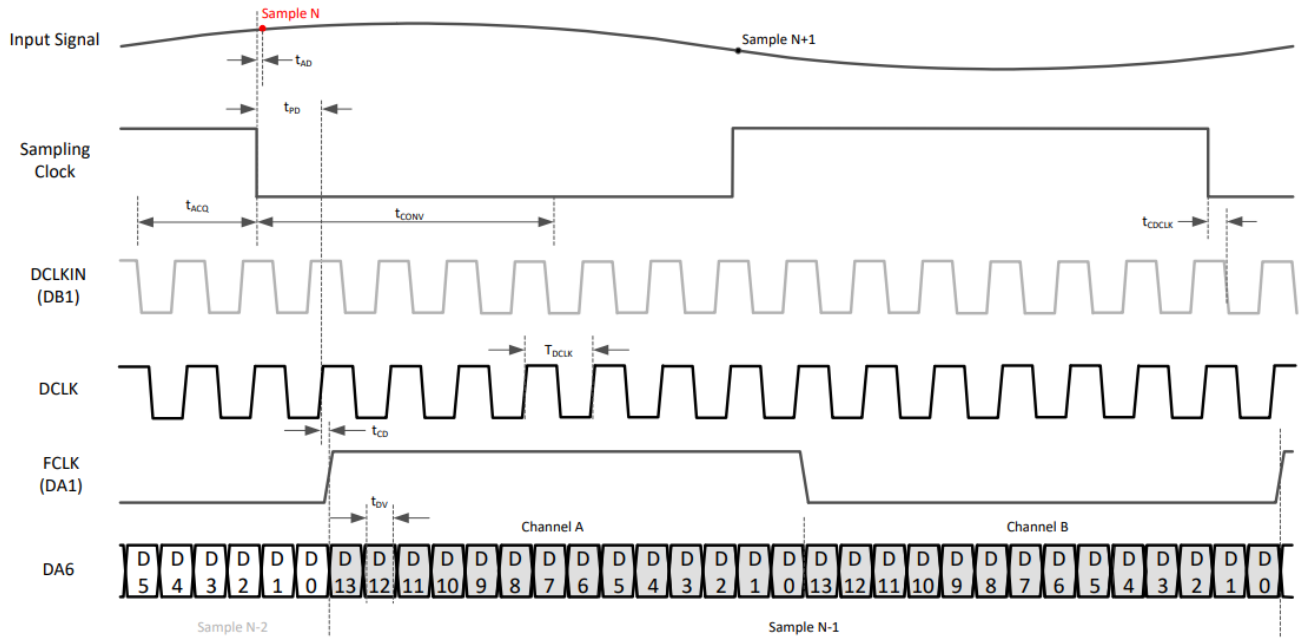

Figure 2-10. Serial CMOS 0.5W Timing Diagram

In summary of CMOS serial interfaces, we can see that there is a tradeoff to be made between the number of data outputs/resistors, and the maximum data rate.

Table 2-7. Serial CMOS Summary (No Decimation)

	Max Sampling Rate (MSPS)	Serialization Rate	Data Rate (Mbps)	Data Pins/ Resistors
2 Wire	35.7	7	250	6
1 Wire	17.8	14	250	4
1/2 Wire	8.9	28	250	3

3 Reduce Data Rates: Decimation

There many benefits to using the on-chip decimation of the ADC36xx family for both the analog and digital functions of the ADC, and the overall system requirements of the application.

When we decimate, we effectively reduce the data rate by a preset decimation factor (from 2 to 32). For example, if we choose to decimate by a factor of 8, we reduce our effective sampling rate by 8, which reduces the output data rate by 8 as well. A lower data rate can allow for a lower cost data capture device (FPGA or micro controller).

Also, every time we decimate by a factor of 2, we are also improving our SNR by ~3 dBFS. Furthermore, using decimation has the added benefit of relaxing anti-aliasing filtering requirements since harmonics (like HD2 and HD3) will be attenuated by the digital low pass decimation filters.

In the figure below, DDR mode is used to show ADC performance at 65 MSPS since the serial CMOS modes have max sample rate of ~35 MSPS while using bypass mode (2Wire). In bypass mode (no decimation) sampling at 65 MSPS with a 1 MHz input, we see about 79 dBFS SNR and 91 SFDR.

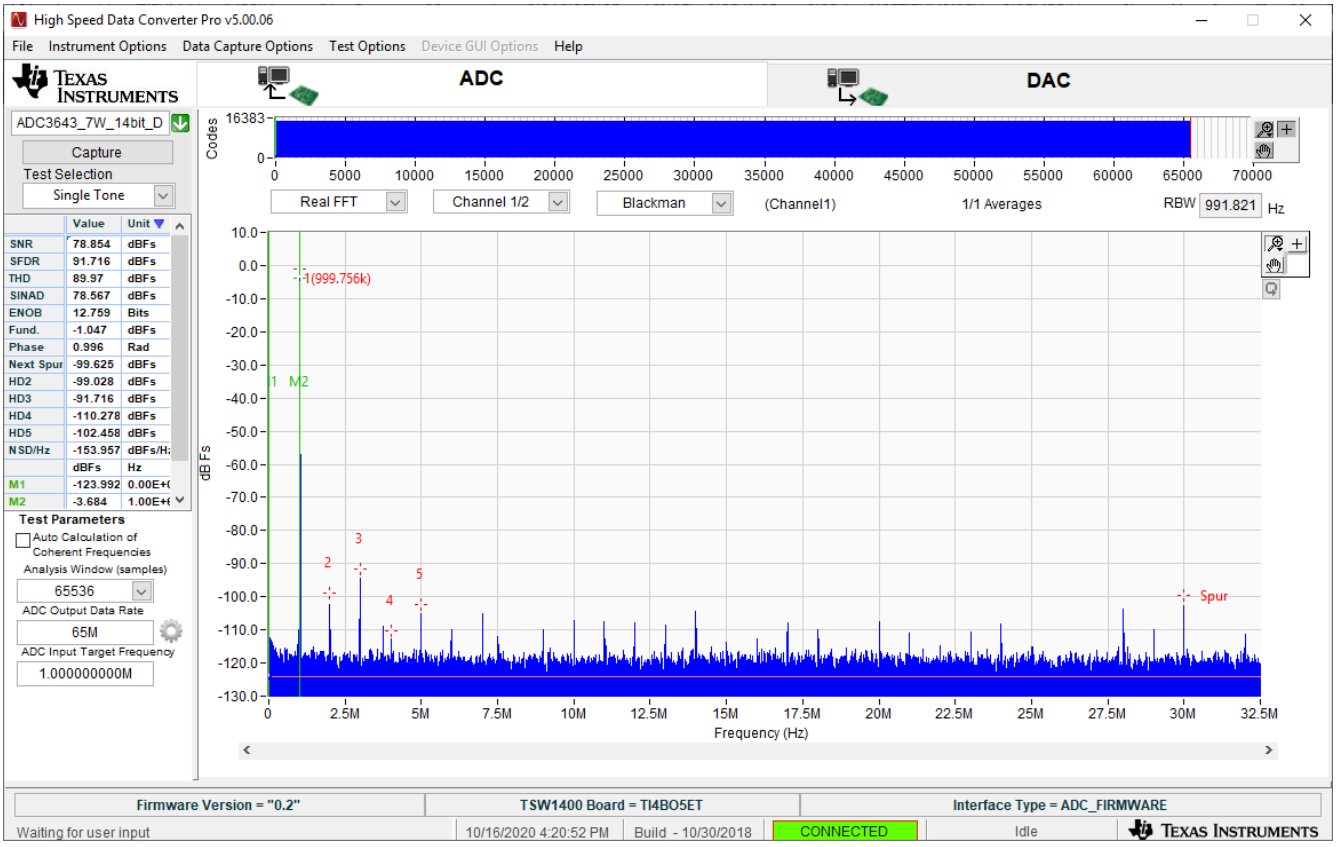

Figure 3-1. ADC3643EVM: 1MHz Fin @ 65 MSPS (No Decimation)

Table 3-1. ADC3643 65 MSPS (No Decimation)

Serial Interface	Sampling Rate (MSPS)	Serialization Rate	Decimation Factor	Data Rate (Mbps)
2 Wire	35.7	7	1	227.5

Table 3-2. ADC3643 65 MSPS (No Decimation) Performance

SNR (-dBFS)	SFDR (-dBFS)	THD (-dBFS)	HD2 (-dBFS)	HD3 (-dBFS)
78.8	91.7	89.9	99	91

If we then apply 16x Real Decimation to the same configuration, we see some interesting things happen. First, SNR and SFDR have increased, and the Nyquist zone (sampling rate divided by 2, or Fs/2) has now become much smaller (32.5 MHz to 2.03125 MHz).

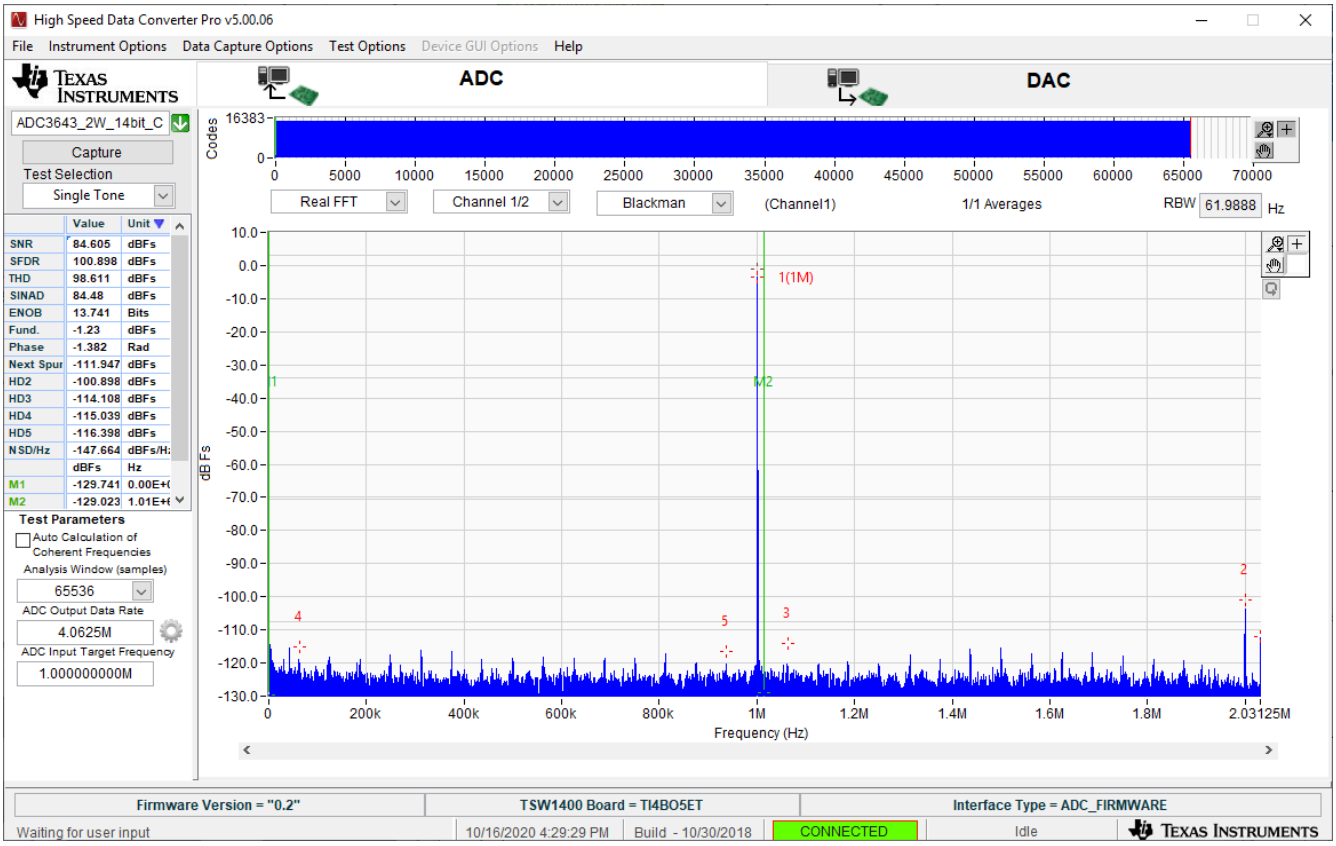

Figure 3-2. ADC3643EVM: 1MHz Fin @ 65 MSPS (16x Real Decimation)

Table 3-3. ADC3643 65 MSPS @ 16x Real Decimation

Serial Interface	Sampling Rate (MSPS)	Serialization Rate	Decimation Factor	Data Rate (Mbps)
2 Wire	65	7	16	28.4375

Table 3-4. ADC3643 65 MSPS at 16x Real Decimation Performance

SNR (-dBFS)	SFDR (-dBFS)	THD (-dBFS)	HD2 (-dBFS)	HD3 (-dBFS)
84.6	100.8	98.6	100.9	114

Taking a step further, applying 32x Real Decimation reduces our data rate even further to 14.21875 Mbps. In terms of AC performance, SNR doesn't improve much since we are reaching the limits of what can be represented by a 14 bit ADC (SNR: 1.76 + 6.02*14= 86 dB), but the SFDR improves from -100 to -108 dBFS since HD2 is now pushed out of the Nyquist zone, into the stop band of our low pass decimation filter.

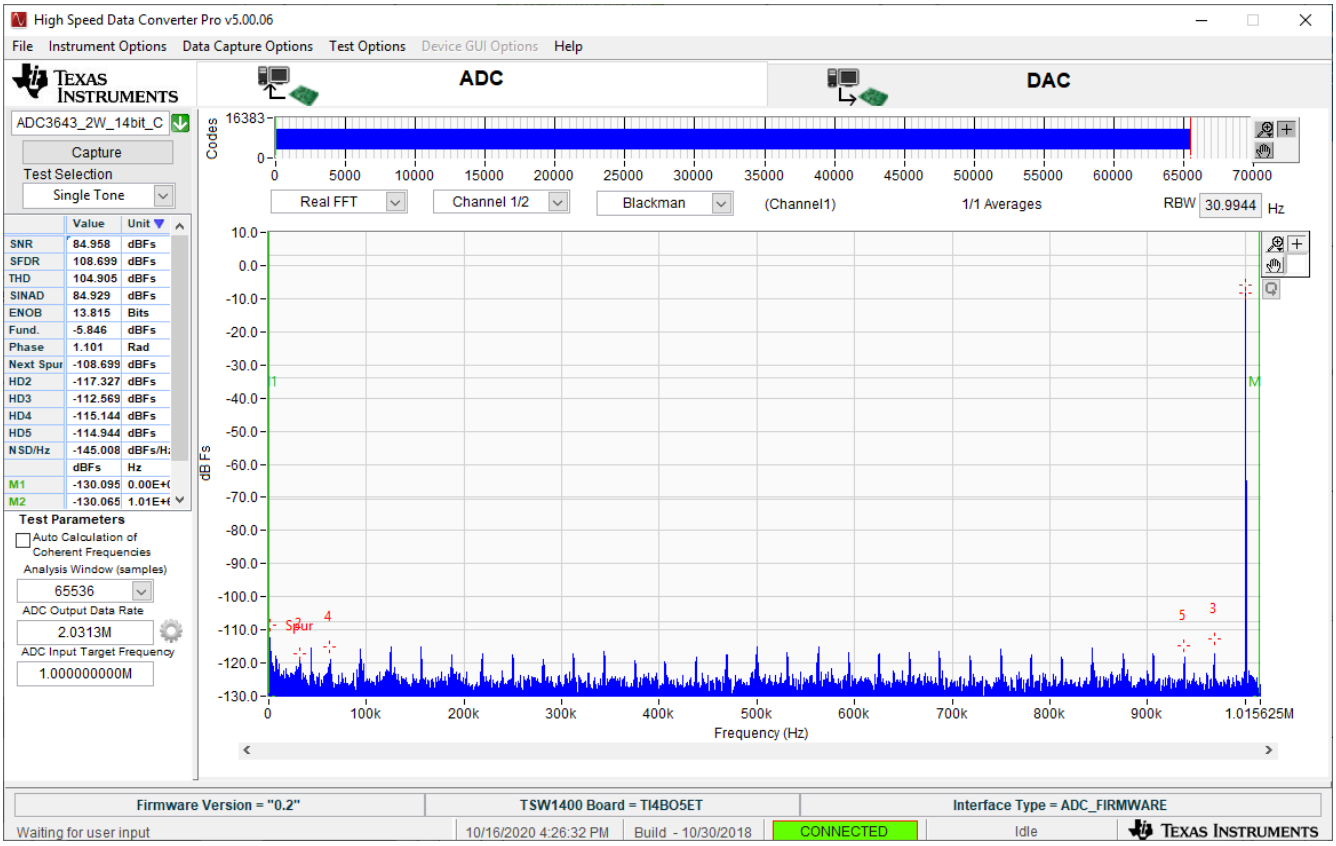

Figure 3-3. ADC3643EVM: 1MHz Fin at 65 MSPS (32x Real Decimation)

Table 3-5. ADC3643 65 MSPS at 32x Real Decimation

Serial Interface	Sampling Rate (MSPS)	Serialization Rate	Decimation Factor	Data Rate (Mbps)
2 Wire	65	7	32	14.21875

Table 3-6. ADC3643 65 MSPS at 32x Real Decimation Performance

SNR (-dBFS)	SFDR (-dBFS)	THD (-dBFS)	HD2 (-dBFS)	HD3 (-dBFS)
~85	108.6	104.9	117.3	112.5

If we also consider the different serial modes that were discussed earlier, our sampling rates were limited by the max output data rate (~250 Mbps). Looking at the table below, it can be seen that the max sampling rate of 65 MSPS can be used when decimation is applied, and very low data rates can be achieved.

Table 3-7. Decimation Data Rates across Serial Interfaces

Serial Interface	Sampling Rate (MSPS)	Serialization Rate	Decimation Factor	Data Rate (Mbps)
2 Wire	65	7	32	14.21875
1 Wire	65	14	32	28.4375
1/2 Wire	65	28	32	56.875

Decimation brings along two great advantages: data rate reduction and AC performance improvement (SNR, THD, SFDR, and so on,). While decimation can be carried out in the DSP or FPGA, the ADC3643 provides this feature on-chip and removes the need for complex DSP implementation, allowing the ADC do the work for you.

4 Summary

Modern high-speed SAR ADCs, like the ADC3643, offer many options that offer ease of use, and allow for optimizations that were not possible with previous generation devices. Options similar to serial CMOS output, and on-chip decimation, can open doors for using high-speed ADCs in your upcoming projects, or help to improve your current design by reducing pin count and data rates.

For more information on decimation, and other high-speed data converter topics, please follow this link to TI's training videos.

5 References

- Texas Instruments, *ADC3541 14-bit Ultra-Low-Power High-SNR ADC with 10-MSPS Sampling Rate data sheet*
- Texas Instruments, *ADC3643 Dual, 14-bit, 1-MSPS to 65-MSPS, low-noise, ultra-low-power, analog-to-digital converter (ADC) data sheet*

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