Adjusting the Input Common-Mode Voltage for SAR ADCs to Avoid Amplifier Output Swing Limitations

Ryan Andrews

Introduction

A fully-differential SAR ADC requires that the input common-mode voltage remain constant throughout the ADC full-scale range. This common-mode voltage restriction is typically limited to one-half of the ADC reference voltage ($V_{REF}/2$) ±100 mV.

TI suggests pairing a fully-differential SAR ADC with a fully-differential amplifier (FDA) to achieve a constant common-mode voltage. FDAs feature an output common-mode pin (V_{OCM}) that sets the common-mode voltage for both the inverting and non-inverting outputs. Applying $V_{REF}/2$ to the V_{OCM} pin allows the FDA to accept either a single-ended or differential input and convert it to a symmetrical, differential output centered around $V_{REF}/2$.

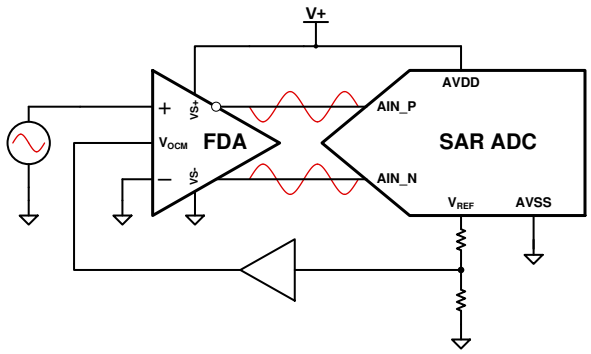


Figure 1. Setting FDA V_{OCM} = ADC $V_{REF}/2$

Amplifier Output Swing Limitations

Most SAR and FDA signal chains share the same positive and negative supply voltages. However, the ADC reference voltage is usually less than the supply, so a mid-reference input common-mode for the ADC is often less than mid-supply of the amplifier. This forces the output of the FDA to swing closer to the negative supply rail than to the positive supply rail.

Amplifiers with limited output swing will enter a non-linear region of operation and introduce additional error for large output signals. Higher output load currents further restrict the amplifier output swing, as load currents can spike for brief instances when the voltage is sampled by a switched-capacitor SAR ADC. Ultimately, these limitations may lead to poor linear performance when the amplifier output signal reaches the ADC full-scale.

Two potential solutions to avoid output swing limitations in the FDA stage include:

1. *Generating a negative supply rail* to drive the negative FDA supply pin below ground. Applying a negative supply rail (i.e. -200 mV) can allow the amplifier output to swing all the way to 0 V without changing the output common-mode voltage.
2. *Shifting the V_{OCM} voltage above mid-reference* to avoid the negative rail. Increasing the output common-mode voltage also increases the linear output swing, but most fully-differential SAR ADCs only allow ±100 mV. This may not always be sufficient to avoid the negative rail completely with a full-scale input signal.

Each of the above solutions require additional components and add to the design cost, complexity, and size. A negative supply rail may require an inverting DC/DC converter plus additional passive components. The shifted common-mode voltage must be buffered because the V_{OCM} pin on an FDA is a relatively low-impedance input.

ADS9224R Fully-Differential SAR ADC

The ADS9224R is a 16-bit, 3-MSPS, dual-channel, simultaneous-sampling SAR ADC with two key features that address this very challenge. This device integrates a buffered mid-reference output that can drive the V_{OCM} pin directly to $V_{REF}/2$. Setting a single bit in the ADS9224R register map increases the $V_{REF}/2$ output by +100 mV. For example, if the reference voltage is 4.096 V, the $V_{REF}/2$ output can be set to either 2.048 V (default) or to 2.148 V. At the same time, the input common-mode voltage range on the ADS9224R has been extended to $V_{REF}/2$ ±200 mV, increasing the acceptable voltage range in cases where additional shift is required. These features help avoid FDA output swing limitations while driving a full-scale ADC input signal, all without adding extra components.

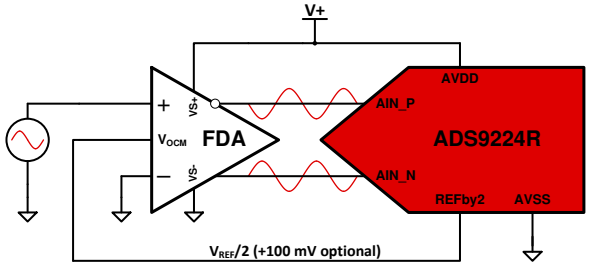


Figure 2. ADS9224R REFby2 Driving FDA V_{OCM}

Measurement Comparison

The performance benefit of the ADS9224R can be directly measured using the ADS9224REVM-PDK. This evaluation module features a wide-bandwidth FDA (TI's THS4551) at the input of each ADS9224R channel operating from the same 5-V supply. The following measurements were collected while sampling at the full 3-MSPS throughput, placing the highest current demand on the THS4551 outputs. The ADS9224R is set to use the internal 2.5-V reference voltage with a gain of 1.634 V/V to achieve V_{REF} = 4.096 V. The mid-reference output ("REFby2") is connected to the V_{OCM} pin of each THS4551 and varied from 2.048 V to 2.148 V.

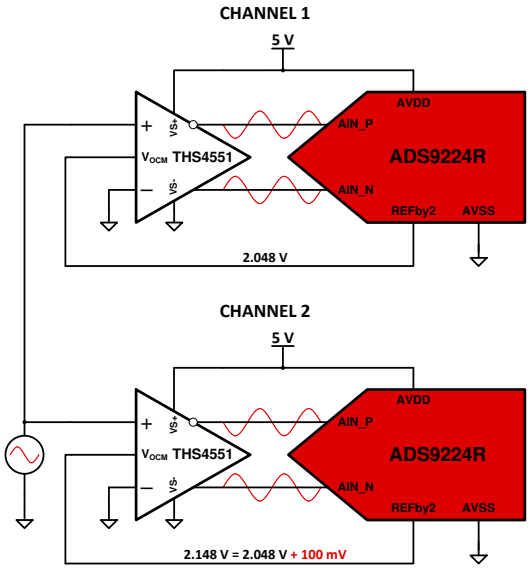


Figure 3. ADS9224R REFby2 Comparison Setup

The applied input signal to each channel is a 2-kHz single-ended sine wave with an amplitude of 8.17 V_{PP} (approximately -0.023 dBFS). Observing the non-inverting output from each THS4551 shows that the negative peak of the Channel 1 output is clipped and distorted, while the Channel 2 output remains nearly 60 mV away from the negative rail.

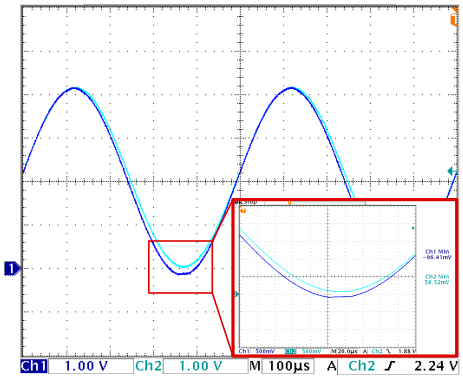
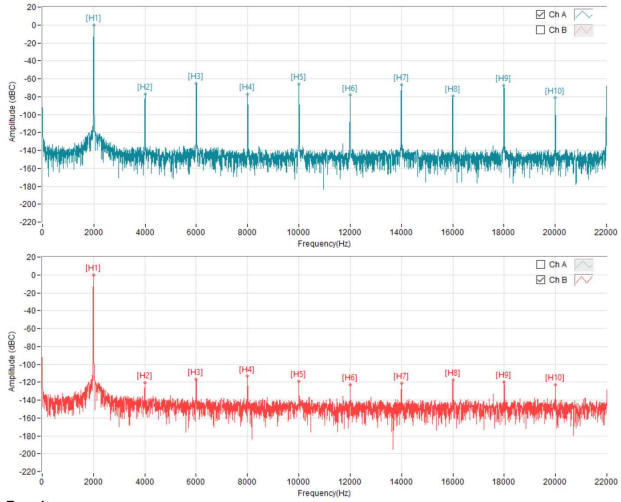


Figure 4. V_{OCM} = 2.048 V (Ch1) vs. 2.148 V (Ch2)

Results

The impact on AC performance is analyzed by computing an FFT on the data collected from each channel. The clipped sine wave output from Channel 1 introduces significant harmonic distortion to the frequency spectrum. The resulting measured SNR and THD (63.13 dB and -59.69 dB, respectively) are well below the data sheet specifications of the ADS9224R. The results from Channel 2 are substantially improved, as shifting the common-mode voltage greatly reduced the harmonic content in the THS4551 output. As a result, this system is able to meet the typical SNR and THD specifications of the ADS9224R (93 dB and -109 dB, respectively).



Results

	SNR (dB)	THD (dB)	Signal Power (dBFS)	SFDR (dB)	SINAD (dB)	ENOB	Fi Calc (Hz)	Max Spur (dBC)	Max Spur (Hz)
Ch A	63.130	-59.685	-0.038	65.342	58.064	9.353	1999.983	-65.342	5999.565
Ch B	93.532	-108.512	-0.003	111.848	93.396	15.222	1999.983	-111.848	2022.743

Figure 5. FFT and AC Results for Ch1 and Ch2

Conclusion

By shifting the input common-mode voltage, the design met the data sheet performance criteria of the ADS9224R with an 8.17-V_{PP} input signal. The amplitude must be limited to 8.015 V_{PP} in order to achieve the same performance without the shift. In other words, shifting the input common-mode by 100 mV increased the linear differential output swing by about 150 mV_{PP} to utilize the entire ADC full-scale range and maintain performance.

Table 1. Alternative Device Recommendations

Device	Description
ADS9234R	14-bit, 3.5-MSPS, Dual-Channel, Simultaneous-Sampling SAR ADC
THS4552	Dual-Channel, Low-Noise, Precision, 150-MHz, Fully-Differential Amplifier

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265