Application Report

AFE79xx Layout Guide

Kang Hsia

ABSTRACT

This document serves as general layout guidelines for the AFE79xx-integrated RF sampling transceiver based on best design practices for high-speed, mixed-signal systems. System designers must refer to this document when designing the PCB with the AFE79xx component. Specific topics include the following:

- Ground plane layout in mixed signal design
- Power supply distribution
- Power supply decoupling
- Clock routing
- JESD204 lane routing

Table of Contents

List of Figures

List of Tables

Trademarks

1 Terminology

CLK Reference clock to the AFE7920 (either directly clocking the RF Sampling Data Converters or providing reference to the on-chip PLL)

TX RF Sampling Transmitter DACs

RX RF Sampling Receiver ADCs

FB RF Sampling Feedback ADCs

SRX SerDes receiver lanes

STX SerDes transmitter lanes

GPIO General Purpose Input/Output

IMD3 Intermodulation Distortion Third Order

ACPR Adjacent Channel Power Ratio

NSD Noise Spectral Density

ESD Electrostatic Discharge

2 Introduction

This EVM layout guide is based on the AFE79xx EVM (DC101), and is intended to provide customers the understanding for the basis of TI AFE79xx EVM layout. The recommendations are best practices in high-speed system design based on the lessons learned during the design, layout reviews, and final tests of the AFE79xx EVM. This layout guide highlights the critical areas that need additional attention and priority in care during the layout process. TI also addresses the strategies when tackling the critical layout nets and routings, and methods that the customers can use to apply the strategy upon their own designs.

3 Stack-Up and Net Placement

Table 3-1 shows the description of each layer and the important nets in the layer.

Table 3-1. AFE79xx EVM Stack-up Information

LAYER	LAYER DESCRIPTION	MATERIAL	THICKNESS (MIL)	CONDUCTIVITY (MHO/CM)	DIELECTRIC CONSTANT	LOSS TANGENT	NETS
Air	Air	N/A	N/A	0	1	0	
Top Surface	Dielectric	FR-4	2	0	4	0.035	
Top	Device Placement Layer	Copper	2.6	595900	4.2	0	Four RX input traces, four TX output traces, two feedback traces, SerDes SRX lanes. Top layer power supply net decoupling capacitors.
Top/2 Dielectric	Dielectric	FR-4	7.2	0	4.2	0.035	
2	Ground Layer	Copper	0.7	595900	4.2	0.035	Ground pour with a slit to isolate digital ground and analog ground.
2/3 Dielectric	Dielectric	FR-4	8	0	4.2	0.035	
3	Power Layer	Copper	1.2	595900	4.2	0	VOUT_1p2V, VOUT_1p2VCLK, PLLA1p8V, VDDA_GPIO_1p8
3/4 Dielectric	Dielectric	FR-4	8	0	4.2	0.035	
4	Ground Layer	Copper	1.2	595900	4.2	0	Ground pour with a slit to isolate digital ground and analog ground.
4/5 Dielectric	Dielectric	FR-4	8	0	4.2	0.035	
5	Power Layer	Copper	1.2	595900	4.2	0.035	VOUT_1p8V, VOUT_1p8V_CLK, VOUT_1p2V_PLL, VOUT_3p3V_LMK*
5/6 Dielectric	Dielectric	FR-4	4.9	0	4.2	0.035	
6	Ground Layer	Copper	0.7	595900	4.2	0.035	Ground pour with a slit to isolate digital ground and analog ground.
6/7 Dielectric	Dielectric	FR-4	5.4	0	4.2	0.035	
7	Signal Layer	Copper	0.7	595900	4.2	0	GPIO routing
7/8 Dielectric	Dielectric	FR-4	3	0	4.2	0.035	
8	Signal Layer	Copper	1.2	595900	4.2	0.035	GPIO routing
8/9 Dielectric	Dielectric	FR-4	8	0	4.2	0.035	
9	VSSCLK Layer	Copper	1.2	595900	4.2	0	General ground layer with focus on clock ground isolation. It has slit to isolate digital ground and analog ground.
9/10 Dielectric	Dielectric	FR-4	8	0	4.2	0.035	

Table 3-1. AFE79xx EVM Stack-up Information (continued)

LAYER	LAYER DESCRIPTION	MATERIAL	THICKNESS (MIL)	CONDUCTIVITY (MHO/CM)	DIELECTRIC CONSTANT	LOSS TANGENT	NETS
10	Power Layer	Copper	1.2	595900	4.2	0	VOUT_0p9V and VOUT_1p8V_PLL
10/11 Dielectric	Dielectric	FR-4	8	0	4.2	0.035	
11	Ground Layer	Copper	1.2	595900	4.2	0.035	Ground pour with a slit to isolate digital ground and analog ground.
11/Bottom Dielectric	Dielectric	FR-4	8	0	4.2	0.035	
Bottom Layer	Device Decoupling Capacitor Placement Layer	Copper	2.6	595900	4.2	0	Ground pour with a slit to isolate digital ground and analog ground. Bottom layer power supply net decoupling capacitors. SerDes STX lanes, AFE79xx clock receiver (REFCLK±) inputs. TX output bias network routing.
Bottom Surface	Dielectric	FR-4	2	0	4	0.035	
Air	Air	N/A	N/A	0	1	0	
*Not an AFE79xx device rail.							

Note

Typical PCB manufacturing industrial practice requires the top half of copper thickness to be symmetrical (in cross sectional perspective) with the bottom half copper thickness. The copper layers, along with the epoxy and dielectric materials, are first heated and pressed during PCB manufacturing. If the top half of copper thickness is not symmetrical with the bottom half copper thickness, uneven surface cooling rate could cause the PCB to warp and bend. In theory, layer 7 and layer 8 are GPIO routing layers and have lower copper thickness content, and could potentially cause warping of the PCB. This is remedied by filling copper in layer 7 and layer 8 to create symmetrical copper thickness.

4 General Placement Methodology

1. Top and bottom layers must be reserved for high speed SerDes, clocking, and RF input and output signals.
   a. RF RX input, RF TX output, RF FB input, and SRX traces are routed on the top layer straight from the connectors to the device to minimize the use of vias. The minimum use of vias reduces the impact of attenuation and impedance variation. The SRX traces can operate at 29.5-Gbps SerDes rate, and minimum usage of vias increases the margin of SRX CTLE and DFE operation.
   b. This design of EVM does not have blind vias or back-drilling of vias. Therefore, if routing from the top layer to middle layers through vias, the effect of stub applies and impacts the impedance quality, as shown in Figure 4-1. Therefore, for additional high-speed signal requiring a different layer routing besides the top layer, the bottom layer is chosen to avoid the effect of stub. For example, the SerDes STX lanes and AFE79xx clock receiver inputs are routed on the bottom layer with RF vias routing from BOTTOM to TOP layer without any stubs being introduced.

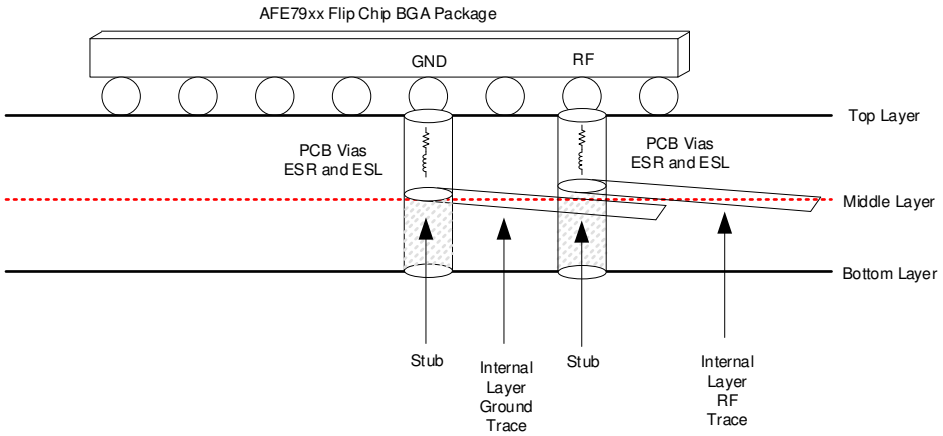


Figure 4-1. Stub Effect of Vias to Middle Layer

2. Clock input (REFCLK±) must be well isolated from the RF signal input and other aggressors. The clock input is either going directly to the data converter sampling clocks (that is direct, external clocking) or going to the on-chip PLL for data converter sampling clock generation. Any RF signal or other sources of aggressors

modulates onto the sampling clock, causing clock pollution. The polluted clock has contents modulating on the RF input and RF output, and these pollutions create distortions, spurs, and degraded noise performance.

5 Power Supply and Ground Layout Methodology

The AFE79xx EVM contains the following power nets and associated ground nets.

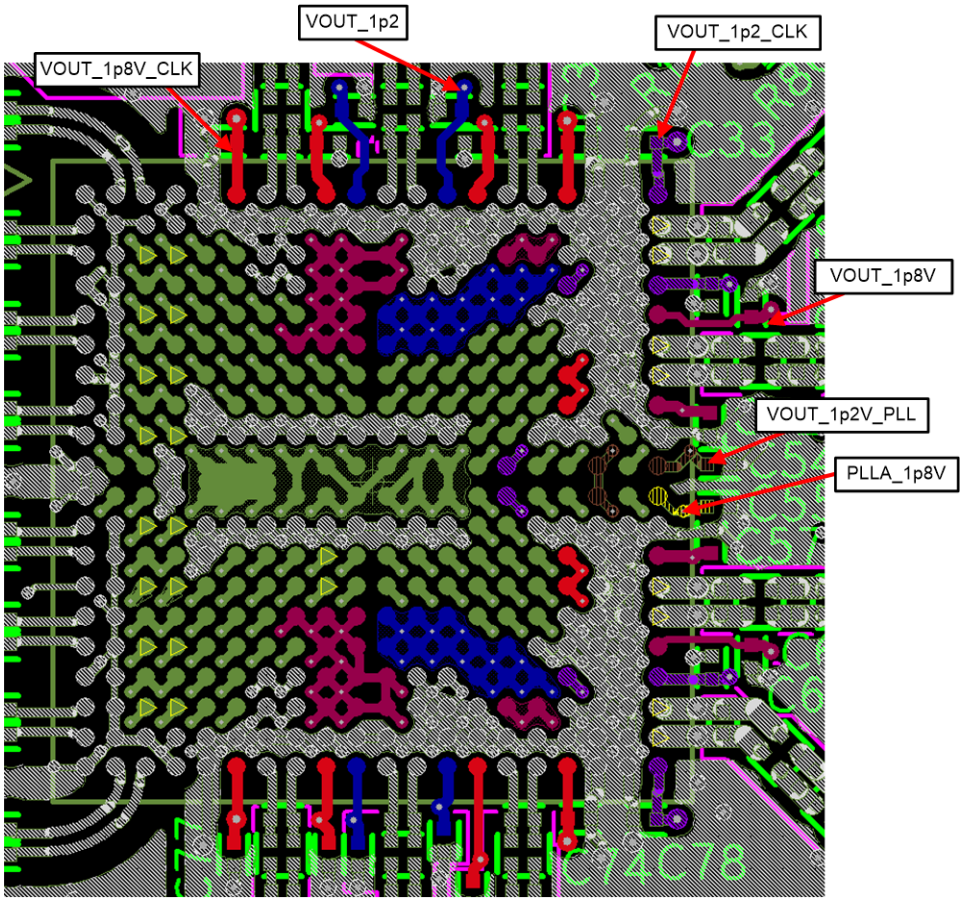
Table 5-1. AFE79xx Power Supply Nets and Associated Ground Return Nets

AFE79xx EVM GENERAL NET NAME	AFE79xx DEVICE POWER PINS	DESCRIPTION OF NETS	ASSOCIATED GROUND NETS
VOUT_0p9V	DVDD	0.9-V digital core power supply nets	DGND
	VDDT	0.9-V SerDes digital core power supply nets	
VOUT_1p2V	VDD1p2FB	1.2-V supply for FB ADC chain	AGND
	VDD1p2RX	1.2-V supply for RX ADC chain	
VOUT_1p2VCLK	VDD1p2TXCLK	1.2-V supply for TX DAC chain clock	Virtual VSSCLK tied to AGND
	VDD1p2TXENC	1.2-V supply for TX DAC encoder	
	VDD1p2PLLRXCML	1.2-V supply for PLL clock distribution to RX ADCs	
	VDD1p2PLLFBCML	1.2-V supply for PLL clock distribution to FB ADCs	
VOUT_1p2V_PLL	VDD1p2PLLCLKREF	1.2-V supply for PLL	Virtual VSSCLK tied to AGND
PLLA1p8V	VDD1p8PLLVCO	1.8-V supply for PLL/VCO. This is a sensitive net and requires extra care in layout	Virtual VSSCLK tied to AGND
VOUT_1p8V_PLL	VDD1p8PLL	1.8-V supply for PLL	Virtual VSSCLK tied to AGND
VOUT_1p8V	VDD1p8TX	1.8-V TX DAC chain analog power supply	AGND
	VDD1p8RX	1.8-V RX ADC chain analog power supply	
	VDD1p8FB	1.8-V FB ADC chain analog power supply	
VOUT_1p8V_CLK	VDD1p8RXCLK	1.8-V RX ADC chain clock power supply	Virtual VSSCLK tied to AGND
	VDD1p8FBCLK	1.8-V FB ADC chain clock power supply	
	VDD1p8TXDAC	1.8-V TX DAC chain clock power supply	
VDDA_GPIO_1p8	VDD1p8GPIO	1.8-V Supply for GPIO	DGND
	VDDA1p8	SerDes Analog core 1.8-V Power Supply Net	

The following strategies highlight the essential cares needed when laying out the power nets and associated ground nets.

1. To improve the effectiveness of the PCB plane decoupling for the power supply planes, the amount of via inductance needs to be reduced. Sensitive power supply nets must be placed on the power layers that are closer to the device placement plane (that is near the top layer in this layout design). In this design, layer 3 and layer 5 contain the sensitive nets such as:
   - VOUT_1p2V
   - VOUT_1p2VCLK
   - PLLA1p8V
   - VOUT_1p8V
   - VOUT_1p8V_CLK
   - VOUT_1p2V_PLL

2. Any noise disturbance on these power supply rails goes through the minimum distance of via from the package to the power planes. The PCB plane itself provides decoupling for the noise. Layer 10 has digital power DVDD and 1.8-V power to the PLL (VOUT_1P8_PLL).
3. Figure 5-1 highlights the power supply nets that have pin-outs near the device edge. The user can route these nets directly to decoupling capacitor on the same layer of the device. This method does not require any use of via on the power supply net routing.



RED: VOUT_1P8_CLK BLUE: VOUT_1P2 PURPLE: VOU_1P2_CLK MAGENTA: VOUT_1P8V GREEN: VOUT_1P2_PLL YELLOW: PLLA_1P8V

Figure 5-1. AFE79xx Analog Power Supply Nets Direct Routing to the Decoupling Capacitor

4. Figure 5-2 is a simplified diagram showing the power supply pin name of the AFE79xx with respect to the PCB net name, and the relative decoupling path connection of actual physical layout as shown in Figure 5-1.

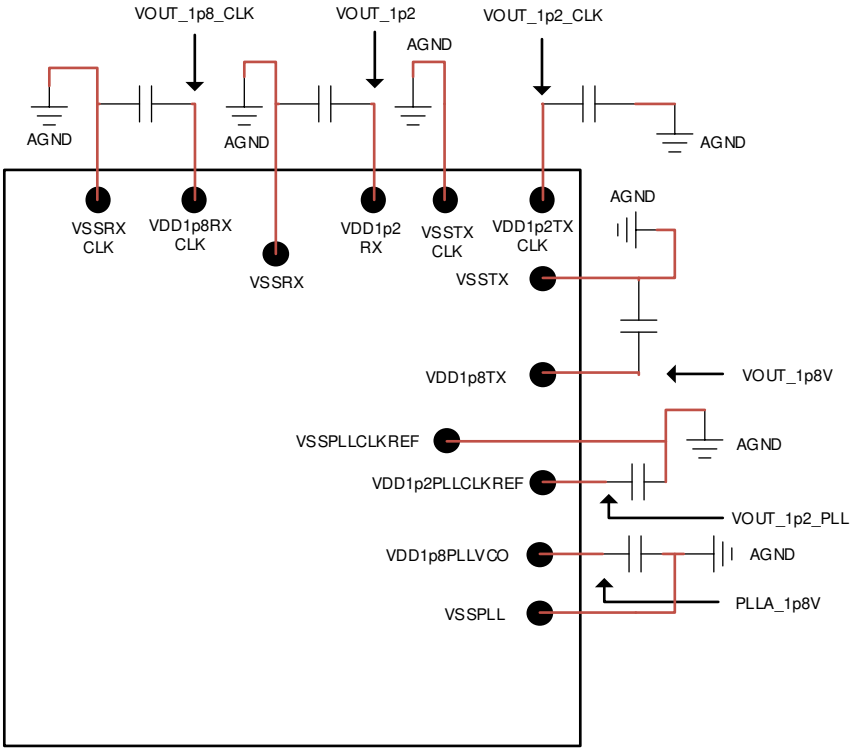


Figure 5-2. Effective Power Net Decoupling

5. Figure 5-3 is a diagram highlighting the sensitive analog power nets with respect to the highlighted power nets as shown in Figure 5-1 and Figure 5-2.

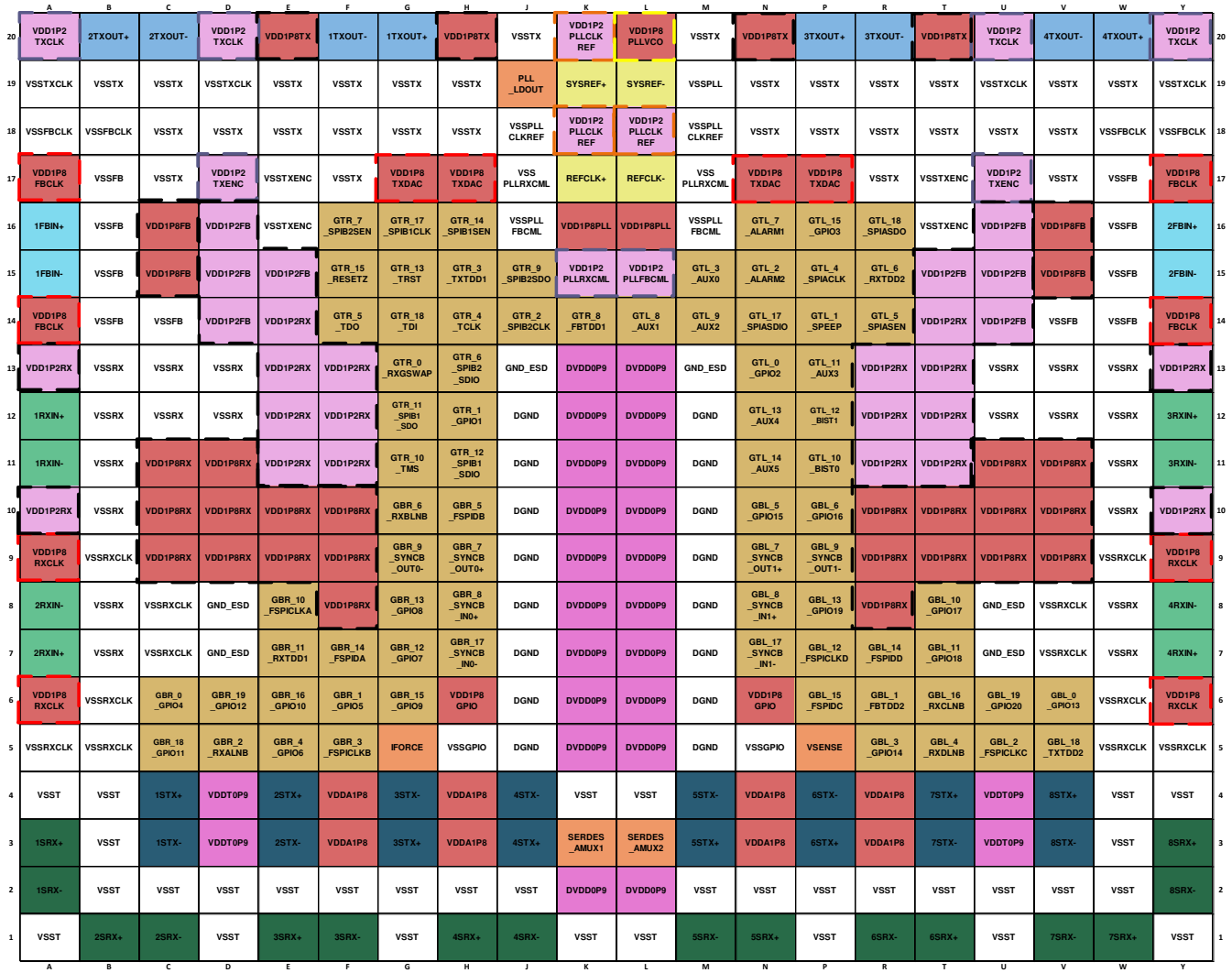


Figure 5-3. Sensitive Analog Power Nets with Respect to the AFE79xx Pin Map

6. Digital power planes VOUT_0p9V (DVDD and VDDT) are placed on layer 10, the last power layer before bottom layer. This allows the digital power plane to reach the bottom decoupling capacitors with minimum via distance from layer 10 to bottom layer for optimal decoupling.
7. Power planes must prevent overlap on top of each other to minimize plane to plane coupling. In this design, layer 3, layer 5, and layer 10 have the majority of the AFE79xx power supply planes. In between the power layers, there are ground layers available to isolate the power layer from other aggressors. The ground layers also prevent the power layer noise leakage onto other sensitive layers. For example, the DVDD digital power supply plane can be an aggressor to other signal layer and other power layers. Moreover, the application of the power plane placed or "sandwiched" in between ground planes allows better higher frequency noise decoupling. The dielectric material between the power plane layer and ground plane layers play the role of decoupling capacitor without much of the parasitic inductance effect of the decoupling capacitors. Therefore, this "sandwich" method improves the overall power supply noise decoupling performance. The effective capacitance is dependent on the area of the dielectric coverage, the distance between the two conductors, and the dielectric material property, as shown in Figure 5-4.

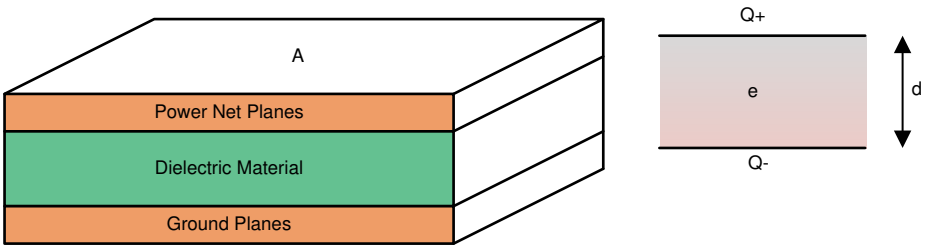


Figure 5-4. Effective Capacitance of the PCB Dielectric Material

8. Isolation among power supplies to the device that are fed using the same power plane can be achieved with the use of the ferrite beads or feedthrough capacitors. In such cases, bypass capacitors are to be placed between the power source, ferrite beads, and the load (AFE79xx power rails), as shown in Figure 5-5.

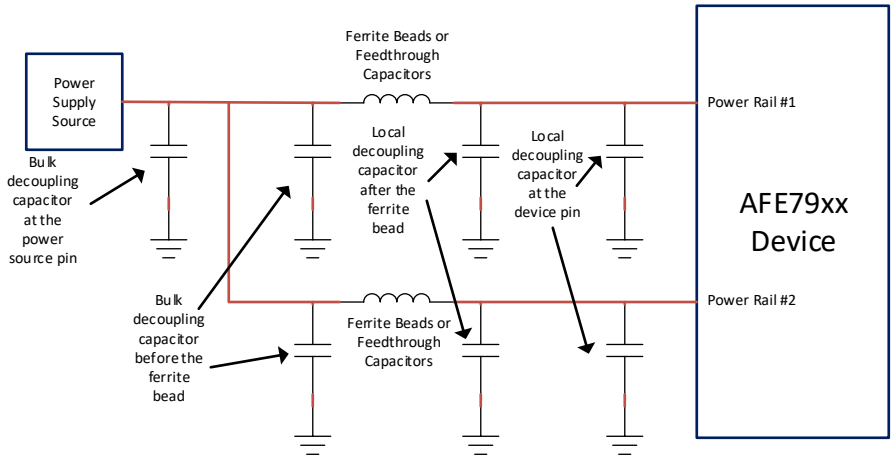


Figure 5-5. Typical Ferrite Bead and Bypass Capacitor Placement for Split Rails

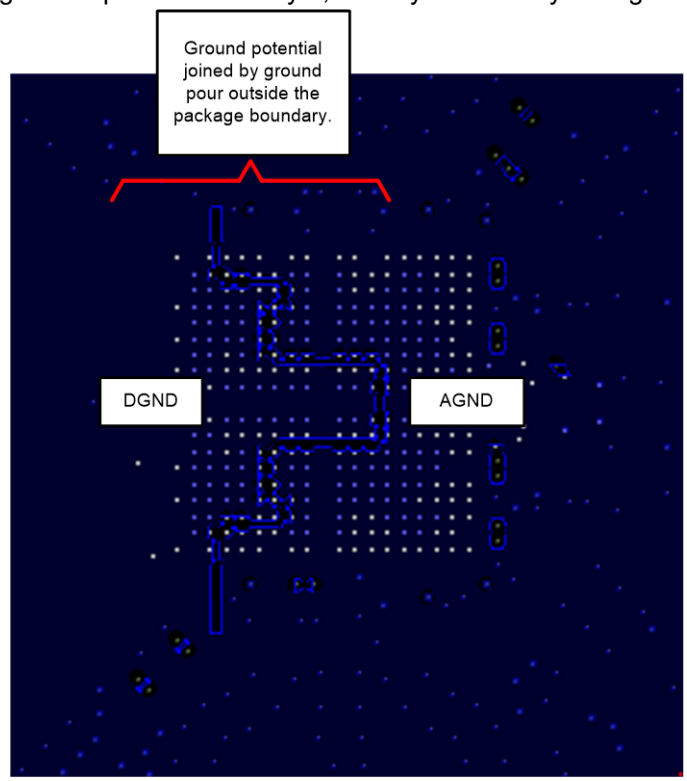
6 Ground Domain

1. TI highly recommends that no two bypass capacitors of different ground domain share the same ground via. Refer to Table 6-1 for reference of the general ground domains in reference to the specific AFE79xx device ground nets.

Table 6-1. AFE79xx Ground Net Descriptions

AFE79xx EVM GENERAL NET NAME	AFE79xx DEVICE POWER PINS	DESCRIPTION OF NETS
DGND	DGND	Digital core supply ground
	VSST	SerDes digital core supply ground
	VSSGPIO	GPIO ground
	ESD_GND	ESD protection circuit ground
AGND	VSSFB	FB ADC chain signal ground
	VSSRX	RX ADC chain signal ground
	VSSTX	TX DAC chain signal ground
Virtual VSSCLK tied to AGND	VSSFBCLK	FB ADC chain clock ground
	VSSPLL	PLL ground
	VSSPLLCLKREF	Clock reference ground
	VSSPLLFBCML	FB ADC chain clock ground
	VSSPLLRXCML	RX ADC chain clock ground
	VSSRXCLK	FB ADC chain clock ground
	VSSTXCLK	TX DAC chain clock ground
	VSSTXENC	TX DAC chain encoder ground

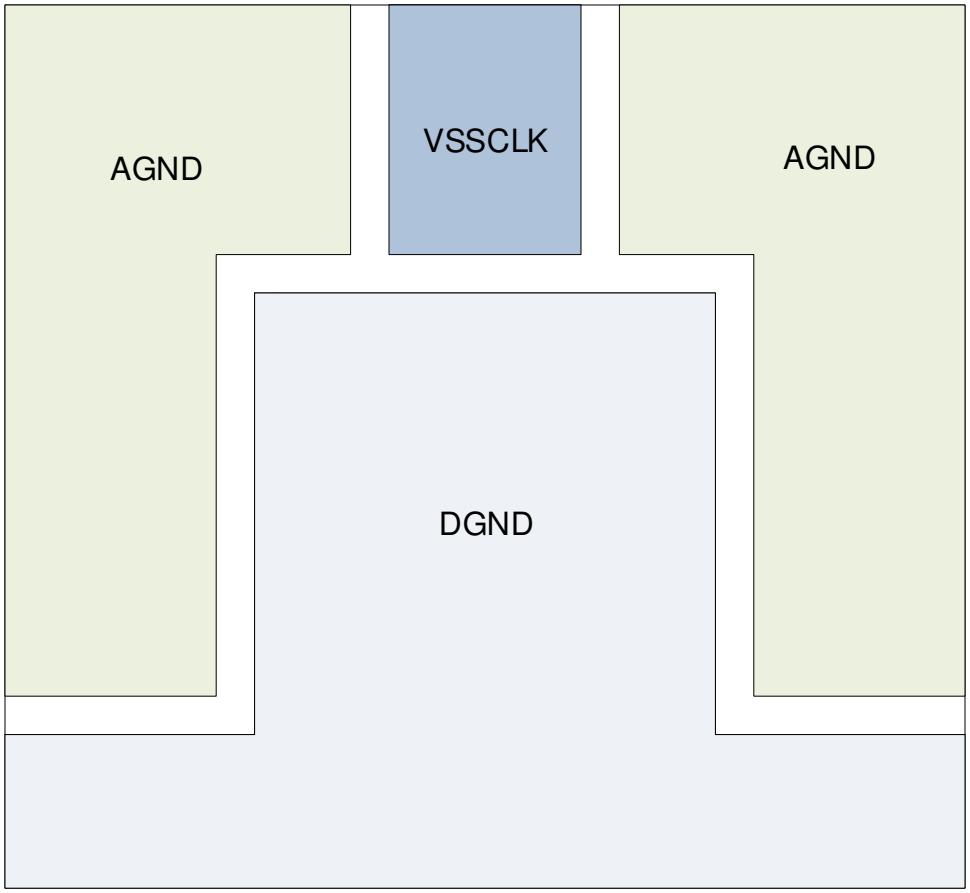
2. Sufficient lateral spacing is desired between the two power planes (approximately three time the thickness of the plane) to minimize inter-plane coupling. Alternatively, the use of ground via stitching between the two power planes further reduces inter-plane coupling.
3. All the ground layers must have ground pour underneath the AFE79xx device with a slit to isolate digital ground and analog ground, as shown in Figure 6-1. The slit must end at the boundary of the device package with sufficient ground pour outside the device package area. The ground pour outside the device package area allow the digital ground and analog to maintain the ground connection and ground potential. Any noise disturbance or ground bounce on one ground plane has to go through the larger ground pour before reaching the other ground plane. The ground pour must absorb the noise and ground bounce through PCB plane decoupling through the top and bottom layer, and layer 2 and layer 11 ground layers, respectively.



Note: VSSCLK is incorporated into AGND.

Figure 6-1. Ground Slit with Respect to the Pin-outs of the Device

4. Figure 6-2 shows the ground cut-out strategy for analog ground (AGND), digital ground (DGND), and theoretical clock ground (VSSCLK). The goal of the ground cut-out is to intentionally create inductance so the noise disturbance of one ground domain does not immediately impact the noise quality of another domain. All grounds are tied together outside the device package area to maintain ground potential. The theoretical VSSCLK ground is tied together with AGND in this PCB design for reasons to be discussed later in the applications note.



Note: VSSCLK is incorporated into AGND.

Figure 6-2. Example Ground Cut-out Strategy with Theoretical VSSCLK Cut-out

5. Figure 6-3 highlights the general ground domain with respect to the device pin mapping. This diagram helps system designers with understanding of the ground cut with respect to the device pin mapping.

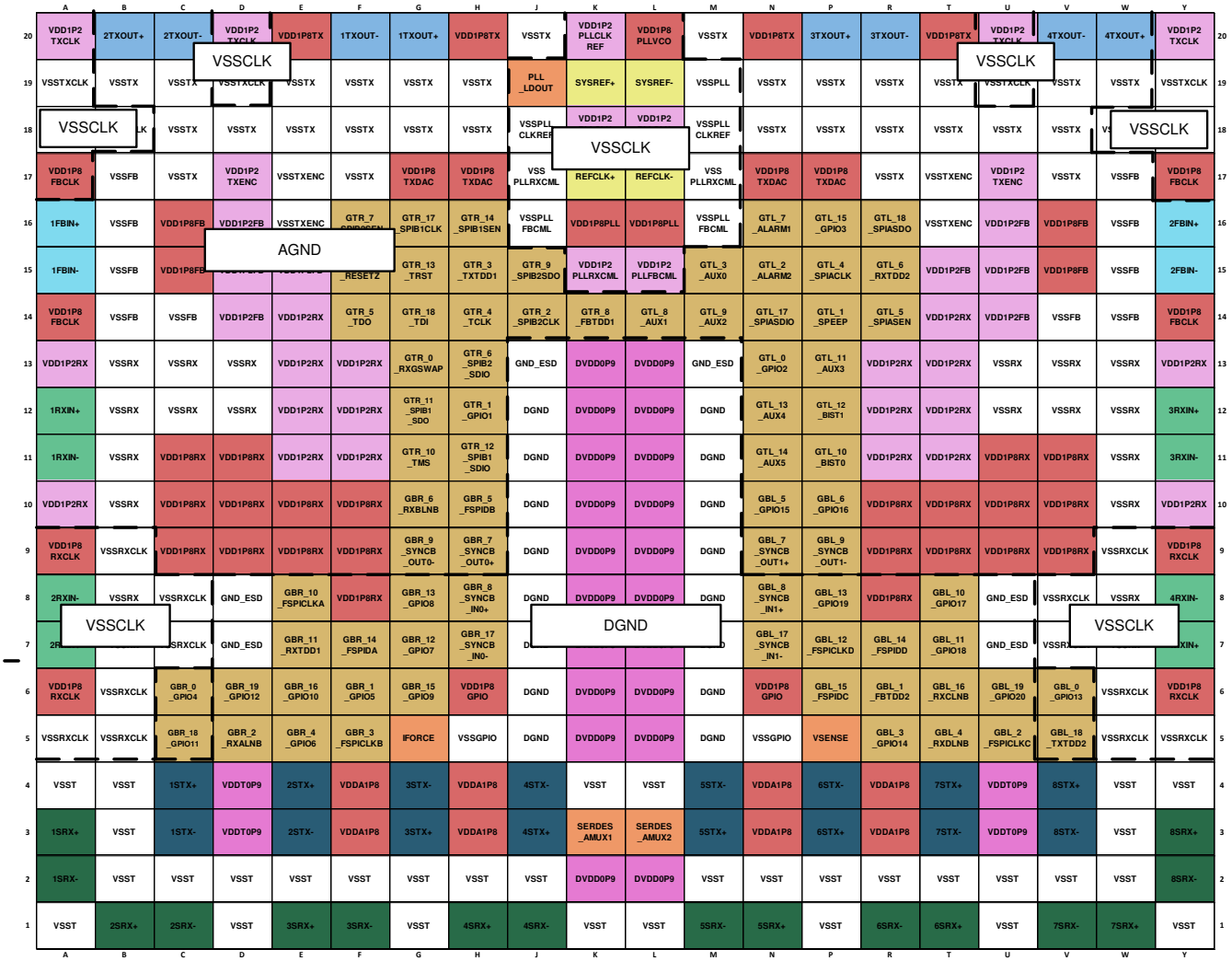


Figure 6-3. Region of DGND, AGND, and the Theoretical CLK Grounds with Respect to the AFE79xx Pin Map.

6. ESD ground (ESD_GND) and GPIO ground (VSSGPIO) are part of the digital ground cut-out (DGND). Based on the AFE79xx EVM DGND cut-out area, the ESD_GND are within the DGND boundary, as shown in Figure 6-4. The VSSGPIO is the associated ground net for the VDD1p8GPIO, as shown in Figure 6-5. The VDD1p8GPIO is typically sourced from shared 1.8-V power supply amongst the analog 1.8-V rails. Therefore, system designers must review the return path from the analog power supply to the VSSGPIO ground to ensure sufficient return path.

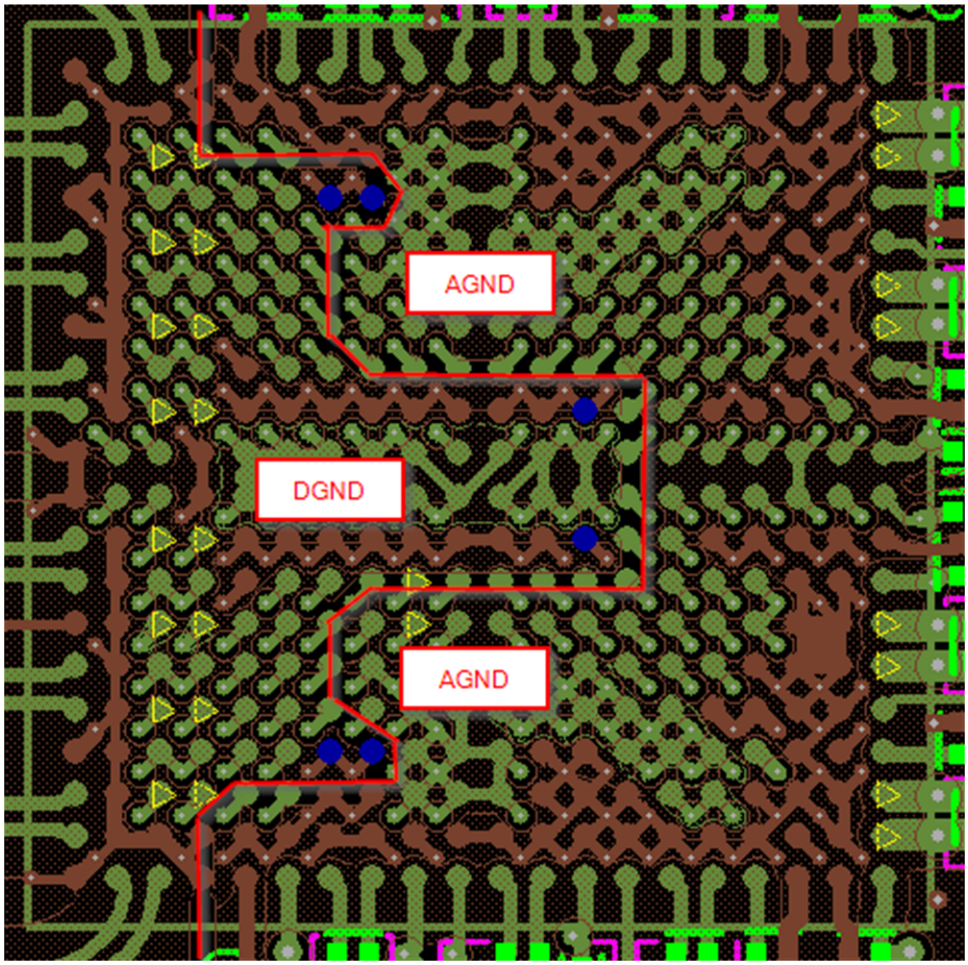


Figure 6-4. ESD_GND Balls (Shown in Blue) with Respect to the DGND Cut-out

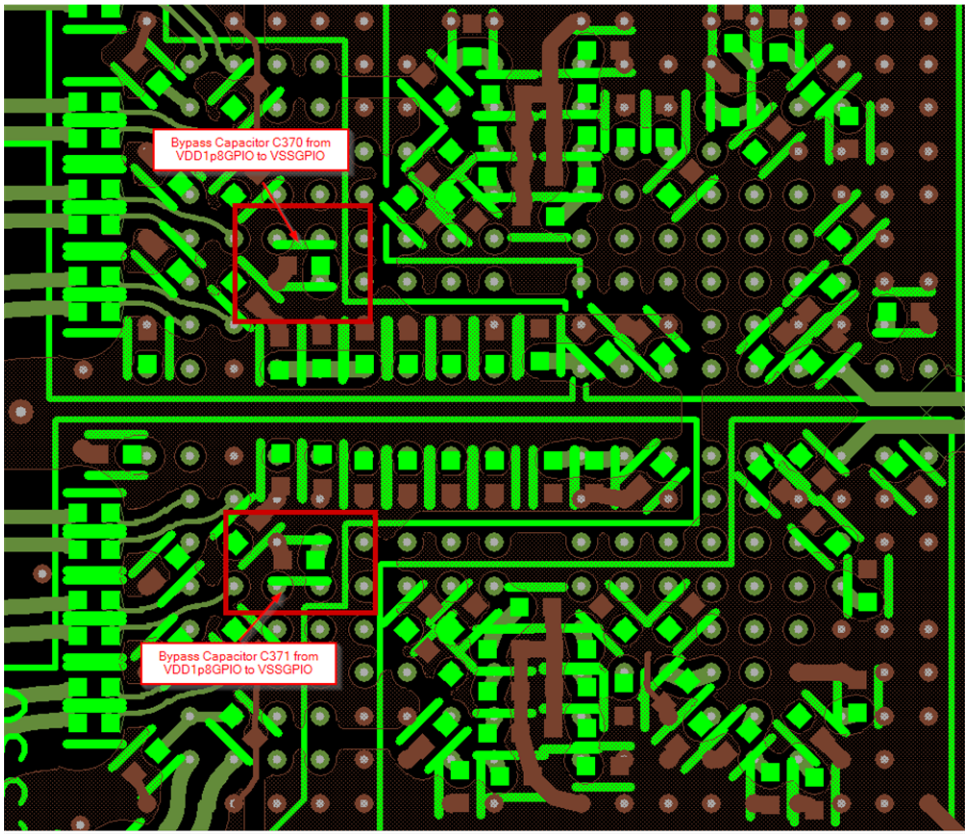


Figure 6-5. VSSGPIO Balls and VDD1p8GPIO Bypass Capacitors with Respect to DGND Cut-out

In theory, there can be another ground slit to separate out the PLL and clock distribution ground returns. Minimizing the coupling of the clocking ground and the RX, FB, and TX grounds improves the quality of the sampling clock within the RX, FB, and TX blocks. If there is coupling of the RX, FB, or TX signal or noise onto the sampling clock, the coupled signal or noise modulates itself onto the sampling clock. With a sampling clock that had been polluted, the RX, FB, and TX signal has the coupled signal modulating onto itself. This type of cyclic modulation creates harmonic distortions and degrades the noise performance of the AFE79xx. See the example diagram shown in Figure 6-6 for an example of the self-coupling of the two-tone output at the TXDAC output impacting the IMD3 performance.

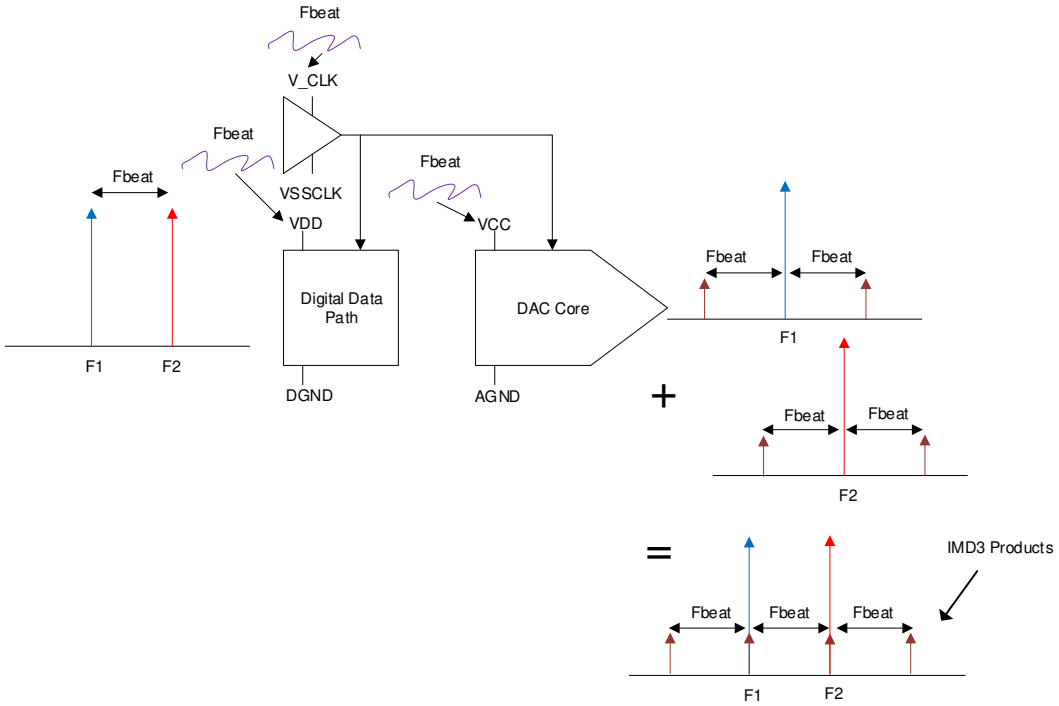
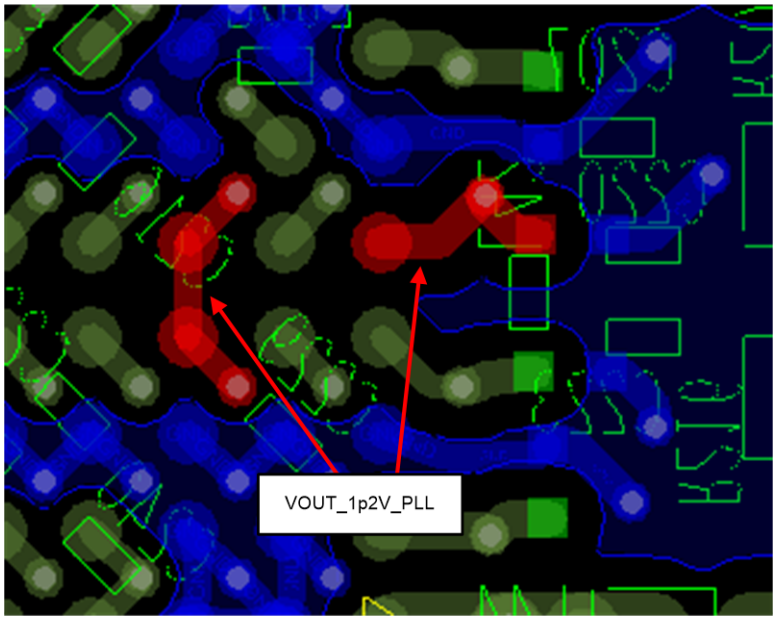


Figure 6-6. Self-Coupling of the Two-Tone Output Impacting IMD3 Performance of TXDAC

Due to space constraints, this design does not incorporate the clock ground slit. Introducing clock ground slit reduces the overall area of effective ground. Therefore, the risk of introducing ground slit can be greater than the benefit. Instead, the following considerations of clock ground isolation were done:

1. Clock power supplies are decoupled and returned to the AGND. The decoupling capacitors are oriented such that one pin is connected to clock power supplies, and another pin connected directly (to the best of ability) towards the associated clock ground. For example, the VDD1p2PLLCLKREF (power supply for the REFCLK± clock receiver) has an associated clock ground of VSS1p2PLLCLKREF.
2. To reduce the inductance introduced by the via, the following clock power supply nets were routed on the top layer: VOUT_1p8CLK, VOUT_1p2_CLK, PLLA1p8V, and VOUT_1p8_PLL. See earlier section for details.
3. Figure 6-7 demonstrates the decoupling capacitor orientation of the VDD1P2PLLCLKREF (power supply for the REFCLK± clock receiver). This routing method has a direct connection from the VDD1P2PLLCLKREF to the VSSPLLCLKREF pins.



VOUT_1p2V_PLL routed on the top layer to minimize the amount of via used for decoupling path.

Figure 6-7. VOUT_1p2V_PLL Routing Example

4. PLL_LDOUT is the internal LDO for the on-chip PLL. The 0.1-µF capacitor must be tied close to the clock ground region. Since the PLL_LDOUT net is related to the internal PLL/VCO/clocking circuitry, the return path of the resistor termination must be routed directly to the VSSPLLCLKREF pin located in pin J18.

Figure 6-8. PLL_LDOUT 0.1-µF Capacitor Routing From Pin J19 (PLL_LDOUT) to Pin J18 (VSSPLLCLKREF)

5. If the PCB design has a common 1.8-V power supply source to share to multiple AFE79xx PLLA1p8V (VDD1p8PLLVCO) nets, then the VDD1p8PLLVCO nets must have sufficient filtering to prevent multiple AFE79xx VCO crosstalk and VCO pulling mechanism through common power supply node. See Figure 6-9 for filtering recommendation.

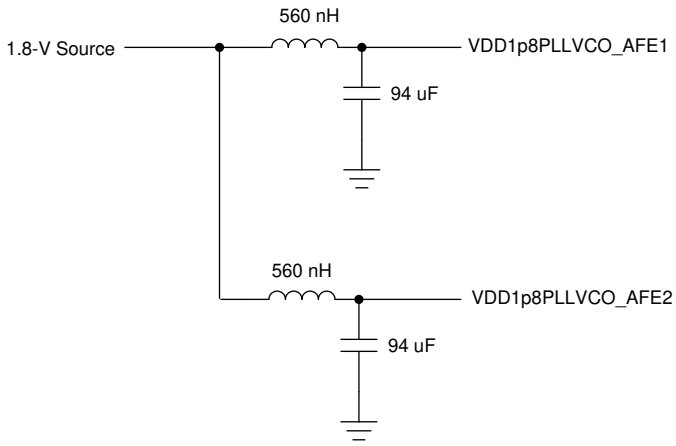


Figure 6-9. Power Net Isolation Filter

7 Bypass Capacitors Guidelines

1. All bypass capacitors must be connected to the planes with a via in pad, and placed between the pin and plane.
2. Minimize stubs on the bypass capacitors to avoid inductance. Any series inductance on the bypass capacitor path degrades the decoupling performance.
3. Local Decoupling Capacitors: the smaller physical size bypass capacitors with largest available capacitance value are placed close to the BGA, preferably as close to the pin as possible. These are for localized decoupling for the device.
4. Bulk Decoupling Capacitors: the larger capacitance value capacitors are placed close to the supply source. These are the bulk decoupling capacitors to stabilize the overall power supply ripples and noise.

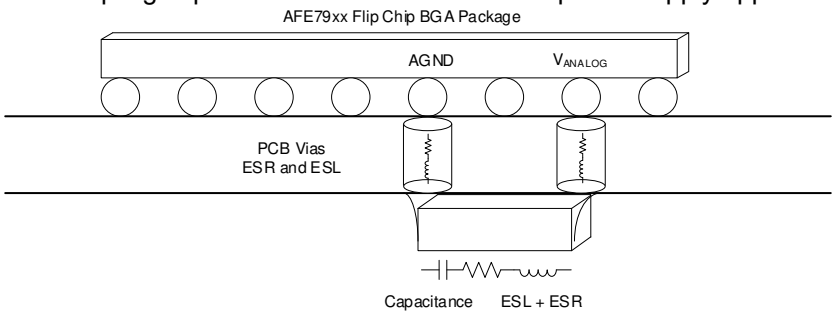


Figure 7-1. Decoupling Capacitor Limitations Due to Capacitor Package ESL and ESR and Via ESL and ESR

8 General RF Placement Methodologies:

1. For optimal isolation of RF signals, the PCB designer can stagger the RF input and RF outputs. For instance, place RX A and RX C on the top layer, and place RX B and RX D on the bottom layer.

Figure 8-1. Example AFE79xx Signal Placement Strategy

2. In this design, all RF inputs and outputs are placed on the same layer to show case typical isolation performance with minimum use of vias in the signal routing.
3. RF ground layer is inserted immediately after the top layer and before the bottom layer for impedance controlled layout.
4. The differential RF traces must be routed as 100-Ω CPWG (coplanar waveguide with lower ground plane) or microstrip. The 100-Ω traces for the RXADC and FBADC are 100-Ω differential to the baluns, and then 50-Ω single-ended from balun to the SMA connectors. The TXDAC outputs are routed as 50-Ω based CPWG from the TXDAC output to the balun, and then 50-Ω single-ended from the balun to the SMA connectors.
5. Power grounds are inserted between the two power layers. This is to minimize coupling of the power supply nets when the power supply nets are overlaying on top of each other. For instance, Layer 4 is a power ground, and it is inserted in between Layer 3 and Layer 5 power layers, as shown in Figure 8-2. Refer to Table 3-1 for stack up information.

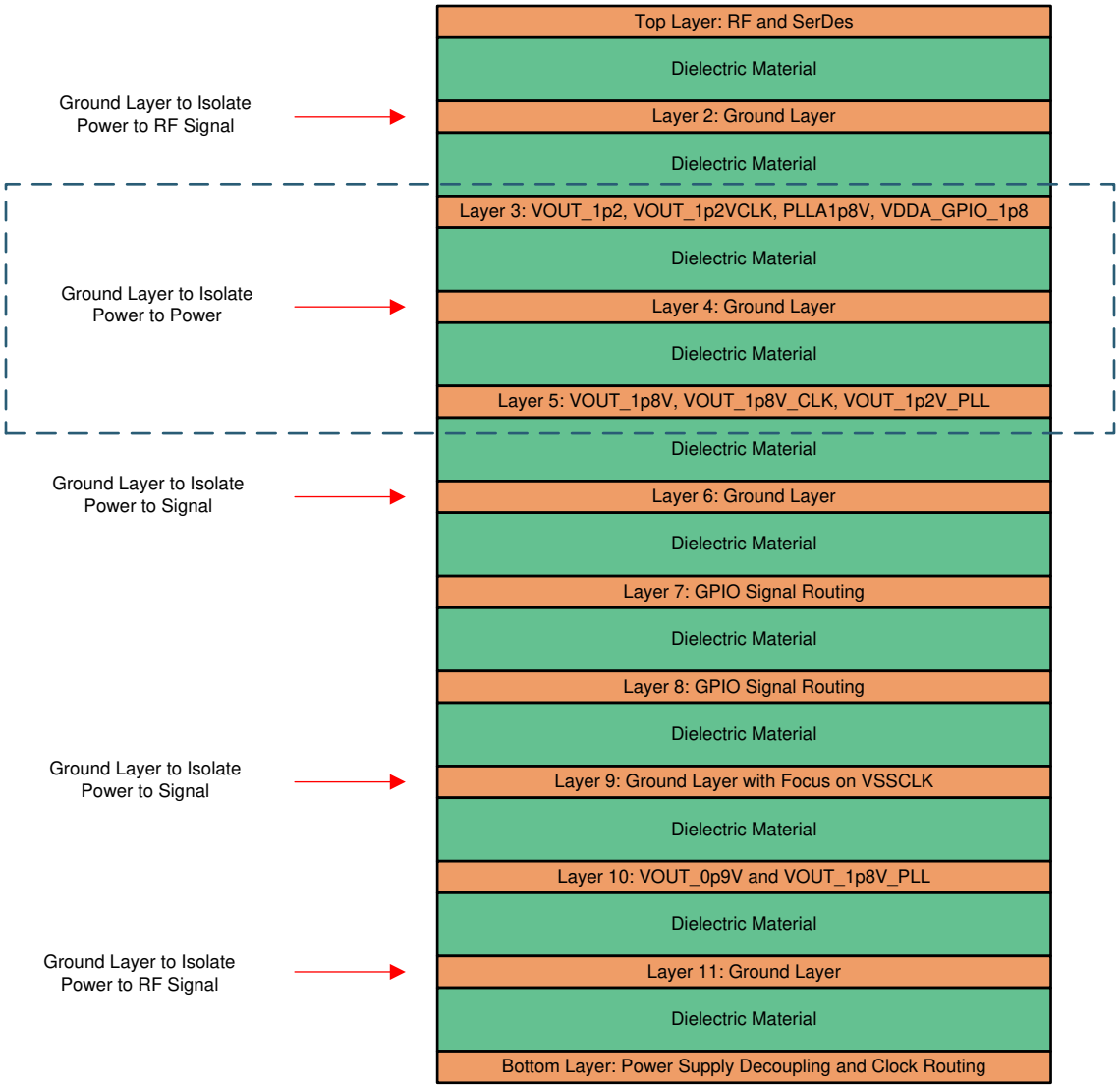


Figure 8-2. AFE79xx Stack-up and Ground Isolation Layers

6. The CLKp/m input must be routed on the furthest layer from the TX outputs and go to the CLKp/m BGA ball through impedance-controlled vias. Because the use of vias is unavoidable, TI recommends having only one differential via routing to transition from the device placement layer (either top layer or bottom layer) to the middle layer. Routing the CLKp/m input on the bottom layer and TX outputs on the top layer helps achieve maximum isolation between CLK and TX. Any TX leakage into the CLK path degrades the harmonic distortion performance of the TX.
7. If the SerDes pairs are not routed on the top/bottom layer, TI recommends using blind vias or back-drilled vias to reach the BGA ball on the top layer. This is primarily to avoid stubs on the signal line.
8. TX Routing Guidelines:
   a. TXDAC output has default 50-Ω internal termination. The traces from the TX is 50-Ω differential and is routed as 50-Ω based CPWG. The bias networks are placed in the bottom layer with condensed RF choke and bypass capacitors, and the bias networks can be treated as lumped element network.
   b. A matching network is required at TXDAC output to match the output impedance to either 50-Ω or 100-Ω. 50-Ω based matching typically yields a wider bandwidth matching. However, in principle, by changing the matching network component values, the user can match it to 100-Ω also. Internal termination must be set at 50-Ω by default. The TX output matching network design strategy is listed as following:
      i. The TXDAC internal termination should be kept as 50-Ω for optimal power delivery and performance.
      ii. Place matching network to match output impedance to 50-Ω or 100-Ω near the AFE79xx TX output pins. The 50-Ω to 100-Ω matching requires matching transformation design technique.
      iii. Check output power and performance.

iv. If the output power need to be increased due to system requirement, changing TX output termination to 100-Ω is possible. The output power will increase by about 2dB at the expense of potential IMD3 and APCR performance degradation.

c. Transformer center bias: the routing of the DC bias to the center tap pin (DC bias pin) of the balun may cause some resonance in certain band matching. Currently, for the TXDAC output, the inductor chokes are used to bias the TXDAC output while the center tap pin is grounded. TI recommends to always follow the manufacturer's DC feed guideline if at all possible to reduce DC feed line resonance.

d. Below is side to side comparison: Figure 8-3 is an example with minimum resonance. RF choke is used on the TXDAC side to bias the DAC with the center tap pin of the balun grounded. This is the current recommended option. Figure 8-4 is an example to use DC feed line of the balun. The DC line had caused some resonance in matching.

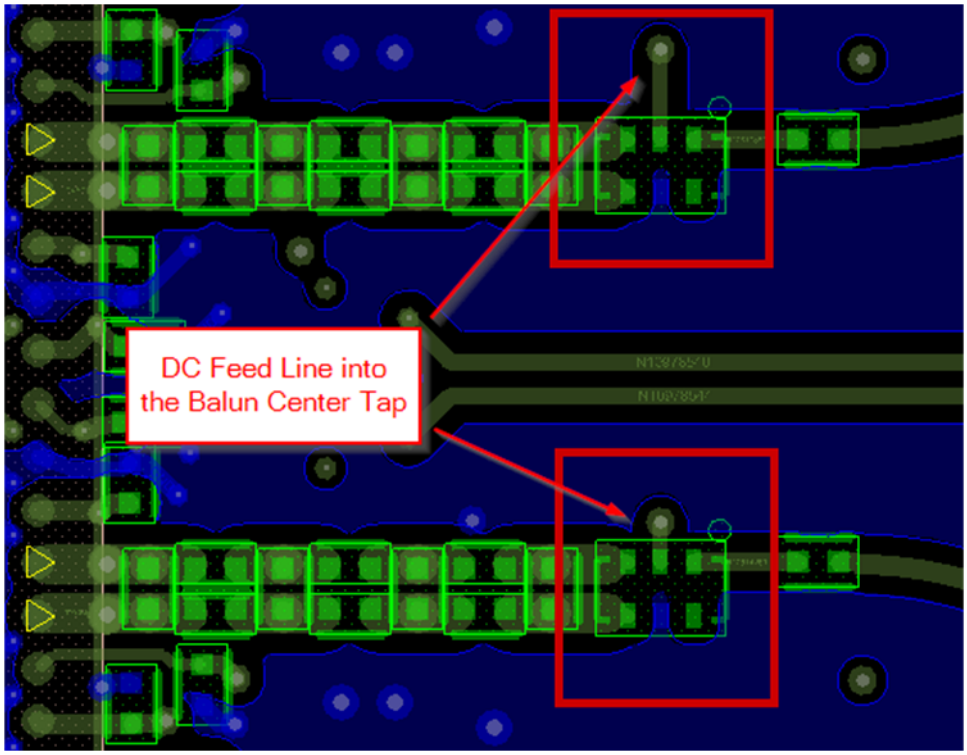


Figure 8-3. Former Implementation: DC Feed Line into the Balun Center Tap

Figure 8-4. Current Implementation: DC Feed Line Directly Grounded. Bais Provided Through RF Chokes

9. For optimal RXADC and FBADC noise figure performance, TI recommends to avoid the usage of STX1 and STX8 SerDes lanes. If these two STX lanes are used, the noise spectral density (NSD) performance will degrade slightly on 2RX and 4RX ADC inputs. The use of JESD204 lane mux help mitigate the usage of STX1 and STX8 SerDes lanes with the following example STX routing.
   a. If number of STX lanes is less than six, avoid STX1 and STX8 lanes and assign JESD204 output to STX2, STX3, STX4, STX5, STX6, and STX7.
   b. If only four STX lanes are required, then assign JESD204 output to STX3, STX4, STX5, and STX6.
   c. If only two STX lanes are required, then assign JESD204 output to STX3 and STX4.
   d. The power-down programming register is tied to group of two STX lanes. For instance, STX1 and STX2 share a power-down register, and STX3 and STX4 share a power-down register. Similarly, each group of four STX lanes have a common SerDes PLL. For instance, STX1, STX2, STX3, and STX4 have one SerDes PLL, while STX5, STX6, STX7, and STX8 have another SerDes PLL. Please consider this power consumption saving feature when planning STX mapping.
   e. The usage of the STX1 and STX8 lanes cannot be avoided if the JESD204 mode requires all eight STX lanes to be active.
10. At the final stage of the layout, perform the following steps:
   a. Stitch up ground layers around the RF and SerDes traces through ground stitching with ground vias.
   b. Remove small patch of ground pour that do not have ground vias to avoid connections to floating grounds.

9 JESD204 Protocol Guidelines

There are many differences in the various high-speed standards that need to be taken into account when designing the layout of a system. The AFE79xx has up to eight pairs of high-speed SerDes transceivers to support JESD204B and JESD204C standard for data converter link transfer. For specific guidelines on the physical layer requirements for the JESD204 standard, refer to section 5 of the JESD204 standard at the JEDEC website.

For reference regarding the JESD204 in general, refer to the following application notes:

- *System Design Considerations when Upgrading from JESD204B to JESD204C Application Note*
- *Ready to Make the Jump to JESD204B? Application Note*

10 General High-Speed Signal Routing

10.1 Trace Impedance

For high-speed signals, trace impedance needs to designed as to minimize the reflections in traces. There are two types of trace impedance that need to be taken into consideration when designing high-speed signals. Single-ended impedance is the trace impedance with reference to ground. Differential Impedance is the impedance between two differential pair signal traces.

The high-speed protocol that is being designed for determines what the single and differential trace impedance the traces need to meet, as well as the tolerance for the impedance (for example, 50 Ω ±15%). To have designs be robust from PCB manufacturing errors and defects, design the traces impedance to be as close to the recommended value as possible. The geometry of the traces, the permittivity of the PCB material and the layers surrounding the trace all impact the impedance of the signal trace.

There are many tools available to calculate the trace impedance on high-speed traces. Most board manufactures have a preferred tool that PCB designers can use to calculate the impedance, but there are also many available online.

10.2 High-Speed Signal Trace Lengths

As with all high-speed signals, keep total trace length for signal pairs to a minimum. Some standards have a maximum trace or cable length that is specified in the various specifications.

10.3 Landing Pad Guideline

Avoid width and spacing difference when entering a landing pad, for example a balun, by tapering or redefining width and space rules for the traces. This minimizes impedance mismatches when entering or exiting devices.

10.4 High-Speed Signal Trace Length Matching

Match the etch lengths of the relevant differential pair traces. Intra-pair skew is the term used to define the difference between the etch length of the + and - lane of a differential pair. Inter-pair skew is used to describe the difference between the etch lengths of a differential pair from another differential pair of the same group. The etch length of the differential pair groups do not need to match. For example the etch lengths of JESD204 TX and RX do not need to match. There are also standards that do not have a inter-pair skew requirement because the different lanes do not have to be the same length. When matching the intra-pair skew of the high-speed signals, add serpentine routing to match the lengths as close to the mismatched ends as possible. Refer to Figure 10-2.

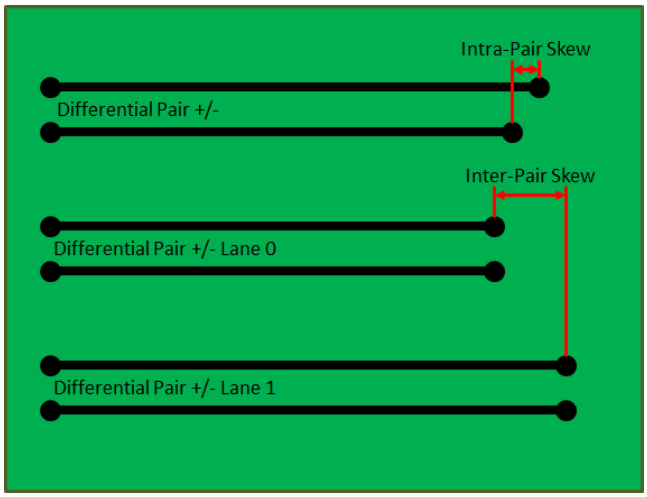


Figure 10-1. Inter Versus Intra Pair Skew

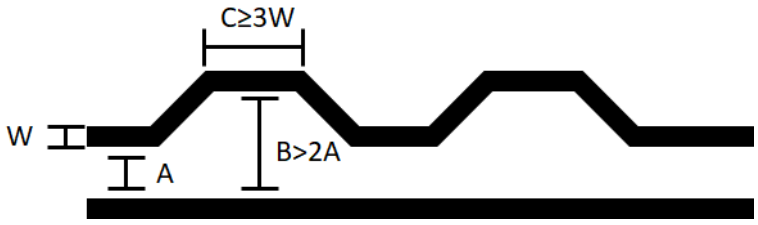


Figure 10-2. Serpentine Trace Geometry

Use the above recommendations for the traces serpentine geometry. For example the width of the trace (W) is 4 mils and the distance between the differential pair (A) is 4.5 mils. These mean that the width of the serpentine (B) is at least 9 mils and the length of C is at least 13.5 mils. These example recommendations are based on FR4 material and an 8-mil distance to the ground.

10.5 Return Path

An electrical circuit must always be a closed loop system. With DC, the return current takes the way back with the lowest resistance for DC signals.

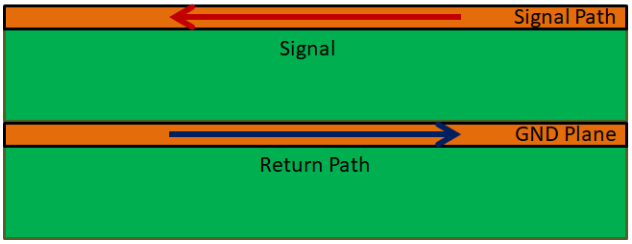
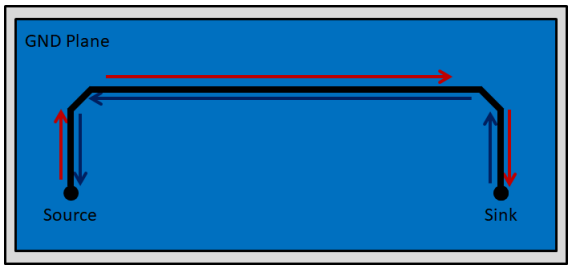


Figure 10-3. Return Path

At higher frequencies, the return current flows along the lowest impedance path. This lowest impedance path is usually the reference plane adjacent to the signal; see the Figure 10-4. For this reason, it is always best to have a ground plane or power plane on the layer above or below a signal layer. This return path helps to reduce impedance changes and decrease EMI issues.

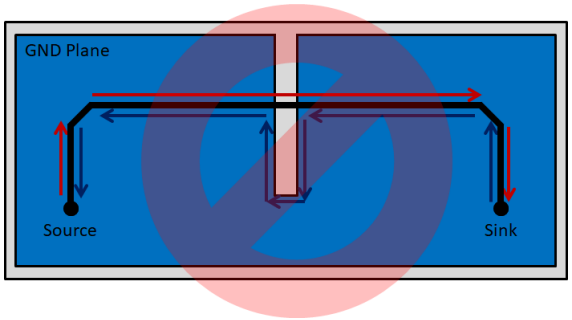


The red arrows are the signal path and the blue arrows are the return path.

Figure 10-4. High Frequency Return Path

10.6 High-Speed Signal Reference Planes

High-speed signals must be routed over a solid GND reference plane, and not across a plane split or a void in the reference plane unless absolutely necessary. TI does not recommend high-speed signal references to power planes unless it is completely unavoidable.



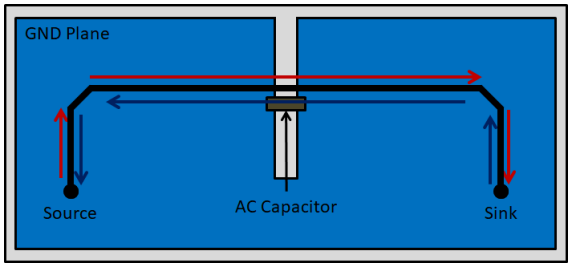
The red arrows are the signal path and the blue arrows are the return path.

Figure 10-5. To Avoid: Routing Across a Split Plane

Routing across a plane split or a void in the reference plane forces return high-frequency current to flow around the split or void. Figure 10-5 shows that the return path must take a longer route than the signal path. This can result in the following conditions:

- Excess radiated emissions from an unbalanced current flow
- Delays in signal propagation delays due to increased series inductance
- Interference with adjacent signals
- Degraded signal integrity (that is, more jitter and reduced signal amplitude)

If routing over a plane-split is completely unavoidable, place stitching capacitors across the split to provide a return path for the high-frequency current. These stitching capacitors minimize the current loop area and any impedance discontinuity created by crossing the split. These capacitors must be 1 µF or lower, and placed as close as possible to the plane crossing.



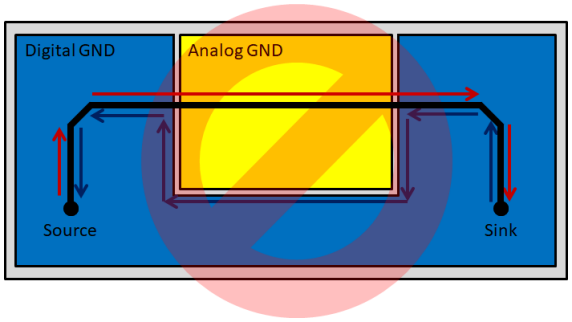
The red arrows are the signal path and the blue arrows are the return path.

Figure 10-6. To Do if Necessary: AC Capacitor Across a Split Plane

When planning a PCB stackup, ensure that planes that do not reference each other are not overlapped because this produces unwanted capacitance between the overlapping areas. To see an example of how this capacitance could pass RF emissions from one plane to the other, refer to Figure 10-7.

It is best to avoid routing across different reference planes because it can cause impedance issues as well as EMI issues.

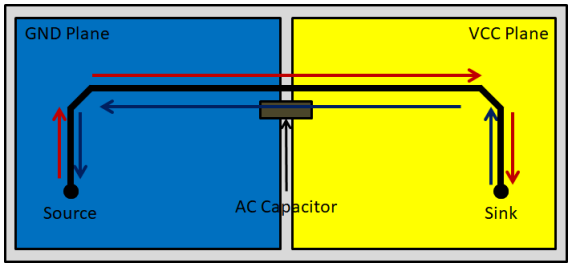
Do not change the reference plane of the high-speed signal trace unless completely unavoidable.



The red arrows are the signal path and the blue arrows are the return path.

Figure 10-7. To Avoid: Routing Across Different Reference Planes

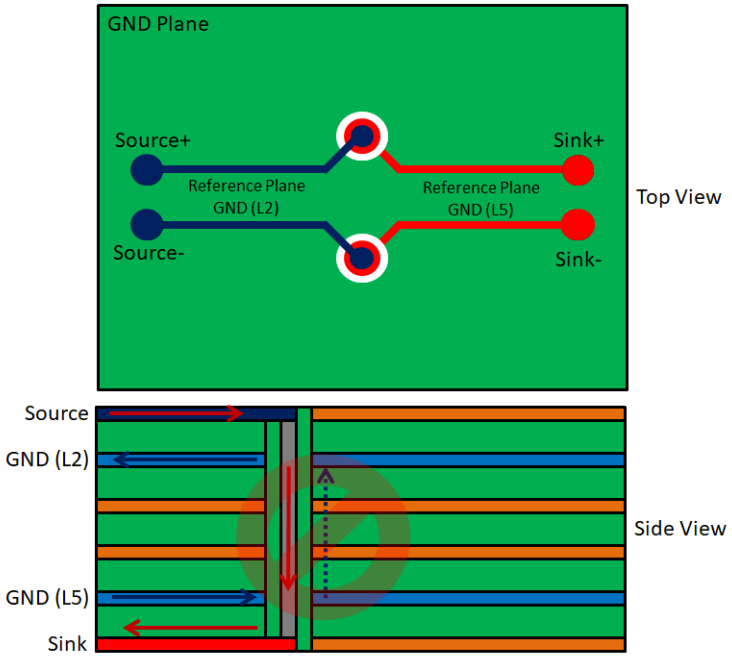
If routing across different reference planes cannot be avoided, use AC capacitors to allow the return current to have a pathway. For the AFE79xx of mixed-signal applications, the type of power plane and ground plane must match in either digital domain or analog domain. For instance, the use of AC coupling capacitor to bridge DVDD and AGND is not acceptable as digital activities leaks into analog ground potential.



The red arrows are the signal path and the blue arrows are the return path.

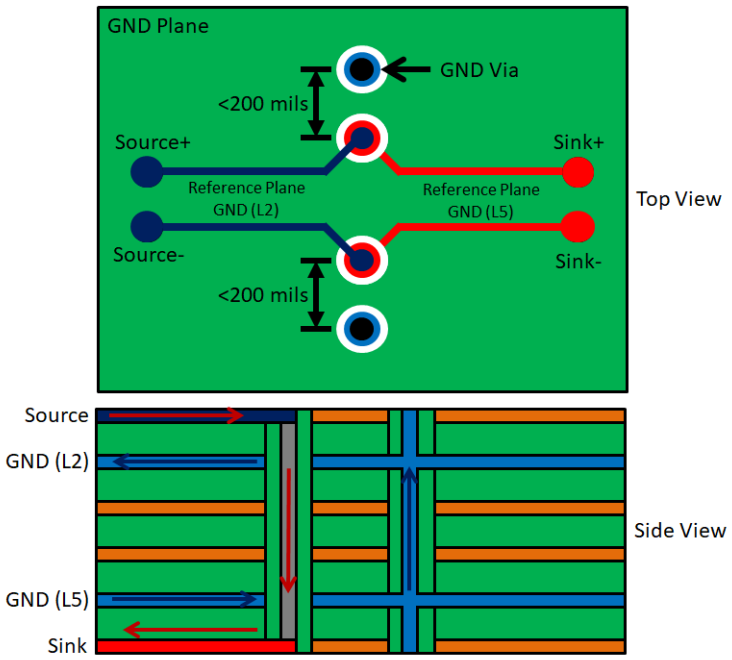
Figure 10-8. To Do if Necessary: Routing Across Different Reference Planes with AC Capacitor

The entirety of any high-speed signal trace must maintain the same GND reference from origination to termination. If unable to maintain the same GND reference, via-stitch both GND planes together to ensure continuous grounding and uniform impedance. Place these stitching vias symmetrically within 200 mils (center-to-center, closer is better) of the signal transition vias. Via stitching is typically done on single-ended, high-speed traces, as the signal trace need to reference to continuous ground. Differential traces rely on both positive and negative traces for the signal return, and may not necessary require via stitching. If via stitching and good ground reference are required for differential traces, then the following diagrams show an example to avoid, and an example to follow.



The red arrows are the signal path and the blue arrows are the return path.

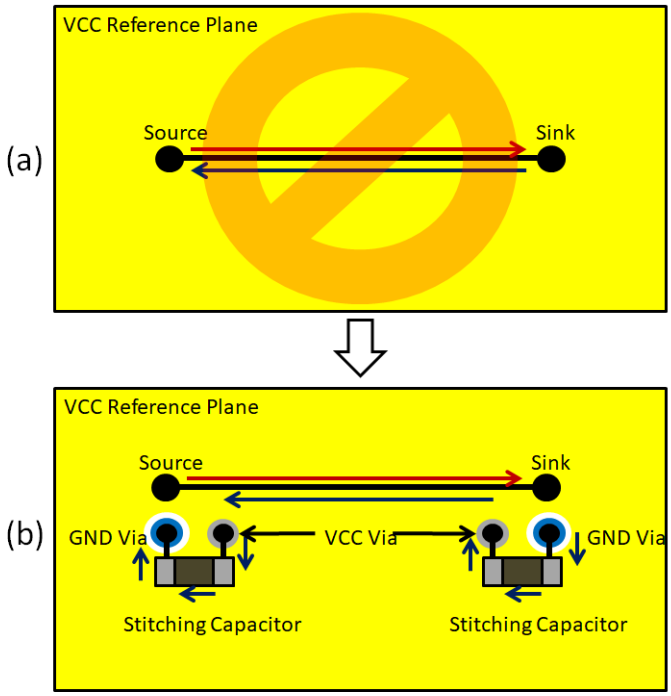
Figure 10-9. To Avoid: Differential Pair Via Return Path Without GND Vias



The red arrows are the signal path and the blue arrows are the return path.

Figure 10-10. To Do at All Times: Differential Pair Via Return Path with GND Vias

TI does not recommend high-speed signal references to power planes unless it is completely unavoidable. If it is unavoidable, it is best to use AC coupling capacitors and ground vias to allow the return signal to have a path back from the sink to the source. Figure 10-11 depicts the use of AC coupling capacitors and ground vias for the return path. The type of power plane to use for the use case depends on the signal. For instance, if the trace is SerDes I/O, then DVDD plane is acceptable. If the trace is RF signal, then analog power plans are acceptable.



The red arrows are the signal path and the blue arrows are the return path.

Figure 10-11. To Do if Necessary: VCC Reference Plane

11 High-Speed Differential Signal Routing

11.1 Differential Signal Spacing

To minimize crosstalk in high-speed interface implementations, the spacing between the signal pairs must be a minimum of five times the width of the trace. This spacing is referred to as the 5W rule. For typical PCB layout, the 5W rule may be too stringent and may not meet the cost and PCB area requirement. Therefore, 3W (or 3 times the width of the trace for spacing) can be acceptable in some cases. A PCB design with a calculated trace width of 6 mils requires a minimum of 30 mils spacing between high-speed differential pairs. Also, maintain a minimum keep-out area of 30 mils to any other signal throughout the length of the trace. Where the high-speed differential pairs come adjacent to a clock or a periodic signal, increase this keep-out to a minimum of 50 mils to ensure proper isolation. For examples of high-speed differential signal spacing, see Figure 11-1 and Figure 11-2.

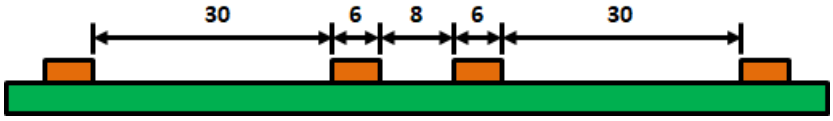


Figure 11-1. Differential Pair Spacing Next to Other Signals

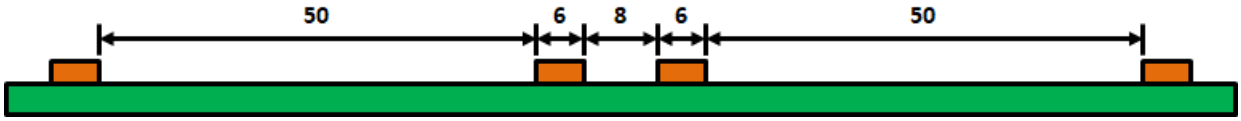


Figure 11-2. Differential Pair Spacing Next to Clock or a Periodic Signal

In devices that include multiple high-speed interfaces, avoiding crosstalk between these interfaces is important. To avoid crosstalk, ensure that each differential pair is not routed within 30 mils of another differential pair after package escape and before connector termination.

11.2 Additional High-Speed Differential Signal Rules

- Do not place probe or test points on any high-speed differential signal.
- Do not route high-speed traces under or near:
  - Crystals
  - Oscillators
  - Clock signal generators
  - Switching power regulators
  - Mounting holes
  - Magnetic devices
  - ICs that use or duplicate clock signals
- After BGA breakout, keep high-speed differential signals clear of the SoC because high current transients produced during internal state transitions can be difficult to filter out.
- When possible, route high-speed differential pair signals on the top or bottom layer of the PCB with an adjacent GND layer.
- Ensure that high-speed differential signals are routed ≥ 90 mils from the edge of the reference plane.
- Ensure that high-speed differential signals are routed at least 1.5 W (calculated trace-width × 1.5) away from voids in the reference plane. This rule does not apply where SMD pads on high-speed differential signals are voided.
- Maintain constant trace width after the SoC BGA escape to avoid impedance mismatches in the transmission lines.
- Maximize differential pair-to-pair spacing when possible.

11.3 Symmetry in the Differential Pairs

Route all high-speed differential pairs together symmetrically and parallel to each other. Deviating from this requirement occurs naturally during package escape and when routing to connector pins. These deviations must be as short as possible, and package break-out must occur within 0.25 inches of the package.

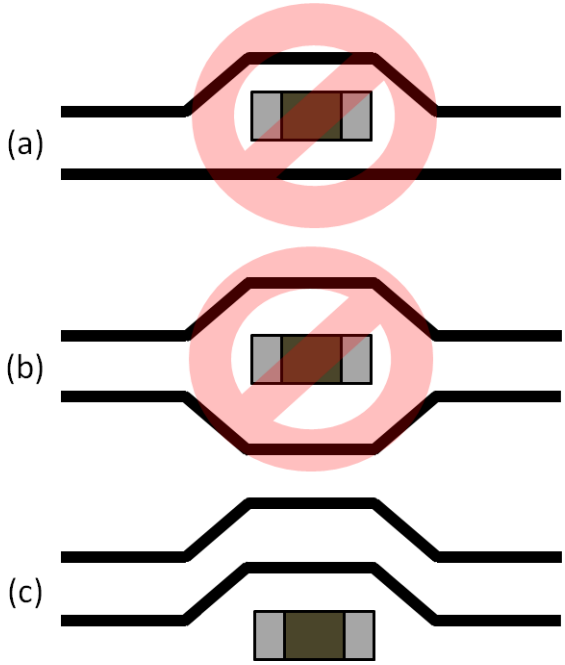
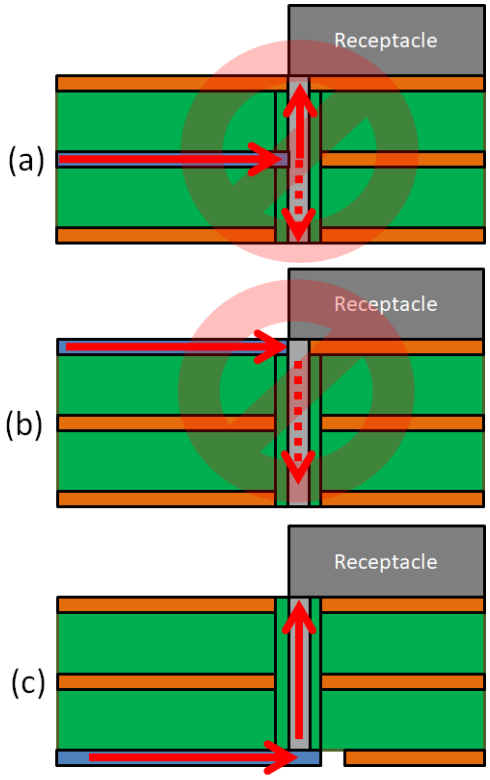


Figure 11-3. Differential Pair Symmetry

11.4 Connectors and Receptacles

When implementing a through-hole receptacle (like a VITA57-based FMC), TI recommends making high-speed differential signal connections to the receptacle on the bottom layer of the PCB. Making these connections on the bottom layer of the PCB prevents the through-hole pin from acting as a stub in the transmission path. For surface-mount receptacles, make high-speed differential signal connections on the top layer. Making these connections on the top layer eliminates the need for vias in the transmission path.



(a): Signal coming from the middle of the PCB
(b): Signal coming from the top of the PCB
(c): Signal coming from the bottom of the PCB

Figure 11-4. Receptacle Stubs Mitigation

11.5 Via Discontinuity Mitigation

A via presents a short section of change in geometry to a trace, and can appear as a capacitive or an inductive discontinuity. These discontinuities result in reflections and some degradation of a signal as it travels through the via. Reduce the overall via stub length to minimize the negative impacts of vias (and associated via stubs).

Because longer via stubs resonate at lower frequencies and increase insertion loss, keep these stubs as short as possible. In most cases, the stub portion of the via presents significantly more signal degradation than the signal portion of the via. TI recommends keeping via stubs to less than 15 mils. Longer stubs must be back-drilled. For examples of short and long via lengths, see Figure 11-5 and Figure 11-6.

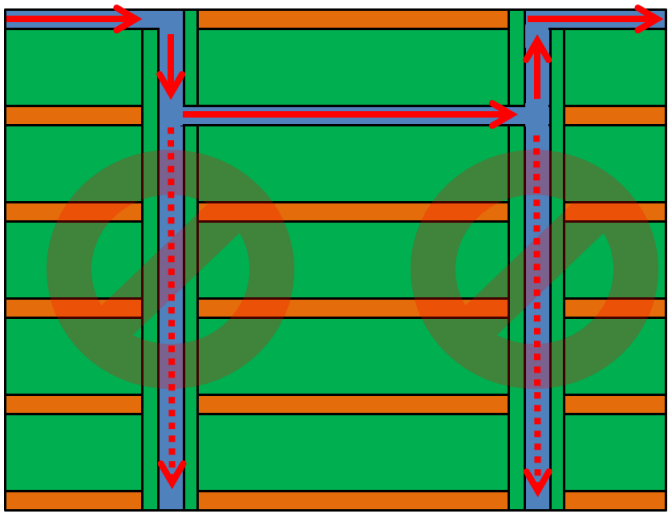


Figure 11-5. To Avoid: Vias With Long Stubs

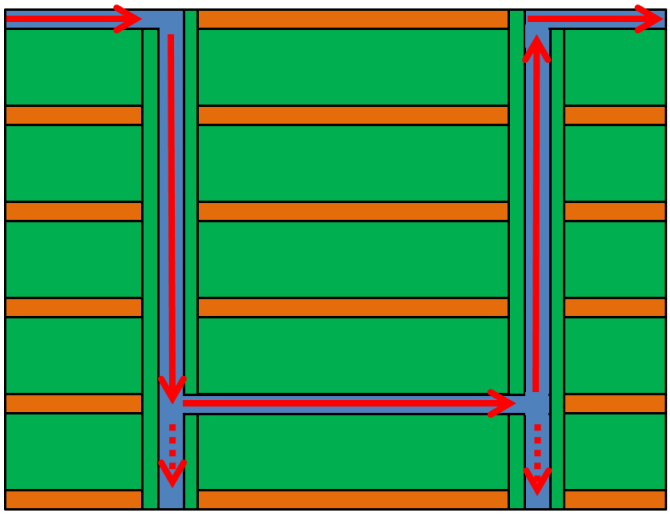


Figure 11-6. To Do if Necessary: Vias With Short Stubs

11.6 Back-Drill Stubs

Back-drilling is a PCB manufacturing process in which the undesired conductive plating in the stub section of a via is removed. To back-drill, use a drill bit slightly larger in diameter than the drill bit used to create the original via hole. When via transitions result in stubs longer than 15 mils, back-drill the resulting stubs to reduce insertion losses and to ensure that they do not resonate.

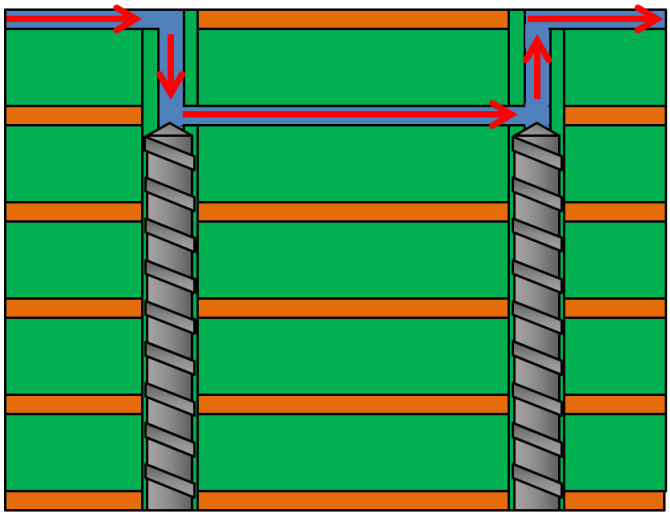


Figure 11-7. To Do: Long Vias With Back-Drilled Stubs

11.7 Trace Stubs

For high-speed signals, it is important to minimize stubs on high-speed traces to reduce increase insertion loss. Figure 11-8 depicts a high-speed trace with a component on a stub. This stub can be reduced to:

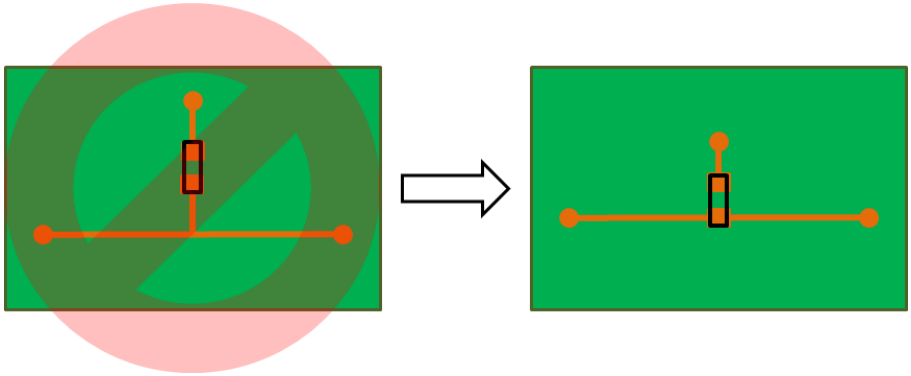


Figure 11-8. To Do: Reducing Stub Length

11.8 Increase Via Anti-Pad Diameter

Increasing the via anti-pad diameter reduces the capacitive effects of the via and the overall insertion loss. Ensure that anti-pad diameter for vias on any high-speed signal are as large as possible (30 mils provides significant benefits without imposing undue implementation hardship). The copper clearance, indicated by this anti-pad, must be met on all layers where the via exists, including both routing layer and plane layers. The traces connecting to the via barrel contain the only copper allowed in this area; non-functional or unconnected via pads are not permitted. For an example of a via anti-pad diameter, see Figure 11-9.

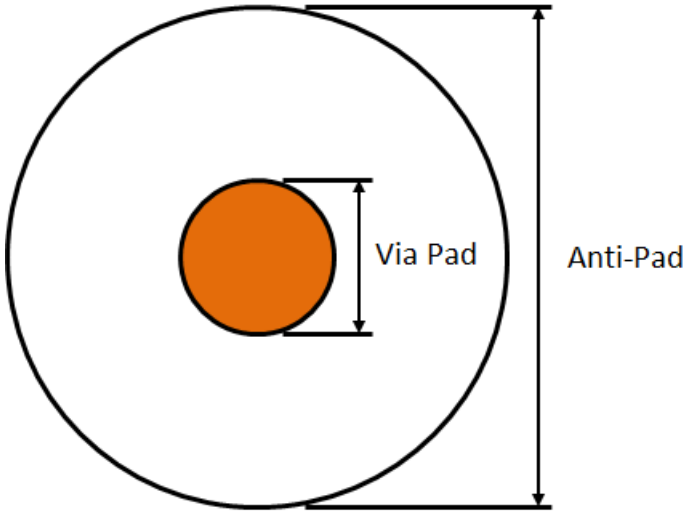


Figure 11-9. Via Anti-Pad

11.9 Equalize Via Count

If using vias is necessary on a high-speed differential signal trace, ensure that the via count on each member of the differential pair is equal, and that the vias are as equally spaced as possible. It is important to make sure that the different lanes that lengths need to match have the same amount of vias on the lines. Also, designers must take into account the length of the vias when verifying parameters like inter-pair skew.

11.10 Surface-Mount Device Pad Discontinuity Mitigation

Avoid including surface-mount devices (SMDs) on high-speed signal traces because these devices introduce discontinuities that can negatively affect signal quality. When SMDs are required on the signal traces (for example, JESD204B/C SerDes Lane AC coupling capacitors), TI strongly recommends using 0402 or smaller

to match the high speed signal trace width. Place these components symmetrically during the layout process to ensure optimum signal quality and to minimize reflection. For examples of correct and incorrect AC coupling capacitor placement, see Figure 11-10.

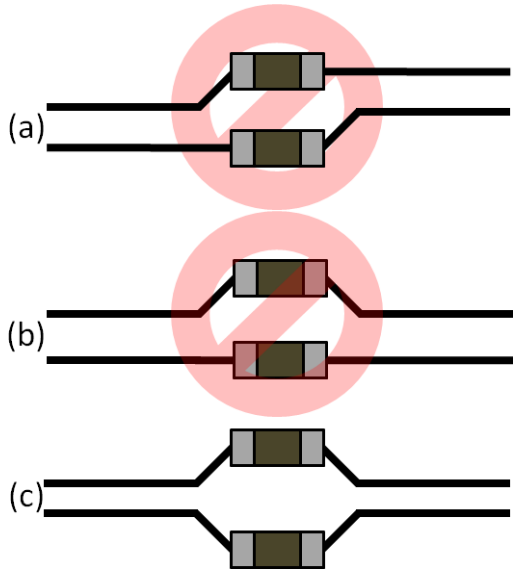


Figure 11-10. AC-Coupling Capacitor Placement

To minimize the discontinuities associated with the placement of these components on the differential signal traces, TI recommends voiding the SMD mounting pads of the reference plane by 100%. This void must be at least two PCB layers deep. For an example of a reference plane voiding of surface mount devices, see Figure 11-11.

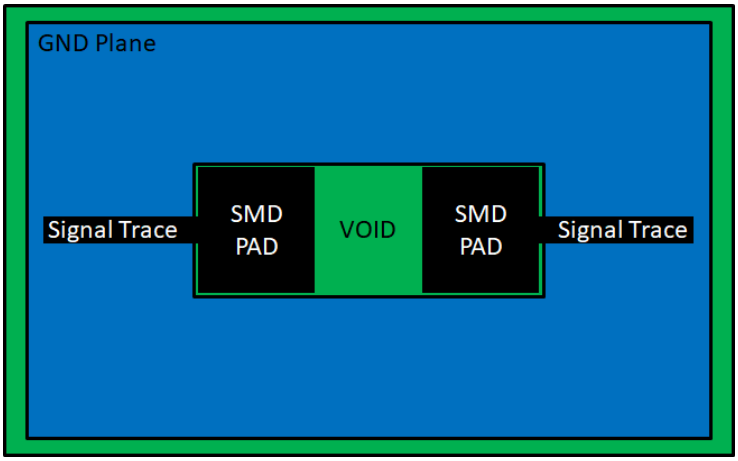


Figure 11-11. Void Below Surface Mount Devices

Also, to minimize the inductance of the AC coupling capacitors, it is best to use 0201 capacitor sizes.

11.11 Signal Bending

Avoid the introduction of bends into high-speed differential signals. When bending is required, maintain a bend angle greater than 135° to ensure that the bend is as loose as a possible. For an example of high-speed signal bending rules, see Figure 11-12.

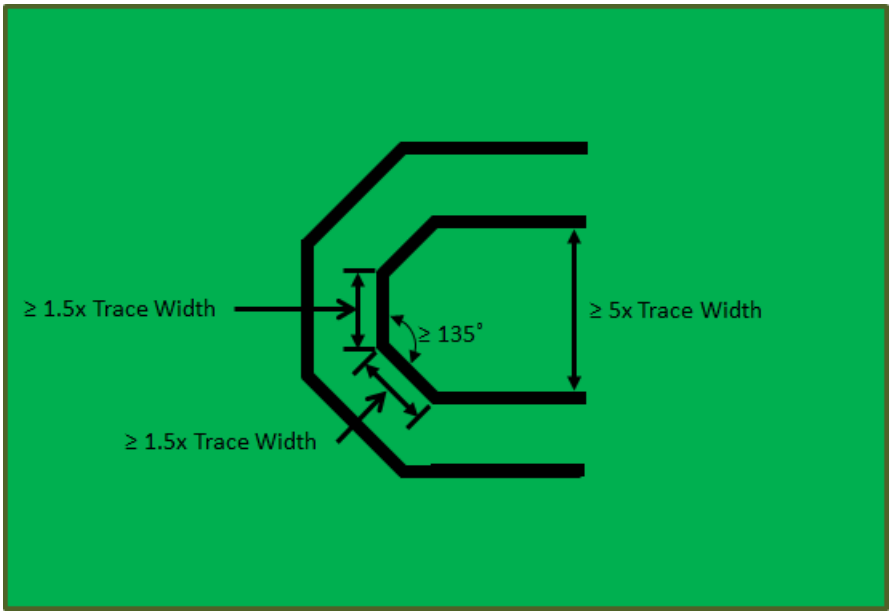


Figure 11-12. Signal Bending Rules

12 References

- Hall, Stephen H., and Garrett W. Hall. *High Speed Digital System Design: A Handbook of Interconnect Theory and Design Practices*. New York: Wiley, 2000.
- Johnson, Howard W., and Martin Graham. *High-speed Signal Propagation: Advanced Black Magic*. Upper Saddle River, NJ: Prentice Hall/PTR, 2003.
- Hall, Stephen H., and Howard L. Heck. *Advanced Signal Integrity for High-speed Digital Designs.* Hoboken, N.J.: Wiley , 2009.
- Stephen C. Thierauf. *High-Speed Circuit Board Signal Integrity*. ISBN-13: 978-1580531313.
- Texas Instruments, *High-Speed Layout Guidelines for Signal Conditions and USB Hubs Application Report*

13 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (April 2020) to Revision B (April 2021)	Page
• Updated the numbering format for tables, figures and cross-references throughout the document	3

Changes from Revision * (December 2019) to Revision A (April 2020)	Page
• Changed AGND to DGND in the *VDDA_GPIO_1p8* row and *ASSOCIATED GROUND NETS* column of Table 5-1.	5
• Changed "Resistor" to "Capacitor" in Figure 6-8 and changed "2-kΩ resistor" to "0.1-µF capacitor" in supporting text	9

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265