Application Report
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TLV320ADCx140 Power Consumption Summary

ABSTRACT

This application report details the power consumption of TLV320ADCx140 devices across various usage scenarios.

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Trademarks

1 Introduction

Power consumption on TLV320AICx140 devices is highly dependent on the usage scenario and features enabled on these devices. The following tables summarize the power consumption based on the following:

- Supply voltage
- Sampling Frequency (FS)
- Number of channels
- DRE enabled or disabled
- Decimation filter options
- Bit clock (BCLK) to Frame sync (FSYNC) ratio
- PLL enabled or disabled
- Converted word length

The tables report the average active current consumed on the Analog Supply, AVDD. This supply includes all the internal analog and digital circuits, but excludes the current consumed by the I/O pins due to its application dependencies. I/O power is dependant upon the following:

- Load capacitance of the system bus interface
- Data output clock rate
- Data conversion output activity
- Bus interface pullups or pulldowns
- Frequency of ADC commands sent by microprocessor

2 Slave Mode Power Consumption with PLL Enabled

Table 1 describes the typical current consumption of the TLV320ADCx140 when the PLL is enabled with AVDD set to 1.8 V and 3.3 V. The PLL is enabled by:

- Setting the bitfield PLL_PDZ in the PWR_CFG register
- Applying a FSYNC and BCLK with the desired sampling rate and BCLK to FSYNC ratio

In this table, when the DRE was enabled, the DRE threshold was set to -36 dB. The current consumption measurements had the Biquad Filters disabled.

Table 1. Typical Current Consumption (PLL Enabled)

SAMPLING FREQUENCY (kHz)	ADC CHANNELS	DRE	DECIMATION FILTERS	BCLK RATIO	WORD LENGTH	AVDD CURRENT AT 3.3 V (mA)	AVDD CURRENT AT 1.8 V (mA)
8	1	Disabled	Linear Phase	32	32	7.75	7.34
	2			48	24	11.27	10.60
	3			96		15.37	14.41
	4			96		19.29	18.06
16	1	Disabled	Linear Phase	24	24	7.92	7.51
			Low Latency			7.87	7.46
	2		Linear Phase	48		11.64	10.96
			Low Latency			11.58	10.90
	3		Linear Phase	96		15.84	14.89
			Low Latency			15.78	14.81
	4		Linear Phase			19.93	18.70
			Low Latency			19.84	18.61
	1	Enabled	Linear Phase	24		8.25	7.83
			Low Latency			8.20	7.79
	2		Linear Phase	48		12.28	11.61
			Low Latency			12.21	11.54
	3		Linear Phase	96		16.77	15.83
			Low Latency			16.70	15.75
	4		Linear Phase			21.40	20.18
			Low Latency			21.32	20.10
24	1	Disabled	Linear Phase	24	24	7.96	7.55
			Low Latency			8.14	7.73
	2		Linear Phase	48		11.62	10.95
			Low Latency			12.00	11.32
	3		Linear Phase	96		15.80	14.84
			Low Latency			16.34	15.40
	4		Linear Phase			19.85	18.62
			Low Latency			20.59	19.36
	1	Enabled	Linear Phase	24		8.35	7.94
			Low Latency			8.53	8.12
	2		Linear Phase	48		12.47	11.81
			Low Latency			12.85	12.19
	3		Linear Phase	96		17.19	16.24
			Low Latency			17.73	16.78
	4		Linear Phase			21.56	20.35
			Low Latency			22.29	21.08

Table 1. Typical Current Consumption (PLL Enabled) (continued)

SAMPLING FREQUENCY (kHz)	ADC CHANNELS	DRE	DECIMATION FILTERS	BCLK RATIO	WORD LENGTH	AVDD CURRENT AT 3.3 V (mA)	AVDD CURRENT AT 1.8 V (mA)
32	1	Disabled	Linear Phase	24	24	8.12	7.72
			Low Latency			8.14	7.73
	2		Linear Phase	48		11.89	11.21
			Low Latency			11.91	11.24
	3		Linear Phase	96		16.17	15.22
			Low Latency			16.20	15.26
	4		Linear Phase			20.31	19.09
			Low Latency			20.37	19.15
	1	Enabled	Linear Phase	24		8.58	8.18
			Low Latency			8.59	8.19
	2		Linear Phase	48		12.88	12.21
			Low Latency			12.90	12.24
	3		Linear Phase	96		17.74	16.80
			Low Latency			17.78	16.84
	4		Linear Phase			22.28	21.07
			Low Latency			22.34	21.12
48	1	Disabled	Linear Phase	24	24	8.47	8.06
			Low Latency			8.36	7.95
	2		Linear Phase	48		12.44	11.77
			Low Latency			12.23	11.55
	3		Linear Phase	96		16.97	16.00
			Low Latency			16.65	15.68
	4		Linear Phase			21.56	20.33
			Low Latency			21.14	19.91
	1	Enabled	Linear Phase	24		9.06	8.65
			Low Latency			8.95	8.55
	2		Linear Phase	48		13.96	13.28
			Low Latency			13.75	13.08
	3		Linear Phase	96		18.88	17.93
			Low Latency			18.56	17.63
	4		Linear Phase			23.74	22.51
			Low Latency			23.33	22.11
96	1	Disabled	Linear Phase	24	24	9.78	9.38
			Low Latency			9.51	9.10
	2		Linear Phase	48		15.10	14.42
			Low Latency			14.55	13.87
	3		Linear Phase	96		20.45	19.49
			Low Latency			19.66	18.69
	4		Linear Phase			25.68	24.43
			Low Latency			24.61	23.37
	1	Enabled	Linear Phase	24		10.96	10.56
			Low Latency			10.69	10.29
	2		Linear Phase	48		17.36	16.67
			Low Latency			16.83	16.14

Table 1. Typical Current Consumption (PLL Enabled) (continued)

SAMPLING FREQUENCY (kHz)	ADC CHANNELS	DRE	DECIMATION FILTERS	BCLK RATIO	WORD LENGTH	AVDD CURRENT AT 3.3 V (mA)	AVDD CURRENT AT 1.8 V (mA)
192	1	Disabled	Linear Phase	24	24	9.60	9.19
			Low Latency			10.61	10.20
	2		Linear Phase	48		14.95	14.26
			Low Latency			17.00	16.30
	3		Linear Phase	96		20.40	19.43
			Low Latency			23.48	22.50
	4		Linear Phase			25.61	24.36
	1	Enabled	Linear Phase	24		11.59	11.18
			Low Latency			12.98	12.58
384	1	Disabled	Linear Phase	24	24	10.91	10.50

3 Slave Mode Power Consumption with PLL Disabled

Table 2 describes the typical current consumption of the TLV320ADCx140 when the PLL is disabled with AVDD set to 1.8 V and 3.3 V. The PLL is disabled by:

- Clearing the bitfield PLL_PDZ in the PWR_CFG register
- Applying a master clock through BCLK, GPIO1, or the GPIx pins
- If GPIO1 is configured as MCLK, setting the appropriate GPIO1_CFG bitfield in the GPIO_CFG0 register
- Indicating the master clock source through DIS_PLL_SLV_CLK_SRC bitfield in the CLK_SRC register
- Setting the appropriate MCLK to FSYNC ratio through the MCLK_RATIO_SEL bitfield and MCLK_FREQ_SEL_MODE bitfield of the CLK_SRC register
- Setting the AUTO_MODE_PLL_DIS bitfield and the corresponding MCLK_FREQ_SEL bitfield of the MST_CFG0 register

In this table, when the DRE was enabled, the DRE threshold was set to -36 dB. The power consumption measurements had the Biquad Filters disabled.

Table 2. Typical Current Consumption (PLL Disabled)

SAMPLING FREQUENCY (kHz)	MCLK FREQUENCY(MHz)	MCLK RATIO	ADC CHANNELS	DRE	DECIMATION FILTERS	BCLK RATIO	WORD LENGTH	AVDD CURRENT AT 3.3 V (mA)	AVDD CURRENT AT 1.8 V (mA)
8	12.288	1536	1	Disabled	Linear Phase	32	32	5.91	5.52
			2			48	24	9.80	9.14
16	12.288	768	1	Disabled	Linear Phase	24	24	6.08	5.69
				Enabled				6.43	6.02
				Disabled	Low Latency			6.05	5.65
				Enabled				6.37	5.98
				Disabled	Ultra-Low Latency			5.92	5.53
				Enabled	Ultra-Low Latency			6.25	5.86
			2	Disabled	Linear Phase	48		10.13	9.47
				Disabled	Low Latency			10.06	9.41
				Disabled	Ultra-Low Latency			9.83	9.18

Table 2. Typical Current Consumption (PLL Disabled) (continued)

SAMPLING FREQUENCY (kHz)	MCLK FREQUENCY(MHz)	MCLK RATIO	ADC CHANNELS	DRE	DECIMATION FILTERS	BCLK RATIO	WORD LENGTH	AVDD CURRENT AT 3.3 V (mA)	AVDD CURRENT AT 1.8 V (mA)
16	24.576	1536	1	Disabled	Linear Phase	24	24	6.36	5.97
				Enabled	Linear Phase			6.70	6.30
				Disabled	Low Latency			6.32	5.93
				Enabled	Low Latency			6.65	6.26
				Disabled	Ultra-Low Latency			6.21	5.81
				Enabled	Ultra-Low Latency			6.54	6.14
			2	Disabled	Linear Phase	48		10.47	9.81
				Enabled	Linear Phase			11.11	10.45
				Disabled	Low Latency			10.41	9.75
				Enabled	Low Latency			11.05	10.39
				Disabled	Ultra-Low Latency			10.17	9.51
				Enabled	Ultra-Low Latency			10.82	10.16
			3	Disabled	Linear Phase	96		14.58	13.65
					Low Latency			14.51	13.57
					Ultra-Low Latency			14.15	13.21
				Enabled	Ultra-Low Latency			15.09	14.16
			4	Disabled	Linear Phase			18.61	17.39
					Low Latency			18.51	17.30
					Ultra-Low Latency			18.04	16.83
16	36.864	2304	1	Disabled	Linear Phase	24	24	6.64	6.25
				Enabled				6.96	6.58
				Disabled	Low Latency			6.60	6.20
				Enabled				6.92	6.53
				Disabled	Ultra-Low Latency			6.48	6.08
				Enabled				6.80	6.42
			2	Disabled	Linear Phase	48		10.74	10.08
				Enabled				11.38	10.72
				Disabled	Low Latency			10.69	10.02
				Enabled				11.32	10.66
				Disabled	Ultra-Low Latency			10.45	9.79
				Enabled				11.09	10.43
			3	Disabled	Linear Phase	96		14.86	13.92
				Enabled				15.78	14.85
				Disabled	Low Latency			14.79	13.84
				Enabled				15.72	14.78
				Disabled	Ultra-Low Latency			14.44	13.49
				Enabled				15.36	14.43
			4	Disabled	Linear Phase			18.94	17.73
				Enabled				20.18	18.97
				Disabled	Low Latency			18.86	17.63
				Enabled				20.09	18.89
				Disabled	Ultra-Low Latency			18.38	17.17
				Enabled				19.62	18.41

Table 2. Typical Current Consumption (PLL Disabled) (continued)

SAMPLING FREQUENCY (kHz)	MCLK FREQUENCY(MHz)	MCLK RATIO	ADC CHANNELS	DRE	DECIMATION FILTERS	BCLK RATIO	WORD LENGTH	AVDD CURRENT AT 3.3 V (mA)	AVDD CURRENT AT 1.8 V (mA)
24	12.288	512	1	Disabled	Linear Phase	24	24	6.09	5.70
				Enabled				6.50	6.10
				Disabled	Low Latency			6.28	5.89
				Enabled				6.67	6.29
				Disabled	Ultra-Low Latency			6.08	5.69
				Enabled				6.48	6.09
			2	Disabled	Linear Phase	48		10.10	9.45
					Ultra-Low Latency	64	32	10.10	9.44
	24.576	1024	1	Disabled	Linear Phase	32	32	6.37	5.99
				Enabled				6.77	6.38
				Disabled	Low Latency			6.57	6.17
				Enabled				6.96	6.57
				Disabled	Ultra-Low Latency			6.37	5.98
				Enabled				6.76	6.38
			2	Disabled	Linear Phase	64		10.46	9.80
				Enabled				11.22	10.57
				Disabled	Low Latency			10.84	10.17
				Enabled				11.59	10.95
				Disabled	Ultra-Low Latency			10.44	9.79
				Enabled				11.21	10.56
			3	Disabled	Linear Phase	128		14.56	13.62
					Low Latency			15.11	14.17
					Ultra-Low Latency			14.55	13.59
			4		Linear Phase			18.55	17.33
					Ultra-Low Latency			18.52	17.30
24	36.864	1536	1	Disabled	Linear Phase	24	24	6.65	6.26
				Enabled				7.05	6.66
				Disabled	Low Latency			6.84	6.44
				Enabled				7.23	6.84
				Disabled	Ultra-Low Latency			6.65	6.25
				Enabled				7.05	6.65
			2	Disabled	Linear Phase	48		10.73	10.07
				Enabled				11.49	10.84
				Disabled	Low Latency			11.10	10.44
				Enabled				11.86	11.21
				Disabled	Ultra-Low Latency			10.71	10.05
				Enabled				11.49	10.82
			3	Disabled	Linear Phase	96		14.81	13.88
				Enabled				15.93	15.00
				Disabled	Low Latency			15.37	14.43
				Enabled				16.49	15.56
				Disabled	Ultra-Low Latency			14.80	13.85
				Enabled				15.93	14.98
			4	Disabled	Linear Phase			18.87	17.65
				Enabled				20.35	19.14
				Disabled	Low Latency			19.61	18.40
					Ultra-Low Latency			18.84	17.63
				Enabled				20.32	19.11

Table 2. Typical Current Consumption (PLL Disabled) (continued)

SAMPLING FREQUENCY (kHz)	MCLK FREQUENCY(MHz)	MCLK RATIO	ADC CHANNELS	DRE	DECIMATION FILTERS	BCLK RATIO	WORD LENGTH	AVDD CURRENT AT 3.3 V (mA)	AVDD CURRENT AT 1.8 V (mA)
32	12.288	384	1	Disabled	Linear Phase	24	24	6.27	5.88
					Low Latency			6.27	5.88
					Ultra-Low Latency			6.16	5.76
				Enabled	Ultra-Low Latency			6.61	6.23
	24.576	768	1	Disabled	Linear Phase			6.55	6.15
				Enabled	Linear Phase			7.01	6.62
				Disabled	Low Latency			6.56	6.16
				Enabled	Low Latency			7.02	6.63
				Disabled	Ultra-Low Latency			6.43	6.04
				Enabled	Ultra-Low Latency			6.90	6.51
			2	Disabled	Linear Phase	48		10.73	10.07
				Enabled	Linear Phase			11.62	10.97
				Disabled	Low Latency			10.75	10.09
					Ultra-Low Latency			10.51	9.85
				Enabled	Ultra-Low Latency			11.40	10.75
			3	Disabled	Linear Phase	96		14.93	13.98
					Low Latency			14.96	14.02
					Ultra-Low Latency			14.58	13.65
			4		Linear Phase			19.01	17.79
					Ultra-Low Latency			18.56	17.35
48	12.288	256	1	Disabled	Linear Phase	24	24	6.61	6.22
					Low Latency			6.49	6.11
					Ultra-Low Latency			6.33	5.95
	24.576	512			Linear Phase	32	32	6.90	6.51
				Enabled				7.50	7.11
				Disabled	Low Latency			6.79	6.40
				Enabled				7.39	7.00
				Disabled	Ultra-Low Latency			6.64	6.24
				Enabled				7.24	6.85
			2	Disabled	Linear Phase	64		11.30	10.64
					Low Latency			11.09	10.42
					Ultra-Low Latency			10.77	10.11
			3		Low Latency	128		15.40	14.46
					Ultra-Low Latency			14.93	13.99
			4		Ultra-Low Latency			18.97	17.74

Table 2. Typical Current Consumption (PLL Disabled) (continued)

SAMPLING FREQUENCY (kHz)	MCLK FREQUENCY(MHz)	MCLK RATIO	ADC CHANNELS	DRE	DECIMATION FILTERS	BCLK RATIO	WORD LENGTH	AVDD CURRENT AT 3.3 V (mA)	AVDD CURRENT AT 1.8 V (mA)
48	36.864	768	1	Disabled	Linear Phase	24	24	7.17	6.78
				Enabled	Linear Phase			7.77	7.38
				Disabled	Low Latency			7.06	6.67
				Enabled	Low Latency			7.66	7.27
				Disabled	Ultra-Low Latency			6.90	6.51
				Enabled	Ultra-Low Latency			7.50	7.11
			2	Disabled	Linear Phase	48		11.55	10.90
				Enabled	Linear Phase			12.70	12.06
				Disabled	Low Latency			11.34	10.68
				Enabled	Low Latency			12.50	11.84
				Disabled	Ultra-Low Latency			11.03	10.37
				Enabled	Ultra-Low Latency			12.19	11.53
			3	Disabled	Linear Phase	96		15.96	15.03
					Low Latency			15.66	14.71
					Ultra-Low Latency			15.19	14.24
			4		Linear Phase			20.33	19.11
					Low Latency			19.89	18.68
					Ultra-Low Latency			19.27	18.06
96	24.576	256	1	Disabled	Linear Phase	32	32	8.26	7.88
					Low Latency			7.99	7.59
					Ultra-Low Latency			7.66	7.27
	36.864	384			Linear Phase	24	24	8.52	8.14
				Enabled	Linear Phase			9.72	9.34
				Disabled	Low Latency			8.25	7.85
				Enabled	Low Latency			9.44	9.05
				Disabled	Ultra-Low Latency			7.93	7.53
				Enabled	Ultra-Low Latency			9.13	8.74
			2	Disabled	Low Latency	48		13.31	12.65
					Ultra-Low Latency			12.67	12.01

4 Digital Microphone Power Consumption

Table 3 and Table 4 describes the typical current consumption of the TLV320ADCx140 when the digital microphone inputs are used with an external PDM modulator 4th and 5th order, respectively. The Digital Microphone is selected by:

- Configuring the corresponding channel for digital microphone input in the CHx_INSRC register
- Configuring the corresponding GPO1 to GPO4 pin as PDMCLK output in the appropriate GPOx_CFG register
- Configuring the corresponding GPI1 to GPI4 pin as PDM input in the appropriate GPI1x_CFG register

Table 3. PDM Typical Current Consumption with an External PDM 4th Order Modulator

PDM CLOCK		6.144 MHz	3.072 MHz	1.536 MHz	0.768 MHz
SAMPLING RATE (kHz)	DIGITAL MICROPHONE CHANNELS	AVDD CURRENT AT 3.3 V (mA)	AVDD CURRENT AT 3.3 V (mA)	AVDD CURRENT AT 3.3 V (mA)	AVDD CURRENT AT 3.3 V (mA)
8	8	7.85	7.93	7.89	7.87
16	8	8.97	9.23	9.19	-
24	8	8.92	8.99	8.99	-

Table 3. PDM Typical Current Consumption with an External PDM 4th Order Modulator (continued)

PDM CLOCK		6.144 MHz	3.072 MHz	1.536 MHz	0.768 MHz
SAMPLING RATE (kHz)	DIGITAL MICROPHONE CHANNELS	AVDD CURRENT AT 3.3 V (mA)	AVDD CURRENT AT 3.3 V (mA)	AVDD CURRENT AT 3.3 V (mA)	AVDD CURRENT AT 3.3 V (mA)
32	8	9.71	9.92	-	-
48	8	11.26	11.69	-	-
96	4	11.87	-	-	-

Table 4. PDM Typical Current Consumption with an External PDM 5th Order Modulator

PDM CLOCK		6.144 MHz	3.072 MHz	1.536 MHz	0.768 MHz
SAMPLING RATE (kHz)	DIGITAL MICROPHONE CHANNELS	AVDD CURRENT AT 3.3 V (mA)	AVDD CURRENT AT 3.3 V (mA)	AVDD CURRENT AT 3.3 V (mA)	AVDD CURRENT AT 3.3 V (mA)
8	8	7.93	7.92	7.88	7.80
16	8	9.25	9.20	9.15	-
24	8	9.04	8.98	8.91	-
32	8	9.93	9.83	9.77	-
48	8	11.71	11.60	-	-
96	4	12.14	12.05	-	-
192	4	11.96	-	-	-

5 Settings for Lowest Power Consumption

To minimize the power consumption of the TLV320ADCx140 devices, ensure that unused modules are disabled, use the lowest sampling rate, bit clock, and master clock needed by the application, and operate at the lowest AVDD and IOVDD supply voltage possible. The following list summarizes the settings and registers for lowest power operation:

- Operate at the lowest supply voltage possible. AVDD and IOVDD support 1.8 V or 3.3 V supply, independently (AVDD and IOVDD can have different supply voltages).
  - Unused analog inputs, tie to analog ground.
  - Unused digital inputs, tie to digital ground.
  - Unused outputs, leave unconnected.
- Disable unused ADC and PDM channels through the IN_CH_EN register.
- Disable any unused output channel through the ASI_OUT_CH_EN register.
- Disable MICBIAS power, if unused, through the PWR_CFG register.
- Operate at the lowest sample rate possible.
- Disable PLL, if the system supplies a low jitter master clock. Refer to *Section 3* for a description of the settings to disable PLL.
- Disable unused post-processing blocks:
  - Disable Biquad filters, if unused, through the BIQUAD_CFG bitfield of the DSP_CFG1 register.
  - Disable DRE or AGC, if unused in an active channel, through the CHx_DREEN bitfield of the CHx_CFG0 register.
- Select ultra-low latency over linear phase decimation filters, if the application allows, through the DECI_FILT bitfield of the DSP_CFG0 register.
- Utilize the smallest word length allowed by the application through the ASI_WLEN bitfield of the ASI_CFG0 register.

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