Analog Engineer's Circuit

Programmable Voltage Output With Sense Connections Circuit

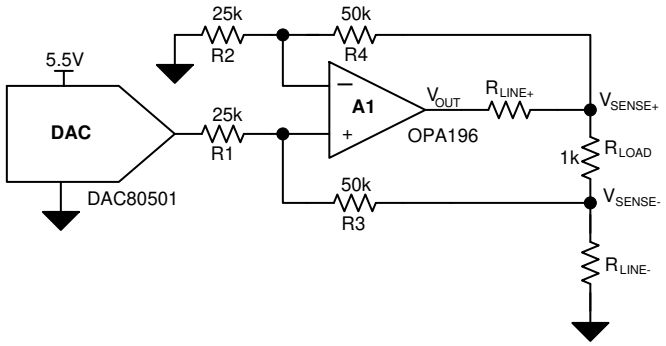
Garrett Satterfield

Design Goals

DAC Output Voltage	Output Voltage V_{LOAD}	Minimum Load Resistance R_{LOAD}	Maximum Line Resistance Compensation	Error
0V–5V	0V–10V	1kΩ	+25% of R_{LOAD}	< 0.25% FSR

Design Description

The programmable voltage output with sense connections circuit provides a precise voltage across a load, compensating for parasitic series resistance. The amplifier A1 uses feedback from the high-side and low-side of the attached load to accurately regulate the voltage between V_{SENSE+} and V_{SENSE-}. The digital-to-analog converter (DAC) output and discrete resistors set the voltage across the load. This circuit is used in applications where additional line resistance can be present and must be compensated for by increasing the output voltage to deliver the correct voltage to the load. Common end equipment that use this circuit include *analog output modules, memory and semiconductor test equipment, spectroscopy,* and *data acquisition (DAQ) cards.*



Design Notes

1. Select a DAC with low total unadjusted error (TUE) and with the required resolution for the application. A DAC with integrated reference, like the DAC80501 device, can be used to minimize components and solution size.
2. Choose a high-voltage amplifier, with rail-to-rail output to provide a sufficient output swing to drive the load and line resistance. Set the amplifer to have low offset voltage and offset voltage drift so it does not significantly contribute to output error.
3. Resistor mismatch directly contributes to gain error at the output. Use resistors with 0.05% tolerance or better and low thermal drift.
4. For correct compensation of additional line resistance the ratio of R2:R4 must match the ratio of R3:R1 as closely as possible.
5. The amplifier supply voltage is chosen based on the required output voltage, additional line resistance, and amplifier output swing at maximum load current.
6. To reduce error at zero-scale a negative voltage can be supplied to the amplifier.

Design Steps

1. The transfer function for V_{OUT} based on DAC voltage and resistor values is:

$$V_{LOAD} = \frac{R3}{R1} \cdot V_{DAC}; \quad \frac{R3}{R1} = \frac{R4}{R2}$$

2. A 50-kΩ resistance is chosen for R3. A relatively large value should be selected to reduce the current in the feedback paths. R1 is then calculated:

$$R1 = \frac{V_{DAC,FS}}{V_{LOAD,FS}} \cdot R3 = \frac{5V}{10V} \cdot 50k\Omega = 25k\Omega$$

3. R4 and R2 are chosen equal to R3 and R1, respectively.
4. Calculate the maximum load current based on the minimum load resistance and full scale V_{LOAD}. The maximum load current impacts the amplifier output voltage swing and the additional line resistance the circuit can compensate.

$$I_{LOAD,max} = \frac{V_{LOAD,FS}}{R_{LOAD,min}} = \frac{10V}{1k\Omega} = 10mA$$

5. The required V_{CC} voltage is calculated to drive 25% additional load resistance and still maintain voltage regulation across R_{LOAD}. $V_{O,rail}$ is the approximate amplifier output swing from V+ at a 10-mA load current.

$$V_{CC,min} = V_{O,rail} + 0.25 \cdot R_{LOAD,min} \cdot I_{LOAD,max} + V_{LOAD,FS} = 500mV + 250\Omega \cdot 10mA + 10V = 13V$$

6. The output error can be approximated based on the DAC TUE, amplifier offset voltage, resistor tolerance, and reference initial accuracy using root sum square (RSS) analysis.

$$\text{Output TUE(\%FSR)} = \sqrt{TUE_{DAC}^2 + \left(\frac{V_{OS}}{FSR} \cdot 100\right)^2 + 4 \cdot R^2_{Tol} + Accuracy^2_{Ref}} = \sqrt{0.1^2 + \left(\frac{100\mu V}{5V} \cdot 100\right)^2 + 4 \cdot 0.05^2 + 0.1^2} = 0.173\%$$

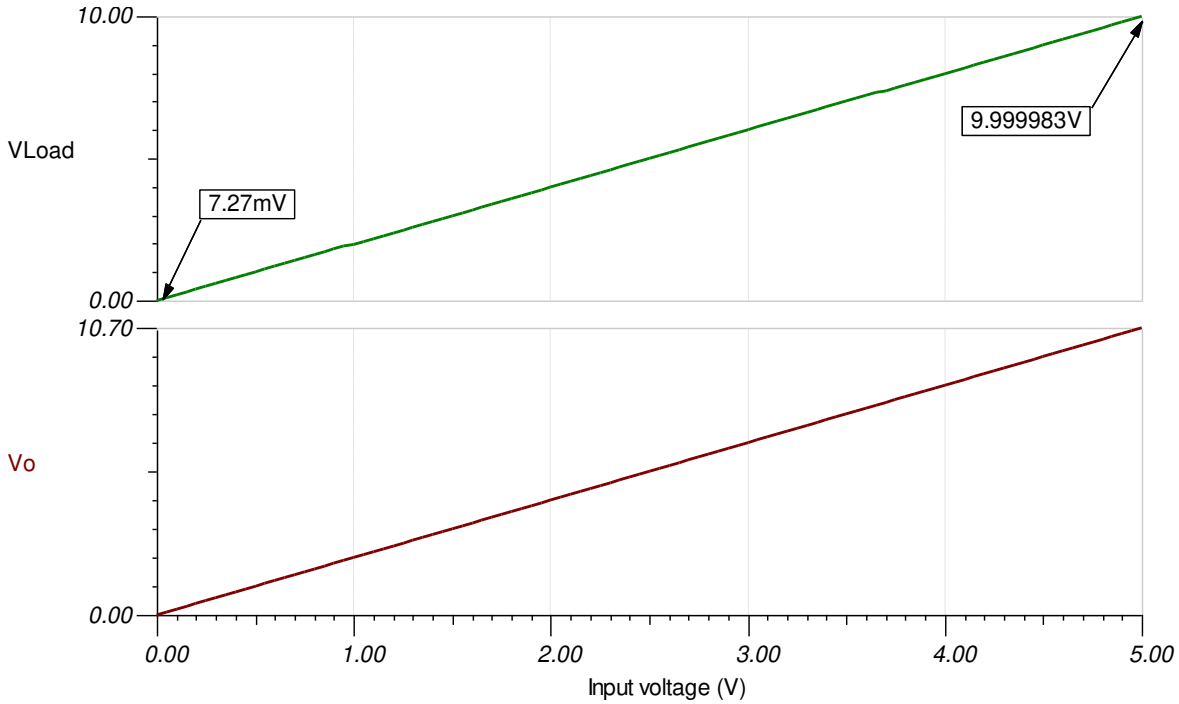


Figure 1-1. DC Transfer Characteristic

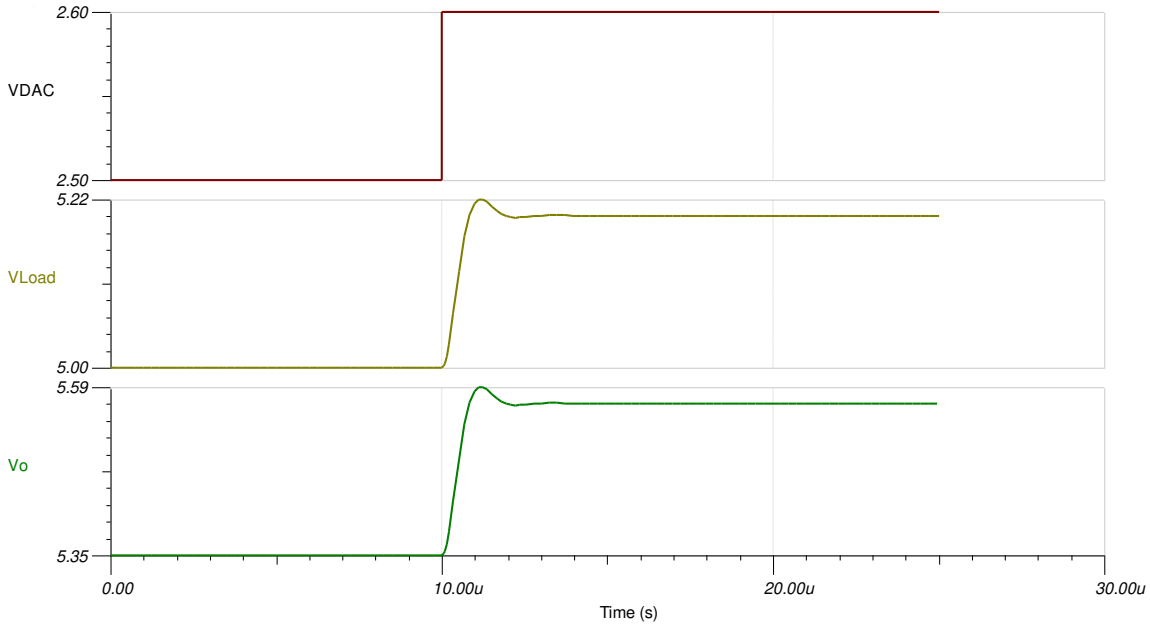


Figure 1-2. Small-Signal Step Response

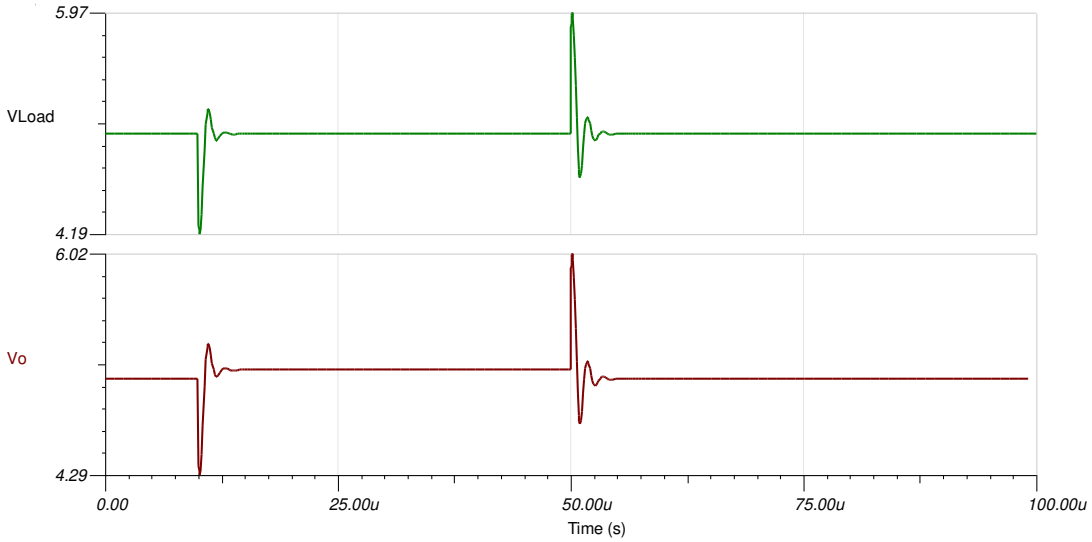


Figure 1-3. Load Transient 10kΩ to 5kΩ R_{LOAD}

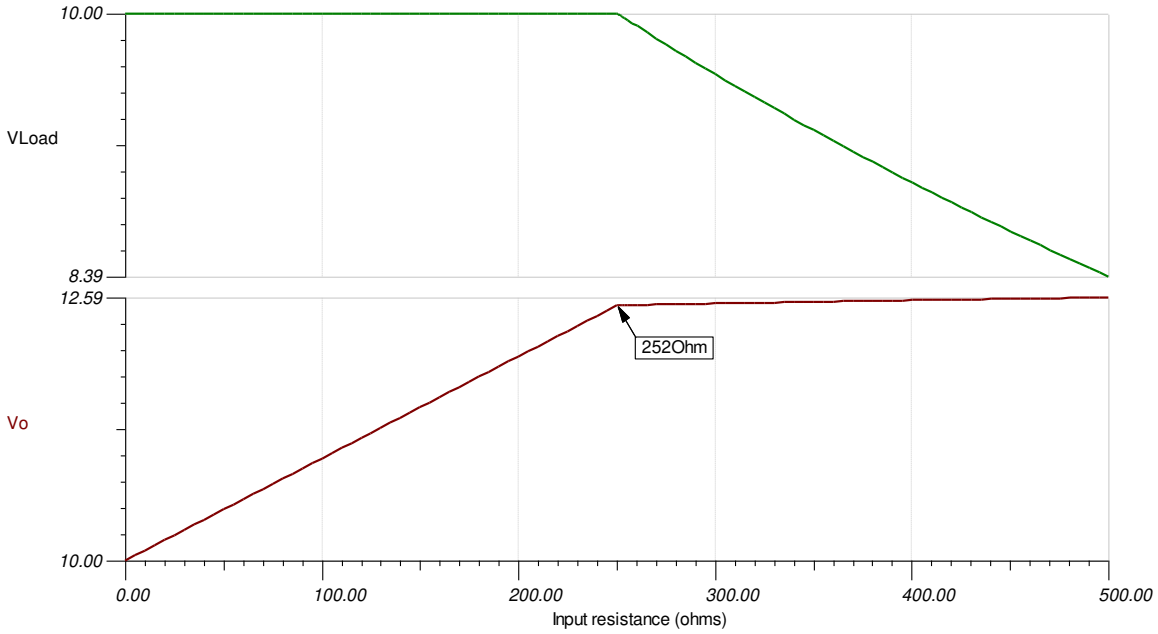


Figure 1-4. Maximum Additional Line Resistance at Amplifier V_{CC} = 13V

Devices

Device	Key Features	Link	Other Possible Devices
DACs			
DAC80501	16-bit resolution, 1-LSB INL, single-channel, voltage output DAC with 5ppm/°C internal reference	True 16-bit, 1-ch, SPI/I2C, voltage-output DAC in WSON package with precision internal reference	Precision DACs (≤10 MSPS)
DAC81416	16-bit resolution, 1-LSB INL, 16-channel ±20-V high-voltage output DAC with 5ppm/°C internal reference	16-channel 16-bit high-voltage output DAC with integrated internal reference	
DAC80508	16-bit resolution, 1-LSB INL, octal-channel, voltage output DAC with 5ppm/°C internal reference	True 16-bit, 8-channel, SPI, voltage-output DAC with precision internal reference	
Op Amps			
OPA196	Low-offset (100µV), Low-drift, rail-to-rail I/O, 2.25V to 36V supply	Single, 36V, low power, all-purpose amplifier with mux-friendly input	Operational amplifiers (op amps)
TLV170	Cost-sensitive, rail-to-rail output, 2.7V to 36V supply	Single, 36V, 1.2MHz, low-power operational amplifier for cost-sensitive applications	
OPA192	Precision, ultra-low offset (5µV) and drift, rail-to-rail I/O, 4.5V to 36V supply	High-Voltage, Rail-to-Rail Input/Output, 5µV, 0.2µV/˚C, Precision Operational Amplifier	

Links to Key Files

Texas Instruments, Programmable Voltage Output with Sense Connections, source files

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