Analog Engineer's Circuit

High-Input Impedance, True Differential, Analog Front End (AFE) Attenuator Circuit for SAR ADCs

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Input Voltage (OPA197 Buffers)	THS4551 Output, ADC Input	ADS8912B Digital Output
VinP = –12V, VinN = +12V, VinMin (Dif) = –24V	VoutDif = –4.00V, VoutP = 0.25V, VoutN = 4.25V	$238E3_H$ -116509_{10}
VinP = +12V, VinN = –12V, VinMax (Dif) = +24V	VoutDif = +4.0V, VoutP = 4.25V, VoutN = 0.25V	$1C71C_H$ +116508_{10}

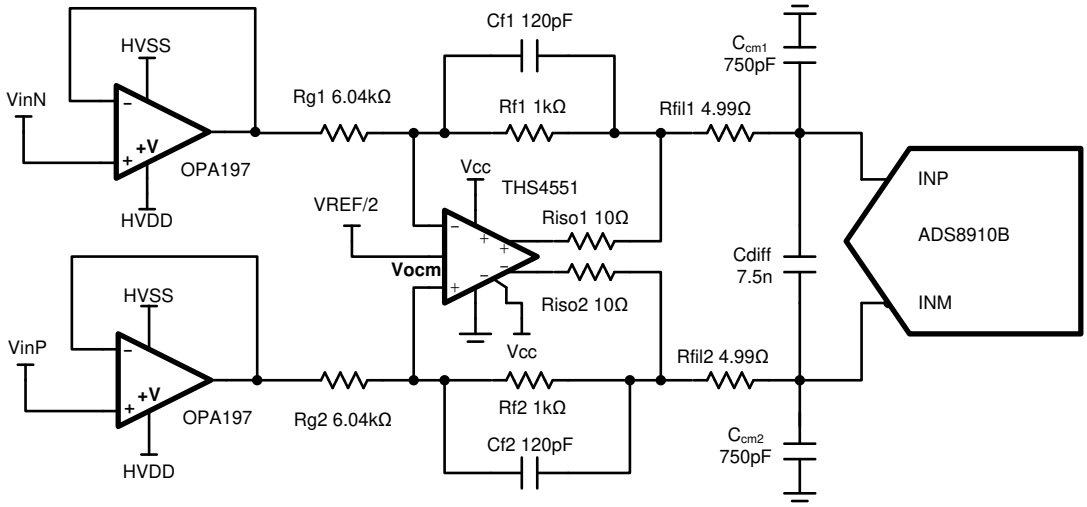
Supplies and Reference

HVDD	HVSS	Vcc	Vee	Vref	Vcm
+15V	–15V	+5.0V	0V	+4.5V	2.5V

Design Description

This analog front end (AFE) and SAR ADC data acquisition solution can measure true differential voltage signals in the range of ±24V (or absolute input range VinP = ±12V, VinN = ±12V) offering high-input impedance supporting data rates up to 500ksps with 18-bit resolution. A precision, 36-V rail-to-rail amplifier with low-input bias current is used to buffer the inputs of a fully-differential amplifier (FDA). The FDA attenuates and shifts the signal to the differential voltage and common-mode voltage range of the SAR ADC. The values in the *component selection* section can be adjusted to allow for different input voltage levels.

This circuit implementation is used in accurate measurement of true differential voltage in *parametric measurement units (PMUs)*, *precision multifunction input and output DAQs*, and *analog input modules* used in *Programmable Automation Control (PAC)*, *Discrete Control System (DCS)*, and *Programmable Logic Control (PLC)* applications.



Specifications

Specification	Goal	Calculated	Simulated
Transient ADC Input Settling (500ksps)	<< 1 LSB; << 34µV	N/A	0.5µV
Noise (at ADC Input)	$10\mu V_{RMS}$	$9.28\mu V_{RMS}$	$9.76\mu V_{RMS}$
Bandwidth	1.25MHz	1.25MHz	1.1MHz

Design Notes

1. Verify the linear range of the op amp (buffer) based on the common mode, output swing specification for linear operation. This is covered in the *component selection* section. Select an amplifier with low input bias current.
2. Find ADC full-scale range and common-mode range specifications. This is covered in the *component selection*.
3. Determine the required attenuation for the FDA based on the input signal amplitude, the ADC full-scale range and the output swing specifications of the FDA. This is covered in the *component selection* section.
4. Select COG capacitors to minimize distortion.
5. Use 0.1% 20ppm/°C film resistors or better for good accuracy, low gain drift, and to minimize distortion.
6. *Understanding and Calibrating the Offset and Gain for ADC Systems* covers methods for error analysis. Review the link for methods to minimize gain, offset, drift, and noise errors
7. *Introduction to SAR ADC Front-End Component Selection* covers methods for selecting the charge bucket circuit Rfilt and Cfilt. These component values are dependent on the amplifier bandwidth, data converter sampling rate, and data converter design. The values shown here will give good settling and AC performance for the amplifier, gain settings, and data converter in this example. If the design is modified, a different RC filter must be selected. Refer to the *Precision Labs* videos for an explanation of how to select the RC filter for best settling and AC performance.

Component Selection and Settings for Buffer Amplifier and FDA

1. Verify the buffer amplifier input range for linear operation:

   Select Supplies $(V-) = -15V$, $(V+) = +15V$ to allow VinP = ±12V VinN = ±12V range

   $(V-) - 0.1V < V_{cm} < (V+) - 3V$ from OPA197 common-mode voltage specification

   $-15.1V < V_{cm} < +12V$ allows required ±12V input voltage range

2. Verify the buffer amplifier output range for linear operation:

   $(V-) + 0.6V < V_{out} < (V+) - 0.6V$ from OPA197 Aol specification for linear operation

   $-14.4V < V_{out} < 14.4V$ allows required ±12V output voltage range

3. Find ADC full-scale input range. In this circuit, $V_{REF} = 4.5V$:

   $ADC_{Full\text{-}Scale\ Range} = \pm V_{REF} = \pm 4.5V$ from ADS8910B data sheet

4. Find the required ADC common-mode voltage:

   $$V_{CM} = \frac{+V_{REF}}{2} = +2.25V$$ from ADS8910B data sheet, therefore set FDA VCOM = 2.25V

5. Find FDA absolute output voltage range for linear operation:

   $0.23 < V_{out} < 4.77V$ from THS4551 output low / high specification for linear operation

   However, the positive range is limited by $ADC_{Full\text{-}Scale\ Range} = \pm 4.5V$, therefore

   $0.23V < V_{out} < 4.5V$ where $V_{outMin} = 0.23V$, $V_{outMax} = 4.5V$

6. Find FDA differential output voltage range for linear operation. The general output voltage equations for this circuit follow:

$V_{outMin} = \frac{V_{outDifMin}}{2} + V_{cm}$ and $V_{outMax} = \frac{V_{outDifMax}}{2} + V_{cm}$

Re-arrange the equations and solve for $V_{outDifMin}$ and $V_{outDifMax}$.

Find maximum differential output voltage range based on worst case:

$V_{outDifMax} = 2 \times V_{outMax} - 2 \times V_{cm} = 2 \times (4.5V) - 2 \times (2.25V) = 4.5V$

$V_{outDifMin} = 2 \times V_{outMin} - 2 \times V_{cm} = 2 \times (0.23V) - 2 \times (2.5V) = -4.04V$

Based on combined worst case, choose $V_{outDifMin}$ = -4.04V and $V_{outDifMax}$ = +4.04V

7. Find the FDA differential input voltage range:

$V_{inDifMax} = V_{inPmax} - V_{inNmin} = +12V - (-12V) = +24V$

$V_{inDifMin} = V_{inPmin} - V_{inNmax} = -12V - (+12V) = -24V$

8. Find FDA required attenuation ratio:

$$Gain_{FDA} = \frac{V_{outDifMax} - V_{outDifMin}}{V_{inDifMax} - V_{inDifMin}} = \frac{(+4.04V) - (-4.04V)}{(+24V) - (-24V)} = 0.166 \frac{V}{V} \approx \frac{1}{6} \frac{V}{V}$$

9. Find standard resistor values to set the attenuation:

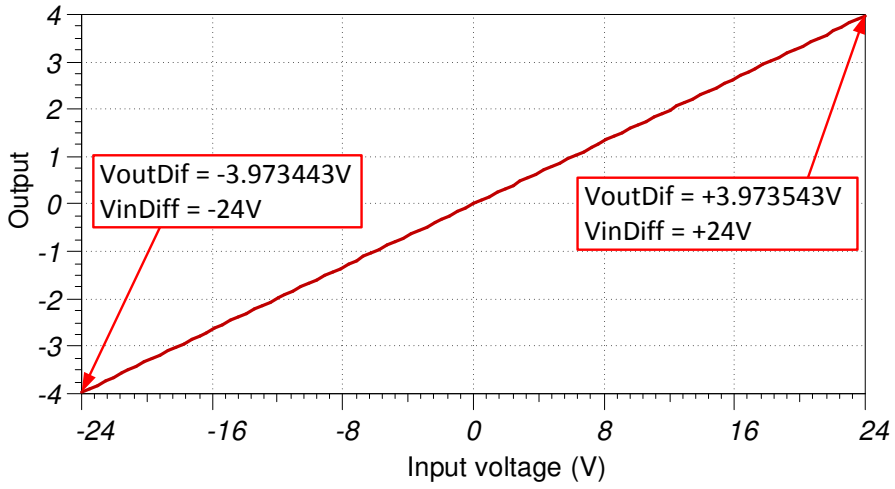
$$Gain_{FDA} = \frac{R_f}{R_g} = \frac{1}{6} V/V \Rightarrow \frac{R_g}{R_f} = \frac{1.00k\Omega}{6.04k\Omega} = \frac{1}{6.04} V/V$$

10. Find C_f for cutoff frequency f_c, R_{fINA} = 1kΩ:

$$C_f = \frac{1}{2 \cdot \pi \cdot f_c \cdot R_{fINA}} = \frac{1}{2 \cdot \pi \cdot (1.25MHz) \cdot (1k\Omega)} = 127pF \text{ or } 120pF \text{ standard value}$$

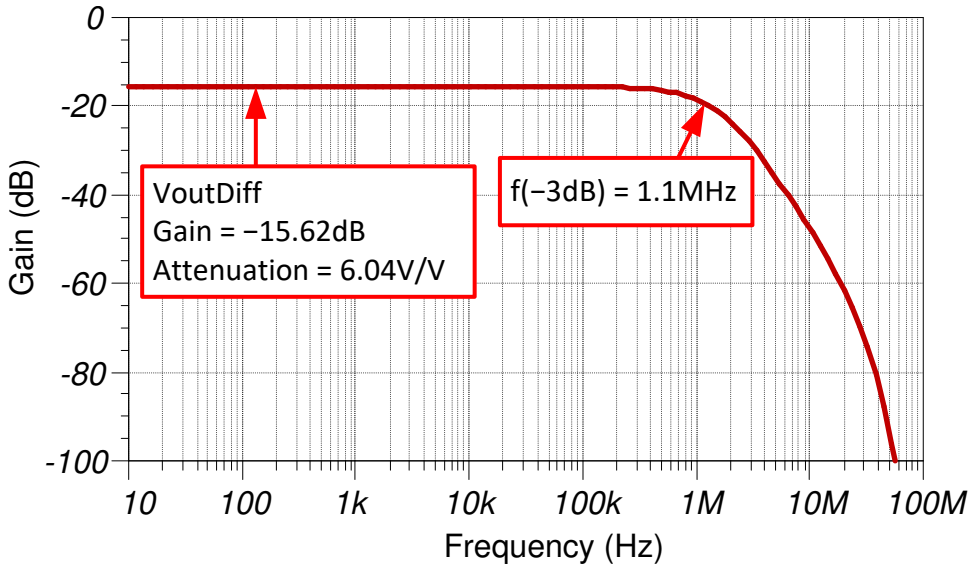
DC Transfer Characteristics

The following graph shows a linear output response for differential inputs from +24V to –24V.



AC Transfer Characteristics

The simulated bandwidth is approximately 1.1MHz and the gain is –15.62dB which is a linear gain of approximately 0.166V/V (attenuation ratio 6.04V/V).



Noise Simulation

Simplified Noise calculation for rough estimate :

$$f_c = \frac{1}{2 \cdot \pi \cdot R_f \cdot C_f} = \frac{1}{2 \cdot \pi \cdot (1\text{k}\Omega) \cdot (120\text{pF})} = 1.33\text{MHz}$$

Noise contribution of OPA197 buffer referred to ADC input

$$E_{nOPA197} = e_{nOPA197} \cdot \sqrt{K_n \cdot f_c} \cdot Gain_{FDA}$$

$$E_{nOPA197} = \left(5.5\text{nV} / \sqrt{\text{Hz}}\right) \cdot \sqrt{1.57 \cdot 1.33\text{MHz}} \cdot 0.166\text{V} / \text{V} = 1.319\mu V_{RMS}$$

Noise of THS4551 FDA referred to ADC input

$$\text{Noise gain} : NG = 1 + R_f / R_g = 1 + \frac{1.00\,\text{k}\Omega}{6.04\,\text{k}\Omega} = 1.166\text{V} / \text{V}$$

$$e_{noFDA} = \sqrt{\left(e_{nFDA} \cdot NG\right)^2 + 2\left(i_{nFDA} \cdot R_f\right)^2 + 2\left(4kTR_f \cdot NG\right)}$$

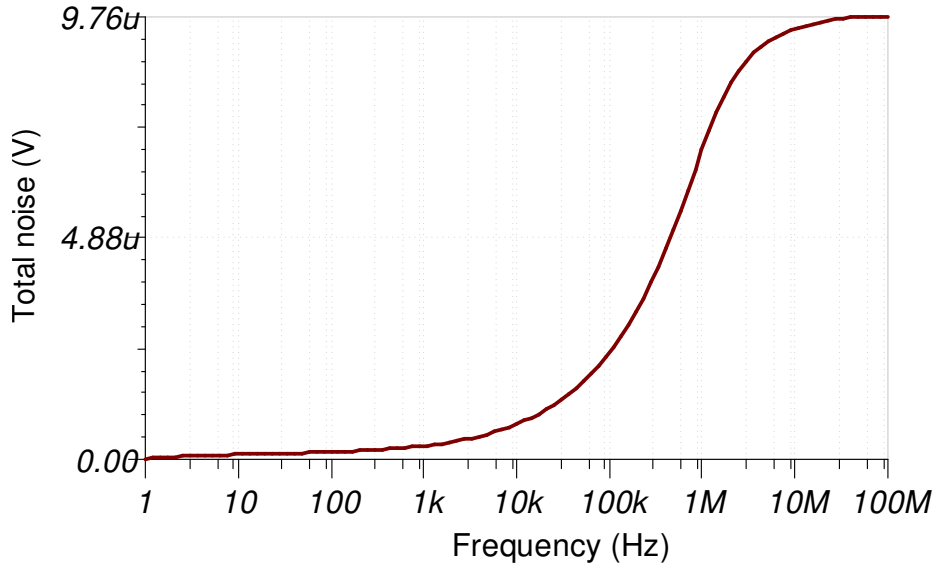
$$e_{noFDA} = \sqrt{\left(3.4\text{nV} / \sqrt{\text{Hz}} \cdot 1.166\text{V} / \text{V}\right)^2 + 2\left(0.5\text{pA} / \sqrt{\text{Hz}} \cdot 1\text{k}\Omega\right)^2 + 2\left(16.56 \cdot 10^{-18} \cdot 1.166\text{V} / \text{V}\right)}$$

$$e_{noFDA} = 7.4\text{nV} / \sqrt{\text{Hz}}$$

$$E_{nFDA} = e_{noFDA} \cdot \sqrt{K_n \cdot f_c} = \left(7.40\text{nV} / \sqrt{\text{Hz}}\right) \cdot \sqrt{1.57 \cdot 1.33\text{MHz}} = 9.28\mu V_{RMS}$$

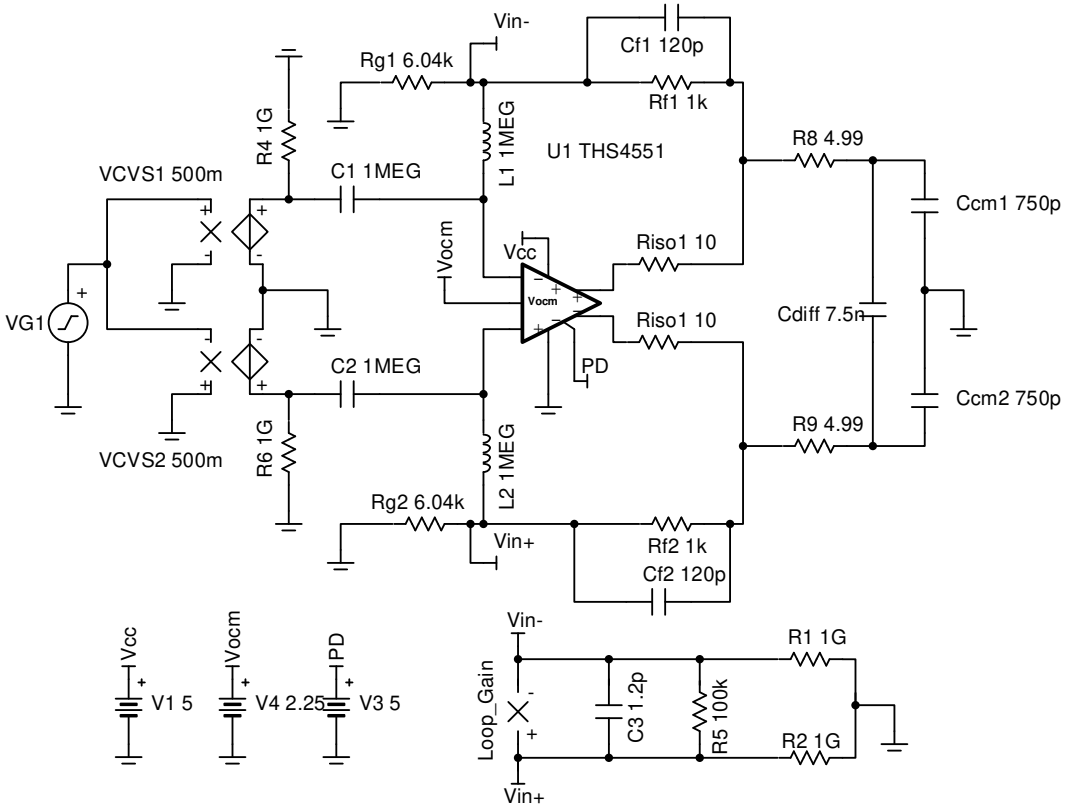
$$\text{Total Noise} = \sqrt{E_{nFDA}{}^2 + E_{nOPA197}{}^2} = \sqrt{\left(9.28\mu V_{RMS}\right)^2 + \left(1.32\mu V_{RMS}\right)^2} = 9.37\mu V_{RMS}$$

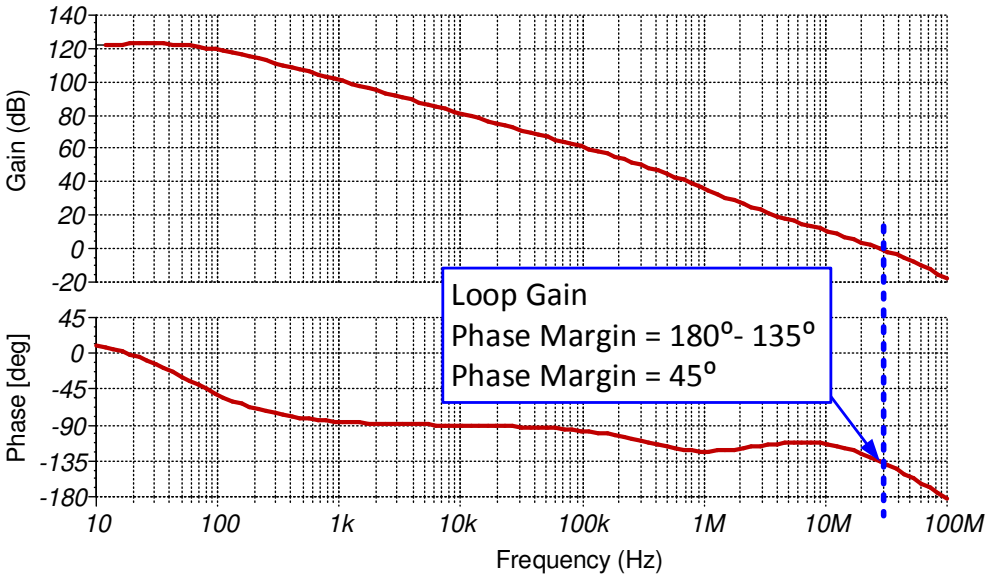
Note that calculated and simulated match well. Refer to *Calculating the Total Noise for ADC Systems* for detailed theory on this subject.



Stability Simulation

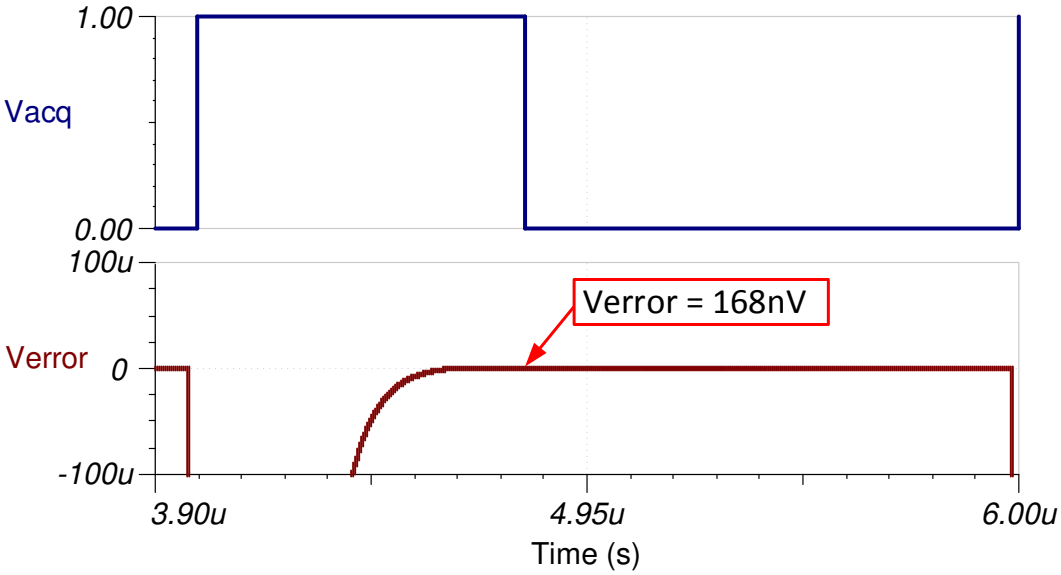
The following circuit is used in TINA to measure loop gain and verify phase margin using AC transfer analysis in TINA. Resistors R_{ISO} = 10Ω are used inside the feedback loop to increase phase margin. The circuit has 45 degrees of phase margin. Refer to *TI Precision Labs - Op Amps: Stability 4* for detailed theory on this subject.





Transient ADC Input Settling Simulation

The following simulation shows settling to a 24-V DC differential input signal with the OPA197 buffers inputs set at +12V and –12V. This type of simulation shows that the sample and hold kickback circuit is properly selected. Refer to *Refine the Rfilt and Cfilt Values* for detailed theory on this subject.



Design Featured Devices

Device	Key Features	Link	Similar Devices
ADS8912B (1)	18-bit resolution, 500-ksps sample rate, integrated reference buffer, fully-differential input, Vref input range 2.5V to 5V.	18-Bit, 1MSPS, 1-Ch SAR ADC with Internal VREF Buffer, Internal LDO and Enhanced SPI Interface	Analog-to-digital converters (ADCs)
THS4551	FDA, 150-MHz bandwidth, Rail-to-Rail Output, VosDriftMax = 1.8µV/°C, e_n = 3.3nV/rtHz	Low Noise, Precision, 150MHz, Fully Differential Amplifier	Operational amplifiers (op amps)
OPA197	36V, 10-MHz bandwidth, Rail-to-Rail Input/Output, VosMax = ±250µV, VosDriftMax = ±2.5µV/°C, bias current = ±5pA	Single, 36V, precision, rail-to-rail input output, low offset voltage op amp	Operational amplifiers (op amps)
REF5045	VREF = 4.5V, 3 ppm/°C drift, 0.05% initial accuracy, 4µVpp/V noise	4.5V, 3-µVpp/V noise, 3-ppm/°C drift precision series voltage reference	Series voltage references

(1) The REF5045 can be directly connected to the ADS8912B without any buffer because the ADS8912B has a built in internal reference buffer. Also, the REF5045 has the required low noise and drift for precision SAR applications. The THS4551 provides the attenuation and common-mode level shifting to the voltage range of the SAR ADC. In addition, this FDA is commonly used in high-speed precision fully-differential SAR applications as it has sufficient bandwidth to settle to charge kickback transients from the ADC input sampling. The OPA197 is a 36-V operational amplifier that provides a very high input impedance front end, buffering the FDA inputs

Link to Key Files

Texas Instruments, SBAC183 source files, software support

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (March 2019) to Revision B (September 2024)	Page
• Updated the format for tables, figures, and cross-references throughout the document	1

Changes from Revision * (February 2018) to Revision A (March 2019)	Page
• Downstyle the title and changed title role to Data Converters and added link to circuit cookbook landing page	1

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