Analog Engineer's Circuit

Circuit To Increase Input Range on an Integrated Analog Front End (AFE) SAR ADC

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Input	ADC Input	Digital Output
VinMin = –40V	AIN-xP = –10V, AIN-xGND = 0V	-131072_{10} or 20000_{H}
VinMax = 40V	AIN-xP = 10V, AIN-xGND = 0V	131071_{10} or $1FFFF_{H}$

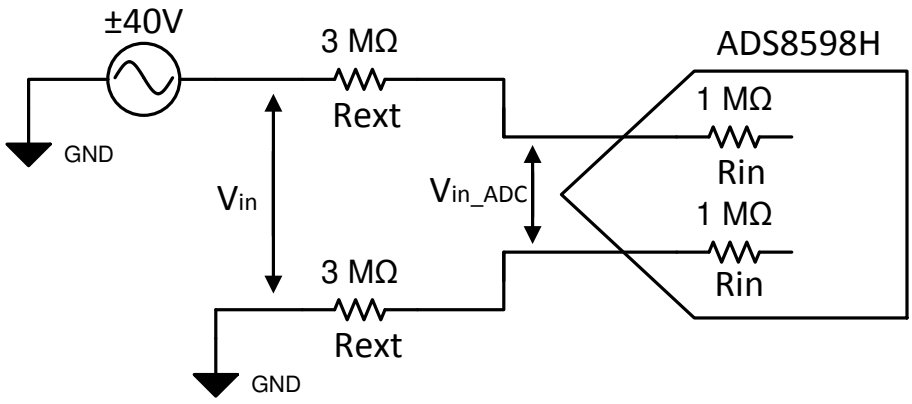
Power Supplies

AVDD	DVDD
5V	3.3V

Design Description

This cookbook design describes how to expand the input range of a SAR ADC with an integrated analog front end (AFE) and decrease the loss of accuracy by implementing a two-point calibration method. This design uses the ADS8598H at the full scale range of ±10V and expands the accessible input range to ±40V. This allows for a wider input range to be used without extra analog circuitry to step down the voltage; instead a simple voltage divider is used to interact with the AFE of the device to step down the voltage near the device input. A calibration method can be implemented to eliminate any error that could occur.

A similar cookbook design, *Reducing Effects of External RC Filter on Gain and Drift Error for Integrated AFE: ±10V, up to 200kHz, 16 bit*, explaining how to measure introduced drift from external components can prove to also be helpful in this application. Increasing the input range that the ADC can measure proves useful in end equipment such as: *Data Acquisition Modules*, *Multi Function Relays*, *AC Analog Input Modules*, and *Control Units for Rail Transport*.



Specifications

Specification	Measured Accuracy Without Calibration	Measured Accuracy With Calibration
±40V	0.726318%	0.008237%

Design Notes

1. Use low-drift resistors to decrease any error introduced due to temperature drift, such as 50ppm/°C with 1% tolerance or better. Note that as resistor values increase to 1MΩ and beyond, low-drift precision resistors can become more expensive.
2. An input filter is frequently required for this configuration. Placing it directly after the large input impedance can cause errors because of the capacitor leakage. If an input filtering capacitor is needed, an alternate schematic is shown in this design.

Component Selection

The internal impedance of the device is 1MΩ, the external resistor is selected based on the desired extended input range (Vin), in this case ±40V. This external resistor forms a voltage divider with the internal impedance of the device, stepping down the input voltage at the ADC input pins (Vin_{ADC}) within the device input range of ±10V.

1. Rearrange the voltage divider equation to solve for the external resistor value. This same equation can later be used to calculate the expected Vin_{ADC} value from the input voltage.

$$V_{in_{ADC}} = V_{in} \cdot \frac{R_{in}}{R_{in} + R_{ext}}$$

$$R_{ext} = \frac{V_{in} \cdot R_{in}}{V_{in_{ADC}}} - R_{in}$$

2. Solve for the external resistor value for the desired extended input voltage. Vin = ±40V, Rin = 1M Ω

$$R_{ext} = \frac{40V \cdot 1M\Omega}{10V} - 1M\Omega$$

The input can be extended to a variety of ranges, depending on what external resistor value is used.

Vin	Rext
±40	3MΩ
±30	2MΩ
±20	1MΩ
±12	200kΩ

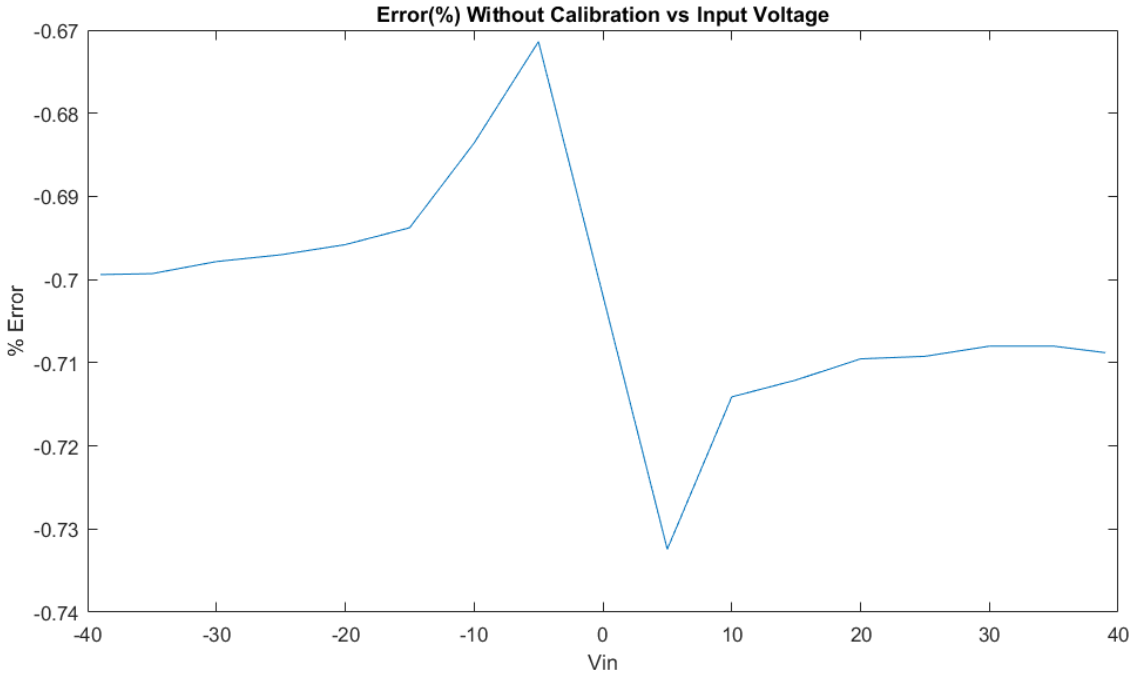
Non-Calibrated Measurements

Different DC input values ranging through the full ±40-V scale were used to measure the ADC voltage input and the accuracy of the measurement. The following equation shows how to calculate the analog voltage read by the ADC. Here the FSR is the system full scale range which is 40V in this case. The factor of 2 is included because this is a bipolar input where the input range is actually ±40V which is a range of 80V. $Vout_{ADC}$ for this equation will range ±40V, which corresponds to the system input.

$$V_{out_{ADC}} = Code_{out} \frac{2 \cdot FSR}{2^N}$$

The percent error of the value is calculated using the next equation:

$$Error(\%) = \frac{V_{in_{ADC}} - V_{out_{ADC}}}{V_{in_{ADC}}} \cdot 100$$



Two-Point Calibration

Calibration can be applied in order to eliminate the reading error introduced by the external resistor. The two-point calibration applies and samples two test signals at 0.25V from the full scale input range within the linear range of the ADC. These sample measurements are then used to calculate the slope and offset of the linear transfer function. Calibration will eliminate both the gain error introduced by the external resistor and the internal device gain error.

1. Apply test signal at –39V:

Vmin	Measured Code
–39V	–128689

2. Apply test signal at 39V:

Vmax	Measured Code
39V	128701

3. Calculate slope and offset calibration coefficients:

$$\text{Error}(\%) = \frac{V_{in_{ADC}} - V_{out_{ADC}}}{V_{in_{ADC}}} \cdot 100$$

$$m = \frac{Code_{max} - Code_{min}}{V_{max} - V_{min}} = \frac{128701 - (-128689)}{39V - (-39V)} = 3299.872$$

$$b = Code_{min} - m \cdot V_{min} = -128689 - 3299.872 \cdot (-39V) = 6.008$$

4. Apply calibration coefficients to all subsequent measurements:

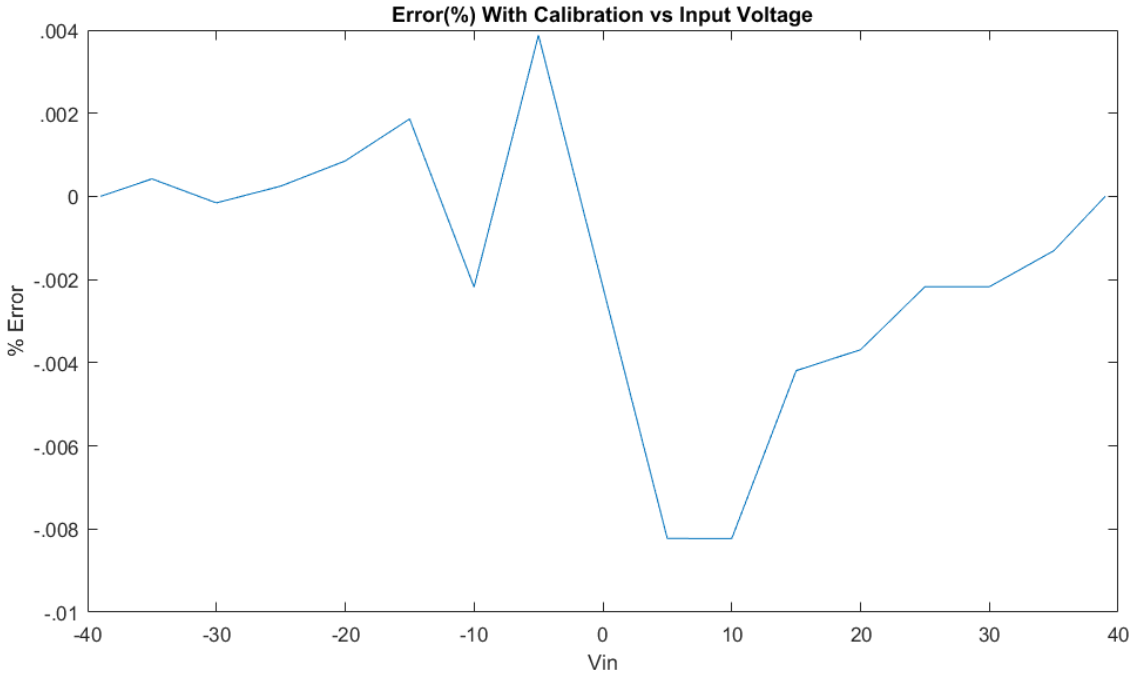
$$V_{in_{Calibrate}} = \frac{Code - b}{m} = \frac{128701 - 6.008}{3299.872} = 38.999$$

Two-Point Calibration Measurements

Calibration Coefficients

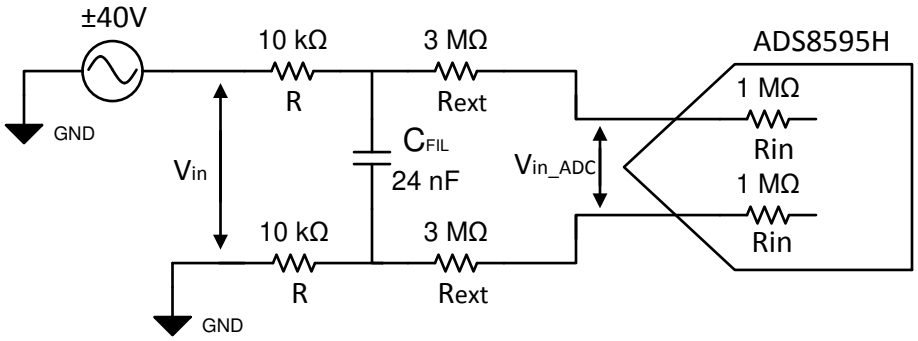
m = 3299.872; *b* = 6.008

When calibration is applied the readings error is dramatically reduced.



Alternate Schematic With Filter Capacitor

Due to the high-value resistors used, introducing a capacitor would lead to significant impact in readings, such as increase drift experienced. This is because of the capacitor leakage. This leakage will vary over time and temperature and will generate errors that are difficult to calibrate out. If an input filter is needed, the alternate schematic can be used to implement it. The capacitor is placed with a balanced resistor-capacitor filter before the external resistors in relation to the input signal.



Alternate Schematic With Filter Capacitor - Component Selection

External anti-aliasing RC filters reduce noise and protect from electrical overstress. A balanced RC filter configuration is required for better common-mode noise rejection; matching external resistors are added to both the negative and positive input paths. These external resistors should also be low-drift resistors as stated in the *Design Notes*.

1. Choose a value of R based on the desired cutoff frequency. This example uses a cutoff frequency of 320Hz, and a resistor value of 10kΩ.

   R = 10kΩ
2. Select C_{FIL}

$$C_{FIL} = \frac{1}{2 \cdot \pi \cdot f_c \cdot 2 \cdot R} = \frac{1}{2 \cdot \pi \cdot 320\text{Hz} \cdot 2 \cdot 10\,\text{k}\Omega} = 24.8\text{nF}$$

   Nearest standard capacitor value available, C_{FIL}= 24nF

Design Featured Devices

Device	Key Features	Link	Similar Devices
ADS8598H	18-bit high-speed 8-channel simultaneous-sampling ADC With bipolar inputs on a single supply	18-Bit 500kSPS 8-Channel Simultaneous-Sampling ADC With Bipolar Inputs on a Single Supply	Precision ADCs

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (March 2019) to Revision B (September 2024) Page

- Updated the format for tables, figures, and cross-references throughout the document..... 1

Changes from Revision * (February 2019) to Revision A (March 2019) Page

- Changed test signal values, equations, calibration coefficients, and graph in the Two-Point Calibration section..... 1
- Added text and an equation to the Non Calibrated Measurements section..... 1
- Downstyle the title and changed title role to 'Data Converters'. Added link to circuit cookbook landing page... 1

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