Analog Engineer's Circuit

High-Voltage Battery Monitor Circuit: ±20V, 0–10kHz, 18-Bit Fully Differential

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Input	ADC Input	Digital Output ADS8910
VinMin = –20V	VoutDif = 4.8V, VoutP = 4.9V, VoutN = 0.1V	$1EB85_H$ or 125829_{10}
VinMax = 20V	VoutDif = –4.8V, VoutP = 0.1V, VoutN = 4.9V	$2147B_H$ or $–125829_{10}$

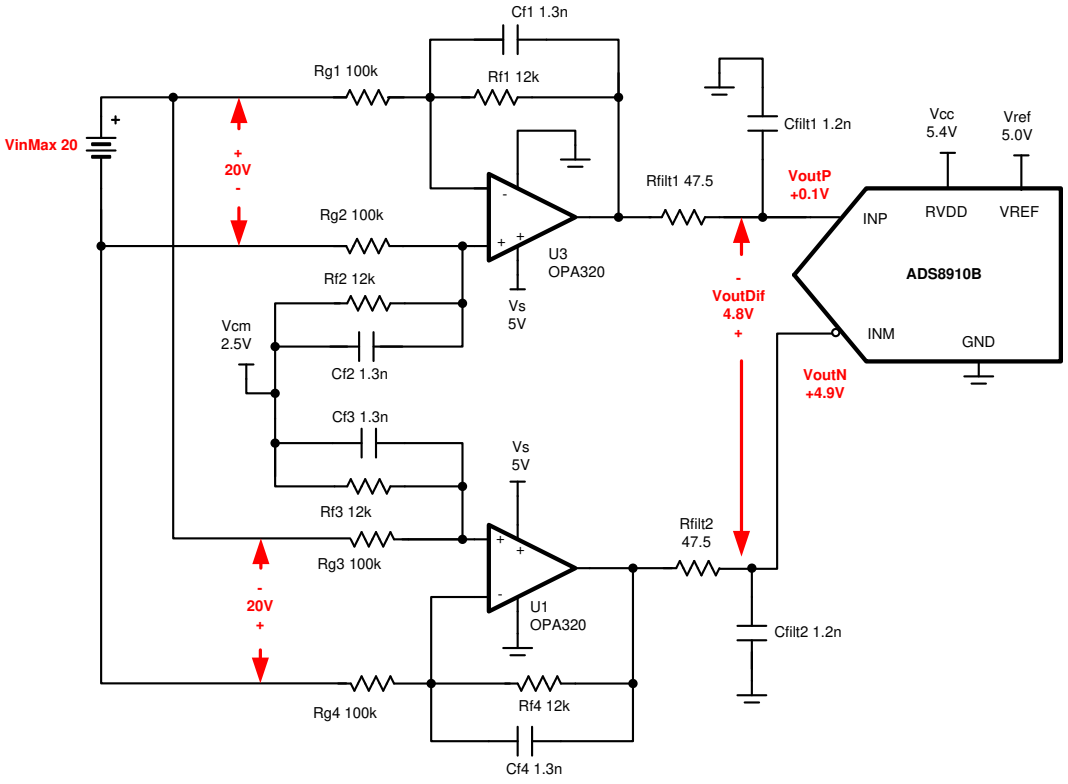
Power Supplies

Vcc	Vee	Vref	Vcm
5.3V	0V	5V	2.5V

Design Description

This design translates an input bipolar signal of ±20V into a fully differential ADC differential input scale of ±4.8V, which is within the output linear operation of amplifiers. The values in the component selection section can be adjusted to allow for different input voltage levels.

This circuit implementation is applicable in accurate voltage measurement applications such as Battery Maintenance Systems, Battery Analyzers, *battery cell formation and test equipment*, *ATE*, and Remote Radio Units (RRU) in wireless base stations.



Specifications

Specification	Calculated	Simulated	Measured
Transient ADC Input Settling	< 0.5LSB or 19µV	6.6µV	N/A
Noise	20.7µVrms	20.65µVrms	30.8µVrms
Bandwidth	10.2kHz	10.4kHz	10.4kHz

Design Notes

1. Determine the linear range of the op amp based on common mode, output swing, and linear open-loop gain specification. This is covered in the component selection section.
2. For capacitors in the signal path, select COG type to minimize distortion. In this circuit Cf1, Cf2, Cf3, Cf4, Cfilt1, and Cfilt2 need to be COG type.
3. Use 0.1% 20ppm/°C film resistors or better for good gain drift and to minimize distortion.
4. Precision labs video series covers methods for error analysis. Review the *Statistics Behind Error Analysis* for methods to minimize gain, offset, drift, and noise errors.
5. The *TI Precision Labs – ADCs* training video series covers methods for selecting the charge bucket circuit R_{filt} and C_{filt}. These component values are dependent on the amplifier bandwidth, data converter sampling rate, and data converter design. The values shown here will give good settling and AC performance for the amplifier, gain settings, and data converter in this example. If the design is modified, select a different RC filter. Refer to *Introduction to SAR ADC Front-End Component Selection* for an explanation of how to select the RC filter for best settling and AC performance.

Component Selection

1. The general equation for this circuit.

$$V_{outMinOpa} = \frac{V_{outDifMin}}{2} + V_{cm}$$

$$V_{outMaxOpa} = \frac{V_{outDifMax}}{2} + V_{cm}$$

$$V_{outDif} = V_{inDif} \times Gain_{dif}$$

$$Gain_{dif} = 2 \times \frac{R_f}{R_g}$$

2. Find op amp maximum and minimum output for linear operation.

$$-0.1\ V < V_{cm} < 5.1V \quad \text{from OPA320 Vcm specification}$$

$$0.035\ V < V_{out} < 4.965\ V \quad \text{from OPA320 Vout swing specification}$$

$$0.1\ V < V_{out} < 4.9\ V \quad \text{from OPA320 Aol specification for linear operation}$$

$$0.1\ V < V_{out} < 4.9\ V \quad \text{Combined worst case}$$

3. Rearrange the equation from part 1 and solve for VoutDifMin and VoutDifMax. Find maximum and minimum differential output voltage based on combined worst case from step2.

$$V_{outDifMax} = 2 \times V_{outMaxOpa} - 2 \times V_{cm} = 2 \times (4.9\ V) - 2 \times (2.5\ V) = 4.8\ V$$

$$V_{outDifMax} = 2 \times V_{outMinOpa} - 2 \times V_{cm} = 2 \times (0.1\ V) - 2 \times (2.5\ V) = -4.8\ V$$

4. Find differential gain based on results from step 3.

$$Gain = \frac{V_{outDifMax} - V_{outDifMin}}{V_{inDifMax} - V_{inDifMin}} = \frac{(4.8\ V) - (-4.8\ V)}{(20\ V) - (-20\ V)} = 0.24$$

5. Find standard resistor values for differential gain. Use *Analog Engineer's Calculator* ("Amplifier and Comparator\Find Amplifier Gain" section) to find standard values for Rf/Rg ratio.

$$\frac{Gain_{dif}}{2} = \frac{R_f}{R_g} = \frac{0.24}{2} = 0.12$$

$$\frac{R_f}{R_g} = 0.12 = \frac{12\ \text{k}\Omega}{100\ \text{k}\Omega} = 0.12$$

6. Find Cf for cutoff frequency.

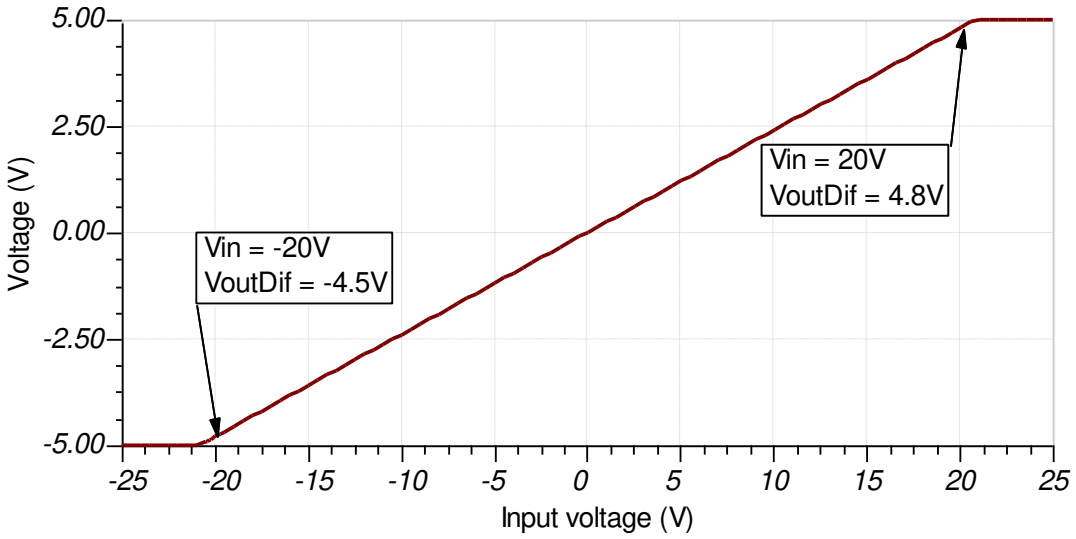
$$f = \frac{1}{2 \times \pi \times C_f \times R_f} = \frac{1}{2 \times \pi \times (1.3\text{nF}) \times (12\text{k}\Omega)} = 10.2\ \text{kHz}$$

$$C_f = \frac{1}{2 \times \pi \times f_c \times R_f} = \frac{1}{2 \times \pi \times (10\ \text{kHz}) \times (12\ \text{k}\Omega)} = 1.326\ \text{nF}\ \text{ or } 1.3\ \text{nF for standard value}$$

$$f = \frac{1}{2 \times \pi \times C_f \times R_f} = \frac{1}{2 \times \pi \times (1.3\ \text{nF}) \times (12\text{k}\Omega)} = 10.2\text{kHz}$$

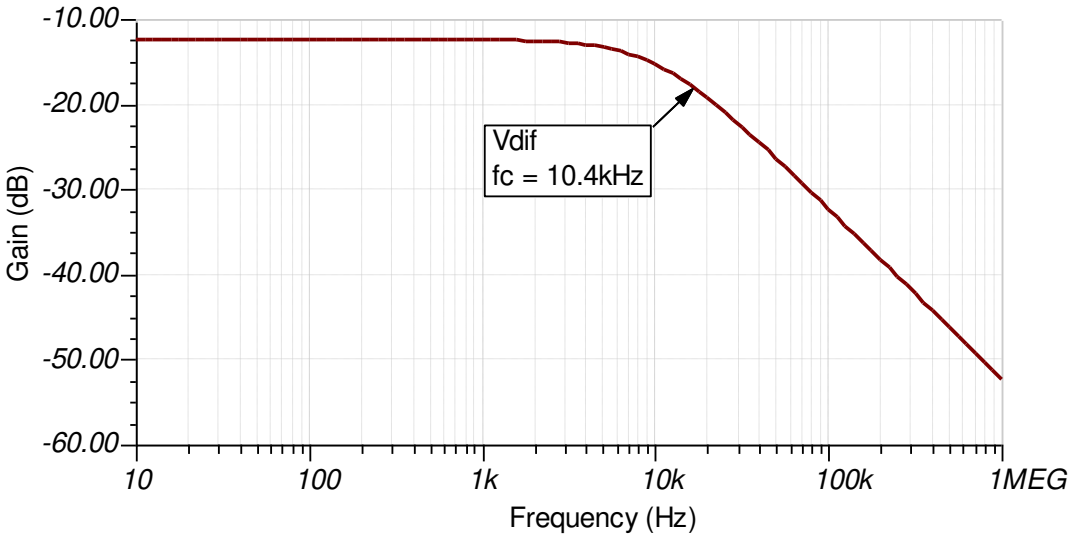
DC Transfer Characteristics

The following graph shows a linear output response for inputs from –20V to +20V. Refer to *Determining a SAR ADC's linear range when using operational amplifiers* for detailed theory on this subject.



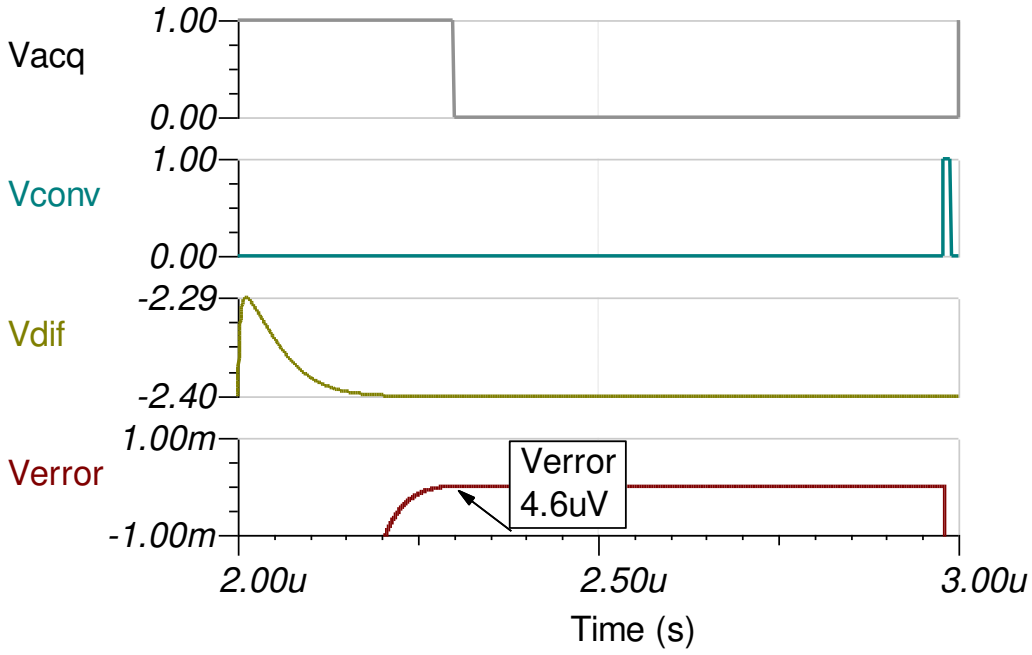
AC Transfer Characteristics

The bandwidth is simulated to be 10.4 kHz, and the gain is –12.4dB which is a linear gain of 0.12. See *Op Amps: Bandwidth 1* for more details on this subject.



Transient ADC Input Settling Simulation

The following simulation shows settling to a –20V dc input signal. This type of simulation shows that the sample and hold kickback circuit is properly selected. Refer to *Introduction to SAR ADC Front-End Component Selection* for detailed theory on this subject.



Noise Simulation

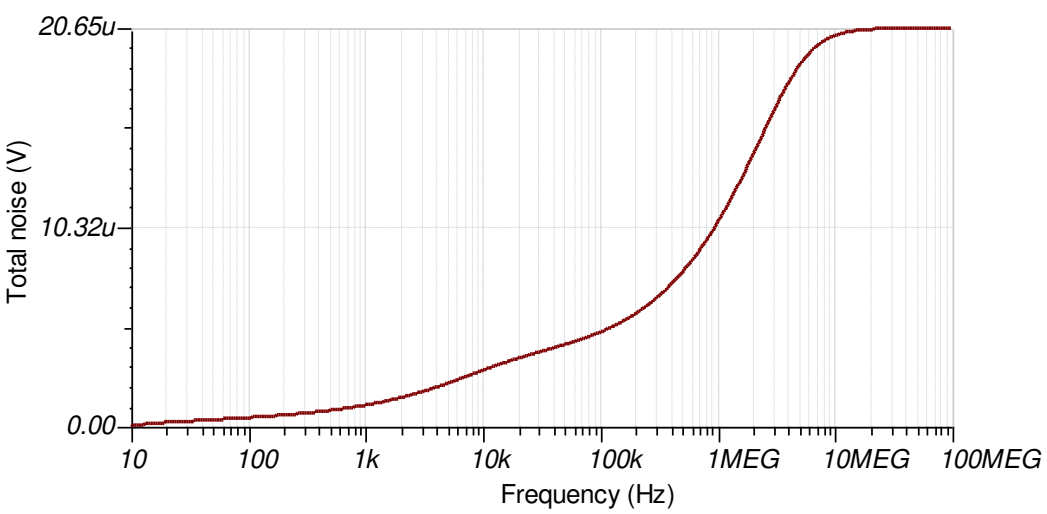
The following simplified noise calculation is provided for a rough estimate. We neglect resistor noise in this calculation as it is attenuated for frequencies greater than 10kHz.

$$f_c = \frac{1}{2 \times \pi \times R_{filt} \times C_{filt}} = \frac{1}{2 \times \pi \times (47.5\Omega) \times (1.2nF)} = 2.8MHz$$

$$E_{n\_se} = e_{n320} \times \sqrt{K_n \times f_c} = \left(7nV \div \sqrt{Hz}\right) \times \sqrt{(1.57) \times (2.8MHz)} = 14.7\mu Vrms \quad \text{for a single ended input}$$

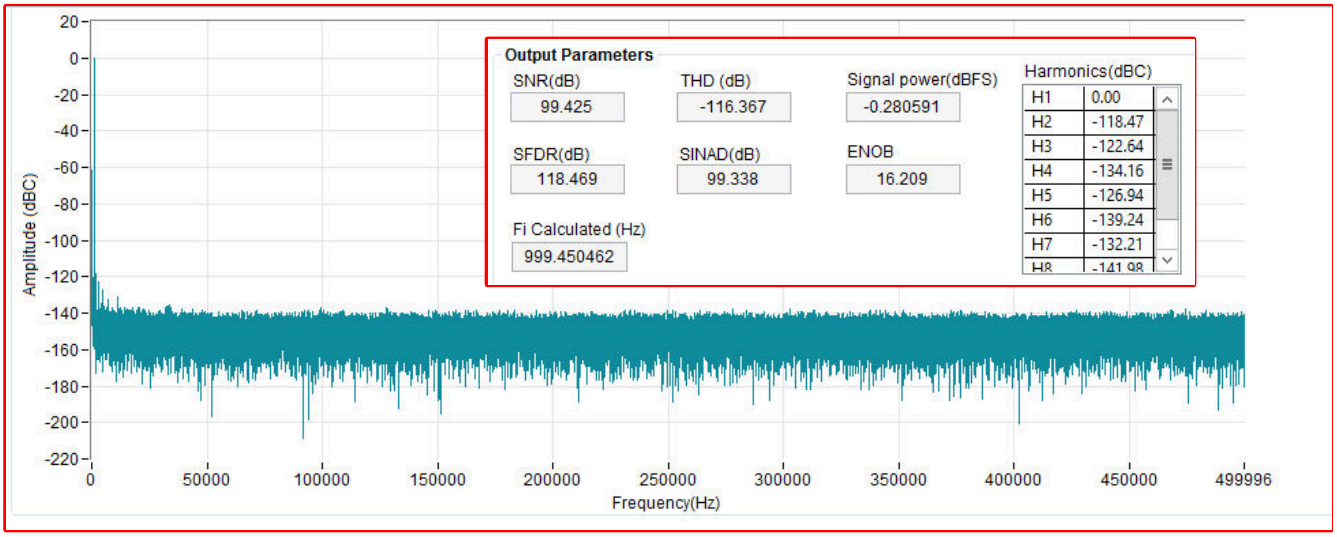
$$E_{n\_tot} = \sqrt{{E_{n\_se}}^2 + {E_{n\_se}}^2} = \sqrt{(14.7\mu V)^2 + (14.7\mu V)^2} = 20.7\mu V \quad rms \quad \text{Total noise for differential amplifier}$$

Note that calculated and simulated match well. Refer to *Calculating the Total Noise for ADC Systems* for detailed theory on this subject.



Measure FFT

This performance was measured on a modified version of the ADS8910BEVM. The AC performance indicates SNR = 99.4dB, and THD = –116.4dB. See *Introduction to Frequency Domain* for more details on this subject.

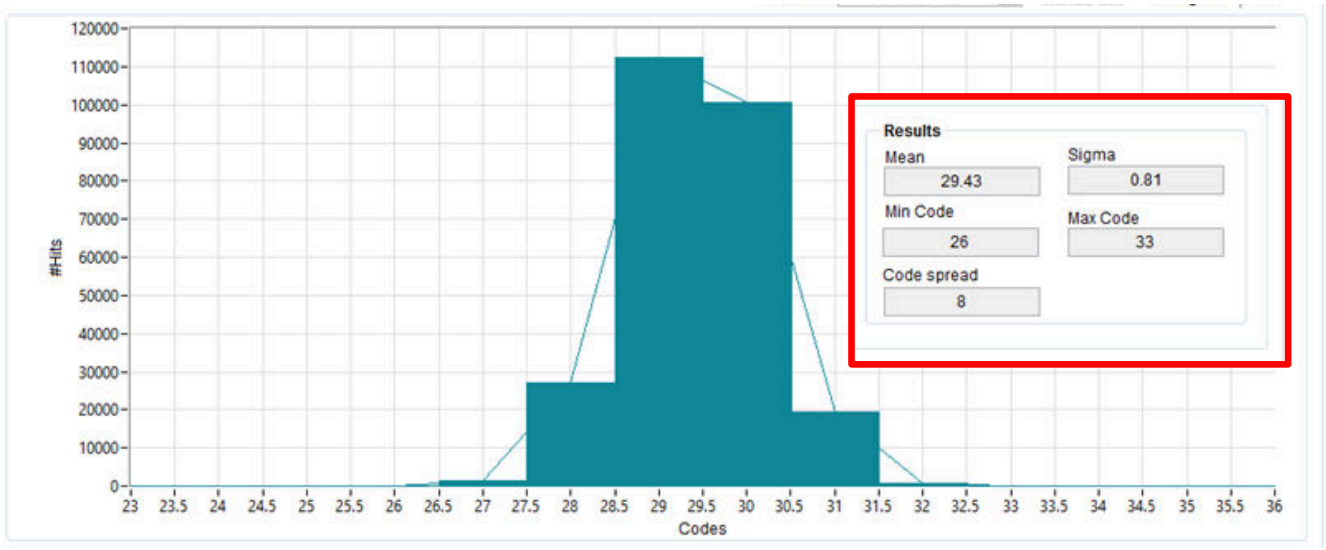


Noise Measurement

The following measured result is for both inputs connected to ground. The histogram shows the system offset and noise. The standard deviation in codes is given by the EVM GUI (0.81), and this can be used to calculate the RMS noise (30.9µV rms) as shown in the following equation.

$$\mathrm{LSB} = \frac{\mathrm{FSR}}{2^{\mathrm{N}}} = \frac{10\ \mathrm{V}}{2^{18}} = 38.14\mu\mathrm{V}$$

$$\mathrm{E_{n\_measured}} = \mathrm{E_{nSigma}} \times \mathrm{LSB} = \left(0.81\right) \times \left(34.14\ \ \mu\mathrm{V}\right) = 30.9\mu\mathrm{Vrms}$$



Design Featured Devices

Device	Key Features	Link	Similar Devices
ADS8900B (1)	18-bit resolution, 1-Msps sample rate, Integrated reference buffer, fully differential input, Vref input range 2.5V to 5V.	20-bit, 1MSPS, one-channel SAR ADC with internal VREF buffer, internal LDO and enhanced SPI	Precision ADCs
OPA320 (2)	20-MHz bandwidth, Rail-to-Rail with Zero Crossover Distortion, VosMax = 150µV, VosDriftMax = 5uV/°C, en = 7nV/rtHz	Precision, zero-crossover, 20MHz, 0.9pA Ib, RRIO, CMOS operational amplifier	Precision op amps (Vos<1mV)
REF5050 (3)	3ppm/°C drift, 0.05% initial accuracy, 4µVpp/V noise	5V, 3µVpp/V noise, 3ppm/°C drift precision series voltage reference	Voltage references

(1) The REF5050 can be directly connected to the ADS8910B without any buffer because the ADS8910B has a built in internal reference buffer. Also, the REF5050 has the required low noise and drift for precision SAR ADC applications. The OPA320 is also commonly used in 1Msps SAR applications as it has sufficient bandwidth to settle to charge kickback transients from the ADC input sampling. Furthermore, the zero crossover distortion rail-to-rail input allows for linear swing across most of the ADC input range.
(2) The REF5050 can be directly connected to the ADS8910B without any buffer because the ADS8910B has a built in internal reference buffer. Also, the REF5050 has the required low noise and drift for precision SAR ADC applications. The OPA320 is also commonly used in 1Msps SAR applications as it has sufficient bandwidth.
(3) The REF5050 can be directly connected to the ADS8910B without any buffer because the ADS8910B has a built in internal reference buffer. Also, the REF5050 has the required low noise and drift for precision SAR ADC applications. The OPA320 is also commonly used in 1Msps SAR applications as it has sufficient bandwidth.

Link to Key Files for High Voltage Battery Monitor

Texas Instruments, SBAC171 design files, software support

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (January 2019) to Revision B (September 2024)	Page
• Updated the format for tables, figures, and cross-references throughout the document	1

Changes from Revision * (December 2017) to Revision A (January 2019)	Page
• Downstyle title, update title role content, added link to circuit cookbook library page	1

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