Application Report
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Low-Cost, Low-Power, Small Size,14-bit AFE: Interleaved ADCs Scalable up to 7.5 MSPS Sampling With 73-dB SNR

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ABSTRACT

Across many segments of the market such as SONAR, thermal cameras, and optical modules there is a need for high-resolution, high-speed, analog-to-digital conversion. Interleaving multiple lower throughput analog-to-digital converters (ADCs) to achieve higher effective throughput offers advantages in terms of lower system power, smaller solution size, and lower system cost. Although interleaving two or more ADCs looks fascinating, it comes with its own set of design challenges. This application note highlights a system design that interleaves three ADS7056 (14 bit, 2.5 MSPS) ADCs to achieve a signal-to-noise ratio (SNR) of 73-dB at an effective sampling rate of 7.5 MSPS. This document also discusses the various possible sources of error and how the unique features of the ADS7056 ADC address these challenges. Design details such as a TINA-TI™ simulation and practical test results are included to give a clear understanding of the system-level performance of the interleaved ADCs.

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Trademarks

1 Overview of the Interleaved ADC Architecture

This section discusses the concept of interleaving of ADCs and the various sources of errors that can limit the performance of the resultant system.

1.1 Concept of Interleaving

Interleaving is a technique of using multiple, identical, lower throughput analog-to-digital converters in parallel to achieve a throughput that is higher than the throughput of each individual ADC. Each ADC receives a phase-delayed signal which initiates the ADC conversion. This signal is also called the ADC conversion start signal. (In various literatures it is also referred as "End of Sampling - EOS or Start of Conversion - SOC signal.) Figure 1 shows a basic block diagram of time-interleaved ADCs. If there are “n” number of ADCs running in parallel, then the phase relationship between conversion start signals is given by Equation 1.

$$\text{Phase } (\theta_k) = 2 \times \pi \times \{(k - 1) / n\} \quad (1)$$

where

- k = 1, 2, 3 ….. n
- n = Number of ADCs used in the system

The effective sampling speed of the system is given in Equation 2.

$$f_{SYSTEM} = n \times f_{SAMPLE} \quad (2)$$

where

- n = Number of ADCs used in the system

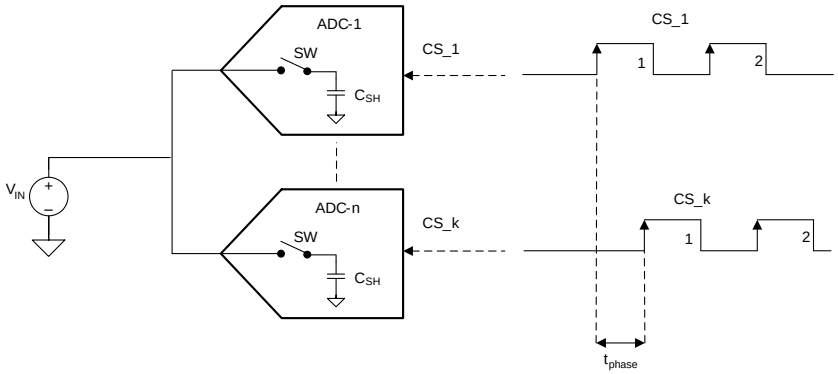

Figure 1. Basic Block Diagram for an Interleaved ADC Architecture

1.2 Errors due to ADC Parameter Mismatch

Interleaving analog-to-digital converters to achieve higher throughput looks attractive and has certain advantages over a single ADC operating at a high sampling rate. However, the possible sources of error that can affect interleaved system performance must be taken into consideration. ADCs that are used in an interleaved fashion are identical but can have mismatches with respect to offset, gain, timing, and ADC sampling bandwidth as a result of slight manufacturing process deviations. We will discuss each error source in detail and see how it affects the overall system performance.

The first source of error that can degrade the performance of an interleaved ADC system is offset mismatch between the individual ADCs. The example here is an interleaved architecture with two ADCs. Suppose each ADC has a different offset and all other parameters are identical. For input voltage close to zero volts, each ADC outputs its own offset in the form of a digitized code at a time interval of 1 / f_{SAMPLE} where f_{SAMPLE} is the sampling frequency of the individual ADC. In time domain, the resultant output code of the interleaved system will alternate between the offset errors of the individual ADCs. In the frequency domain, the error signal is seen as a peak at frequencies that are multiples of the sampling rate (f_{SAMPLE}) of the individual ADCs because the period of the error signal is equal to 1 / f_{SAMPLE}. The noise spur in the frequency domain will appear at the frequency calculated using Equation 3.

$$f_{offset\ noise} = (k \times f_{SAMPLE}) \quad (3)$$

where

- k = 1, 2, 3 ….n
- f_{offset} noise is the frequency where the offset noise occurs
- n is the number of ADCs used in the system
- k is the index of a particular converter

These noise peaks cause signal-to-noise ratio (SNR) degradation in the interleaved system. This SNR degradation is due to the offset mismatch between the individual ADCs and is independent of the input signal amplitude and frequency. The magnitude of the degradation depends on the actual offset mismatch between individual ADCs. A higher offset mismatch will cause more SNR degradation. So, it is recommended to match offset error between the ADCs used in an interleaved system.

The second source of error is gain mismatch between the individual ADCs. Assume again an interleaved architecture with two ADCs and that all parameters are identical between the two ADCs with the exception of gain. ADC gain mismatch error is dependent upon the input signal and increases as the ADC reaches its full-scale input range. The basic error appears with a period of 1 / f_{SAMPLE} while the magnitude of the error depends on the input signal frequency and amplitude. The noise spur in the frequency domain will appear at the frequency calculated using Equation 4.

$$f_{gain\ noise} = f_{in} \pm (k \times f_{SAMPLE}) \quad (4)$$

where

- k = 1, 2, 3 ….n

The third consideration is a timing mismatch between sampling instance of the ADCs. ADC timing mismatch has a multiple of components to it such as clock skew, clock jitter and conversion start signal delay. The basic error due to timing mismatch occurs at the period of 1 /f_{SAMPLE}. The magnitude of the error caused due to skew in the system depends on the input signal frequency (or slew rate). Thus, the noise spur in the frequency domain appears at the frequency calculated using Equation 5.

$$f_{timing\ mismatch\ noise} = f_{in} \pm (k \times f_{SAMPLE}) \quad (5)$$

where

- k = 1, 2, 3 ….n

The fourth consideration is the difference in INL (integral non-linearity) between the converters. For the given input voltage, the INL represents the number of Least Significant Bits (LSBs) or codes that the output of a converter might be in error compared to an ideal ADC. It is not unusual for a converter to have an INL error of a few codes over a majority of its input voltage range. In most ADCs, the INL at a particular output code is not completely un-deterministic. It is often a function of the inherent mismatches in the silicon components. This means that in an interleaved system, the INL mismatch between the ADCs is often far better than the data sheet specification.

The last consideration is the bandwidth mismatch of the converters. Error introduced due to the bandwidth mismatch is dependent upon the input signal frequency and has a gain and phase component to it. If the bandwidth of the converters is just over half their sampling rate, then it would not do much good to interleave them. Fortunately, the bandwidth of most modern data converters is often many times higher than their sample rate and this error introduced due to the bandwidth mismatch can be ignored in most cases.

1.3 System Level Sources of Error in an Interleaved ADC Architecture

The error sources discussed in Section 1.2 relate to mismatches in the specifications of the ADC. At system level, there are various other error sources such as errors introduced due to the offset, offset drift or linearity of the input driver amplifier; drift and settling performance of voltage references; or power supply variation used to power the individual ADCs can affect the performance of the interleaved system.

Figure 2 shows a typical arrangement of interleaved ADC where each ADC is driven using a separate driver amplifier and powered with a separate voltage reference. There is a high possibility that each driver amplifier will have slightly different characteristics with respect to offset, offset drift, linearity and so on. Also, voltage references which are used to provide a stable supply voltage to each ADC may vary with respect to initial accuracy, temperature drift, load regulation, and so forth. Just like ADC mismatches, these mismatch errors in individual driver amplifier and reference can affect interleaved ADC system performance.

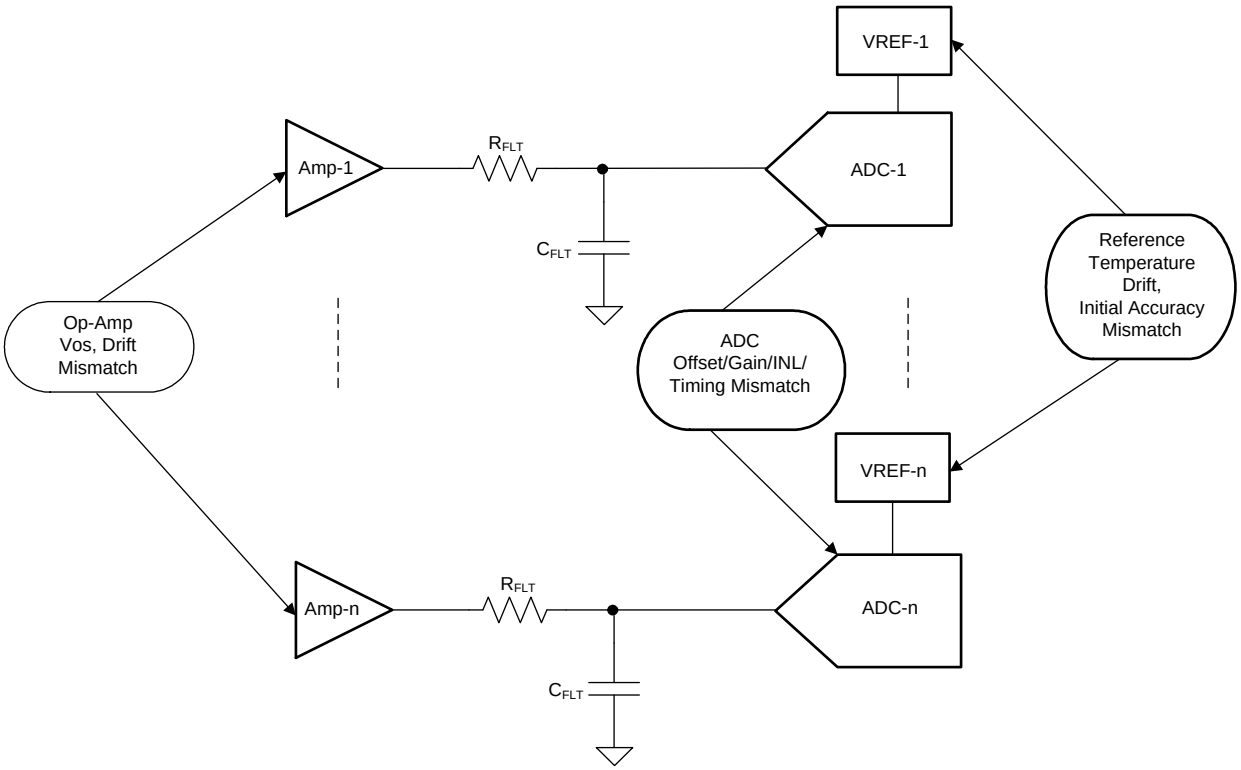

Figure 2. System-Level Sources of Error in an Interleaved ADC System

Analyzing errors associated with multiple driver amplifiers and voltage references requires complex and thorough analysis. There are several research papers which discuss the errors associated with an interleaved ADC architecture as a whole and is found in Section 8.

A better way of dealing with system-level sources of errors is to use a single ADC driver amplifier and single voltage reference for the entire system. This makes sure that errors introduced due the driver amplifier and voltage reference is common for all of the ADCs and that the mismatches introduced by using different amplifier and different reference sources are eliminated. A common driver amplifier is possible if the internal sampling capacitor of the ADCs is small enough such that the time required to

charge this capacitor is minimized and the effect of charge kick back introduced by the internal sampling capacitor is minimized. Also, a common voltage reference is possible if the current requirement from the reference input pin of the ADC is low, then it will not disturb the reference voltage enough to affect the ADC performance. Figure 3 shows a single driver amplifier and voltage reference driven interleaved architecture block diagram and the possible system level errors associated with it.

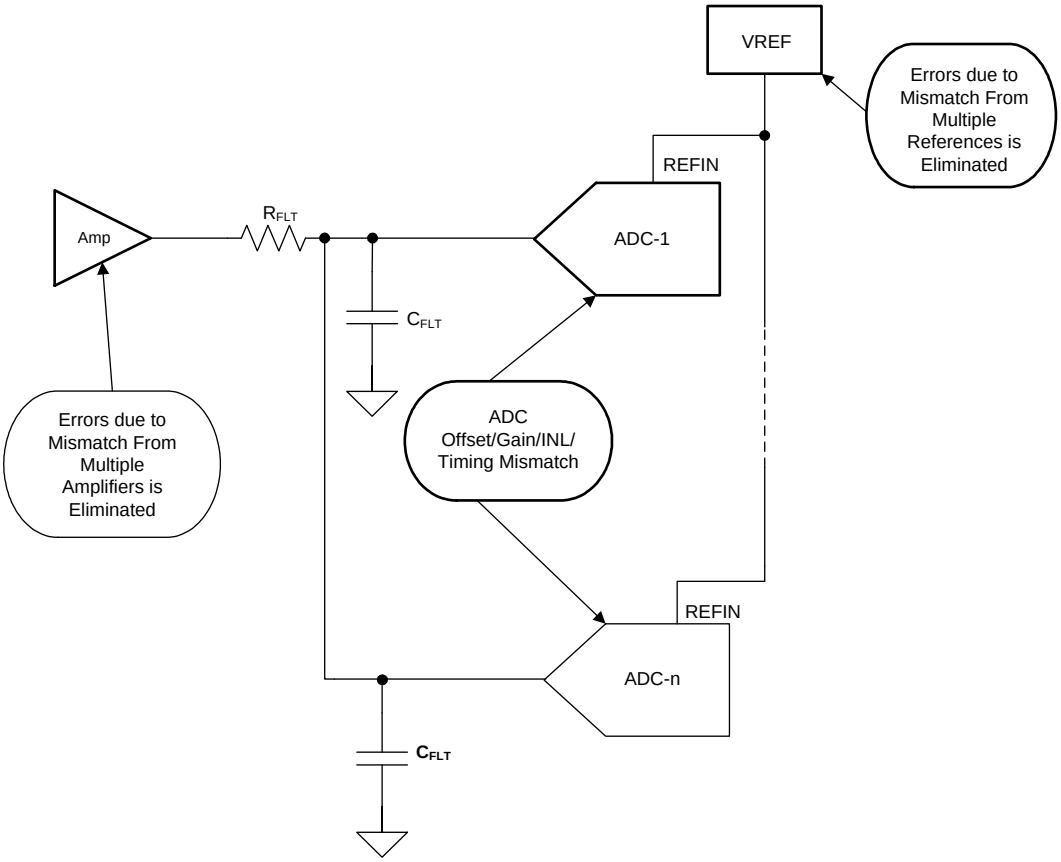

Figure 3. System-Level Errors for a Single Driver, Single Reference Driven Interleaved ADC Architecture

2 Design Considerations

In order to discuss specific design considerations, an example system needs to be defined with a few key system specifications. These specifications will help determine which individual components should be selected to achieve the best system-level performance when using an interleaved ADC architecture.

2.1 Key System Specifications

Table 1 lists the key system specifications.

Table 1. Key System Specifications

Parameter	Performance Specification
Signal-to-noise ratio (SNR) (dB)	73
Total harmonic distortion (THD) (dB)	–85
Sampling speed (MSPS)	7.5
Integral non-linearity (INL) (LSBs)	±3
Offset error (% FSR max)	±0.075
Gain error (% FSR max)	±0.1
Input signal frequency (max) (kHz)	10

2.2 ADC Device Selection (ADS7056)

The ADS7056 is a 14-bit, 2.5-MSPS, analog-to-digital converter (ADC). The device includes a capacitor-based, successive-approximation register (SAR) ADC architecture that supports a wide analog input voltage range (0 V to AVDD, for AVDD in the range of 2.35 V to 3.6 V). The SPI-compatible serial interface is controlled by the $\overline{CS}$ and SCLK signals. The input signal is sampled with the $\overline{CS}$ falling edge and SCLK is used for both the conversion and serial data output clock. The device supports a wide digital supply range (1.65 V to 3.6 V) independent of AVDD voltage, enabling direct interface to a variety of host controllers. The ADS7056 is available in an 8-pin, miniature, X2QFN package measuring 1.5 mm by 1.5 mm and is specified to operate over the extended industrial temperature range (–40°C to 125°C). The miniature form factor and extremely low power consumption make this device suitable for space-constrained applications, or battery-powered applications, or both.

The AVDD pin of the ADS7056 acts as a reference for conversion and demands very low input current. This enables multiple ADS7056 ADCs to be powered from a single voltage reference as the power supply source. The ADS7056 also incorporates an internal offset calibration circuit. This feature is useful for matching the ADC offset errors mentioned earlier that are common with the interleaving architecture. The ADS7056 has a very small internal sampling capacitor (16 pF) which allows multiple ADS7056 ADCs to be driven using a single driver amplifier.

2.3 Driver Amplifier Selection (OPA836)

The selection criterion for the input amplifier is highly dependent upon the input signal type as well as the performance goals of the data acquisition system. Some key amplifier specifications to consider when selecting an appropriate amplifier to drive the inputs of the ADC are:

Small-signal bandwidth: Select the small-signal bandwidth of the input amplifiers to be as high as possible while still meeting the power budget of the system. Higher bandwidth reduces the closed-loop output impedance of the amplifier, thus allowing the amplifier to more easily drive the charge kickback filter at the inputs of the ADC. Higher bandwidth also minimizes the harmonic distortion at higher input frequencies. For a detailed explanation of the driver amplifier selection process, refer to (SLYP166).

One of the important parameters to consider when selecting a driver amplifier for a high sampling speed interleaved ADC system is the step settling response of the amplifier. Figure 4 shows a typical block diagram for interfacing a driving amplifier with an ADC.

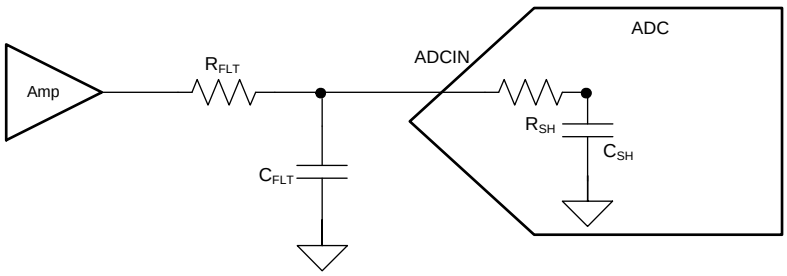

Figure 4. Cascade RC Load at Output of ADC Driver Amplifier

The R-C filter used at the output of the amplifier serves as a charge kick back filter. It is expected that the ADC input voltage V_{IN} should settle to within one LSB of the full-scale range (FS – ½ LSB) within the ADC acquisition time (t_{ACQ}). R_{SH} and C_{SH} are internal to the ADC and are defined in the data sheet. Thus, settling performance highly depends on the selection of the filter components and driver amplifier. A higher value of C_{FLT} will result in poorer settling performance but will also improve the noise performance. A driver amplifier with low output impedance, high output drive capability, high bandwidth and low settling time would be ideal to drive the ADC input.

For the application circuit shown in Figure 5, the OPA836 is selected for its high bandwidth (205 MHz) and low noise (4.6 nV/√Hz), high output drive current (45 mA) and fast settling time (22 ns).

2.4 Voltage Reference Selection (REF2033)

The ADS7056 uses the analog supply voltage (AVDD) as the reference voltage for the analog-to-digital conversion. During the conversion process, the internal capacitors are switched to the level of the AVDD pin as per the successive approximation algorithm. It is important to select a voltage reference with low temperature drift, high output current drive, and low output impedance. For this application, we have selected the REF2033 as the voltage reference and analog power supply for the ADC. The REF2033 has excellent temperature drift performance (25 ppm/°C), good initial accuracy (0.1%), high output drive capability (25 mA), and low quiescent current (360 µA). The REF2033 also has a bias voltage output of half the reference voltage (VREF / 2) which can be used as the common mode input for the amplifier. TI recommends a 3.3-µF (C_{AVDD}), low equivalent series resistance (ESR) ceramic capacitor between the AVDD and GND pins. This decoupling capacitor provides the instantaneous charge required by the internal circuit during the conversion process and maintains a stable dc voltage on the AVDD pin.

3 System Block Diagram

Figure 5 shows the system-level block diagram for three ADS7056s used in an interleaved architecture. The OPA836 is used in a non-inverting buffer configuration to drive the single-ended inputs of all three ADCs. The REF2033 is used to power the AVDD pin of the ADS7056 which also acts as the reference input for the ADC conversion. Each ADC receives a phase-delayed conversion signal from the host controller which is discussed in detail in Section 4. Each ADC operates at its full throughput (14-bit, 2.5 MSPS). The effective throughput of the interleaved system is 7.5 MSPS at 14-bit resolution.

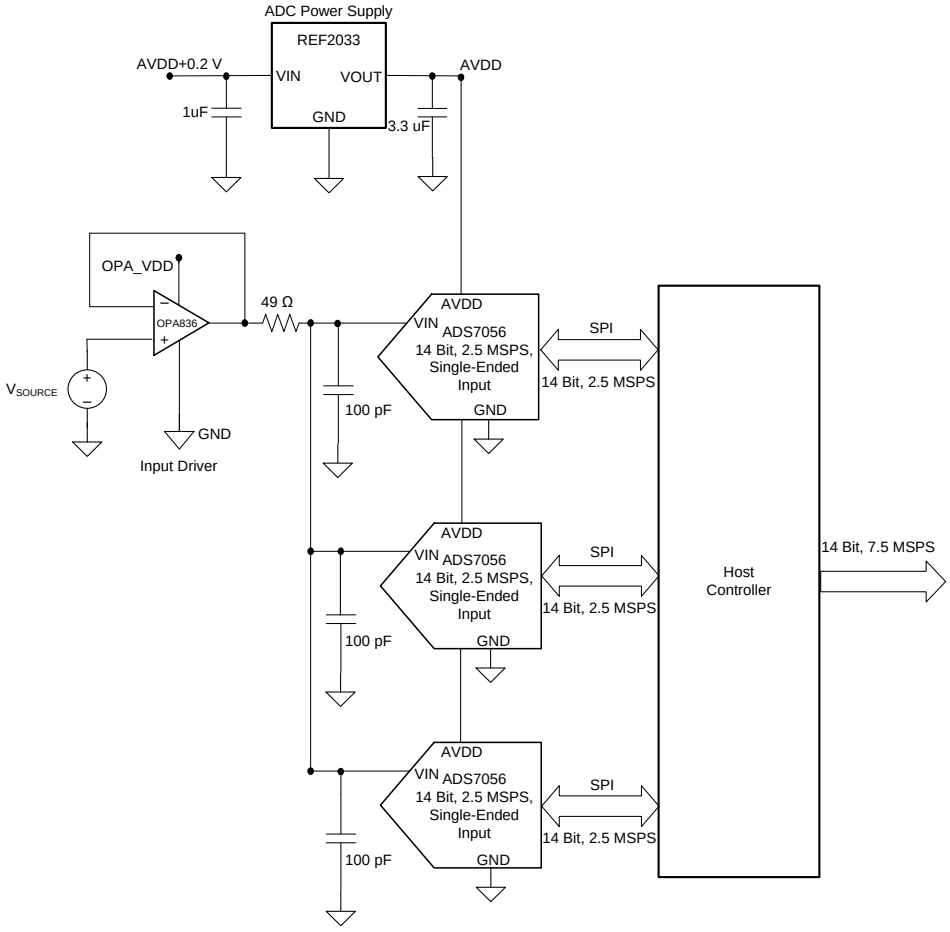

Figure 5. System Block Diagram for Interleaved ADS7056 With Sampling Rate of 7.5 MSPS

4 System Design Theory

4.1 ADS7056 Serial Interface

The ADS7056 ADC supports a simple, SPI-compatible interface to the external host. The $\overline{CS}$ signal period defines one conversion and a serial data transfer frame. The cycle starts with a $\overline{CS}$ falling edge and ends with a $\overline{CS}$ rising edge. The SDO pin is tri-stated when $\overline{CS}$ is high. With $\overline{CS}$ low, the clock provided on the SCLK pin is used for conversion as well as data transfer and the output data is available on the SDO pin. The ADS7056 supports three functional states: Acquisition (ACQ), Conversion (CNV), and Offset Calibration (OFFCAL). The device state depends on the $\overline{CS}$ and SCLK signals provided by the host controller.

During the acquisition phase of the ADS7056, the input sampling switches are closed and the analog input signal is acquired on the internal sampling capacitor of the device. This phase should last for a minimum of 95 ns. This is given as "t_{ACQ}" in the device data sheet. The conversion process requires a minimum of 18 SCLK falling edges be provided within the frame. After the end of the conversion phase, the device automatically moves from the conversion phase back to the acquisition phase.

Assuming that the ADS7056 is operating at the full throughput of 2.5 MSPS, the ADC will require a clock signal frequency of 60 MHz (resulting in a clock period of 16.66 ns). If we calculate the acquisition time in terms of the number of clock cycles required, then the acquisition time required for the ADC is given by Equation 6.

$$\text{Number of clocks in ACQ Cycle} = 95\ \text{ns} / 16.66\ \text{ns} = 6\ \text{Clocks} \quad (6)$$

Thus, the device requires 24 clock cycles to complete both the signal acquisition and conversion cycles. Figure 6 shows the timing diagram for the acquisition and conversion phase of a single ADS7056 ADC.

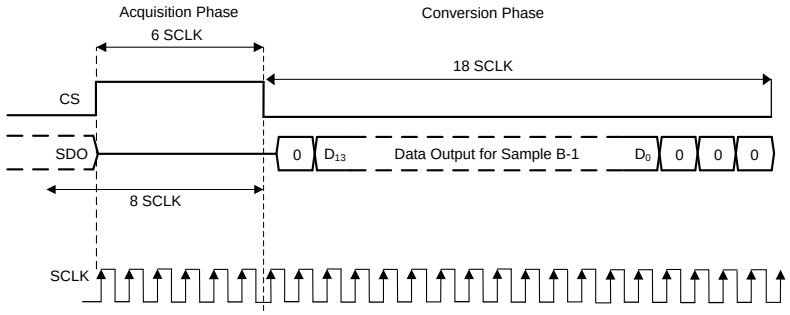

Figure 6. ADS7056 Timing Diagram for One Acquisition + Conversion Cycle

4.2 Architecture for Interleaving Three ADS7056 ADCs to Achieve a Sampling Speed of 7.5 MSPS

Section 1.1 discussed that the architecture of interleaving of multiple ADCs can be achieved by providing a phase-shifted control signal to initiate each ADC conversion cycle. This can be achieved with the ADS7056 by using a phase-delayed conversion start signal ($\overline{CS}$) to initiate the conversion phase for each ADC. This allows for the same clock signal to be used for the conversion and serial data output of each ADC. Furthermore, the ADC conversion start signal ($\overline{CS}$) is derived from the same system clock. Thus, the $\overline{CS}$ falling edge used for the start of conversion and the $\overline{CS}$ rising edge used for the acquisition phase are in-sync with the clock source. This eliminates any displacement of sampling instant from its ideal position. Figure 7 shows the timing diagram for the interleaved ADS7056 system.

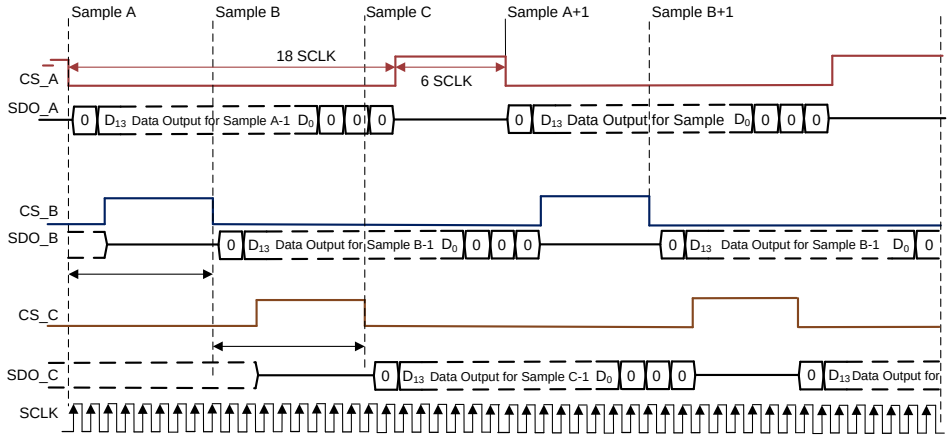

Figure 7. Timing Diagram for Interleaving Three ADS7056 to Achieve Sampling Speed of 7.5 MSPS

The phase relationship between the conversion start signals in the time-interleaved system is given by Equation 7:

$$\text{Phase } (\theta_k) = 2 \times \pi \times \{(k - 1) / n\} \quad (7)$$

where

- k is the sequence order in which the ADC is given a conversion start signal
- n is total number of ADCs in the system

Thus, for a system that uses three ADCs in an interleaved manner, the phase difference between the conversion start signal should be 120°. Using the ADS7056, this can be achieved by phase-shifting the conversion start signal for each ADC ($\overline{CS}$) by 8 clocks. This is equivalent to the total number of required clocks for the acquisition and conversion cycle of each ADC divided by the number of ADCs (24 clocks / 3 ADCs).

4.3 Matching ADC Offset and Gain Errors in an Interleaved System

The effect of offset and gain mismatches in an interleaved system has been studied extensively and several resources are listed in Section 8. When an input signal is not present, each ADC converts its own offset and outputs a code. Thus, for a time-interleaved ADC system output, changes between offset output by each ADC at a frequency which is equal to the sampling speed of ADC. This can introduce a tone at the sampling frequency of each ADC (f_{SAMPLE}). This can add to the overall noise and increase harmonic power which degrades the AC performance of the ADC to a great extent. ADC offset and gain errors can be calibrated in the digital domain but this requires effort and possibly additional power consumption on the processor side.

When ADC offset errors are not matched, then each ADC digitizes its own offset voltage and gives a corresponding output code. This can be seen by plotting a DC histogram of all of the ADCs (refer to Section 6.1). One more way to see the effect that the offset errors of the individual ADCs have on system performance is to do an FFT analysis by applying a known sine wave signal to the input of the interleaved ADC system. A tone at the sampling frequency of the individual ADCs in the frequency domain will appear due to the offset mismatch between the individual ADCs. This tone degrades overall SNR and THD performance (refer to Section 6.2).

One of the very important reasons why the ADS7056 is best suited for an interleaved ADC architecture is its integrated offset calibration feature.

In the offset calibration state, the device calibrates and corrects for its internal offset errors. The sampling capacitors are disconnected from the analog input pins (AINP and AINM). Device offset can be calibrated when the device is powered on or it can be a user-initiated calibration during normal operation. The offset calibration is effective for all of the subsequent conversions until the device is powered off. For more information on offset calibration of ADS7056 refer to the ADS7056 device data sheet (SBAS769).

During the ADS7056 calibration process, the input sampling switch is opened and the input voltage is compared with the reference voltage (derived from AVDD) to calibrate the offset errors. This pin demands very low input current which enables it to power up multiple ADS7056s from a single power supply. Since all of the ADS7056 ADCs are powered from the same voltage reference source, the resulting output code of the ADCs will match after calibration. This can be verified by plotting a DC histogram of the interleaved system and looking for the offset mismatch tone in the FFT spectrum. The reduced magnitude of the tone at the sampling frequency indicates an improvement in the AC performance, refer to Section 6.2.

Gain mismatch of the interleaved system can be measured by applying a known input voltage close to the maximum full-scale range of the system. If there is gain mismatch between the ADCs, it will appear as a spur in the frequency domain with the spur centered at $f_{SAMPLE} \pm f_{in}$, where f_{SAMPLE} is the sampling frequency of a single ADC and f_{in} is the input signal frequency. The best way to reduce gain mismatch between different ADCs is to configure the gain of one ADC as the reference and match the gain of the other ADCs to this ADC. As shown in Figure 8, the variation of gain error for the ADS7056 across 6000 devices is only 0.02% (or 3.2 LSBs). Therefore, matching and calibration of gain error to achieve a system performance of 73-dB SNR is not required.

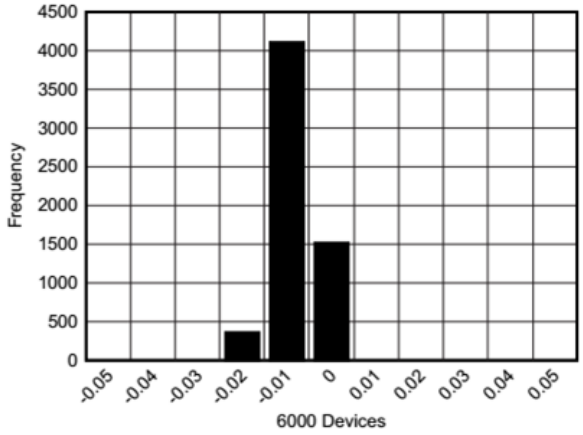

Figure 8. Gain Error Variation of ADS7056

The internal offset calibration feature of the ADS79056 ADC enables us to match ADC offset while the system is running. The internal offset calibration and very low gain error specification gives fairly good performance provided that all ADC offsets are matched with an error of less than 1 LSB. Using the internal offset calibration feature of the ADS7056 yields very good results for the 14-bit system. A more comprehensive method may be needed for higher resolution interleaved ADCs.

4.4 Addressing Bandwidth Mismatch

Bandwidth mismatch is one of the trickiest parameters when it comes to an interleaved ADC system. Bandwidth mismatch is dependent upon the input signal frequency and has a gain and phase component. The easiest way to deal with bandwidth mismatch is to select an ADC with a full power bandwidth much higher than half of its sampling speed (f_{SAMPLE} / 2). The full power bandwidth of the ADS7056 is 200 MHz which is much higher than half of the sampling speed (1.25 MHz) and makes this device suitable for interleaving applications. The bandwidth of the charge kickback filter at the input of ADC is approximately 10 MHz (R = 49 Ω, C = 3 × 100 pF). Thus, the bandwidth of the external filter dominates. Any mismatch in capacitor values used at the analog input of each ADC dominates the bandwidth mismatch for the interleaved design. It is recommended to use COG or NP0 ceramic capacitors with better than 5% tolerance to limit the errors due to bandwidth mismatch.

4.5 Addressing INL Mismatch

Figure 9 shows the variation of INL across 6000 ADS7056 devices. The variation of the minimum INL is 1.5 LSB and the variation of the maximum INL is 1 LSB. These variations are not expected to affect the desired system performance of 73-dB SNR.

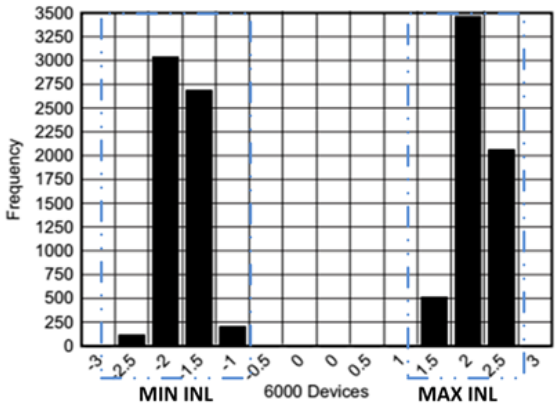

Figure 9. INL Variation of ADS7056

5 Simulation Results

In order to verify overall system performance, the input driver circuit was simulated for stability and noise performance while the voltage reference circuit was simulated for settling performance. Figure 10 shows the TINA-TI simulation circuit used for the simulation.

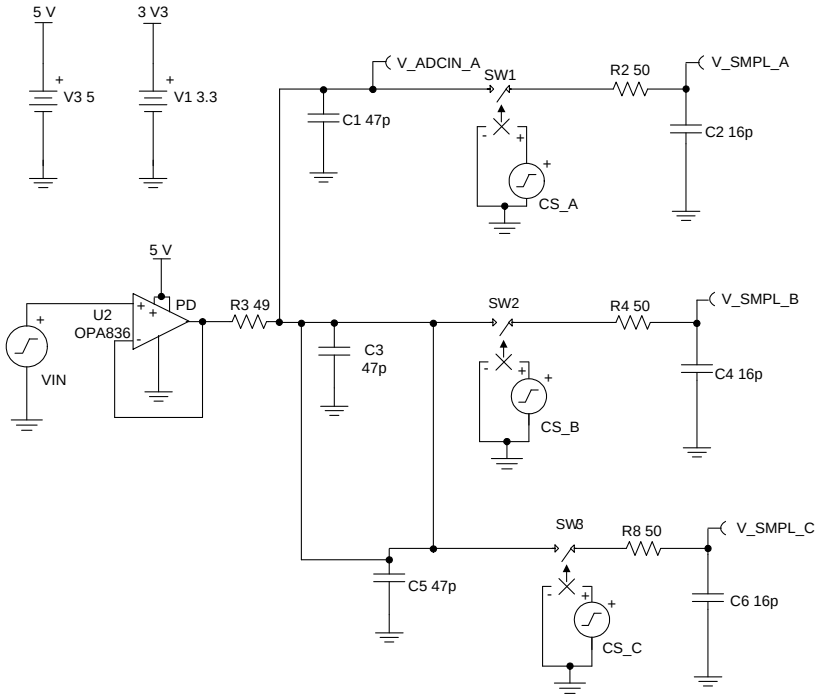

Figure 10. TINA-TI™ Schematic for Input Driver Settling and Noise Analysis

5.1 Settling Analysis of Input Driver Circuit

To check the settling of the input driver circuit, a step input of 3 V was applied to the inputs of the amplifier and the ADC sample and hold inputs were measured. The ADC input settles to the final value and does not show any oscillations. The designed circuit is stable for a step input and does not introduce any unwanted signals. Figure 11 shows the resulting output waveform for the step input. To achieve full-scale step settling response, a charge kickback filter capacitor value of 47 pF is selected. Whereas, to achieve the best signal-to-noise ratio, a filter capacitor value of 100 pF is recommended.

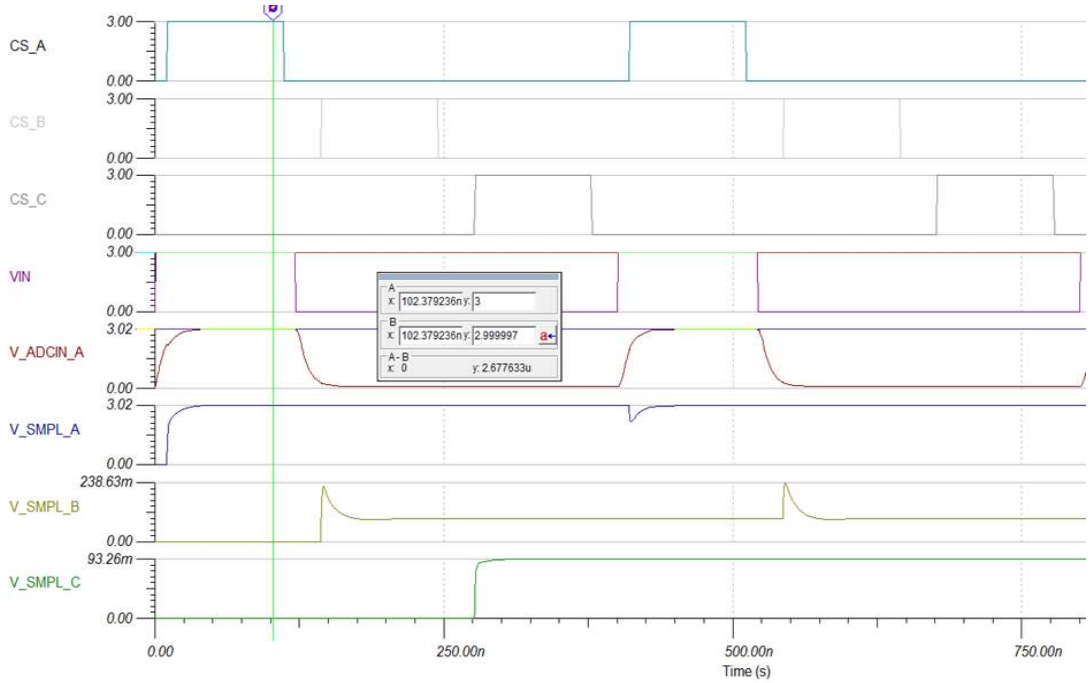

Figure 11. TINA-TI™ Simulation Results for Input Driver Settling

5.2 Noise Analysis of Input Driver Circuit

Ideally, to calculate the referred-to-output (RTO) noise from the input driver, the voltage noise density curve must be integrated to infinity. For a realistic approximation of the RTO noise, integration to beyond twice the bandwidth of the system is sufficient. Figure 12 shows the TINA-TI™ simulation circuit for measuring the system noise. Figure 13 shows that the simulated integrated noise from the amplifier input driver referred to the output is 73.68 μV_{RMS}.

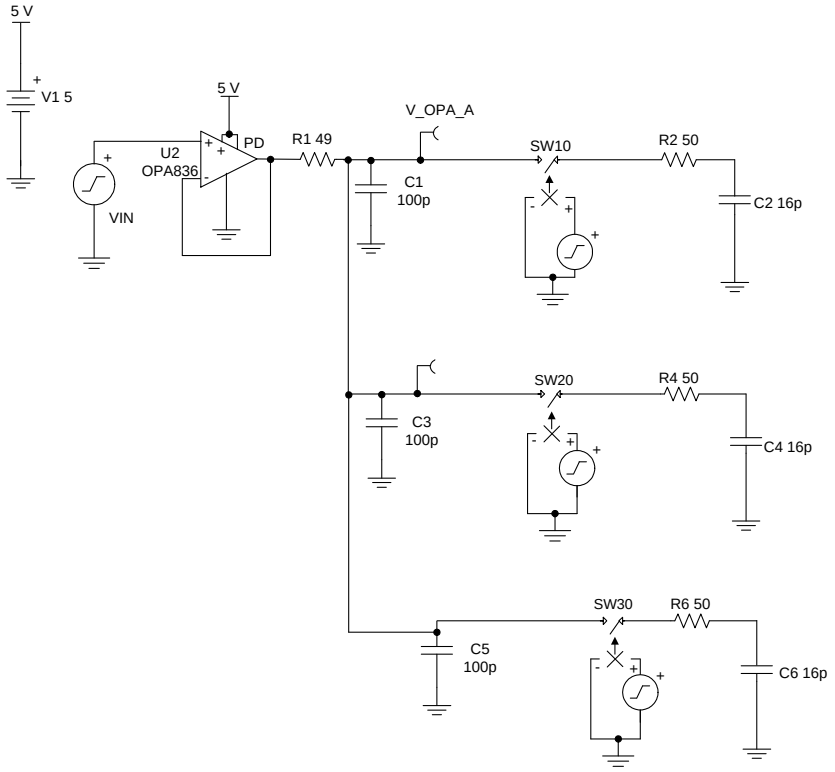

Figure 12. TINA-TI™ Schematic for Noise Analysis of Front End Driver

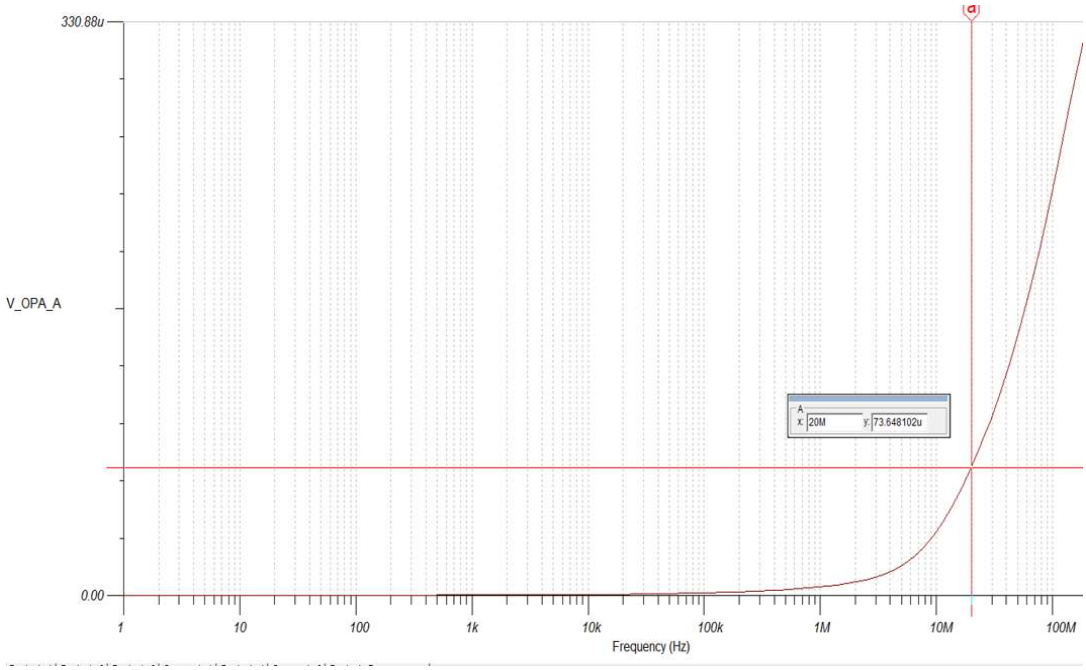

Figure 13. TINA-TI™ Simulation Results for Input Driver Noise Analysis

5.3 Settling Analysis of Voltage Reference Circuit

To maintain the overall system performance, the voltage at the REF2033 output pin must settle to less than 1 LSB of the ADS7056 ADC. To simulate reference settling performance, REF2033 is loaded with equivalent current sources modeled for AVDD current of ADS7056. The TINA-TI schematic shown in Figure 14 is used to check the settling of the reference which is used to power the ADC. Simulation results in Figure 15 shows that the ADS7056 consumes approximately 1-mA current at 2.5 MSPS of throughput from the AVDD supply. The switching current consumed by each ADC is provided by the decoupling capacitor (2.2 µF) on the AVDD pin of the ADC. The reference sees a DC load current of 3.5 mA and settles to (FS – ½ LSB) in less than 1 ms and remains stable while all the ADCs are converting at 2.5-MSPS throughput.

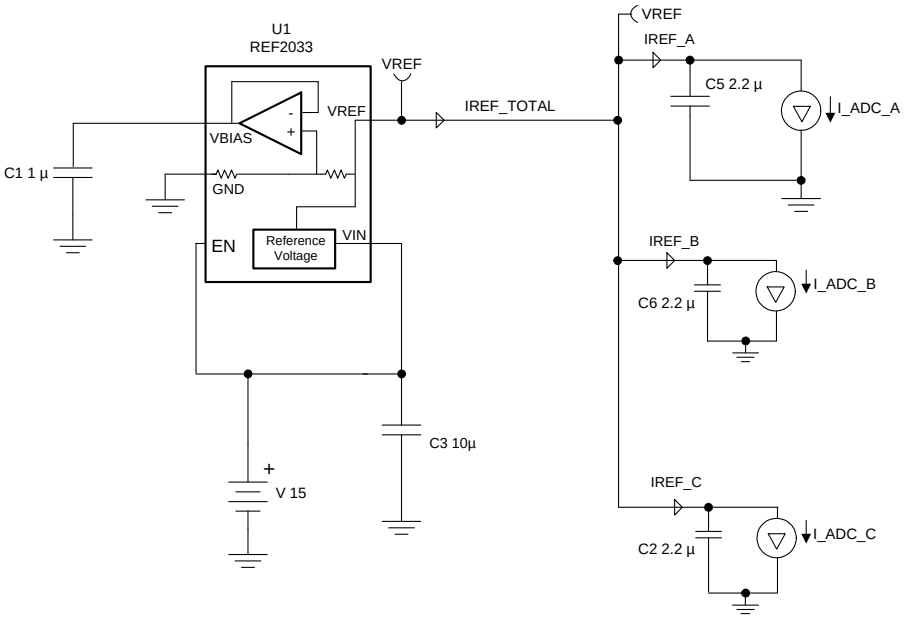

Figure 14. TINA-TI™ Schematic for Voltage Reference Settling

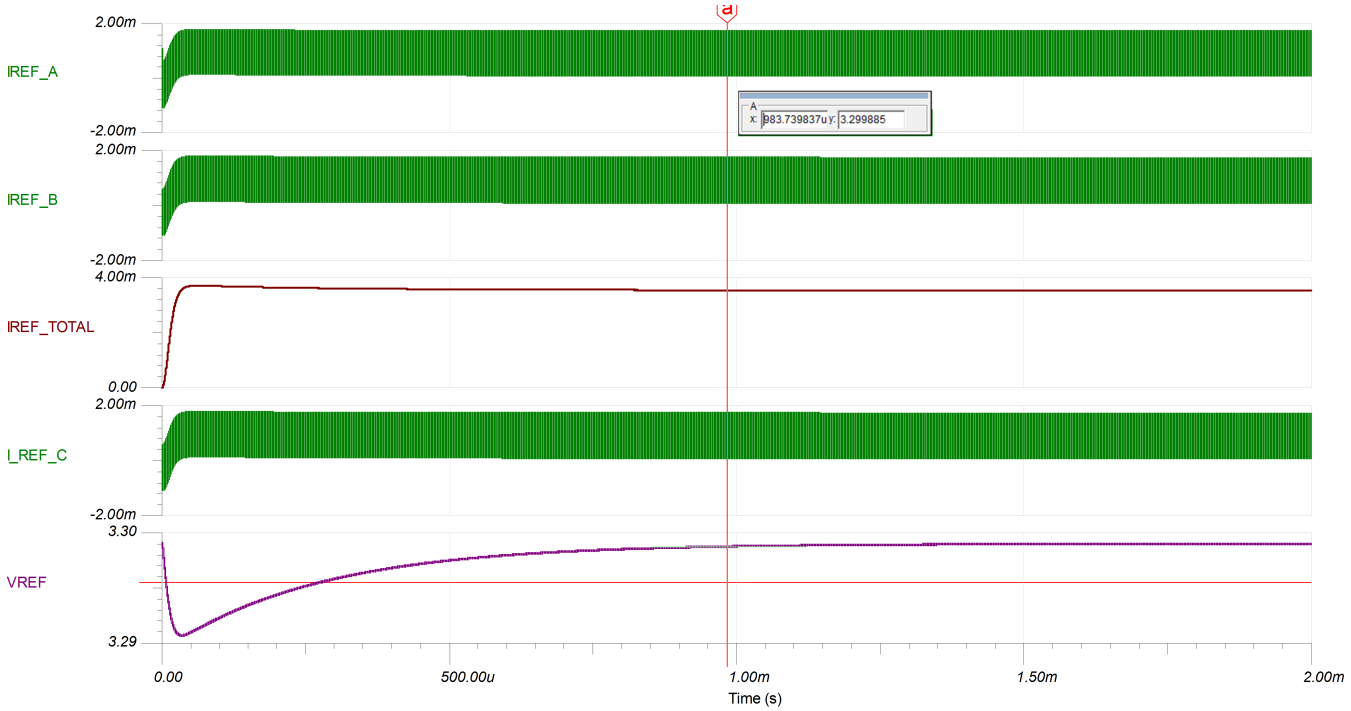

Figure 15. TINA-TI™ Simulation Results for Voltage Reference Settling

6 Experimental Results

This section lists measurement results for verification of this design. Various ADC-related parameters such as a histogram at zero input and full-scale input and an FFT plot highlighting SNR and THD performance at 2 kHz are captured to highlight the difference in performance of an uncalibrated and a calibrated system.

6.1 DC Histogram

6.1.1 DC Histogram at Zero Input and Full-Scale ADC input for an Uncalibrated System

To see the effect of offset mismatch between individual ADCs, the interleaved system histogram is captured at zero input and at an input close to the full-scale range of the system. For the uncalibrated system, each of the ADCs outputs a different code based on the offset mismatch between the individual ADCs.

Figure 16 shows the histogram for an uncalibrated system when the input applied to the interleaved ADC is zero. Figure 17 shows the histogram for an uncalibrated system when the input applied is close to the full-scale input range (3.1 V).

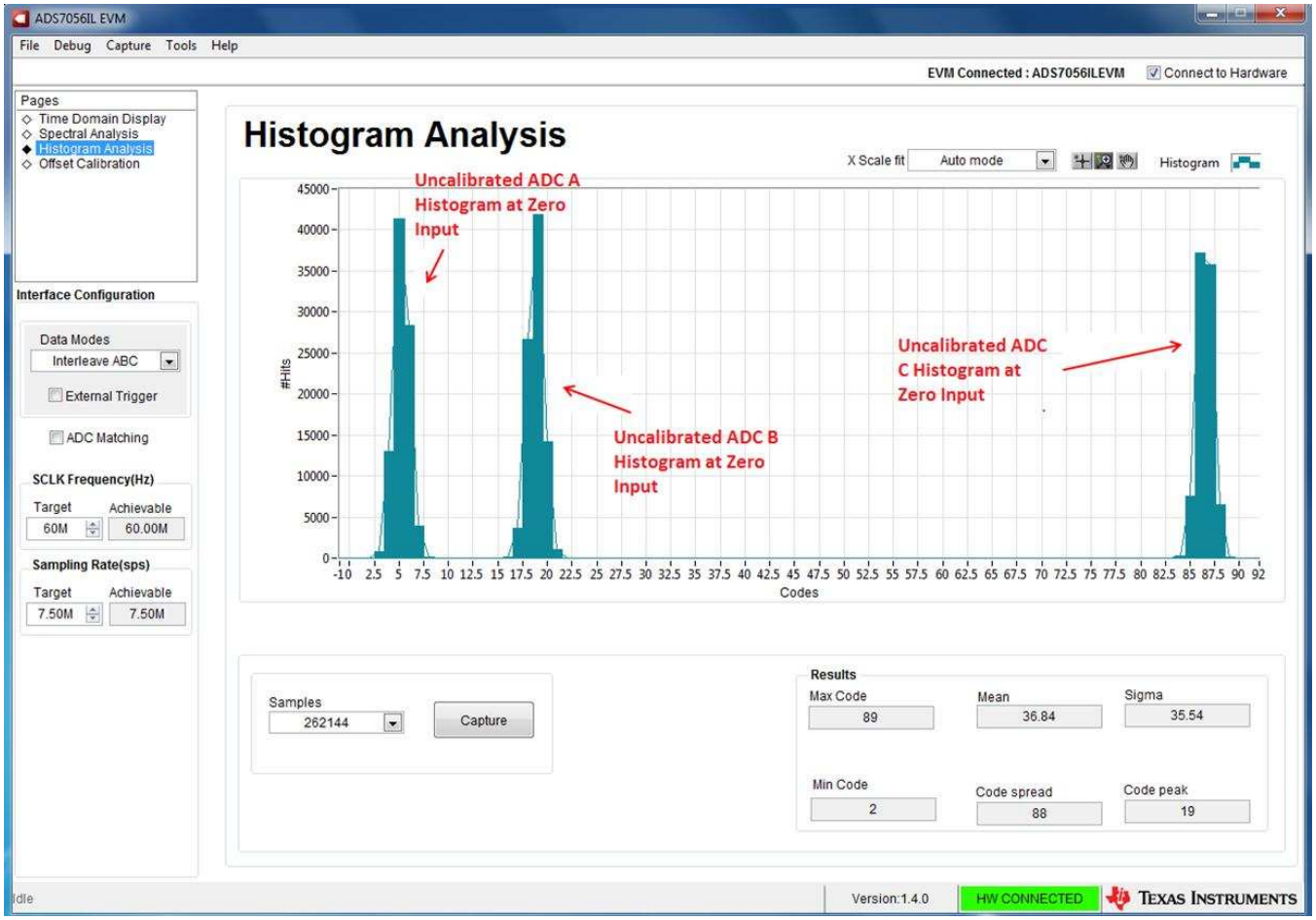

Figure 16. Histogram Plot for Uncalibrated Interleaved ADS7056 System at Zero Input

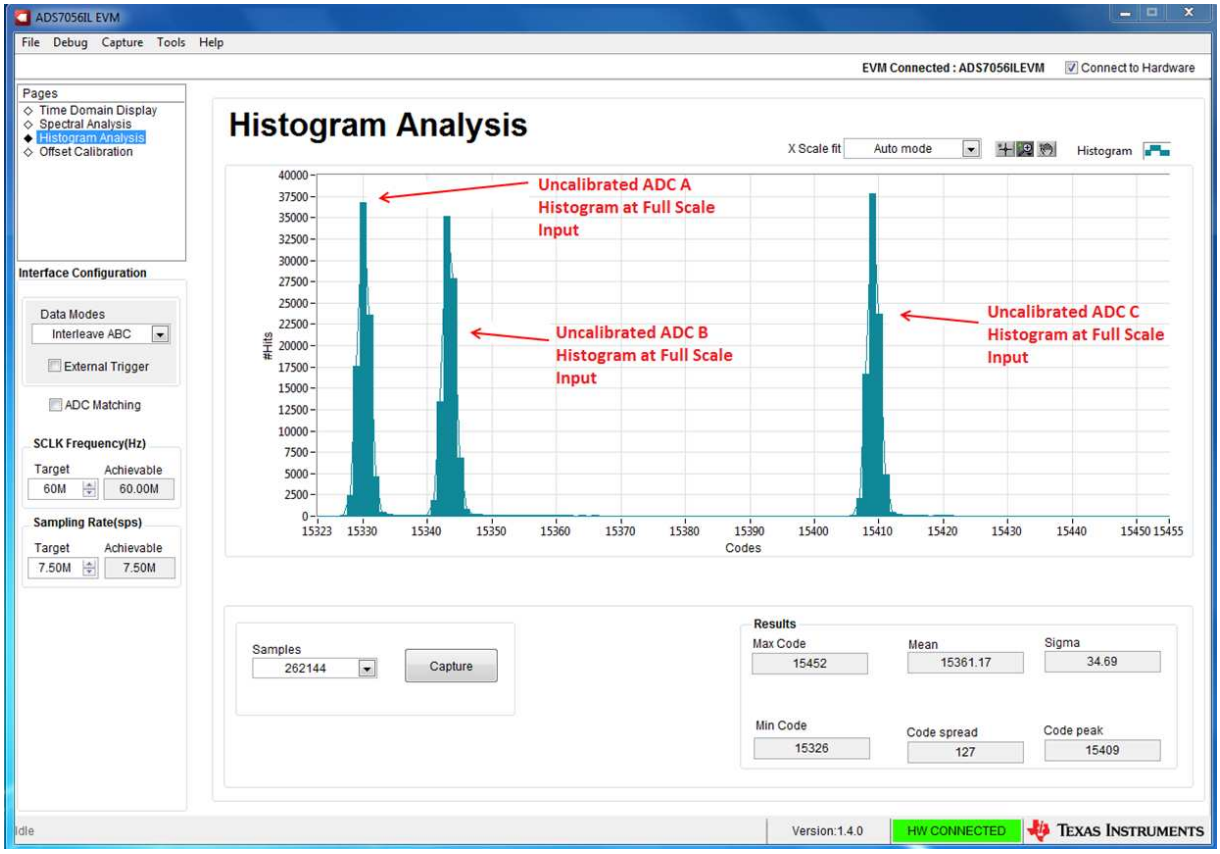

Figure 17. Histogram Plot for Uncalibrated Interleaved ADS7056 System at Full-Scale Input (3.1 V)

6.1.2 DC Histogram at Zero Input and Full-Scale ADC Input for a Calibrated System

The ADS7056 offset calibration feature allows us to calibrate each ADC. During the ADS7056 calibration process, the input sampling switch is opened and the input voltage is compared with the reference voltage (derived from AVDD) to calibrate offset errors. Since all three ADCs in the system are powered from the same reference, the offset mismatch between ADCs after calibration is minimal. This can be seen by plotting a histogram of the calibrated interleaved system. The histograms for the individual ADCs after calibration overlap showing that all the ADCs are matched with respect to offset.

Figure 18 shows the histogram for a calibrated system when the input applied to the interleaved ADC is zero. Figure 19 shows the histogram for a calibrated system when the input applied is close to the full scale (3.1 V).

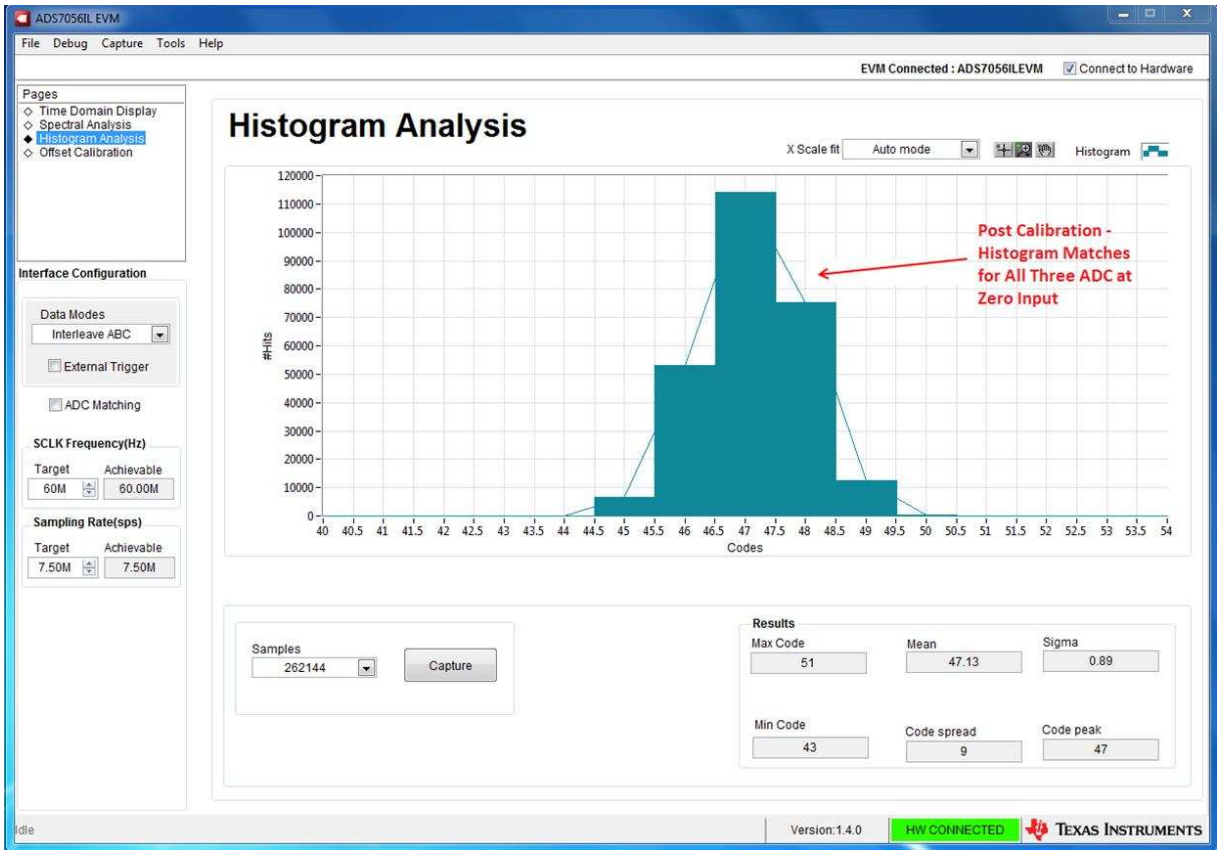

Figure 18. Histogram Plot for Calibrated Interleaved ADS7056 System at Zero Input (0 V)

To see the effect of gain error on code spread of a calibrated ADC system, a histogram is captured by applying an input close to the full-scale voltage of the ADC. Even with the full-scale input, the histogram for the individual ADCs matches and appears as a single histogram (see Figure 19). This indicates that the offset is the dominant error and gain error is not significant.

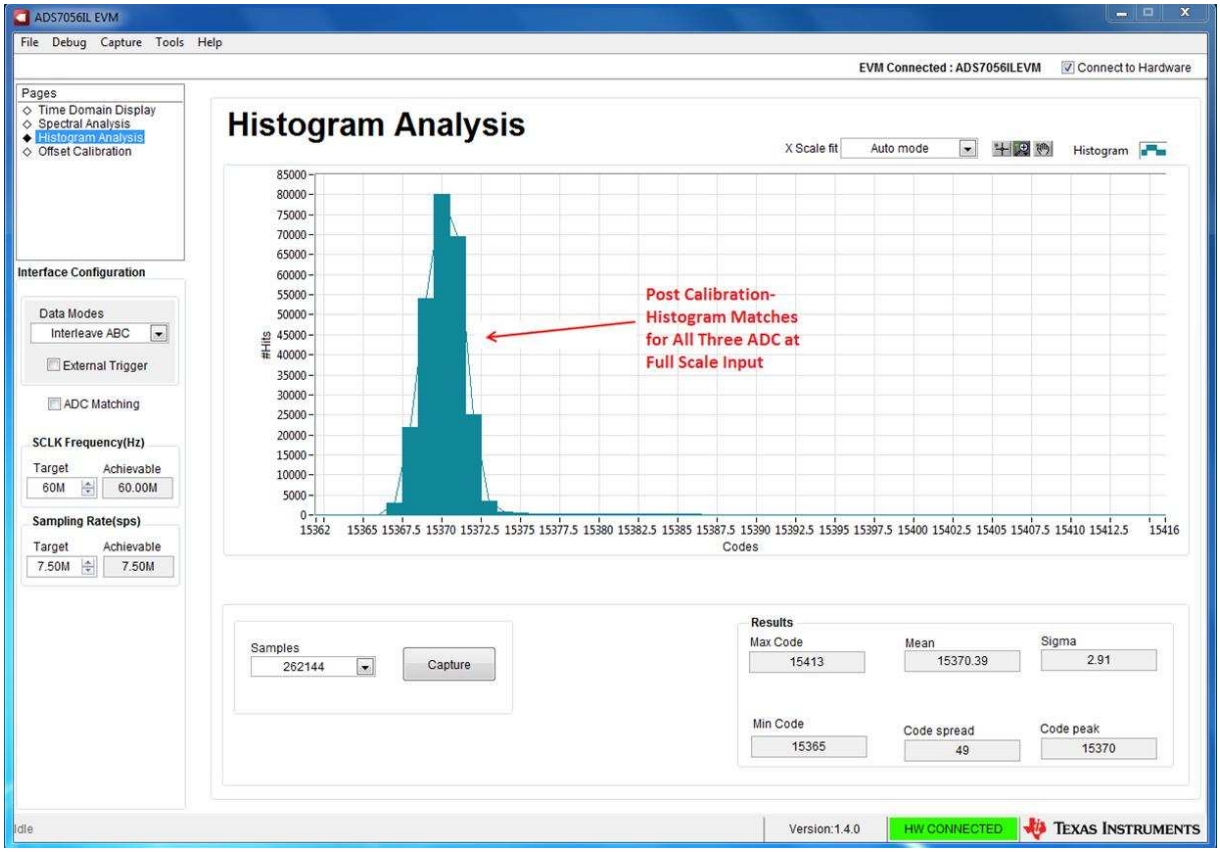

Figure 19. Histogram Plot for Calibrated Interleaved ADS7056 System at Full-Scale Input (3.1 V)

6.2 FFT Analysis

To analyze the impact of offset, gain, and timing mismatches on the system performance of an interleaved ADC, a 2-kHz sine wave input was applied to an interleaved ADC system. An FFT plot is captured to showcase the difference in SNR and THD performance of the calibrated and uncalibrated systems. In the uncalibrated system, the noise peak at the sampling frequency of the individual ADCs due to offset mismatch is dominant and degrades system AC performance (SNR: 43.85 dB).

After calibrating each ADC against its offset, we see the noise peak due to offset mismatch reduced by a significant margin which results in an AC performance improvement of the system (SNR: 73 dB).

Figure 20 shows the FFT plot for a calibrated interleaved ADS7056 system, Figure 21 shows the FFT plot for a calibrated interleaved ADS7056 system.

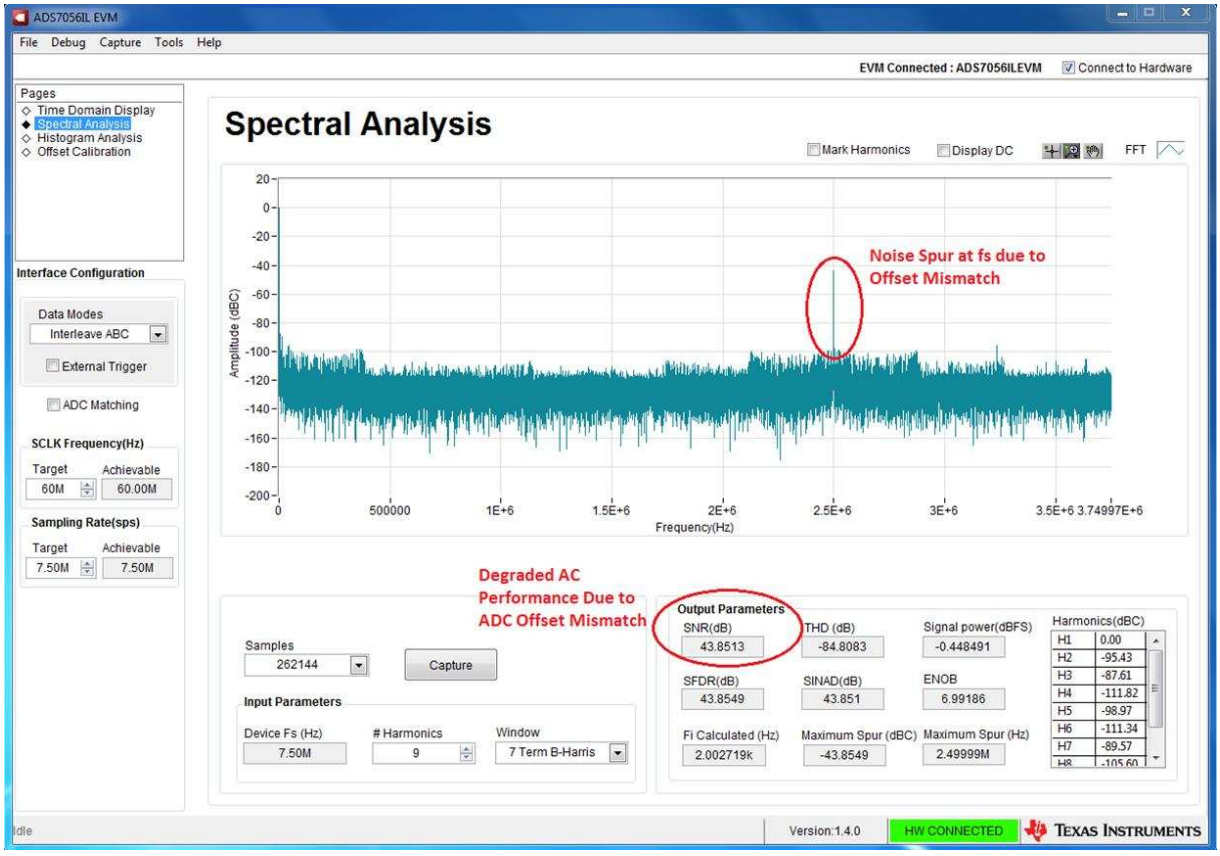

Figure 20. FFT Plot of an Uncalibrated System at –0.5 dBFS Signal Power

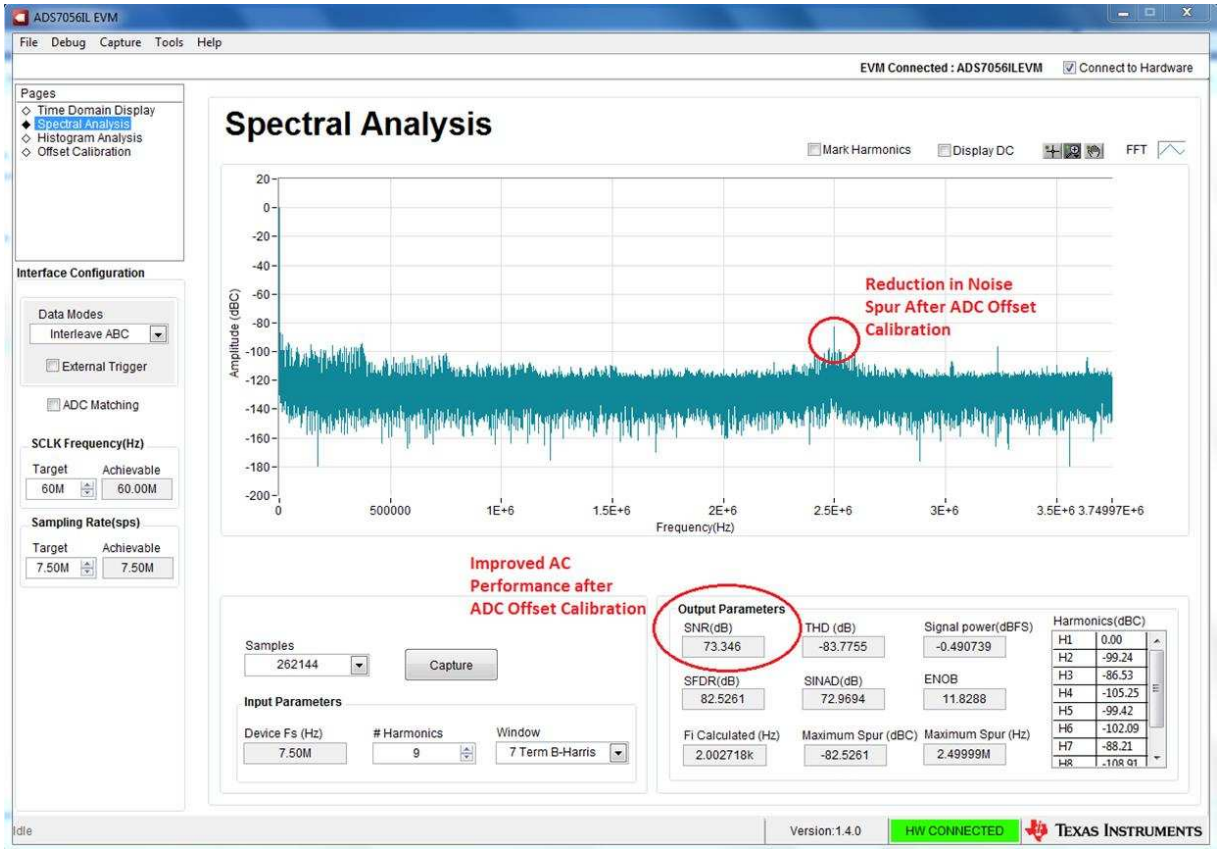

Figure 21. FFT Plot of Calibrated System at –0.5 dBFS Signal Power

7 Design Files

7.1 Schematics

Figure 22 illustrates the three ADS7056 interleaved system schematic.

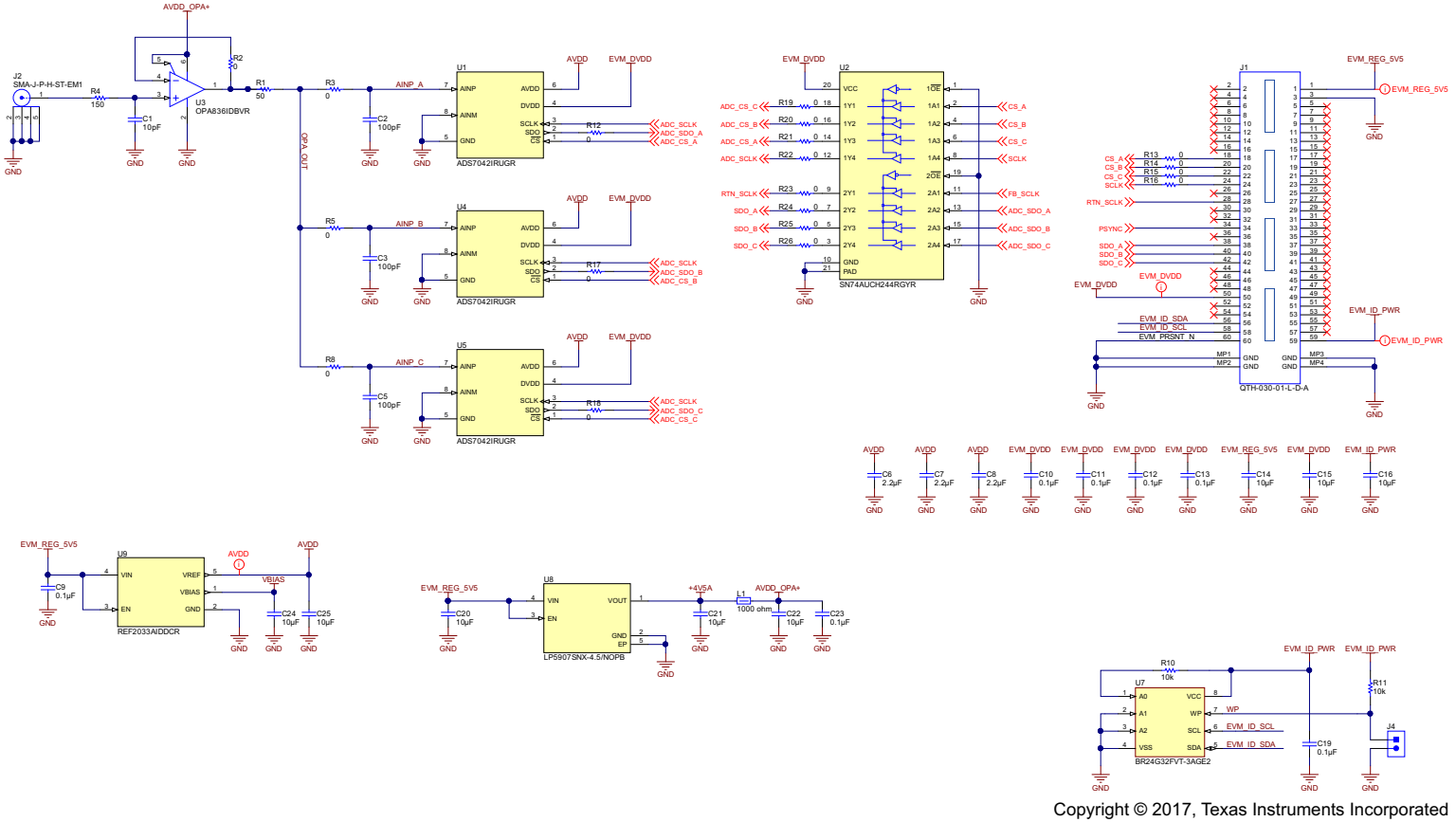

Figure 22. Schematic for Three ADS7056 Interleaved System

7.2 Bill of Materials

Table 2 lists the bill of materials.

Table 2. Bill of Materials for Three ADS7056 Interleaved System (Shown in the Schematic)

Designator	Description	Manufacturer	Part Number	QTY
C1	CAP, CERM, 10 pF, 50 V, ±5%, C0G/NP0, 0402	Murata	GRM1555C1H100JA01D	1
C2, C3, C5	CAP, CERM, 100 pF, 50 V, ±1%, C0G/NP0, 0402	AVX	04025A101FAT2A	3
C6, C7, C8	CAP, CERM, 2.2 µF, 16 V, ±10%, X5R, 0402	TDK	C1005X5R1C225K050BC	3
C9	CAP, CERM, 0.1 µF, 16 V, ±5%, X7R, 0402	Murata	GRM155R71C104JA88D	1
C10, C11, C12, C13, C19, C23	CAP, CERM, 0.1 µF, 16 V, ±10%, X7R, 0402	Wurth Elektronik	885012205037	6
C14, C15, C16, C20, C21, C22, C24, C25	CAP, CERM, 10 µF, 10 V, ±20%, X5R, 0402	Murata	GRM155R61A106ME11	8
H1, H2, H3, H4	MACHINE SCREW PAN PHILLIPS 4-40	B&F Fastener Supply	PMSSS 440 0025 PH	4
H5, H6	ROUND STANDOFF M3 STEEL 5MM	Wurth Elektronik	9774050360R	2
J1	Header(Shrouded), 19.7mil, 30x2, Gold, SMT	Samtec	QTH-030-01-L-D-A	1
J2	SMA Jack, 50 Ohm, Gold, R/A, SMT	Samtec	SMA-J-P-H-ST-EM1	1
J4	Header, 2.54mm, 2x1, Tin, SMT	Samtec	TSM-102-03-T-SV	1
L1	Ferrite Bead, 1000 ohm @ 100 MHz, 0.35 A, 0402	Murata	BLM15AX102SN1D	1
LBL1	Thermal Transfer Printable Labels, 0.650" W x 0.200" H - 10,000 per roll	Brady	THT-14-423-10	1
R1	RES, 50, 1%, 0.125 W, AEC-Q200 Grade 1, 0402	AT Ceramics	504L50R0FTNCFT	1
R2, R3, R5, R8	RES, 0, 5%, 0.063 W, 0402	Vishay-Dale	CRCW04020000Z0ED	4
R4	RES, 150, 5%, 0.063 W, 0402	Vishay-Dale	CRCW0402150RJNED	1
R10, R11	RES, 10 k, 5%, 0.1 W, AEC-Q200 Grade 0, 0402	Panasonic	ERJ-2GEJ103X	2
R12, R13, R14, R15, R16, R17, R18, R19, R20, R21, R22, R23, R24, R25, R26	RES, 0, 5%, 0.05 W, 0201	Panasonic	ERJ-1GE0R00C	15
U1, U4, U5	Ultra-Low Power, Ultra-Small Size, 12-Bit, 1-MSPS, SAR ADC, RUG0008A	Texas Instruments	ADS7042IRUGR	3
U2	Octal Buffer and Driver With 3-State Outputs, RGY0020A	Texas Instruments	SN74AUCH244RGYR	1
U3	Very Low Power, Rail to Rail Out, Negative Rail In, VFB Operational Amplifier, 2.5 to 5.5 V, –40 to 125 degC, 6-pin SOT23 (DBV6), Green (RoHS & no Sb/Br)	Texas Instruments	OPA836IDBVR	1
U7	I2C BUS EEPROM (2-Wire), TSSOP-B8	Rohm	BR24G32FVT-3AGE2	1
U8	Ultra Low-Noise, 250-mA Linear Regulator for RF and Analog Circuits, DQN0004A	Texas Instruments	LP5907SNX-4.5/NOPB	1
U9	Low-Drift, Low-Power, Dual-Output, VREF and VREF / 2 Voltage References, DDC0005A	Texas Instruments	REF2033AIDDCR	1

8 References

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2. Christian Vogel “The Impact of Combined Channel Mismatch Effects in Time-Interleaved ADCs” IEEE TRANSACTIONS ON INSTRUMENTATION AND MEASUREMENT, VOL. 54, NO. 1, FEBRUARY 2005.
3. Behzad Razavi “Design Considerations for Interleaved ADCs”, IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. 48, NO. 8, AUGUST 2013.
4. Properties of the IEEE-STD-1057 Four-Parameter Sine Wave Fit Algorithm, IEEE TRANSACTIONS ON INSTRUMENTATION AND MEASUREMENT, VOL. 49, NO. 6, DECEMBER 2000.

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