Application Report
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# Implementing JESD204B SYSREF and Achieving Deterministic Latency With ADC32RF45

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**ABSTRACT**

SYSREF is a critical signal for data converters with a JESD204B interface and a deep understanding of it is imperative for application engineers. This application note provides details for deriving SYSREF frequency for a given mode of the device, SYSREF timing to achieve deterministic latency across converters, and the AC characteristics of this signal to choose the appropriate SYSREF driver for an industry-first 3-Gsps, RF-sampling ADC – ADC32RF45.

**Contents**



**List of Figures**



**List of Tables**

# 1 Introduction

## 1.1 Using SYSREF in ADC32RF45

The SYSREF signal is typically a periodic signal which is sampled by the ADC32RF45 device clock, and is used to align the boundary of the local multi-frame clock inside the data converter for subclass 1 operation to achieve deterministic latency across converters. The device also uses the same signal to reset critical blocks such as the clock divider for the interleaved ADCs, NCOs, decimation filters, and so on. The ADC32RF45 needs SYSREF to put the device into the right state even before loading the device configuration. The same device also offers subclass 0 operation for applications that do not require deterministic latency by replacing the SYSREF signal with SPI based trigger via SPI writes.

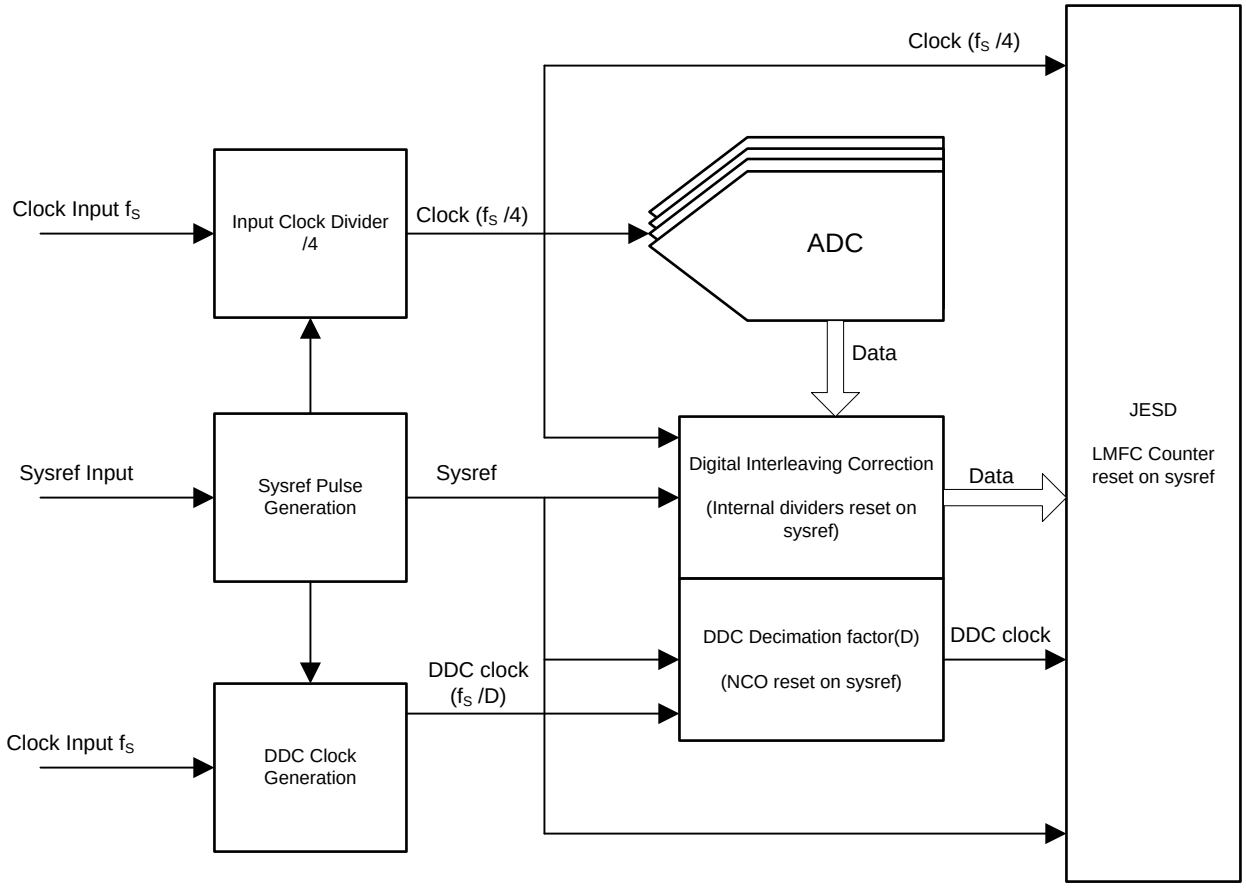


**Figure 1. Sysref Distribution in ADC32RF45, Shown for a Single Channel**

SYSREF is used to synchronize all dividers in the device. In the DDC bypass mode, SYSREF is used for resetting the input clock $f_S$ / 4 divider that is used to clock the four ADC cores, interleaving correction clock dividers, and the JESD local multi-frame clock (LMFC) generation. In the DDC mode, SYSREF is also used to reset the DDC clock generation module and to reset the NCOs of the DDC. It is important to gate the SYSREF externally or internally to the device in the DDC mode after the JESD link is established as the NCO phase is reset on SYSREF.

## 2 Calculating SYSREF Frequency

The ADC32RF45 has two main modes of operation; the first is wide-band RF sampling bypassing the internal DDC and the second is decimation mode to extract only the required bandwidth of the incoming RF signal.

1. **SYSREF frequency for 3 GHz RF sampling (DDC bypass mode):**

   The ADC32RF45 has a unique way of packing 12-bit samples onto the JESD lanes using bit packing to improve the efficiency over the lanes. The JESD block takes in 20 samples of 12 bits. On each lane it combines 5 consecutive 12-bit samples and appends four 0s to make 64 bit which is encoded to 80 bits by the 8b-10b encoder. The 80 bits are sent over each lane and, in effect, 20 samples over 4 lanes per channel as shown in Table 1.

**Table 1. Data Packing of Lanes for LMFS = 82820 Mode**

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| DA0 | A0 [11:4] | A0[3:0] A1[11:8] | A1 [7:0] | A2 [11:4] | A2[3:0] A3[11:8] | A3 [7:0] | A4 [11:4] | A4[3:0] 0000 |
| DA1 | A5 [11:4] | A5[3:0] A6[11:8] | A6 [7:0] | A7 [11:4] | A7[3:0] A8[11:8] | A8 [7:0] | A9 [11:4] | A9[3:0] 0000 |
| DA2 | A10 [11:4] | A10[3:0] A11[11:8] | A11 [7:0] | A12 [11:4] | A12[3:0] A13[11:8] | A13 [7:0] | A14 [11:4] | A14[3:0] 0000 |
| DA3 | A15 [11:4] | A15[3:0] A16[11:8] | A16 [7:0] | A17 [11:4] | A17[3:0] A18[11:8] | A18 [7:0] | A19 [11:4] | A19[3:0] 0000 |
| DB0 | B0 [11:4] | B0[3:0] B1[11:8] | B1 [7:0] | B2 [11:4] | B2[3:0] B3[11:8] | B3 [7:0] | B4 [11:4] | B4[3:0] 0000 |
| DB1 | B5 [11:4] | B5[3:0] B6[11:8] | B6 [7:0] | B7 [11:4] | B7[3:0] B8[11:8] | B8 [7:0] | B9 [11:4] | B9[3:0] 0000 |
| DB2 | B10 [11:4] | B10[3:0] B11[11:8] | B11 [7:0] | B12 [11:4] | B12[3:0] B13[11:8] | B13 [7:0] | B14 [11:4] | B14[3:0] 0000 |
| DB3 | B15 [11:4] | B15[3:0] B16[11:8] | B16 [7:0] | B17 [11:4] | B17[3:0] B18[11:8] | B18 [7:0] | B19 [11:4] | B19[3:0] 0000 |

The high-speed JESD link between transmitter and receiver is configured by specifying the following parameters:

LMFS = 82820 with K = 16:

- L is the number of lanes per device
- M is the number of converters per device
- F is the number of octets per lane per frame clock
- K is the number of frames per multi-frame clock.

The actual SYSREF frequency is determined by the following 2 constraints:

- SYSREF must be a sub-multiple of the local multiple frame clock.
  - Sampling clock, $f_S$ = 3000 MHz
  - JESD frame clock = $f_C = f_S / S$ = 3000 / 20 = 150 MHz as S = 20
  - Lane rate = $f_C \times f \times 10$ = 150 × 8 × 10 = 12 Gbps
  - LMFC (Local multi-frame clock) = LMFC = FC / K = $f_S$ / (K × S)= 15 MHz / 16 = 9.375 MHz
  - Maximum SYSREF frequency = LMFC
- SYSREF also needs sub-multiple of $f_S$ / 64 from ADC digital block design.
  - Maximum SYSREF = $f_S$ / 64

Combining the two constraints yields, Maximum SYSREF to be = $f_S$ / LCM(64,20 × K)

Where LCM is least common multiple

Generalized expression, SYSREF = $f_S$ / LCM(64,20 × K) / N where N is a integer (1,2…)

For the previous example, SYSREF = 3000 / LCM(64,20 × 16) / N
= 3000 / 320 / N = 9.375 / 4 (choosing N = 4)
= 2.34375 MHz

2. **SYSREF frequency for DDC mode:**

ADC32RF45 also supports the feature-rich DDC block. Section 3 shows how to derive the SYSREF for one of the DDC modes.

$f_S$ = 3000 MHz

DDC factor (D) = 8

DDC output rate = $f_S$ / D = 3000 / 8 = 375 MHz

LMFS for dual-band DDC per channel = 8821. Each I and Q of the complex output is treated as one converter.

| | | LMFS = 8821 | | | |
|---|---|---|---|---|---|
| Channel A first band, Complex I/Q output | DA0 | $A1I_0$[15:8] | $A1I_0$[7:0] | $A1I_1$[15:8] | $A1I_1$[7:0] |
| | DA1 | $A1Q_0$[15:8] | $A1Q_0$[7:0] | $A1Q_1$[15:8] | $A1Q_1$[7:0] |
| Channel A second band, Complex I/Q output | DA2 | $A2I_0$[15:8] | $A2I_0$[7:0] | $A2I_1$[15:8] | $A2I_1$[7:0] |
| | DA3 | $A2Q_0$[15:8] | $A2Q_0$[7:0] | $A2Q_1$[15:8] | $A2Q_1$[7:0] |
| Channel B first band, Complex I/Q output | DB0 | $B1I_0$[15:8] | $B1I_0$[7:0] | $B1I_1$[15:8] | $B1I_1$[7:0] |
| | DB1 | $B1Q_0$[15:8] | $B1Q_0$[7:0] | $B1Q_1$[15:8] | $B1Q_1$[7:0] |
| Channel B second band, Complex I/Q output | DB2 | $B2I_0$[15:8] | $B2I_0$[7:0] | $B2I_1$[15:8] | $B2I_1$[7:0] |
| | DB3 | $B2Q_0$[15:8] | $B2Q_0$[7:0] | $B2Q_1$[15:8] | $B2Q_1$[7:0] |

**Figure 2. Data Packing of Lanes for LMFS = 8821 Mode**

The actual SYSREF frequency is determined by the following 2 constraints for DDC 8 × mode, LMFS =8821:

- SYSREF needs to be s sub-multiple of local multiple frame clock.
  - Sampling clock, $f_S$ = 3000 MHz
  - Decimated output rate = $f_S$ / D where D is the decimation factor
  - JESD frame clock= FC = $f_S$ / D / S = 3000 / 8 / 1 = 375 MHz
  - Lane rate = FC × F × 10 = 375 × 2 × 10 = 7.5 Gbps
  - LMFC (local multi-frame clock) = LMFC = FC / K = $f_S$ / (D × K × S)=375 MHz / 16 = 23.4375 MHz.
  - Maximum SYSREF frequency = LMFC
- SYSREF also needs sub-multiple of $f_S$ / 64 from ADC digital block design.
  - Maximum SYSREF = $f_S$ / 64

Combining the two constraints yields, Maximum SYSREF to be = $f_S$ / LCM(64,20 × K)

Generalized expression, SYSREF = $f_S$ / LCM(64,D×K×S) / N where N is a integer (1,2…)

For the previous example, SYSREF = 3000 / LCM(64,8 × 16 × 1) / N
= 3000 / 128 / N
= 23.4375 / 16 (choosing N = 16)
= 1.46484375 MHz

**Summarizing the SYSREF frequency calculation:**

**Table 2. SYSREF Frequency for Different ADC32RF45 Modes**

| Operating Mode | LMFS Setting | LMFC Clock or Max SYSREF Frequency |
|---|---|---|
| Bypass | 82820 | $f_S$ / LCM(64, 20 × K), S=20 |
| Bypass | 8224 | $f_S$ / LCM(64, 4 × K), S=4 |
| Bypass | 4211 | $f_S$ / LCM(64, 1 × K), S =1 |
| Decimation | Various | $f_S$ / LCM(64,D × K × S) |

**Allowable values of SYSREF frequency = LMFC clock / N where N is a integer (N = 1,2…)**

Typically, it is always desirable to keep SYSREF frequency < 5 MHz (choose N accordingly) to avoid SYSREF coupling both on board and device to clock and RF input signal and highly recommended to switch off SYSREF to device once the JESD link is established.

## 3 Driving SYSREF of ADC32RF45

The ADC32RF45 SYSREF receiver has 100-Ω differential internal termination with no self-bias. SYSREF always must be DC coupled with a common mode of 1.2 V. A standard LVDS driver from the LMK04828 clock chip can be used as SYSREF, as shown in Figure 3.

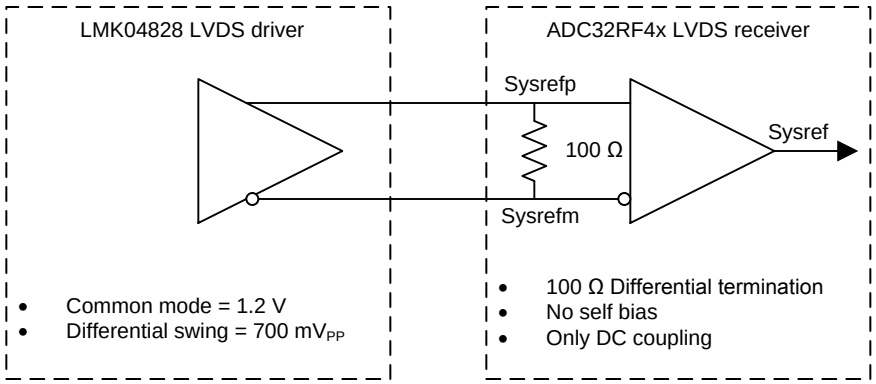


**Figure 3. SYSREF Driving Circuit**

## 4 SYSREF Timing and Deterministic Latency

The ADC32RF45 samples the incoming SYSREF on the rising edge of the device clock. Figure 4 shows the setup and hold time with regard to device clock at 3 GHz. The actual setup and hold numbers are yet to be finalized from device characterization. The simulation numbers and **not** Silicon data are presented in Figure 4.

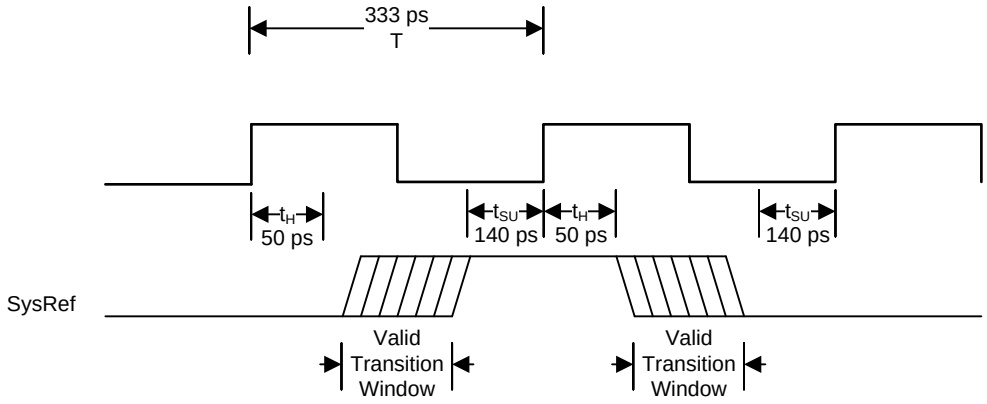


**Figure 4. SYSREF Timing With Regard to Rising Edge of Device Clock at 3 GHz $T_{SU}$ = 140 ps and $T_H$ =50 ps**

**NOTE:** The numbers are from design simulations across process, voltage and temperature. Characterization is ongoing The system must meet the SYSREF timing to achieve deterministic latency from power up to power up and across devices. The device also offers SYSREF internal delay programmability for any skew adjustment between SYSREF and device clock introduced on the board.

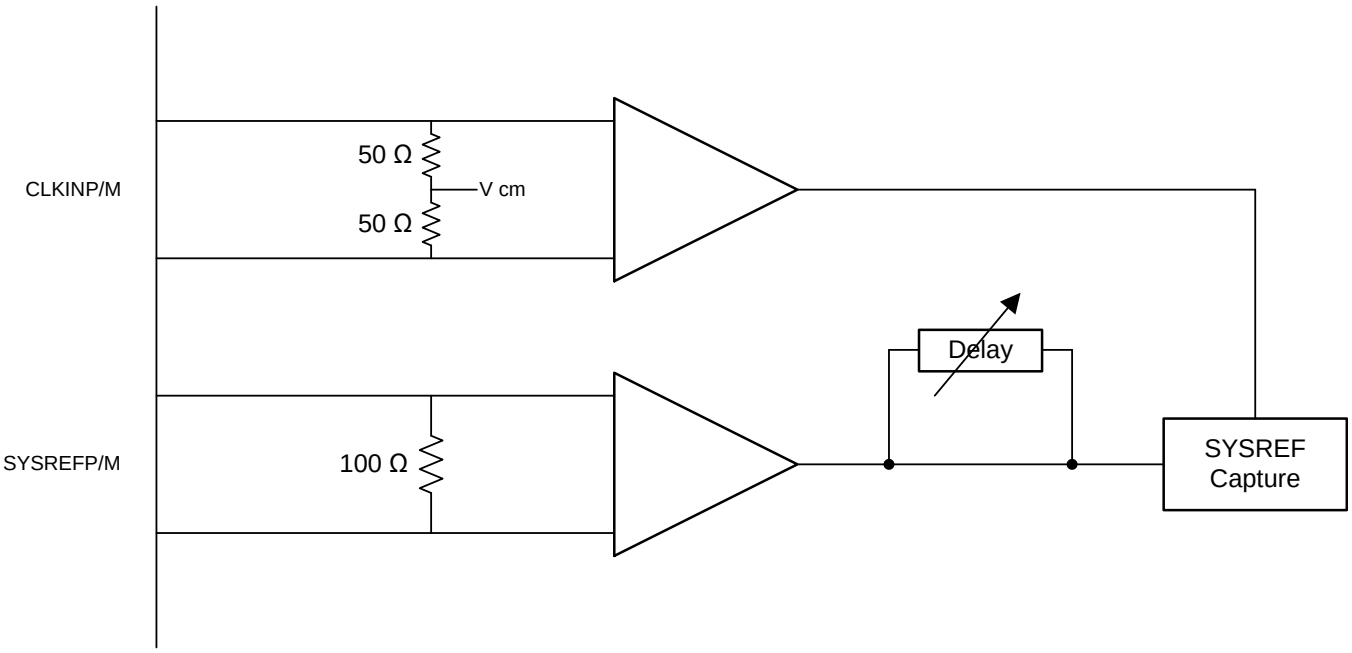


**Figure 5. SYSREF Internal Programmable Delay**

## 5 Can the Device Operate Without SYSREF (Subclass 0 Operation)?

The ADC32RF45 requires SYSREF to be established even before programming the device as it resets the clock dividers and is needed to get a stable clock. The device offers JESD SUBCLASS 0 operation where the external SYSREF can be replaced with a trigger based on SPI.

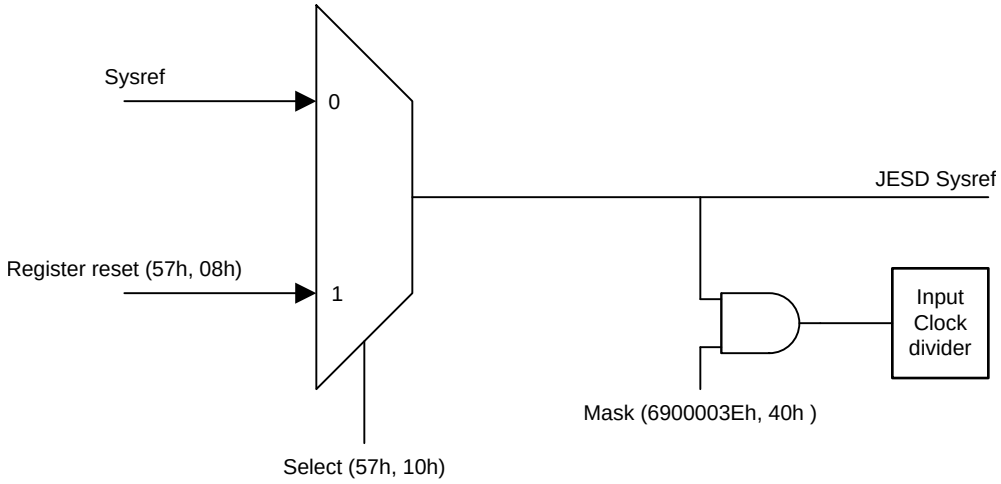


**Figure 6. SYSREF Duplication via SPI Writes**

The following sequence can be used to operate the device in subclass 0 without using external SYSREF. For details on specifics of SPI programming, please refer to datasheet.

1. Select manual SYSREF and pulse SYSREF ro reset the input clock divider (address, data).
   - 12h,04h (Select Master page)
   - 57h, 10h
   - 57h, 18h
   - 57h, 10h
2. Program the device. Source all the needed.defaults
3. Mask the SYSREF to input clock divider.
   - 4001h, 00h
   - 4002h, 00h
   - 4003h, 00h
   - 4004h, 69h
   - 603Eh, 40h
4. Repeat Step 1, to reset JESD. Provide a reset to the LMFC counter.

## 6 Conclusion

It is imperative for engineers to have a thorough understanding of SYSREF signals for a converter with JESD interface to bring up the device. This application note explains in detail the SYSREF parameters needed to successfully design-in ADC32RF45 in a system

## 7 Reference

1. *ADC32RF45 Dual-Channel, 14-Bit, 3.0-GSPS, Analog-to-Digital Converter* (SBAS747)
2. *ADC32RF45 EVM User Guide* (SLAU620)

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