

Using the Sequencer and Pseudo-Differential Features of the ADS8363

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ABSTRACT

This application report presents an introduction to the sequencer found in the ADS8363, a dual, 16-bit 2x2 or 4x2 channel simultaneous sampling analog-to-digital converter. The ADS8363 has pin-compatible 14-bit and 12-bit versions, which are the ADS7263 and ADS7223, respectively. This application report explains how to use the sequencer found in these devices as well as how to setup and operate the pseudo-differential mode of operation.

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1 Introduction

The ADS8363 is configurable as a 2x2 channel (with four fully differential inputs) or 4x2 channel (with eight pseudo-differential inputs), simultaneously sampled 16-bit analog-to-digital converter (ADC) capable of sampling at rates up to 1 MSPS. The inputs are grouped in two pairs A and B, with two independent sample and hold circuits followed by two independent successive approximation register (SAR) ADC channels. The conversion results are then presented through two serial data output lines for operation at full speed. For applications using one serial bus, the ADS8363 can be configured to use a single serial output for both A and B channel conversion results. To ease the identification of conversion data when operated in fully differential mode, channel ID bits are inserted into the conversion results ahead of the most significant bit (MSB) output data.

Control of the serial outputs and sampling scheme are accomplished by using dedicated MODE pins M0 and M1. [Table 1](#) shows the pin state with the resultant channel selection method and serial output or outputs used.

Table 1. Channel Selection

Mode	M0 Pin	M1 Pin	Channel Selection	SDOx Used
I	0	0	Manual (via serial data input commands)	SDOA and SDOB
II	0	1	Manual (via serial data input commands)	SDOA only
III	1	0	Automatic sequencing	SDOA and SDOB
IV	1	1	Automatic sequencing	SDOA Only

Control of the ADS8363 is based on a series of five user programmable registers: CONFIG, REFDAC1, REFDAC2, SEQFIFO, and REFCM. This application report focuses on the CONFIG and SEQFIFO registers, which control the channel selection process.

2 Fully Differential Versus Pseudo-Differential Operation

In fully-differential mode (device default at power-up, PDE bit = 0), the input channel selection is controlled by bit, C1, the MSB in the CONFIG register. When C1 = 0, differential pair 0 is selected and the A/B multiplexors switch to CHA0P/CHA0N and CHB0P/CHB0N. When C1 = 1, the multiplexors switch to CHA1P/CHA1N and CHB1P/CHB1N. In differential mode, bit C0 is don't care.

For manual channel selection in either fully-differential mode or pseudo-differential mode, the only bits that need to change under normal operation are bits C1 and C0. This would be the equivalent of transmitting 0x0000 or 0x8000 to the SDI in fully-differential mode. In pseudo-differential mode, transmitting 0x0000, 0x4000, 0x8000, or 0xC000 (changing only the MSBs) allows the user to cycle through all of the input channels.

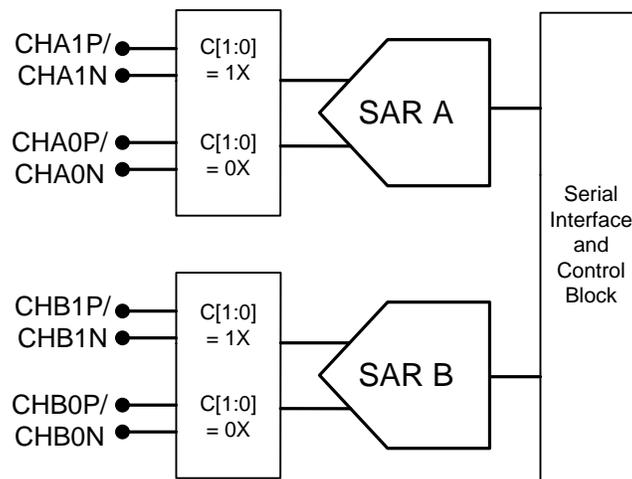


Figure 1. Fully-Differential MUX Configuration

In pseudo-differential mode (PDE bit is set to 1), input channel selection is controlled by bits C1 and C0, the two MSBs in the CONFIG register. Channel selection follows a standard binary count from 00 to 11. When $C[1:0] = 00$, the CHA0 and CHB0 inputs are selected and sampled against the common mode or reference inputs depending on the configuration of the REFCM register. When $C[1:0] = 01$, the multiplexors switch to CHA1 and CHB1. Channels A2 and B2 are switched in when $C[1:0] = 10$ and channels A3/B3 are switched in when $C[1:0] = 11$.

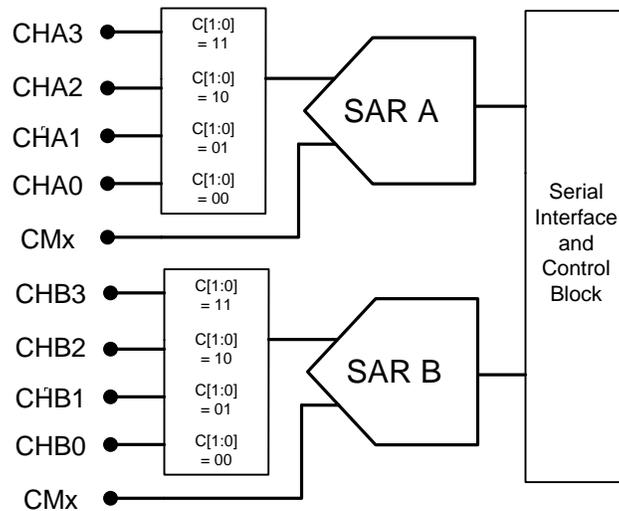


Figure 2. Pseudo-Differential MUX Configuration

To enter pseudo-differential mode, bits $R[1:0]$ must be set to 01 in order to set PDE (bit 6) in the CONFIG register. Setting bits $R[1:0] = 01$ also allows the user to access the additional registers found in the ADS8363 depending on the state of bits $A[3:0]$. Note that after the pseudo-differential mode is entered, the ADS8363 will stay in this configuration until a software reset is issued or a power cycle occurs. If bits $R[1:0] = 00$ or 11, the remaining SDI stream is ignored and no configuration changes take place.

For the examples presented in the following sections, the ADS8363 was configured such that CHA0 was tied to GROUND with CHB3 connected to the 5-V supply. Series resistors were then connected between CHA0 to CHA1, CHA1 to CHA2, and so forth.

3 Example Manual Channel Selection in Mode 1 (M0 = 0, M1 = 0)

Manual channel selection is controlled by the logic level present at the M0 pin and the applied serial data input (SDI) to the CONFIG register bits C[1:0]. When M0 = 0, the two MSBs applied to the SDI pin determine which channel will be selected at the input multiplexor for the next conversion cycle.

The following sequence of instructions sent to the ADS8363 will allow manual channel selection in pseudo-differential mode of operation:

- (A) Write to the reference buffer registers to turn them ON (default is OFF) – send 0x1042 to the SDI pin. This command enables the configuration register update control, sets the PDE bit and sets up the REFDAC1 register to accept data in the next command cycle.
- (B) Write to the REFDAC1 control register – send 0x03FF to the SDI pin. This command clears the DAC1 power-down bit and sets the DAC1 value at its maximum level of 2.5 V.
- (C) Enable writing to the REFDAC2 register – send 0x1045 to the SDI pin. This repeats the configuration register data and enables access to the REFDAC2 register.
- (D) Write to the REFDAC2 control register – send 0x03FF to the SDI pin. This command clears the DAC2 power-down bit and sets the DAC2 value at its maximum level of 2.5 V.
- (E) Write sequentially 0x0000, 0x4000, 0x8000, and 0xC000 to convert channels CHX_0 through CHX_3 while reading the conversion results on SDOA and SDOB.

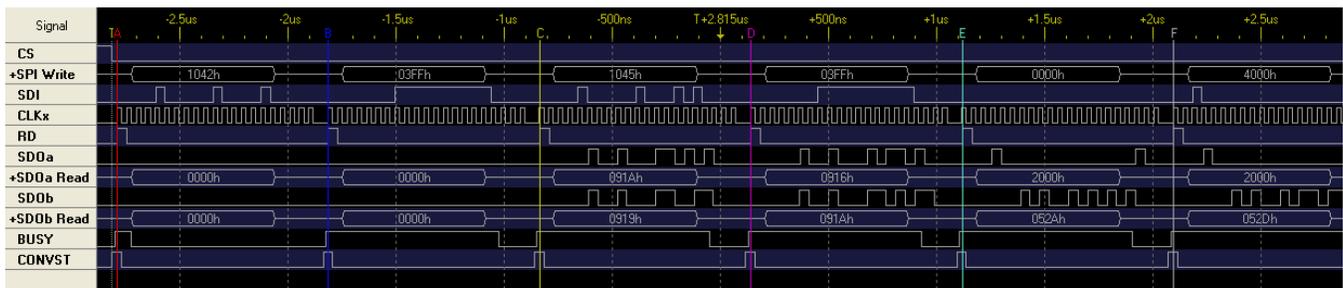


Figure 3. Configuration Sequence

Figure 3 depicts the configuration sequence. Figure 4 is captured from step E, where the first CH0 command is sent to the ADS8363.

The red arrows (in Figure 4) show the relationship of the channel selection commands to the output serial data. During the first command cycle, CHA0 and CHB0 are multiplexed into the sample and hold capacitors. The ADS8363 acquires these input signals beginning with the falling edge of BUSY that began at cursor A. The CONVST applied at cursor B begins the conversion process while the 0x4000 command is being sent to the SDI. The first conversion results are then applied to the SDO pin beginning with the CONVST located at cursor C.

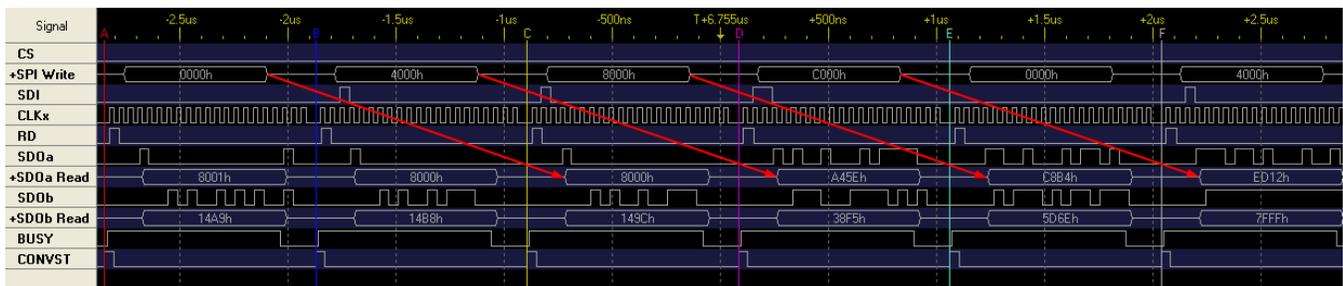


Figure 4. Channel Selection and Conversion Results

4 Automatic Channel Sequencing

Auto channel sequencing is also controlled by the state of the logic level applied to the M0 pin. When M0 = 1, access to the various sequencing options is available through the SEQFIFO register. To enter the SEQFIFO register, the data transmitted to the SDI input must allow access to the CONFIG register by setting R[1:0] = 01 and enable writing of the SEQFIFO register by setting A[3:0] to 1001.

The SEQFIFO register allows the ADS8363 user to influence the:

- Behavior of the CONVST input pin and BUSY output pin
- Length of a conversion sequence
- Number and order of channels to be converted
- Depth of the FIFO in burst read mode if the FE bit is set in the CONFIG register

SEQFIFO bits [15:14] are the sequencer mode selection bits S[1:0]. When S[1:0] = 0x, the CONVST input must toggle with each channel to be converted. The BUSY output will toggle with each conversion defined in the sequence. When S[1:0] = 10, a single CONVST will initialize the conversion process for all channels defined in the sequence with an individual BUSY output for each conversion that takes place. Finally, when S[1:0] = 11, a single CONVST input will trigger the conversion of each channel in the sequence with one BUSY output pulse that stays high through the conversion of all channels defined in the sequence.

Figure 5 shows the behavior of the CONVST input and BUSY output based on the setting of S[1:0].

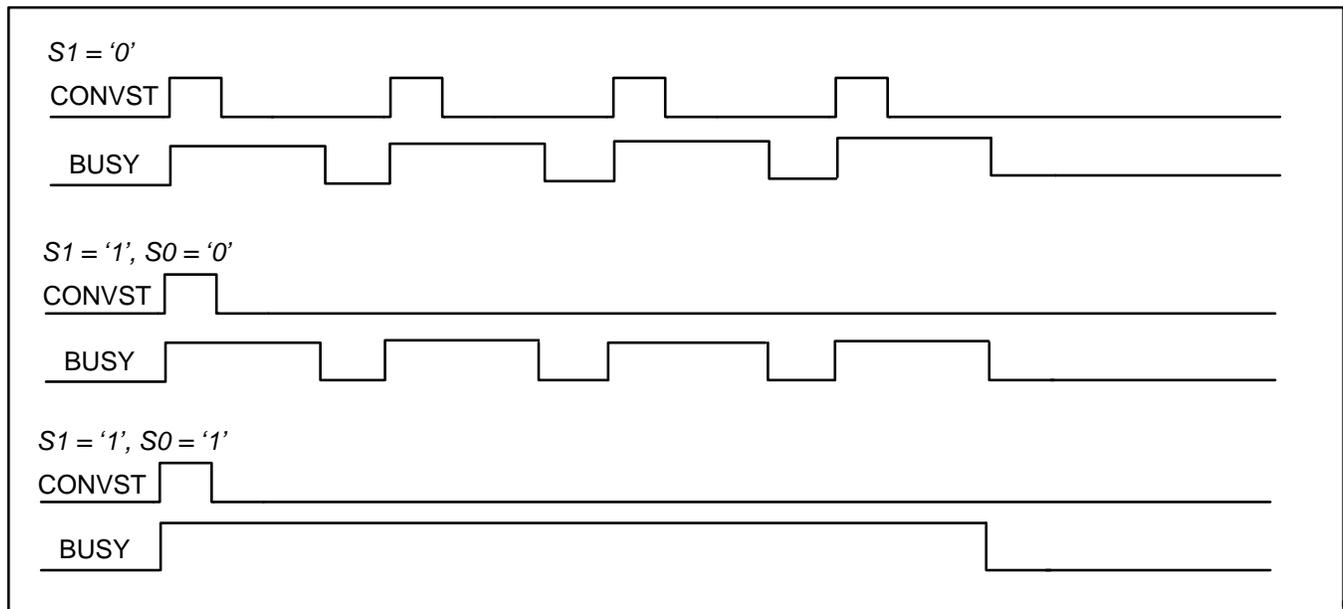


Figure 5. Sequencer Modes

5 Example Auto Channel Sequencing in Mode 3 (M0 = 1, M1 = 0)

The following sequence of instructions sent to the ADS8363 allows automatic channel sequencing in pseudo-differential mode of operation (see [Figure 6](#)):

- (A) Write to the reference buffer registers to turn them ON (default is OFF) – send 0x1042 to the SDI pin. This command enables the configuration register update control, sets the PDE bit, and sets up the REFDAC1 register to accept data in the next command cycle.
- (B) Write to the REFDAC1 control register – send 0x03FF to the SDI pin. This command clears the DAC1 power-down bit and sets the DAC1 value at its maximum level of 2.5 V.
- (C) Enable writing to the REFDAC2 register – send 0x1045 to the SDI pin. This repeats the configuration register data and enables access to the REFDAC2 register.
- (D) Write to the REFDAC2 control register – send 0x03FF to the SDI pin. This command clears the DAC2 power-down bit and sets the DAC2 value at its maximum level of 2.5 V.
- (E) Write to the CONFIG register and enable access to the SEQFIFO register – send 0x1049 to the SDI pin. This command retains the configuration data and sets up the SEQFIFO register to accept data in the next command cycle.
- (F) Write to the SEQFIFO control register – send 0xB1B0 to the SDI pin. This command allows a single CONVST input to be applied to convert the entire sequence. It also provides a BUSY output for each conversion in the sequence. The sequence length is set to four and the channel conversion order is set to CHA0/B0, CHA1/B1, CHA2/B2, and finally CHA3/B3.

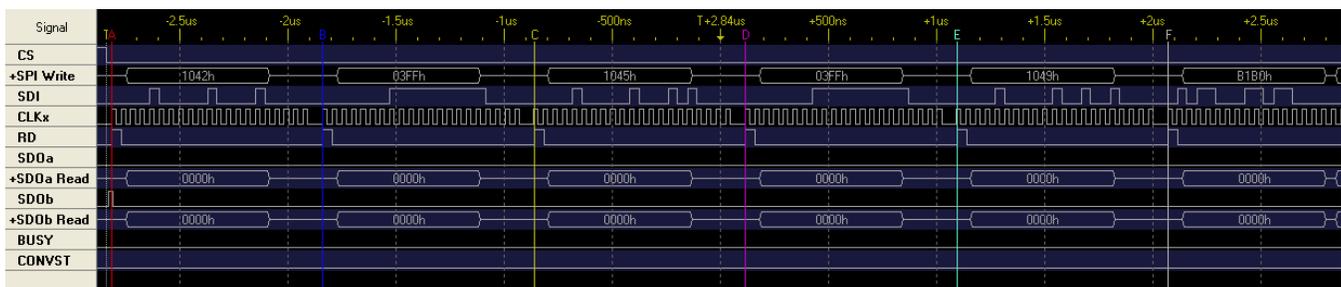


Figure 6. Auto Sequencing Mode 3 Setup

[Figure 7](#) shows the conversion read process. For each conversion cycle, the BUSY pin toggles low when the process is complete. The RD input is applied and the serial data is output through SDOA and SDOB starting from CH0 and progressing through CH3. As seen in [Figure 7](#), if RD is applied without pulsing the CONVST again, the last conversion results are repeated on the outputs.

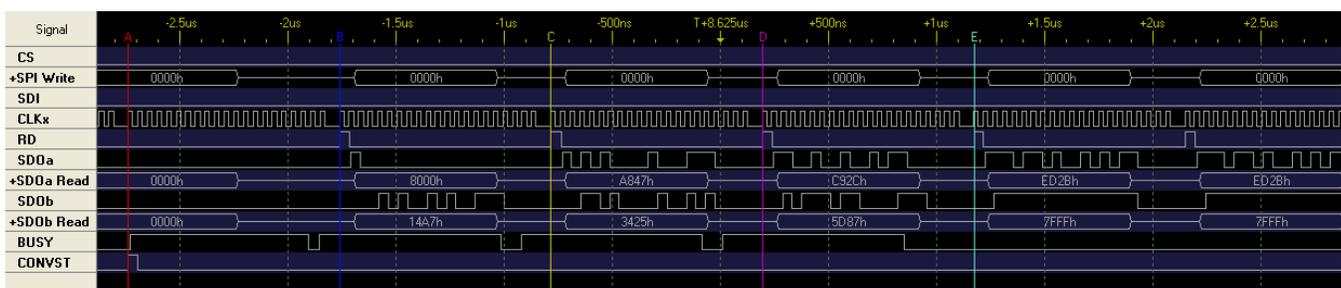


Figure 7. Reading Data in Auto Sequence Mode 3

6 Example Auto Channel Sequencing in Mode 3 (M0 = 1, M1 = 0) Using the FIFO

The following sequence of instructions sent to the ADS8363 will allow automatic channel sequencing in pseudo-differential mode of operation:

- (A) Write to the reference buffer registers to turn them ON (default is OFF) – send 0x1342 to the SDI pin. This command enables the configuration register update control, sets the PDE bit, the FIFO enable bit, the SR bit, and sets up the REFDAC1 register to accept data in the next command cycle.
- (B) Write to the REFDAC1 control register – send 0x03FF to the SDI pin. This command clears the DAC1 power-down bit and sets the DAC1 value at its maximum level of 2.5 V.
- (C) Enable writing to the REFDAC2 register – send 0x1345 to the SDI pin. This repeats the configuration register data and enables access to the REFDAC2 register.
- (D) Write to the REFDAC2 control register – send 0x03FF to the SDI pin. This command clears the DAC2 power-down bit and sets the DAC2 value at its maximum level of 2.5 V.
- (E) Write to the CONFIG register and enable access to the SEQFIFO register – send 0x1349 to the SDI pin. This command retains the configuration data and sets up the SEQFIFO register to accept data in the next command cycle.
- (F) Write to the SEQFIFO control register – send 0xF1B0 to the SDI pin. This command allows a single CONVST input and single BUSY output for the entire sequence. The sequence length is set to four and the channel conversion order is set to CHA0/B0, CHA1/B1, CHA2/B2, and finally CHA3/B3.

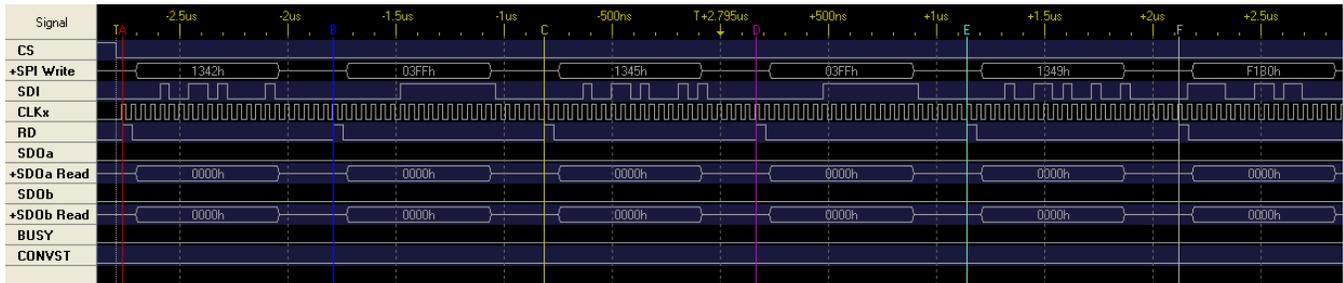


Figure 8. Auto Sequence With FIFO Initialization

Figure 8 shows the configuration sequence. After the configuration is complete, a single CONVST is applied to the ADS8363, which initiates the conversion of all eight pseudo-differential inputs as depicted in Figure 9.

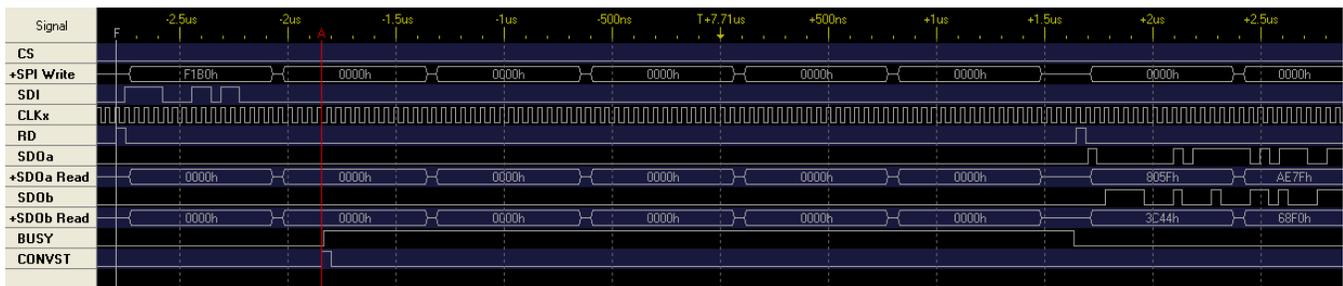


Figure 9. Starting a Conversion Sequence using FIFO

After BUSY returns low, the conversion results from channels A0 through B3 are presented to the SDOA and SDOB outputs.

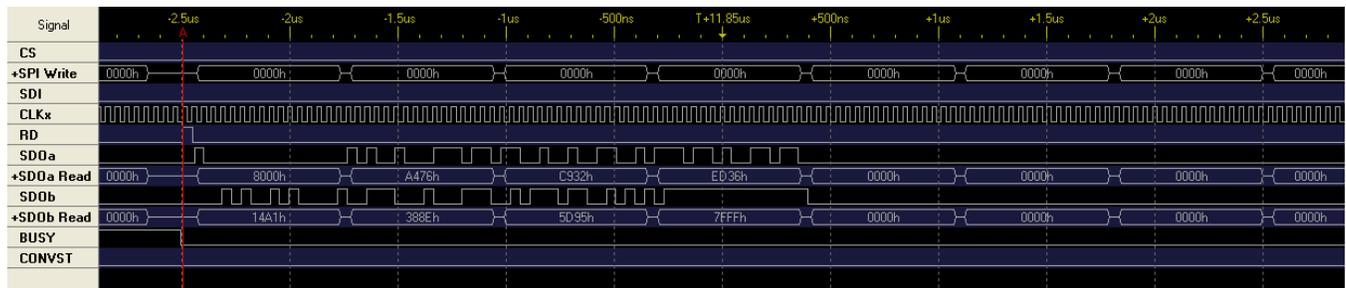


Figure 10. Reading Data from the FIFO

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