Application Report
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Combined Voltage and Current Output with the DACx760

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ABSTRACT

The DAC7760 and DAC8760 (DACx760) devices are used in industrial process control and other applications to generate voltage and current outputs. Creating a combined voltage and current output is desired in applications where the number of output terminals must be minimized. This application report describes how to create a single combined voltage and current output terminal with the DACx760.

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1 DACx760 Output Circuit Overview

Figure 1 shows a simplified version of the DACx760 output circuits when used in an application with separate voltage and current output terminals. The current output (IOUT) circuit is comprised of a standard two-stage current source. The first op amp, A1, takes the ground referenced digital-to-analog converter (DAC) voltage and acreates a supply referenced input voltage for the second op amp, A2, which controls the IOUT current through the Q2 MOSFET. The voltage output (VOUT) circuit consists of a standard noninverting op amp, A3, with different feedback options to accommodate different voltage output ranges.

In most applications, the VOUT and IOUT circuits are not active simultaneously. Setting the RANGE bits (DB2:DB0) in the *Control* register (0x55) selects the output type and range. Some applications do simultaneously activate the VOUT and IOUT circuits by writing a 1 to the DUAL OUTEN bit (DB8) of the configuration register (0x57). In this mode, both outputs are active, and are controlled by the same DAC output voltage.

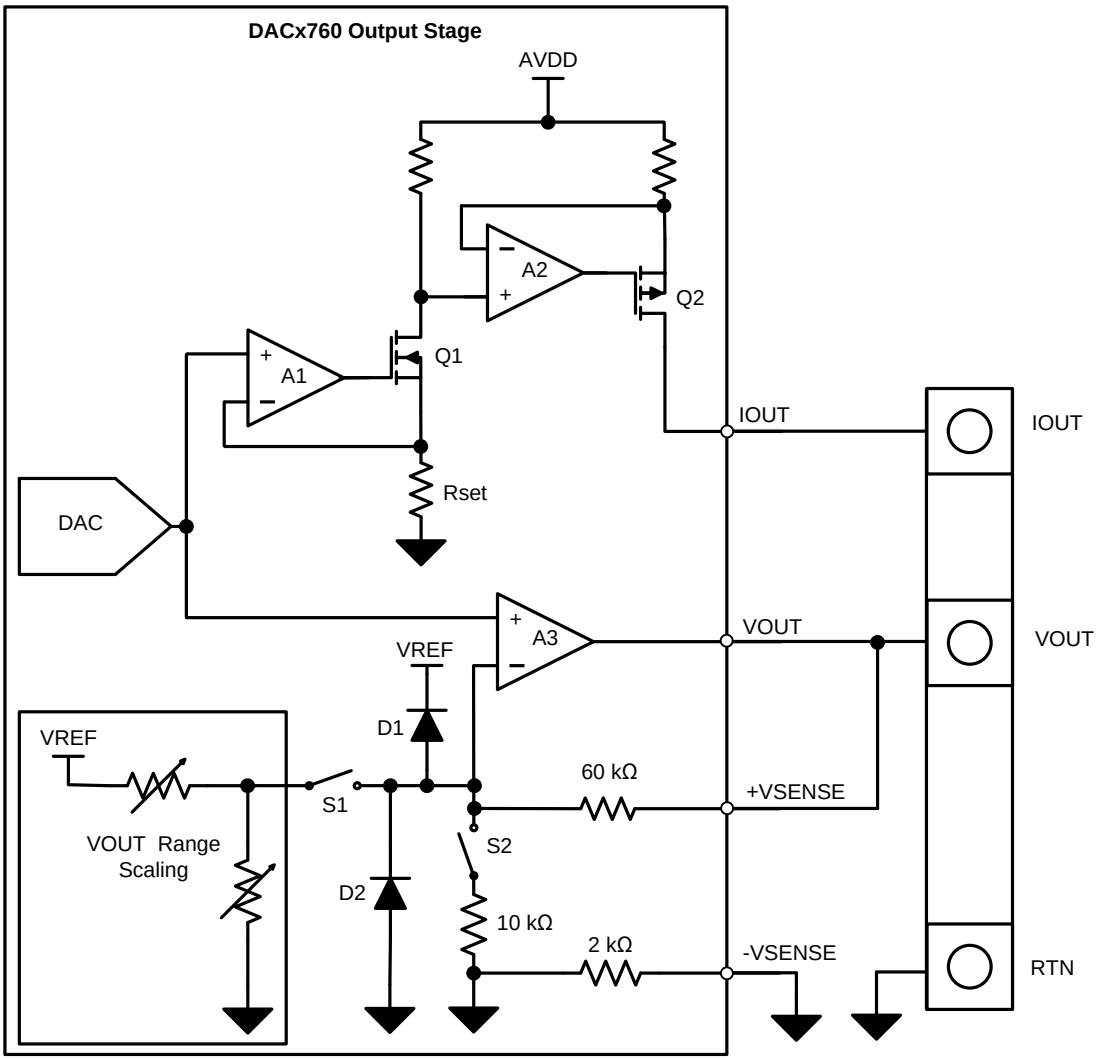

Figure 1. Simplified DACx760 Output Circuit with Separate Output Terminals

2 Combining the Voltage and Current Outputs

Creating a combined VOUT-IOUT output is accomplished by connecting the VOUT, +VSENSE, and IOUT pins together, as shown in Figure 2. The +VSENSE pin should be connected directly at the VOUT-IOUT connector to reduce errors resulting from printed circuit board (PCB) parasitic resistance.

CAUTION

When operating with a combined voltage and current connection, do not set the DUAL OUTEN bit (DB8, register 0x57) or device damage may occur.

As shown in Figure 2, the S1 and S2 switches remain open upon power up until the device registers are configured for a mode that closes these switches.

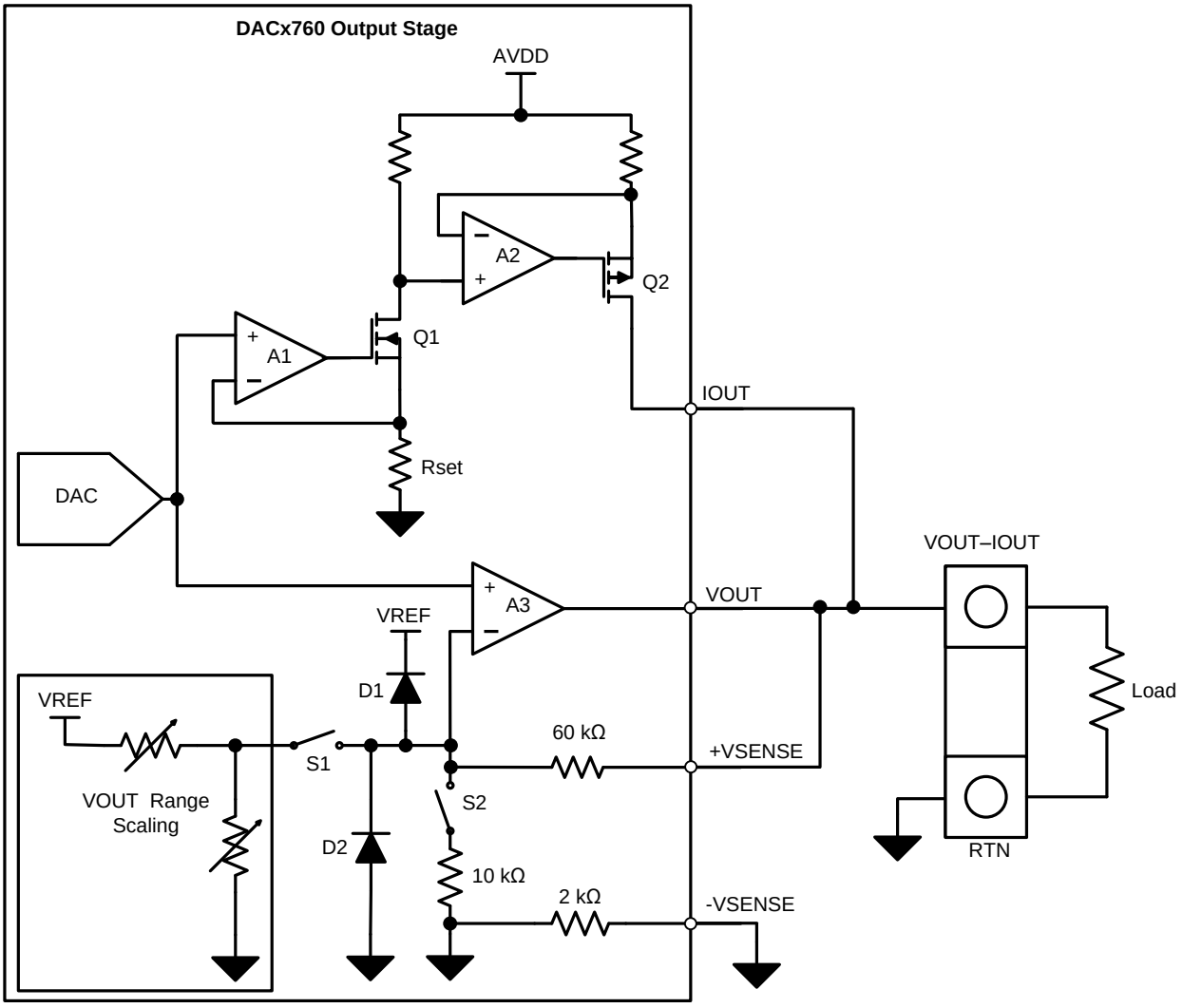

Figure 2. Combining the Voltage and Current Output Circuits

3 Voltage Output with a Combined Voltage and Current Connection

When the RANGE bits (DB2:DB0) in the control register (0x55) are configured for any of the VOUT ranges (0b000 to 0b011), the IOUT circuit becomes inactive, the VOUT op amp becomes active, switch S2 opens, and switch S1 closes. The appropriate feedback network is connected to A3 based on the selected output range.

Figure 3 shows an example of the VOUT circuit with a combined output connection. When the IOUT circuit is inactive, the Q2 PMOS is forced to a high-impedance state that does not load the dc voltage output. As a result, creating a combined output with the DACx760 does not significantly affect the VOUT circuit. With a combined connection, capacitive loads placed on IOUT also load VOUT, thus affecting the ac performance, and therefore require appropriate compensation by using the CMP pin.

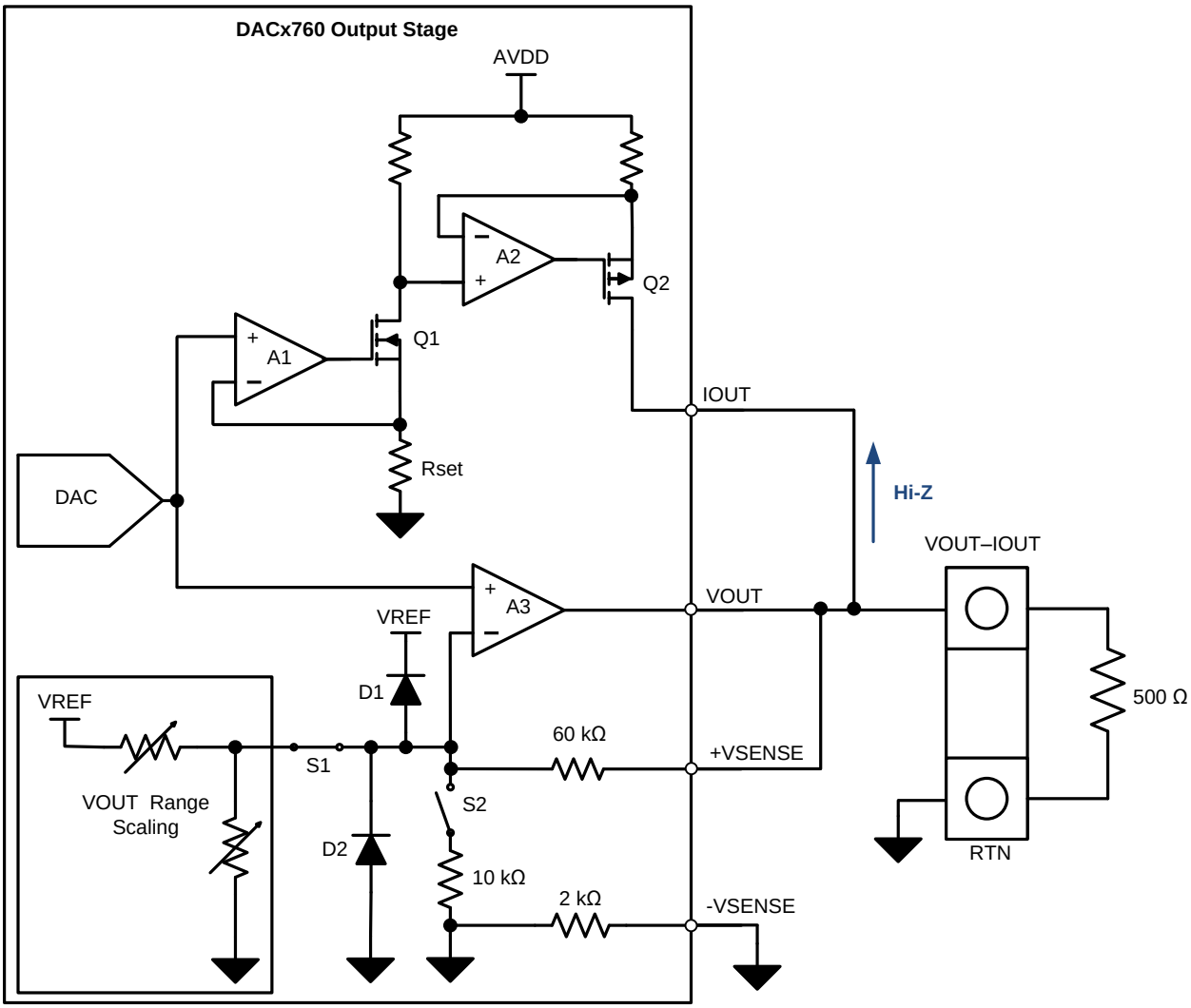

Figure 3. Voltage Mode Operation with a Combined VOUT-IOUT Connection

The measured performance results of two devices with and without a combined connection configured for ±10-V voltage outputs are shown in Table 1. The results confirm that a combined output has minimal effect on the dc VOUT performance. Voltage outputs with single-supply power supplies are similarly unaffected by the combined connection.

Table 1. ±10-V Output Performance Results with a Combined VOUT-IOUT Connection

Output Connection	DUT No.	DNL Max (LSB)	DNL Min (LSB)	Bipolar Zero (mV)	Full-Scale Error (%FSR)	Gain Error (%FSR)	INL Max (LSB)	INL Min (LSB)
Separate VOUT	1	0.185	–0.147	–0.492	–0.039	–0.055	6.430	–1.470
	2	0.167	–0.365	–1.774	–0.055	–0.070	7.105	1.400
Combined VOUT + IOUT	1	0.178	–0.146	–0.527	–0.039	–0.055	6.476	–1.481
	2	0.161	–0.374	–1.806	–0.055	–0.069	7.156	–1.462

4 Current Output with a Combined Voltage and Current Connection

When the RANGE bits (DB2:DB0) of the control register (0x55) are configured for any of the IOUT ranges (0b101 to 0b111), the IOUT circuit becomes active, the VOUT op amp is disabled, and the S1 switch is opened. In this configuration, the IOUT performance is unaffected, as long as the voltage developed by the load (V_{LOAD}) on the VOUT-IOUT connection is less than V_{REF}.

If the load resistance pushes the VOUT-IOUT voltage above V_{REF}, the positive clamp diode on the inverting input, D1, begins to conduct, which diverts current from the load into the +VSENSE pin and causes a gain error; see Figure 4. The current that flows into the diode, I_{DIODE}, can be roughly calculated using Equation 1. Note that diode current is never negative. Unfortunately, because the diode voltage, V_{DIODE}, varies over many factors, the calculation does not produce a reliable solution and cannot accurately calibrate out the resulting gain error. The calculation also excludes the non-linear current that begins to flow when the load voltage is greater than V_{REF}, but not by more than V_{DIODE}.

$$I_{DIODE} = \frac{V_{LOAD} - (V_{REF} + V_{DIODE})}{60\ k\Omega} > 0\ A \quad (1)$$

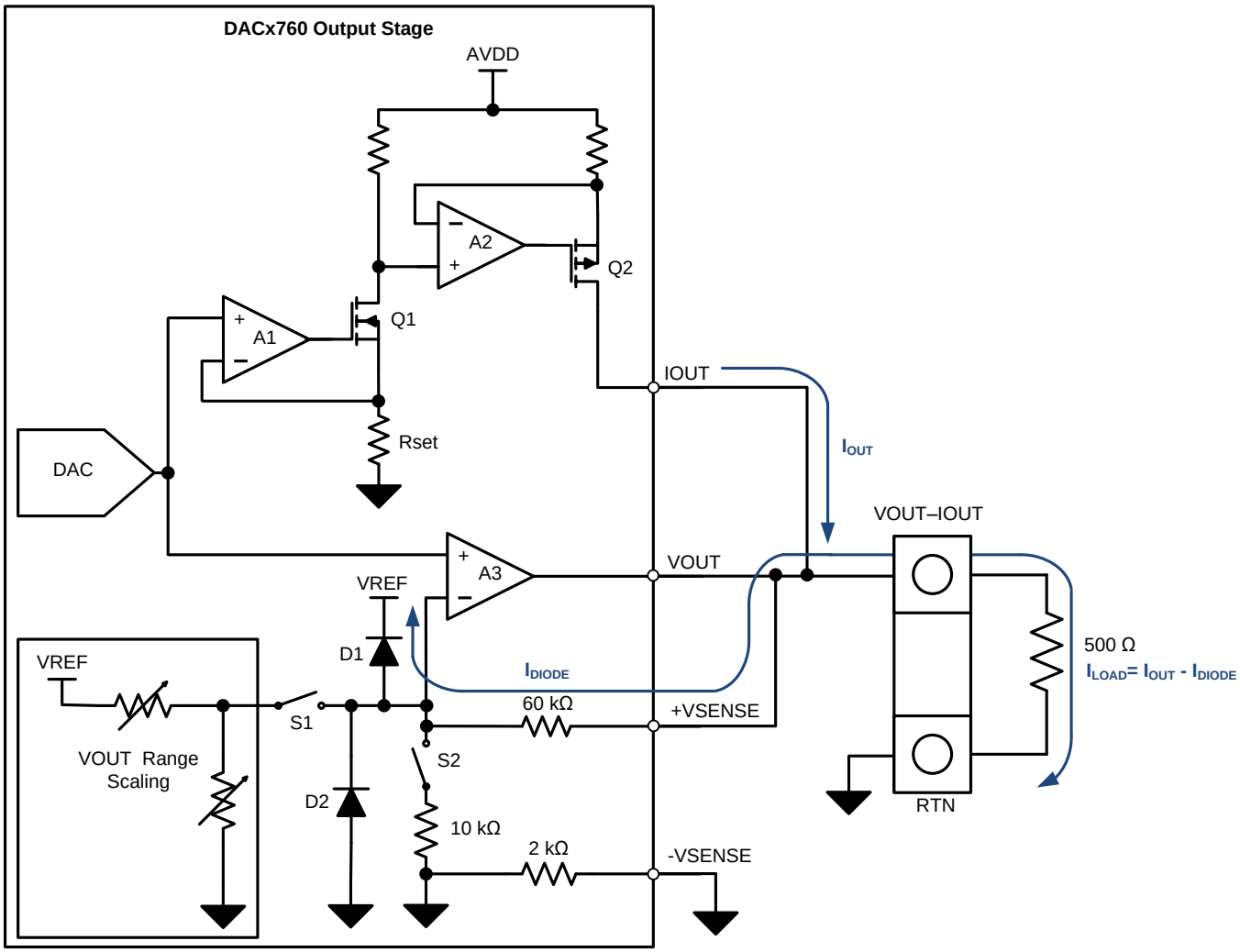

Figure 4. Current Mode Operation with a Combined VOUT-IOUT Connection

The performance results for two devices with and without a combined output connection are shown in Table 2. Full-scale error, gain error, and INL are all negatively affected when the diode conducts current away from the load. While the full-scale gain errors can be corrected, the drastic increase in INL resulting from the nonlinearity of the diode current cannot be corrected.

Table 2. 4-mA to 20-mA Output Performance Results with a Combined VOUT-IOUT Connection

Output Connection	DUT No.	DNL Max (LSB)	DNL Min (LSB)	Offset (%FSR)	Full-Scale Error (%FSR)	Gain Error (%FSR)	INL Max (LSB)	INL Min (LSB)
Separate IOUT	1	0.418	–0.411	0.004	0.062	0.057	1.612	–5.438
	2	0.562	–0.575	0.002	0.072	0.066	1.781	–5.380
Combined VOUT + IOUT	1	0.483	–0.421	0.007	–0.372	–0.377	120.011	–0.661
	2	0.480	–0.535	0.005	–0.351	–0.343	116.936	–0.673

5 Solutions to Improve Accuracy in Current Mode with Combined Outputs

A few methods are provided in the following sections to improve the accuracy of the IOUT circuit because the linearity and gains errors with a combined output are unacceptable in most applications. A list of measured results for the methods described in this section are summarized in Table 7 of the *Section 6* section.

5.1 Digital Correction for the +VSENSE Error

The increased INL resulting from the nonlinear behavior of the D1 current prevents the calibration registers from being effective. Prevent D1 from conducting by setting bit 7 of the configuration register to 1, which closes the S2 switch. Closing S2 creates a resistor divider between the 10-kΩ resistor and the 60-kΩ feedback resistor, thus limiting the voltage at the inverting input of the A3 amplifier. The voltage divider appears in parallel to the load, forming a gain error as shown in Figure 5. In this configuration, the gain error can be calculated by Equation 2 and Equation 3, and can therefore be minimized using the calibration registers.

$$\text{GainError (\%)} = \frac{R_{LOAD}}{R_{LOAD} + 70\ k\Omega} \bullet 100 \tag{2}$$

The current delivered to the load is defined in Equation 3:

$$I_{LOAD} = I_{OUT} \bullet \left(1 - \frac{\text{GainError}}{100}\right) \tag{3}$$

In a 4-mA to 20-mA system with a 500-Ω load, the gain error is approximately 0.71%. At full-scale, the gain error results in a 141.8-µA error current, delivering only 19.86 mA to the load.

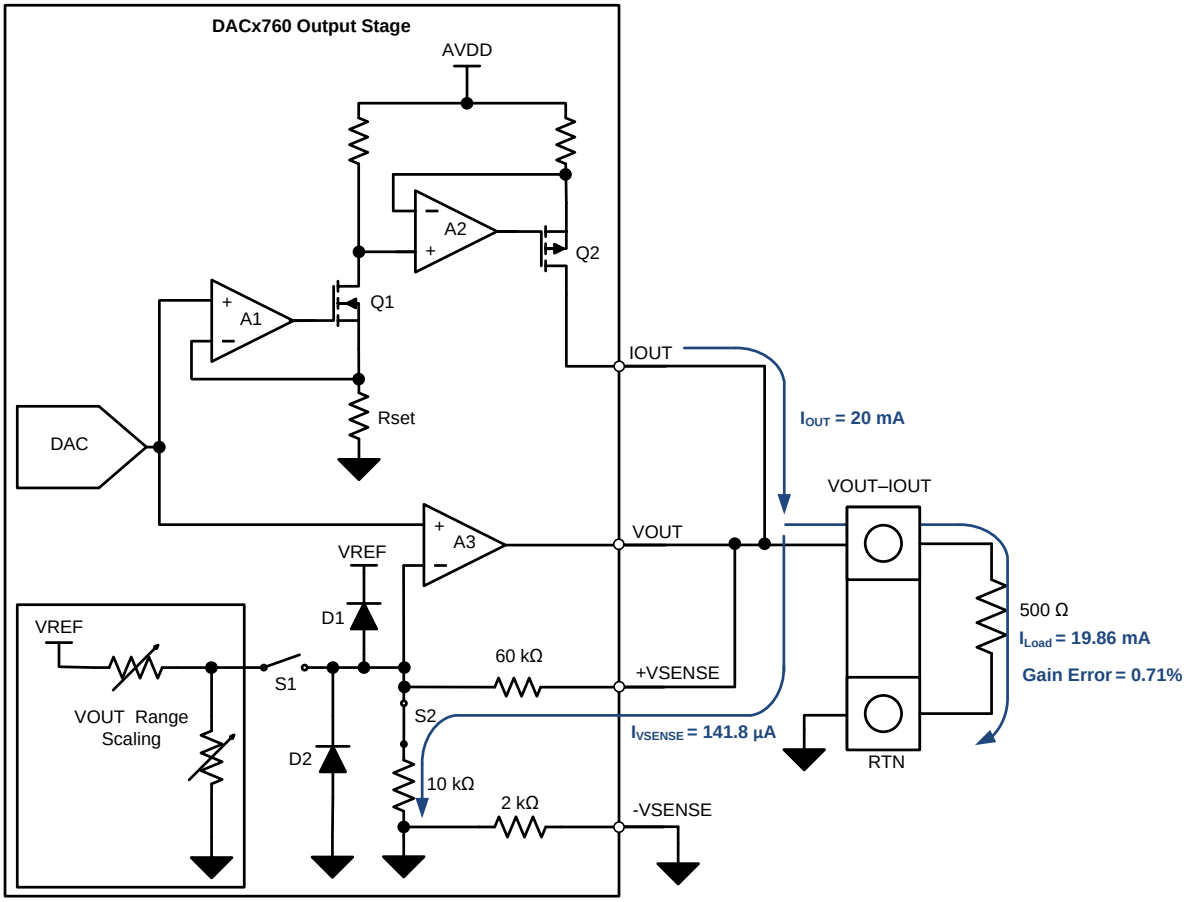

Figure 5. Closing S2 in Current Mode with a Combined VOUT-IOUT Connection

For the calibration to be successful, the resistance of the load (R_{LOAD}) must be known. Determining this value may not be possible in some systems, and may be further complicated by any wiring resistance between the connector and the load. Rounding errors in the digital calibration reduces the linearity (DNL and INL) of the IOUT output from the datasheet specifications, but results in significantly better performance than the nonlinearity caused by allowing the i_{DIODE} current to conduct.

In 0-mA to 20-mA and 0-mA to 24-mA modes, minimize the gain error from the internal resistance with a gain calibration using the gain calibration register (0x58). To implement the calibration, calculate the gain based on the load resistance and apply the calculated value to the gain calibration register. An example is shown in Equation 4 and Equation 5 for a 0-mA to 24-mA output with a load resistance of 500 Ω.

$$\text{Gain} = \frac{R_{LOAD} + 70\ k\Omega}{70\ k\Omega} = \frac{70.50\ k\Omega}{70\ k\Omega} = 1.0071428 \quad (4)$$

$$\text{Gain Cal Register} = (\text{Gain} \bullet 2^{16}) - 2^{15} = 33236 = 0x81D4 \quad (5)$$

The results for a 0-mA to 24-mA output in Figure 6 display the possible improvement with SW2 closed before and after calibration using the gain calibration register (0x58). Figure 6 is configured with a logarithmic y-axis to more clearly view the results of the gain calibration.

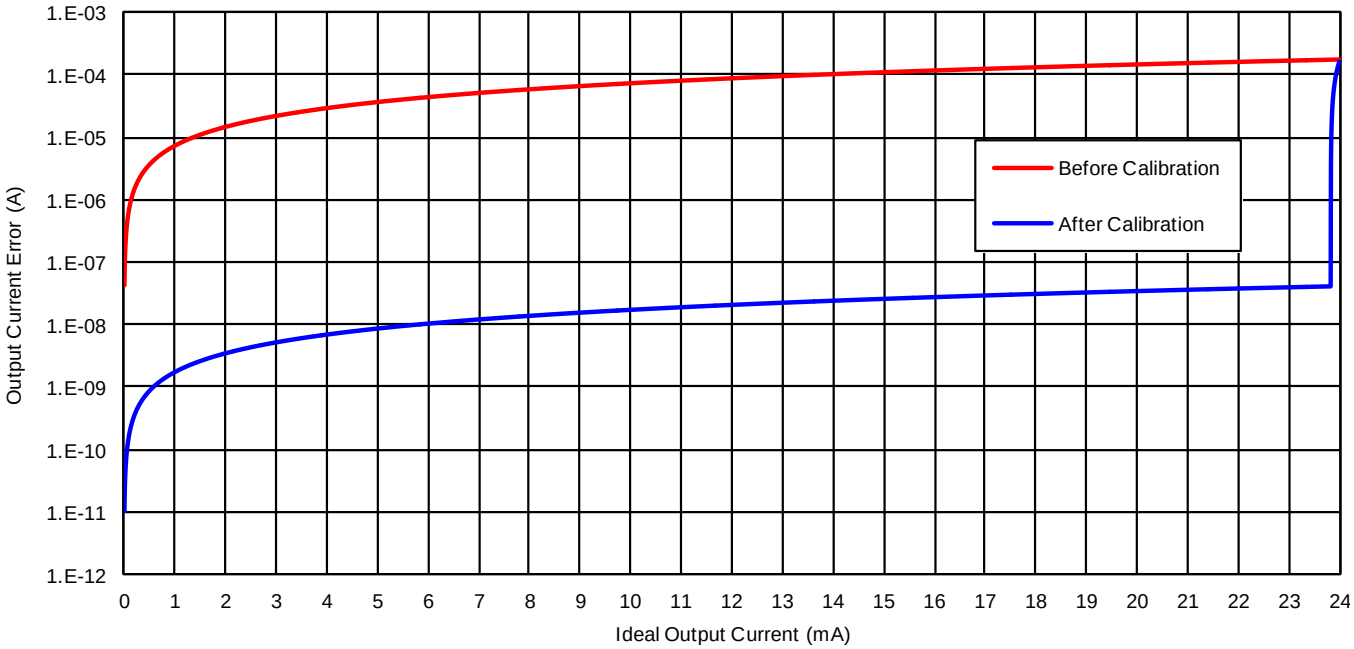

Figure 6. IOUT Error Reduction Using Gain Calibration with a 500-Ω Load in 0-mA to 24-mA Mode

Calculating the error in terms of full-scale resolution (%FSR), and plotting the data on a linear y-axis makes the improvement more noticeable, as shown in Figure 7.

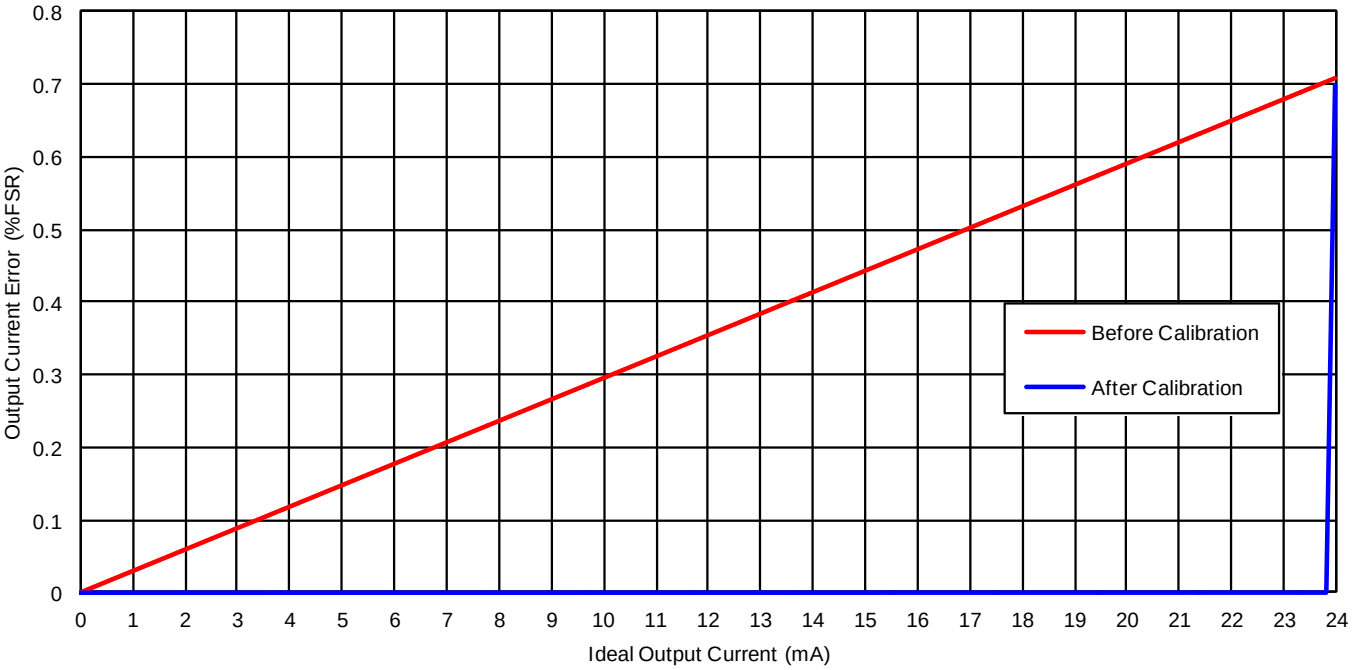

Figure 7. IOUT Error (%FSR) Reduction Using Gain Calibration with a 500-Ω Load in 0-mA to 24-mA Mode

The error after calibration suddenly increases to the level of the original error near the end of the output range because the calibration only affects the digital code and does not affect the restrictions of the analog output circuit. Therefore, in the 0-mA to 24-mA mode, the maximum output is still restricted to 24 mA based on the analog circuitry limitations resulting in a *dead zone* of codes, where the output no longer changes even with an increase in input code because the analog output is saturated. Therefore, this digital correction method is best applied in the 0-24 mA mode because the 4-20 mA section of the output range maintains low error.

If the method is applied in the 4-mA to 20-mA mode, the offset at the 4-mA, zero-scale level must be cancelled. To cancel, use the offset calibration register (0x59), as shown in Equation 6 and Equation 7. The calculation for the gain calibration register (0x58) is the same as shown in the 0-mA to 24-mA case.

$$\text{Offset} = \frac{R_{LOAD}}{R_{LOAD} + 70k\Omega} \bullet 4\ mA = 0.02837\ mA \quad (6)$$

$$\text{Offset Cal Register} = \frac{\text{Offset} \bullet 2^{16}}{16\ mA} = 116 = 0x0074 \quad (7)$$

The results of the error (%FSR) are plotted with a linear y-axis in Figure 8. The results on a log y-axis looks similar to the results illustrated in Figure 6.

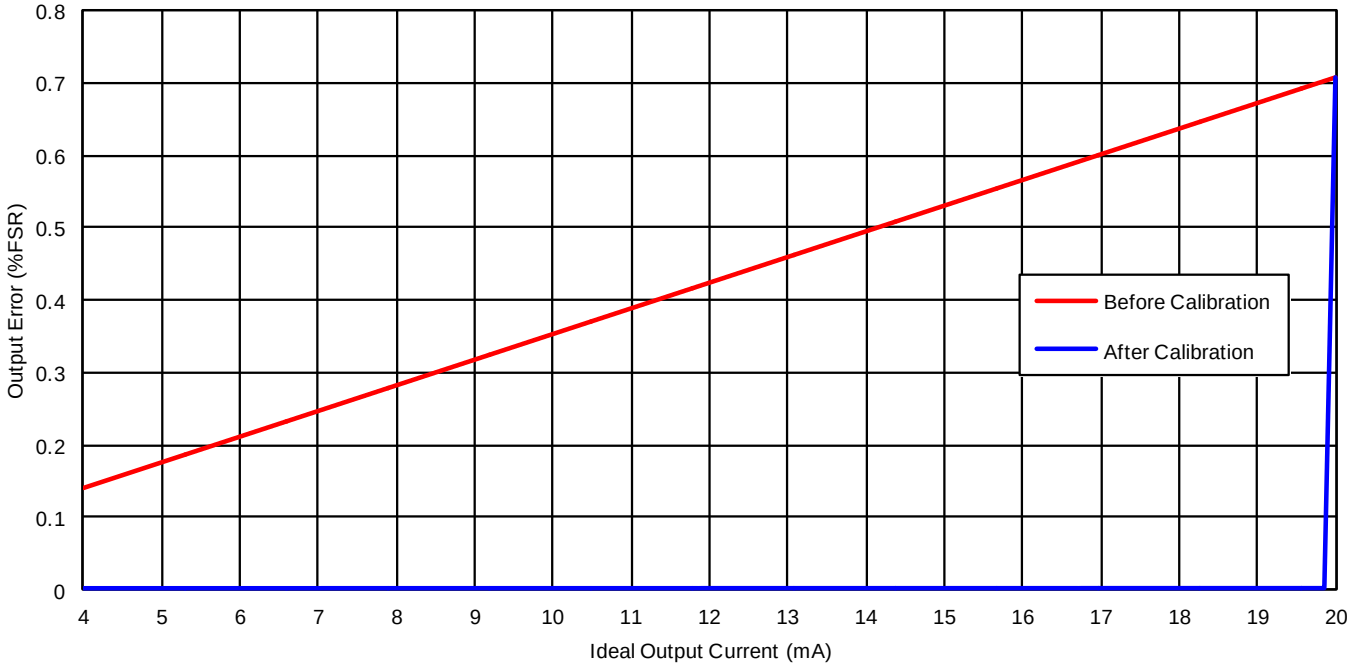

Figure 8. IOUT Error (%FSR) Reduction Using Gain Calibration with a 500-Ω Load in 4-20 mA Mode

The measured performance results using the digital calibration methods can be seen in Table 3. The results show that preventing the diode from conducting by closing S2 brings the INL back to an acceptable level. However, with S2 closed, the full-scale and gain errors become worse because a larger current flows through the resistors to GND than through the D1 diode to VREF. Applying calibration with S2 closed brings the offset, full-scale, and gain errors almost back to the levels with a separate IOUT. However, calibration reduces the DNL compared with the original levels because of rounding errors between the calibrated code value and the possible code value.

Table 3. 4-20mA Output Performance Results Using Digital Calibration

Output Connection	DUT No.	DNL Max (LSB)	DNL Min (LSB)	Offset (%FSR)	Full-Scale Error (%FSR)	Gain Error (%FSR)	INL Max (LSB)	INL Min (LSB)
Separate IOUT	1	0.418	–0.411	0.004	0.062	0.057	1.612	–5.438
	2	0.562	–0.575	0.002	0.072	0.066	1.781	–5.380
Combined VOUT + IOUT	1	0.483	–0.421	0.007	–0.372	–0.377	120.011	–0.661
	2	0.480	–0.535	0.005	–0.351	–0.343	116.936	–0.673
S2 closed before calibration	1	0.405	–0.561	-0.170	–0.810	–0.635	1.433	–5.250
	2	0.456	–0.466	-0.172	–0.802	–0.606	1.647	–5.119
S2 closed after calibration	1	0.882	–0.371	0.004	0.074	0.067	2.130	–5.380
	2	0.856	–0.587	0.002	0.082	0.076	2.418	–5.904

5.2 Analog Correction for the +VSENSE Error

The preferred method to solve the gain error issue is to use an external amplifier to buffer the +VSENSE connection, as shown in Figure 9. An op amp buffer is placed between the combined output connection and the +VSENSE input to provide the current into the +VSENSE pin. This configuration reduces the load on the combined connection to the input bias current (I_B) of the noninverting input of the op amp. For a typical CMOS amplifier, I_B is in the order of a few hundred picoamps or less, which does not significantly affect the accuracy of the IOUT circuit.

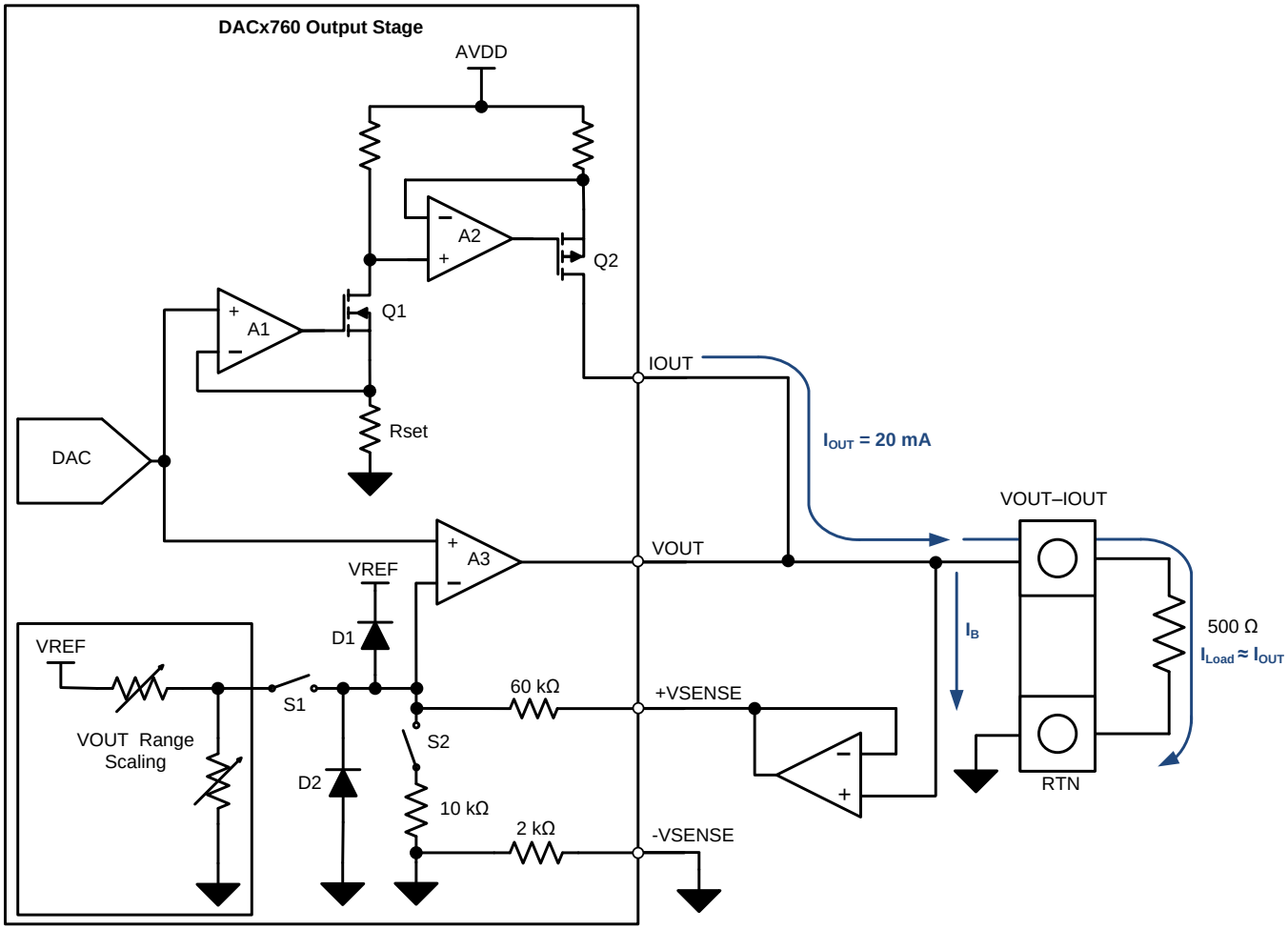

Figure 9. Buffering the +VSENSE Pin Using an External Amplifier

5.2.1 +VSENSE Buffer Selection and Results

The +VSENSE buffer op amp must be able to tolerate the power-supply voltages applied to it as well as the voltages the DACx760 applies to its inputs in both VOUT and IOUT modes. When the IOUT circuit is active, high load impedances or an open-circuit cause the voltage on the shared connection to approach the positive supply voltage of the DACx760. Therefore, avoid situations where the op amp power supply is less than the DACx760 supply because it can lead to damage of the op amp input, unless the combined output connection is clamped to the op amp supply with an external protection circuit.

The buffer op amp is part of the VOUT circuit feedback network, and therefore adds errors to the VOUT output. The op amp primarily affects the offset performance based on the input offset voltage (V_{IO}) specification of the op amp. Do not ignore the effects of temperature drift, common-mode rejection ratio (CMRR), and power-supply rejection ratio (PSRR) on the offset voltage of the amplifier because they may contribute significant additional error. To reduce these errors, choose an amplifier with low initial offset voltage, low offset voltage drift, high CMRR, and high PSRR. Chopper-stabilized, zero-drift amplifiers such as the OPA188 or precision e-Trim™ amplifiers such as the OPA192 work very well in applications requiring high performance. For successful single-supply operation, the op amp must have a common-mode input range that includes the negative supply. Additionally, the output swing-to-rail performance of the DACx760 is very good. Make sure that any buffer amplifiers selected for this application have a rail-to-rail output stage with good swing-to-rail performance. Other 36-V devices that work well in this application are the OPA140, OPA170, or OPA277.

The results using the OPA188, OPA192, and OPA170 buffer amplifiers are shown in Table 4. The results show that the buffer amplifiers return a combined VOUT-IOUT performance similar to the performance with IOUT and VOUT separate.

Table 4. 4-20 mA Output Performance Results Using OPA188, OPA192, and OPA170 Buffers

Output Connection	DUT No.	DNL Max (LSB)	DNL Min (LSB)	Offset (%FSR)	Full-Scale Error (%FSR)	Gain Error (%FSR)	INL Max (LSB)	INL Min (LSB)
Separate IOUT	1	0.418	–0.411	0.004	0.062	0.057	1.612	–5.438
	2	0.562	–0.575	0.002	0.072	0.066	1.781	–5.380
Combined VOUT + IOUT	1	0.483	–0.421	0.007	–0.372	–0.377	120.011	–0.661
	2	0.480	–0.535	0.005	–0.351	–0.343	116.936	–0.673
OPA188 buffer	1	0.367	–0.435	0.003	0.060	0.055	1.614	–5.379
	2	0.437	–0.535	0.002	0.070	0.065	1.647	–5.847
OPA192 buffer	1	0.438	–0.415	0.002	0.059	0.054	1.666	–5.501
	2	0.410	–0.611	0.002	0.070	0.065	1.500	–5.654
OPA170 buffer	1	0.443	–0.555	0.002	0.069	0.064	1.569	–5.572
	2	0.430	–0.434	0.002	0.059	0.055	1.514	–5.528

5.2.2 Unipolar Configuration and Results

In applications that only require the unipolar 0-V to 10-V and 0-V to 5-V outputs, use a single-supply power connection for both the DACx760 and the op amp, as shown in Figure 10. In this configuration, the amplifier must have a common-mode input voltage range that includes the negative rail and an output stage that has swing-to-rail characteristics similar to the DAC7760 and DAC8760.

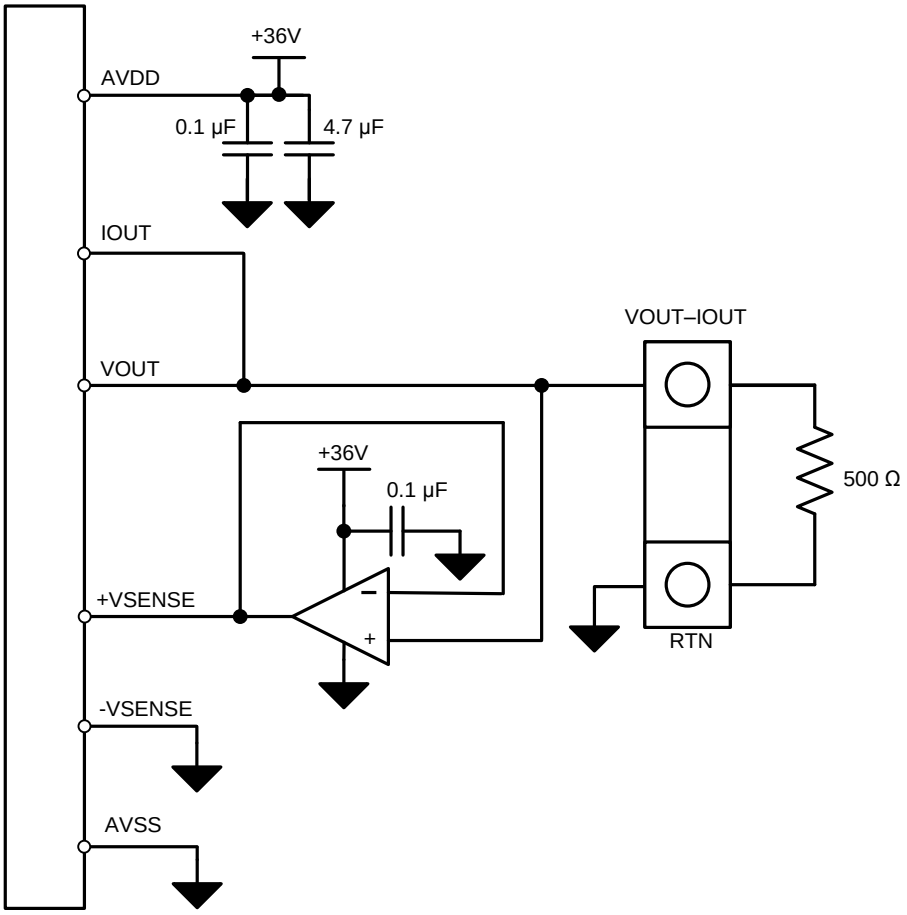

Figure 10. Unipolar Supply Connections for the +VSENSE Buffer

The performance results for a 4-mA to 20-mA output and 0-V to 10-V output with a single-supply connection using the OPA188, OPA192, and OPA170 as buffers are shown in Figure 11 and Figure 12, respectively. The results are only shown for input codes near zero-scale and full-scale because the difference between the curves is not visible on larger scales. The improvement that the buffers provide for IOUT performance is easily visible near the full-scale current levels with the buffered results compared closely to the separate output case. In VOUT mode, the buffered outputs closely track the combined output with an offset error based on the op amp offset voltage.

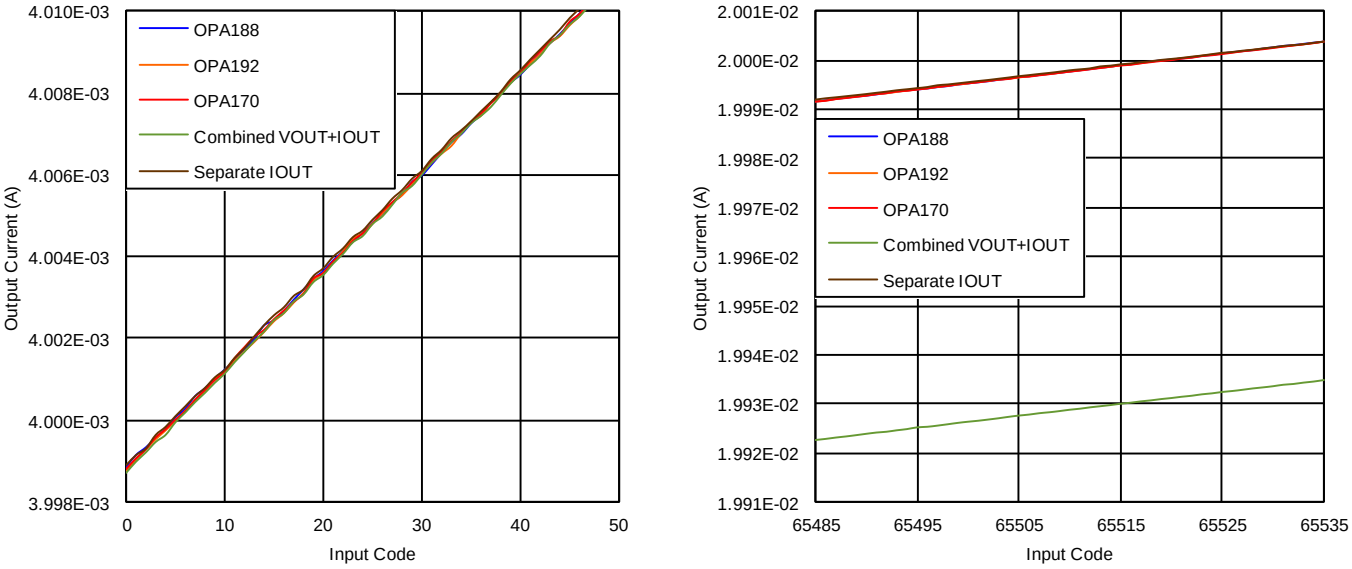

Figure 11. 4-mA to 20-mA Output Results with Unipolar Supplies

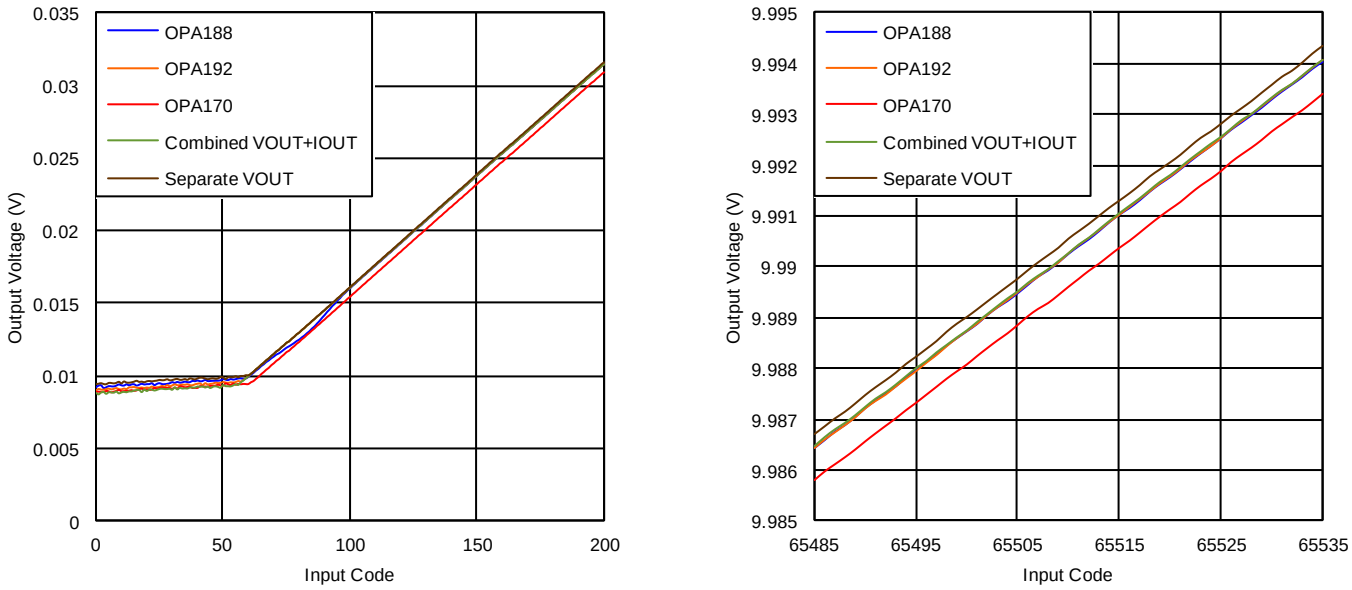

Figure 12. 0-V to 10-V Output Results with Unipolar Supplies

The VOUT performance results with a unipolar supply are shown in Table 5. The op amps do not have much affect on linearity or gain errors, but do affect the offset performance (see Figure 11 and Figure 12).

Table 5. 0-V to 10-V Output Performance Results with a Buffer Amplifier

Output Connection	DUT No.	DNL Max (LSB)	DNL Min (LSB)	Offset (mV)	Full-Scale Error (%FSR)	Gain Error (%FSR)	INL Max (LSB)	INL Min (LSB)
Separate VOUT	1	0.227	–0.167	0.957	–0.017	–0.026	4.689	–1.931
	2	0.202	–0.378	0.910	–0.021	–0.029	5.189	–2.489
Combined VOUT + IOUT	1	0.244	–0.145	0.929	–0.019	–0.028	4.740	–1.998
	2	0.184	–0.409	0.883	–0.023	–0.031	5.328	–2.679
OPA188 buffer	1	0.221	–0.151	0.930	–0.018	–0.027	4.404	–1.969
	2	0.196	–0.372	0.879	–0.023	–0.031	5.164	–2.565
OPA192 buffer	1	0.228	–0.161	0.935	–0.018	–0.026	4.283	–1.983
	2	0.212	–0.459	0.884	–0.023	–0.030	5.168	–2.572
OPA170 buffer	1	0.215	–0.177	1.000	–0.017	–0.026	4.480	–1.989
	2	0.218	–0.384	0.222	–0.029	–0.030	5.188	–2.557

5.2.3 Bipolar Configuration and Results

The example circuit in Figure 13 shows how to connect the op amp device to the DACx760 system if both positive and negative voltage outputs are desired. The example displays how to remain within the 36-V operational voltage of most industrial amplifiers while still accepting a 24-V field supply by using a –12-V negative supply. Other supply combinations can be used, as long as the supply voltage and input voltages remain with the absolute maximum ratings of the DACx760 and op amp devices.

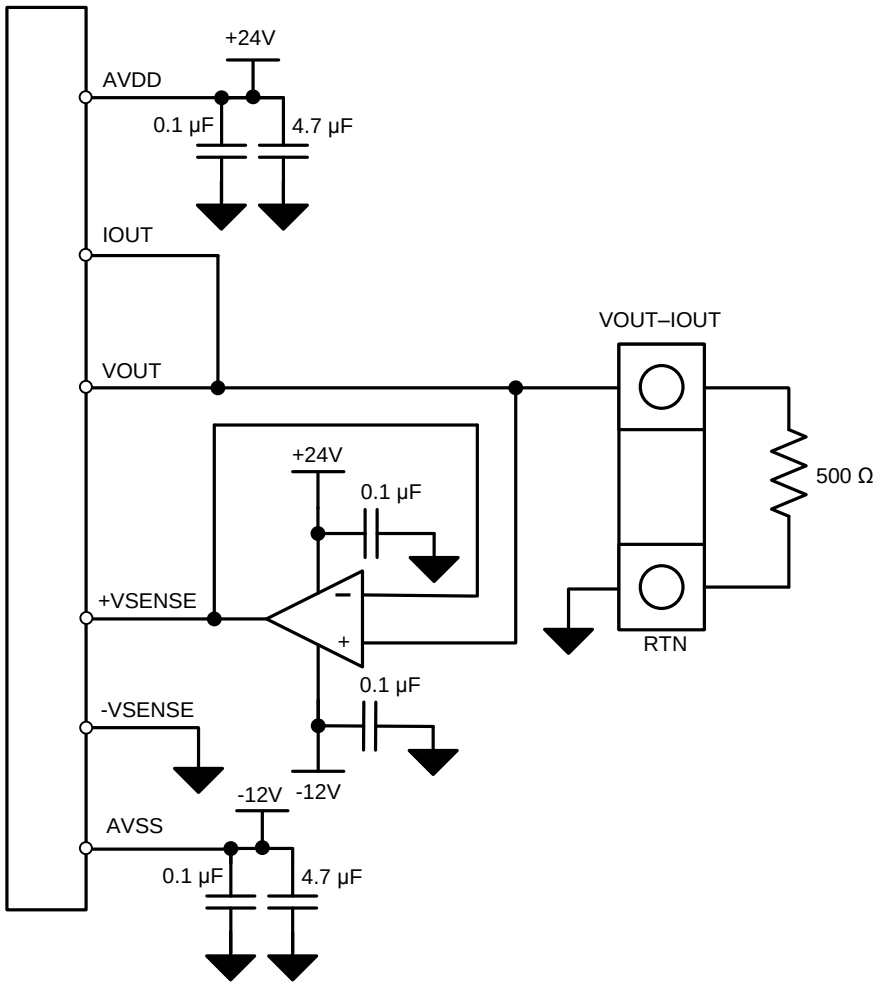

Figure 13. Bipolar Supply Connections for the +VSENSE Buffer

The results for a 4-mA to 20-mA output and ±10-V and outputs are shown in Figure 14 and Figure 15, respectively. The bipolar IOUT performance is very similar to the unipolar case, and the improvement from the buffers is easily visible. Because the negative supply is configured for –12 V, the output of the amplifiers is not affected by swing-to-rail limitations, and very closely tracks the combined output case.

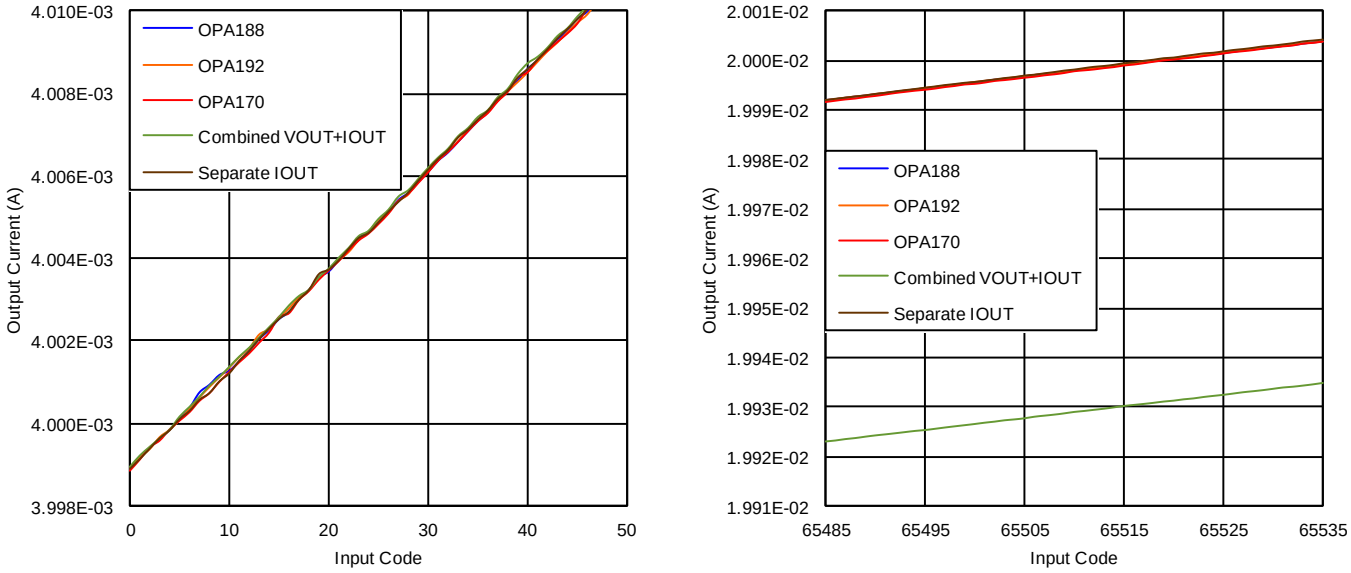

Figure 14. 4-mA to 20-mA Output Results with Bipolar Supplies

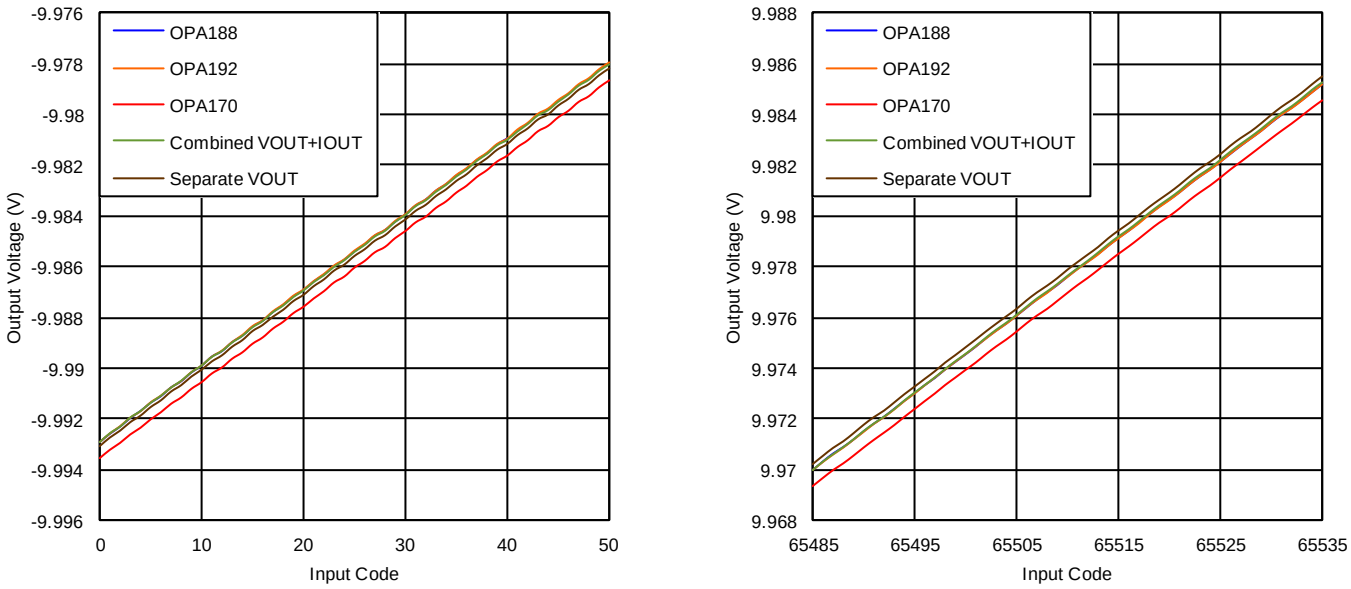

Figure 15. ±10-V Output Results with Bipolar Supplies

The VOUT performance results with a bipolar supply are shown in Table 6. The results are very similar to the unipolar case with minimal affect on linearity or gain, but some affect on offset performance.

Table 6. ±10-V Output Performance Results with a Buffer Amplifier

Output Connection	DUT No.	DNL Max (LSB)	DNL Min (LSB)	Bipolar Zero (mV)	Full-Scale Error (%FSR)	Gain Error (%FSR)	INL Max (LSB)	INL Min (LSB)
Separate VOUT	1	0.185	–0.147	–0.492	–0.039	–0.055	6.430	–1.470
	2	0.167	–0.365	–1.774	–0.055	–0.070	7.105	1.400
Combined VOUT + IOUT	1	0.178	–0.146	–0.527	–0.039	–0.055	6.476	–1.481
	2	0.161	–0.374	–1.806	–0.055	–0.069	7.156	–1.462
OPA188 buffer	1	0.177	–0.178	–0.517	–0.038	–0.052	6.219	–1.418
	2	0.159	–0.370	–1.813	–0.055	–0.070	7.126	–1.479
OPA192 buffer	1	0.179	–0.161	–0.512	–0.038	–0.052	6.260	–1.475
	2	0.167	–0.388	–1.807	–0.055	–0.069	7.131	–1.486
OPA170 buffer	1	0.175	–0.151	–0.458	–0.038	–0.052	6.254	–1.424
	2	0.158	–0.386	–2.458	–0.058	–0.070	7.170	–1.491

6 Results Summary

When creating a combined voltage and current output with the DACx760, the IOUT circuit is negatively affected by current flowing into the +VSENSE pin. While digital calibration methods are possible, the preferred solution for a high-performance combined output circuit includes a precision op amp to buffer the +VSENSE input. Make sure the op amp has low input bias current so that IOUT performance is unaffected, as well as low input offset voltage and good output swing-to-rail performance to maintain high accuracy for the VOUT circuit. Table 7 displays the results for current outputs in all of the configurations discussed in this document.

Table 7. Summary of Performance Results for 4-20mA Output Configurations

Connection	DUT No.	DNL Max (LSB)	DNL Min (LSB)	Offset (%FSR)	Full-Scale Error (%FSR)	Gain Error (%FSR)	INL Max (LSB)	INL Min (LSB)
Separate IOUT	1	0.418	–0.411	0.004	0.062	0.057	1.612	–5.438
	2	0.562	–0.575	0.002	0.072	0.066	1.781	–5.380
Combined VOUT + IOUT	1	0.483	–0.421	0.007	–0.372	–0.377	120.011	–0.661
	2	0.480	–0.535	0.005	–0.351	–0.343	116.936	–0.673
S2 closed before calibration	1	0.405	–0.561	–0.170	–0.810	–0.635	1.433	–5.250
	2	0.456	–0.466	–0.172	–0.802	–0.606	1.647	–5.119
S2 closed after calibration	1	0.882	–0.371	0.004	0.074	0.067	2.130	–5.380
	2	0.856	–0.587	0.002	0.082	0.076	2.418	–5.904
OPA188 buffer	1	0.367	–0.435	0.003	0.060	0.055	1.614	–5.379
	2	0.437	–0.535	0.002	0.070	0.065	1.647	–5.847
OPA192 buffer	1	0.438	–0.415	0.002	0.059	0.054	1.666	–5.501
	2	0.410	–0.611	0.002	0.070	0.065	1.500	–5.654
OPA170 buffer	1	0.443	–0.555	0.002	0.069	0.064	1.569	–5.572
	2	0.430	–0.434	0.002	0.059	0.055	1.514	–5.528

7 Creating a Combined Voltage and Current Output with Boost Transistor

The same theory described in Section 2 applies when using a boost transistor. Voltage mode operation is unaffected by the shared connection because the IOUT path is still high impedance when inactive. The VOUT circuit may need proper compensation using the CMP pin if capacitive loading is applied to the shared output terminal. The IOUT circuit with a boost transistor shows error as a result of loading by the internal VOUT circuitry; the same as was shown without the boost transistor.

The options to improve the current accuracy discussed in Section 5 also apply when using a boost transistor. Figure 16 shows the analog correction method using an op amp to buffer the +VSENSE pin when using a boost transistor.

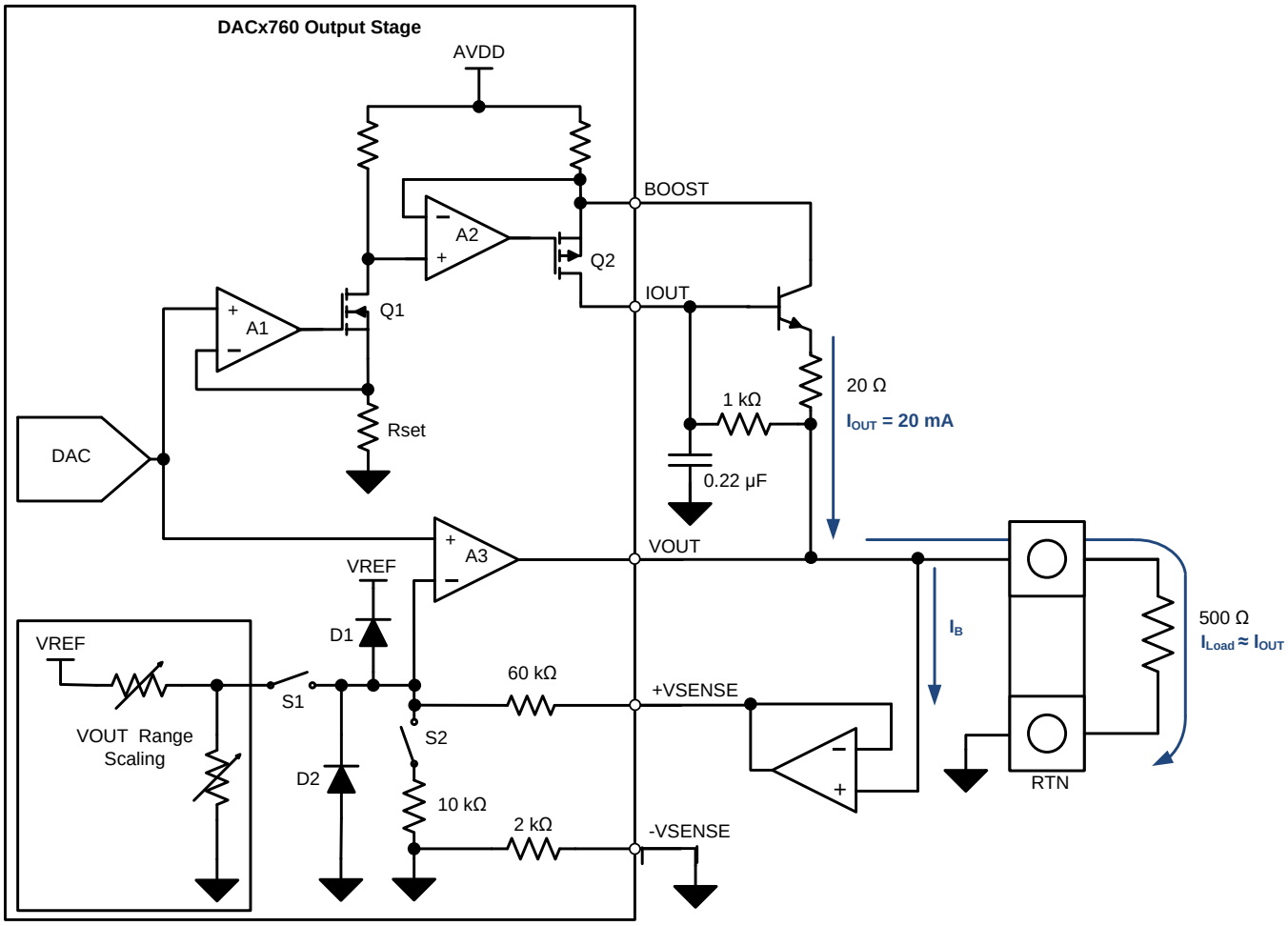

Figure 16. Buffering the +VSENSE Pin Using an External Amplifier with a Boost Transistor

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