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ΔΣ ADC Design for Bridge Sensor Applications

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ABSTRACT

This application report reviews several different types of bridge sensors, including characteristics of each type, and discusses the key parameters of delta-sigma (ΔΣ) analog-to-digital converters (ADCs) at the system level. Additionally, the parameters of a ΔΣ ADC are considered for use in common bridge sensor applications.

Contents

1 Bridge Sensor Introduction 1
2 Noise-Free Bits of ΔΣ ADCs 2
3 System Budget 3
4 Summary 6
5 References 6

1 Bridge Sensor Introduction

A bridge sensor consists of four resistive elements. The respective resistance of one or more of these elements changes with respect to the input parameter under consideration. Typical bridge sensor applications include strain gauges, pressure sensors, and load cells. There are three types of bridge sensors, as illustrated in Figure 1.

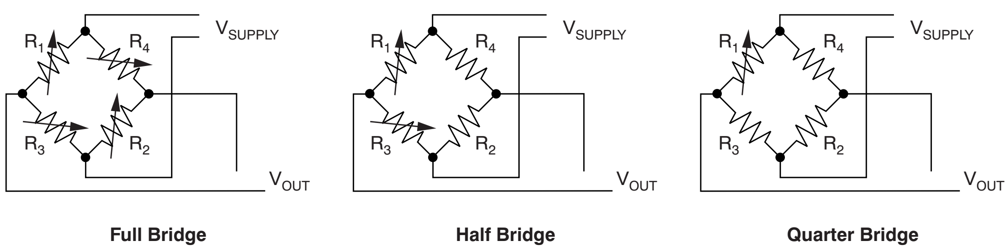

Figure 1. Bridge Sensor Types

In a full bridge sensor, all four elements change resistance. For example, a load cell is constructed with four individual strain gauges connected in a standard bridge configuration. When the load is applied to the beam, R_1 and R_2 decrease in value, and R_3 and R_4 increase in value.

In a half bridge configuration, two elements change resistance while two elements are fixed. In a quarter bridge architecture, on the other hand, only one element changes its resistance; the other three elements remain fixed. Note that these fixed resistors must be precision, low-temperature coefficient types for the greatest accuracy.

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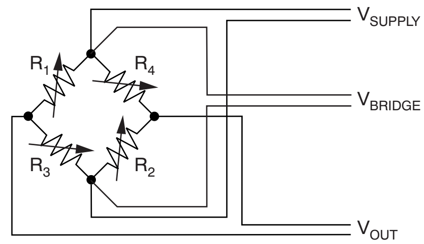
All of the examples illustrated in Figure 1 have four wires connected to the bridge. Consequently, they are known as *four-wire bridges*. In a four-wire system, the voltage drop in the power supply leads is assumed to be small, so the bridge input voltage is measured at the power supply. However, if there is a significant resistance in the power wires, then the voltage measured at the supply and bridge ends of the supply wires is different, which could lead to measurement errors. In this case, it is necessary to use a six-wire bridge system (shown in Figure 2) where two wires supply power to the bridge, two wires measure the actual voltage present at the bridge (thus removing any voltage drops in the power-supply leads), and two wires measure the bridge output.



Six-Wire Bridge

Figure 2. Six-Wire Bridge Sensor

Kelvin sensing is used to eliminate errors that occur as a result of the wiring resistance in the bridge excitation lines. The bridge is driven directly from the power supply, and the sense lines serve as the ADC reference voltage, thereby ensuring fully ratiometric operation as previously described. The need for a complicated filter is also eliminated; simple ceramic capacitor decoupling on each analog and reference input is sufficient. However, we must also pay attention to the dc common-mode voltage on the small differential output voltage.

2 Noise-Free Bits of ΔΣ ADCs

The noise-free bit parameter (or peak-to-peak resolution) calculates up to how many bits are stable from the ADC output with a full-scale input. The noise-free bit (peak-to-peak resolution) is defined as Equation 1:

$$\text{Noise-free bit} = \text{Log}_2\ (\text{FSR/peak-to-peak noise}) \quad (1)$$

Based on the ADS1232 product data sheet, the input range = ±19.5 mV at a gain of 128, with V_{REF} = 5 V, as described in Table 1.

Table 1. ADS1232 Noise Performance Comparison: AVDD = 5 V, V_{REF} = 5 V, Data Rate = 10 SPS

Gain	RMS Noise	Peak-to-Peak Noise[1]	ENOB (RMS)	Noise-Free Bits
1	420 nV	1.79 µV	23.5	21.4
2	270 nV	900 nV	23.1	21.4
64	19 nV	125 nV	22.0	19.2
128	17 nV	110 nV	21.1	18.4

(1) Peak-to-peak noise data are based on direct measurement.

We can calculate these two items:

- Noise-free bits = Log_2 (FSR/peak-to-peak noise) = Log_2(2 × 19.5 mV/ 0.11 µV) = 18.435 bits
- ENOB = Log_2 (FSR/RMS noise) = Log_2(2 × 19.5 mV/17 nV)= 21.1295 bits

Thus, we can see that the data are same as that presented in the ADS1232 product data sheet.

Additionally, when we test the RTI noise of the ADC, we must allow a zero input at the analog input of a ΔΣ ADC; the digital output words are then collected, as illustrated in Figure 3. These codes come from the ADS1232EVM, with the PGA = 1 and data rate = 80 SPS. Noise is measured as the variability of the output at a constant input.

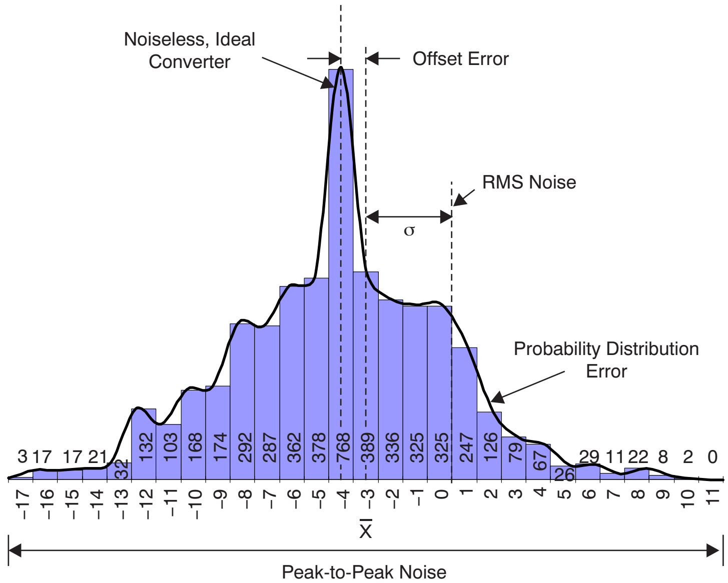


Figure 3. ADC Noise Histogram

We can get the mean and variance from a lot of output codes, as Figure 3 shows, and the mean is the average value, which is the same as the offset error. The variance describes the variability of the distribution about the mean; and the standard deviation is the square root of the variance, which is a measurement of the RMS noise. Based on the information in Figure 3, we can calculate the following RTI noise performance:

- Peak-to-peak noise = 8.34 μV
- Noise-free bits = 19.19 bits
- RMS noise = 1.24 μV and ENOB = 21.94 bits

Peak-to-peak noise can be determined from the RMS noise value. For random noise, the peak-to-peak noise = 6.6 × RMS noise. The noise-free bit value is equal to (ENOB – 2.7224). (For more information, see Ref 4.)

3 System Budget

3.1 Accuracy

An important distinction must be made between resolution and accuracy before we proceed. Having more resolution does not necessarily produce more accuracy. Accuracy and resolution are not the same, though these parameters can be measured in the same units. Resolution is similar to sensitivity; it is the smallest possible change of a given parameter that can be detected. Accuracy, on the other hand, is a deviation between the measured and the factual value. In other words, accuracy can be described as the maximum operating error that can be expected under worst-case conditions. Accuracy can be read repeatably and reliably.

Example: Design a weigh scale with the following load cell parameters:

- Maximum weight: 5 kg
- External counts: 5,000
- Load-cell maximum: 10 kg
- Load-cell sensitivity: 2 mV/V
- Internal counts = 50,000
- Supply voltage: 5 V

Calculation:

Load cell output at maximum weight:

= Supply voltage × Load cell sensitivity × (Weigh Scale Max /Load Cell Max)

= 5 mV

To account for the loss of dynamic range resulting from the mismatch between the ADC and the load cell, then one needs additional discussion:

$$\text{Log}_2 \text{ (ADC full-scale input / load cell full-scale input)} \quad (2)$$

Assuming a typical full-scale input of ±20 mV, one would need an additional 3 bits ($\log_2$ [40/5]).

50,000 noise-free internal counts are equivalent to $\log_2$ (50,000) = 15.6 noise-free bits.

To summarize, then, the ADC must have 3 + 15.6 = 18.6 bits of noise-free resolution at ±20-mV input full-scale.

We can then check the noise performance table (vs gain/data rate) in the product data sheet to confirm whether the ΔΣ ADC can meet the demands of this application.

3.2 Linearity

Integral nonlinearity is the difference between the ideal and measured code transition levels after correcting for static gain error and offset error. Integral nonlinearity is usually expressed as percentages of full-scale (% F_S) or in units of LSBs.

If the maximum Integral nonlinearity (INL) of one ΔΣ ADC is 2 ppm of FSR (that is, 0.0002% of the full-scale range); in other words, an LSB of 18.932 bits [$\log_2$ (2 ppm × 2^{24}) = 5.068 bits].

In the example given earlier, the MCU does not need to perform the nonlinearity compensation. If the LSB value of INL is less than 18.6, then MCU must perform the compensation in code. In practice, the nonlinearity bottleneck is the linearity of the bridge sensor, not the INL of the ADC.

3.3 Normal-Mode and Common-Mode Rejection

3.3.1 Normal-Mode Rejection (50-Hz/60-Hz Interference)

In a traditional bridge sensor, the critical system requirement is a low-pass filter (LPF) to remove noise and 50-Hz/60-Hz interference. Assuming a 3-dB signal bandwidth of 10 Hz, the filter should be down at least 60 dB at 50 Hz: a challenging filter design, to put it lightly. At the very least, we must implement a fifth-order low-pass filter.

In most contemporary ΔΣ ADCs, there is a digital filter, such as Sinc(x), which can act as a 50-Hz/60-Hz notch filter to reject one powerline frequency; or, we can attenuate both 50-Hz/60-Hz frequencies simultaneously. Usually, you must check the rejection of 50 Hz ±1 Hz and/or 60Hz ±1 Hz, because the powerline frequency changes very slowly within the 50-Hz/60-Hz (±1 Hz) range. An example of the rejection at harmonics of these frequencies for the ADS1232 is shown in Figure 4. It is clear that the rejection is greater than 120 dB, enough for the bridge sensor application.

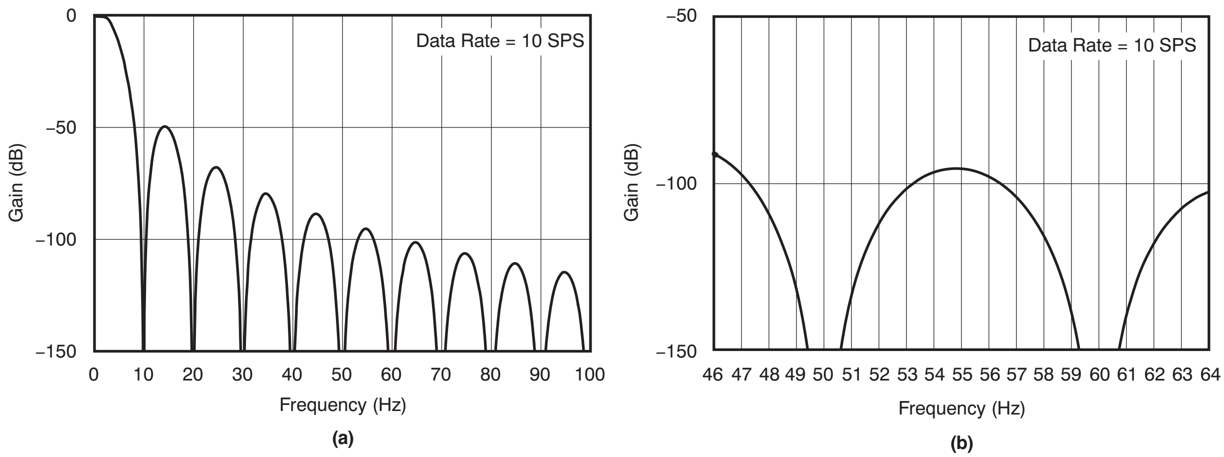


Figure 4. ADS1232 50-Hz/60-Hz Rejection

Normal-mode rejection (given in the data sheet, as Table 2 shows) indicates this performance, which notes that the attenuation to the 50-Hz/60-Hz signal comes from the analog input channel as the differential signal.

Table 2. Normal-Mode and Common-Mode Rejection Specifications (ADS1232)

Parameter	Conditions	Min	Typ	Max	Units
Normal-mode rejection	Internal oscillator, f_{DATA} = 10 SPS f_{IN} = 50 Hz or 60 Hz, ±1 Hz	100	110		dB
	External oscillator, f_{DATA} = 10 SPS f_{IN} = 50 Hz or 60 Hz, ±1 Hz	120	130		dB
Common-mode rejection	at dc, Gain = 1, ΔV = 1 V	95	110		dB
	at dc, Gain = 128, ΔV = 0.1 V	95	110		dB

The output data rate and frequency of the filter are functions of the modulator frequency, decimation ratio, and filter order. The modulator frequency is a function of the ΔΣ ADC clock. We must also attend to the clock tolerance effect on the 50-Hz/60-Hz rejection performance. When selecting a data rate, we must take care to ensure there is also sufficient rejection at harmonics of the main frequency interference, and any inaccuracies in the clock frequency are considered.

3.3.2 Common-Mode Rejection

If the 50-Hz/60-Hz rejection acts as a common-mode signal on the input of analog input channel, you may need to check the graph of representative common-mode rejection data at 50-Hz/60-Hz in the data sheet, or you test it yourself if the data sheet does not mention it.

In our previous example, it is acceptable if the 50-Hz/60-Hz rejection can exceed 100 dB. The dc common-mode voltage results in an offset voltage, which depends on this common-mode rejection. Most ADCs available now have an offset calibration function that easily cancels this effect.

3.4 Offset and Gain Error

In most ΔΣ ADCs, it is easy to add some calibration features inside for the specific ΔΣ architecture. Such features are usually high-quality, digitally intensive capabilities (such as self-calibration, system calibration, and so forth). When performing a calibration, the analog input pins are disconnected within the ADC, and the appropriate signal is applied internally to perform the calibration. The worst-case error is given in Equation 3.

$$\text{Worst- case error} = (\text{maximum gain error} + \text{maximum gain drift} \times T) \times FSR + \text{maximum offset error} + \text{maximum offset drift} \times T \quad (3)$$

Where:

- T = The temperature changing range from 25°C of the device under test.

In general, most ΔΣ ADCs have a system offset error calibration, and it is easy to perform the gain error calibration in code.

Then, the main error is from the offset and gain error drift, as described by Equation 4:

$$\text{Error} = \text{Maximum gain drift} \times T \times FSR + \text{Max offset drift} \times T \quad (4)$$

For example, in a typical weigh scale (1/3000 system accuracy) application, the offset drift error is within 0.5 μV per 5 degrees. The gain drift error is within 1σ per 20 degrees.

4 Summary

Based on the above discussion, you can now determine the key specification calculations for the requirements of a specific system, and your design for a bridge sensor application is now much easier to complete.

5 References

These documents are available for download from the TI website except where indicated.

1. ADS1232/ADS1234 Product data sheet. Literature number SBAS350F.
2. ADS1248 Product data sheet. Literature number SBAS426E.
3. Oljaca, M. and Hendrick, T. (2003). Combining the ADS1202 with an FPGA digital filter for current measurement in motor control applications. Application report. Literature number SBAA094.
4. Institute of Electrical and Electronics Engineers, Inc. (2001). IEEE STD-1241-2000: IEEE Standard for Terminology and Test Methods for Analog-to-Digital Converters. Available at IEEE.org.