Application Report
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Using the AMC1210 in Resolver Motor Control Systems

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ABSTRACT

Resolver motor control systems typically have used either closed-loop Resolver-to-Digital Converters (RDCs) or open-loop Analog-to-Digital Converters (ADCs) to obtain position and velocity data from the resolver outputs. Texas Instruments has developed a new method of resolver decoding using the dual delta-sigma modulator ADS1205 and the AMC1210, a digital filter device designed specifically for use in motor control applications. This technique uses the flexibility of the AMC1210 by providing a carrier signal and digital demodulation of a constant bitstream supplied by the ADS1205. This solution provides 16-bit demodulated data for angle calculations to the microcontroller at a higher speed and lower cost than typical 16-bit systems.

Contents

List of Figures

1 Overview

Resolvers require an input signal to serve as a reference, or a carrier, for the two output signals. This signal is usually a sine wave with a frequency from 4kHz to 20kHz. The input carrier signal is often magnetically coupled to a coil on the rotor of the motor, providing a reliable brushless connection. The carrier signal is then coupled into two orthogonally-placed coils on the stator, generating two AM-modulated signals. One of these signals represents the sine of the angle of the motor, and the other represents the cosine. These output signals can then be analyzed to determine the velocity and position of the motor.

Previous approaches to this decoding process involved a feedback circuit, in which resolution and bandwidth must be compromised to achieve stability. The combination of the ADS1205 and the AMC1210 demodulates both Output 1 and Output 2, and leaves the calculations to the microcontroller/DSP in the application, removing the resolution/bandwidth tradeoff necessary in other methods. See Figure 1.

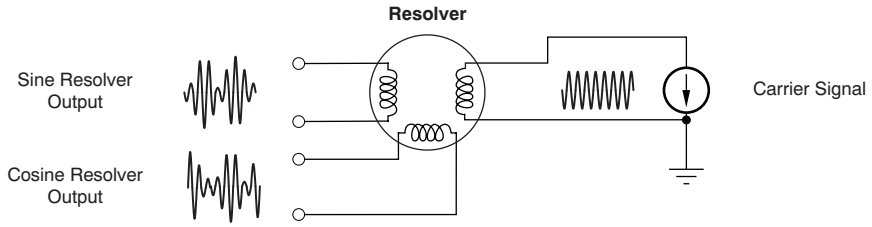

Figure 1. Basic Resolver Diagram (with Associated Signals)

The two outputs of the resolver can be fed directly to the ADS1205. The ADS1205 is a 10MHz, 2nd-order delta-sigma modulator capable of accurate resolutions up to 16 bits. Delta-sigma (ΔΣ) modulators output a bitstream that has a ratio of 0s to 1s that is proportional to the input voltage. By digitally filtering these bitstreams, a digital word can be generated that represents the input voltage. The ADS1205 outputs can be fed directly to two of the AMC1210 inputs in order to perform the digital filtering. See Figure 2.

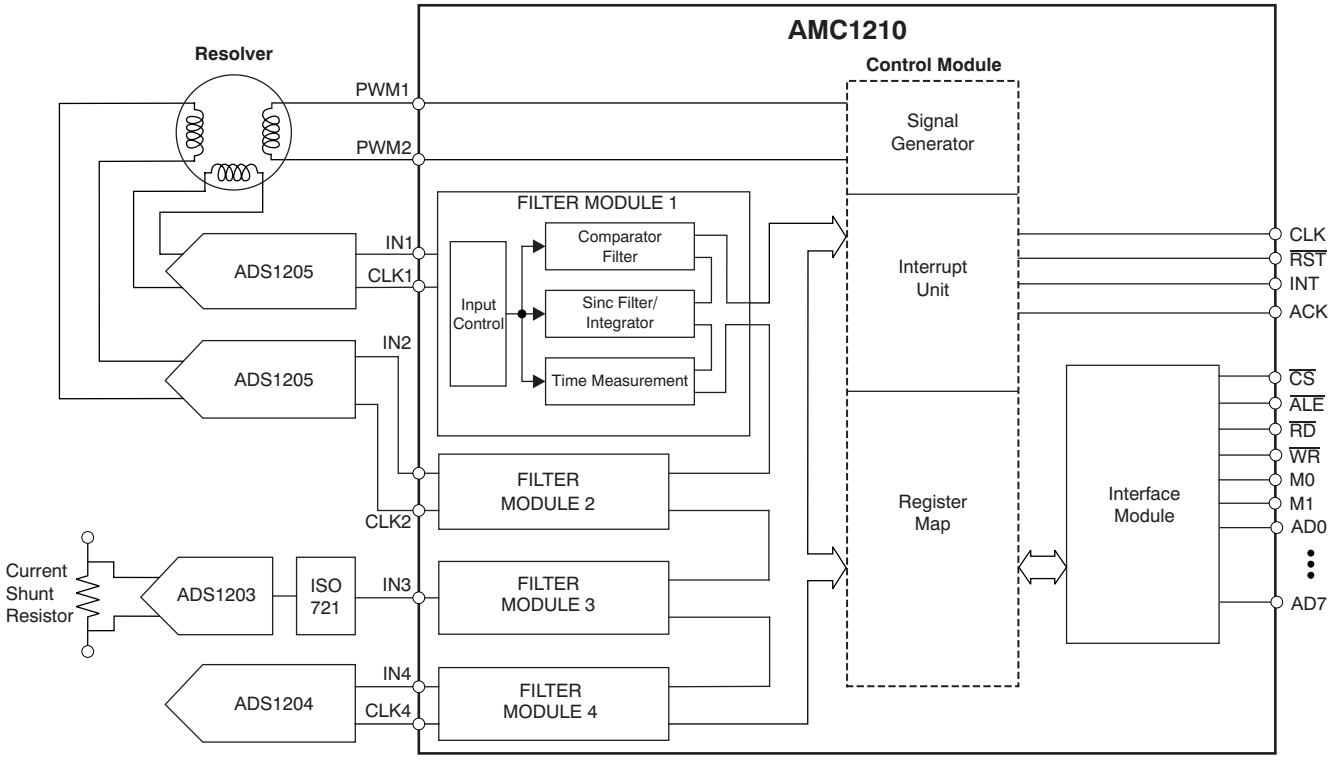

Figure 2. AMC1210 Block Diagram

After the bitstream is digitally filtered by the AMC1210, the signal is then demodulated using the demodulator and integrator units. The demodulator synchronously rectifies the digital signal with the carrier frequency. Next, the integrator–when programmed correctly–digitally integrates half-cycles of the carrier frequency, effectively filtering the modulator signal from the motor signal. The corresponding outputs can then be read by the microprocessor.

Figure 3 shows the sequence of signals and the corresponding circuit block.

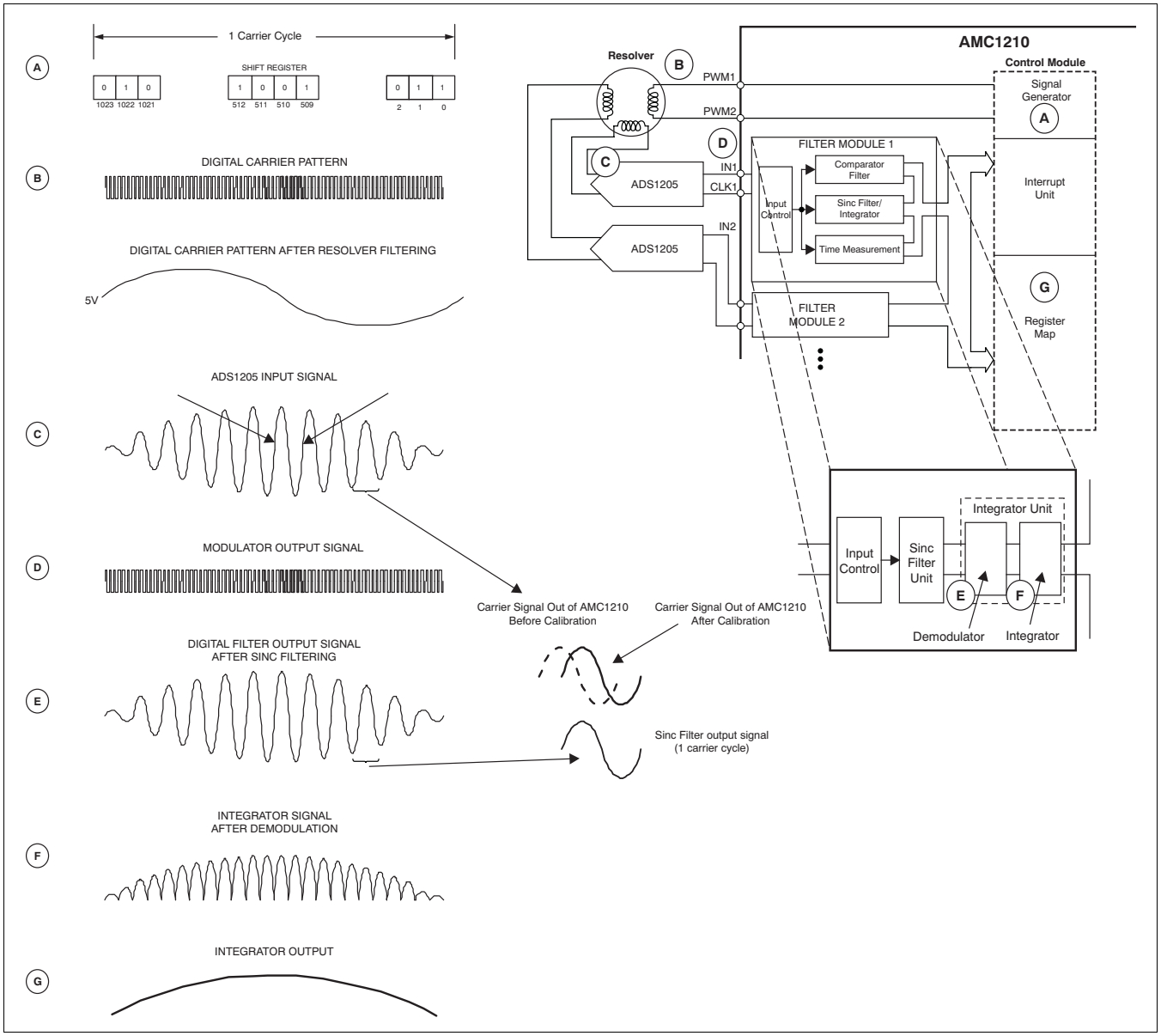

Figure 3. AMC1210 Signal Processing Sequence

2 Calculating System Parameters

The AMC1210 can be configured in a variety of ways. Each filter module contains its own sinc filter, timer, window comparator, demodulator and integrator unit, each with individually programmable parameters. This section uses software written in MATLAB® to calculate and verify that the system parameters are correct and generate valid results.

All parameters depend on the system timing and clocks. The user must first establish the desired motor control loop frequency. This frequency is the rate at which the control system updates the motor driving circuitry, and is typically around 8kHz. A common application synchronizes the carrier frequency with the motor control loop frequency. For the examples in this application note, it is assumed that the motor control loop frequency is the same as the carrier frequency; both will be set to 8kHz.

3 Using Delta-Sigma Modulation for Carrier Signal Generation

Note: For a more detailed description of delta-sigma modulator operation, see TI application note SBAA094, *Combining the ADS1202 with an FPGA Digital Filter for Current Measurement in Motor Control Applications*.

The signal generator unit in the AMC1210 can create the carrier frequency for a resolver. The signal generator is primarily composed of a digital shift register with a maximum length of 1024. A pattern can be loaded into the shift register that represents one cycle of the carrier signal. This pattern is output on the pins PWM1 and PWM2 as a differential digital signal. A pattern must be generated that, when filtered by the resolver input coils, provides a smooth analog carrier frequency because the outputs of pins PWM1 and PWM2 are digital. It is recommended that this pattern be generated using a delta-sigma modulation algorithm. The length of the pattern is set by the bits PC0–9 in the Control Register. Details for loading the pattern are addressed in Section 6.

The first graph of Figure 4 shows a single cycle of the desired analog waveform. The frequency is determined by the clock speed, signal length, and clock divider ratio. (These parameters are discussed in Section 4.) The second graph in Figure 4 shows the digital carrier pattern output at the PWM1 pin before any filtering occurs. This graph shows a high density of 1s when the analog signal is high, an even density of 1s and 0s when the signal is around midscale, and a high density of 0s when the signal is low. This pattern was generated using a 2nd-order, delta-sigma modulator algorithm that simulates the ADS1205. Delta-sigma modulation quantizes the original signal into a binary pattern that effectively pushes the quantization noise into higher frequency ranges. The original analog signal can then be recovered by filtering the high-frequency noise. In this application, the resolver coil and output impedance of the driver pins serve as a low-pass filter, removing the quantization noise from the modulated signal.

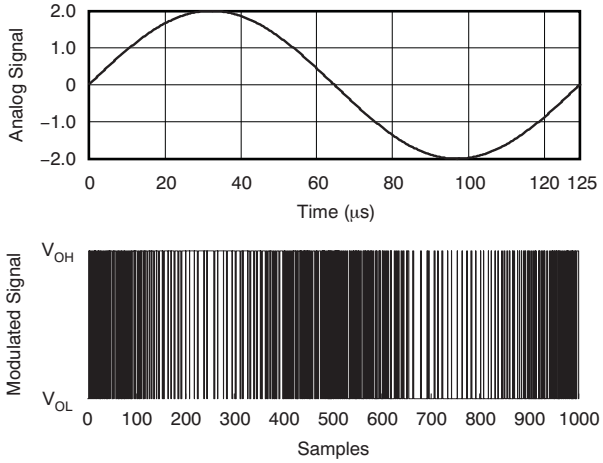

Figure 4. Analog Input Signal and Corresponding Delta-Sigma Modulator Output

Figure 5 shows the power spectral density (PSD) of a simulated ADS1205 (2nd-order, delta-sigma modulator) sine wave output. The analog input sine wave is 8kHz, and the modulator sampling rate is 8MHz.

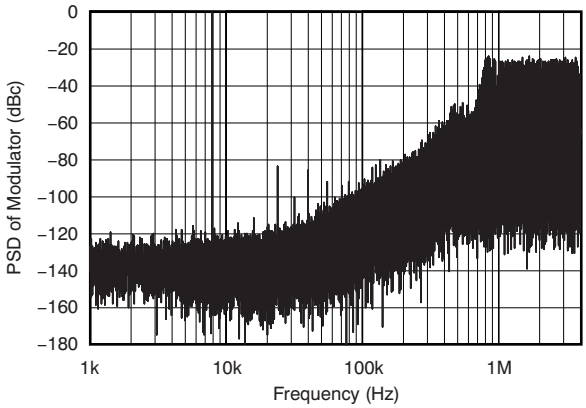

Figure 5. Power Spectral Density of a Delta-Sigma Modulator Signal

In Figure 5, the bulk of the noise gets pushed into frequencies above 10kHz. Increasing the data rate pushes the noise into a higher frequency range, thereby making a low-pass filter more effective. For this reason, it makes sense to run the digital carrier data frequency as fast as possible.

Figure 6 shows several cycles of the modulator signal presented in Section 4 when passed through a first- and second-order Butterworth (RC) filter with a cutoff (–3dB) frequency at 10kHz. The amount of filtering that occurs depends on the resolver coil impedance. Additional passive circuitry can be added to increase the filtering effect; however, increases will come at the expense of signal amplitude.

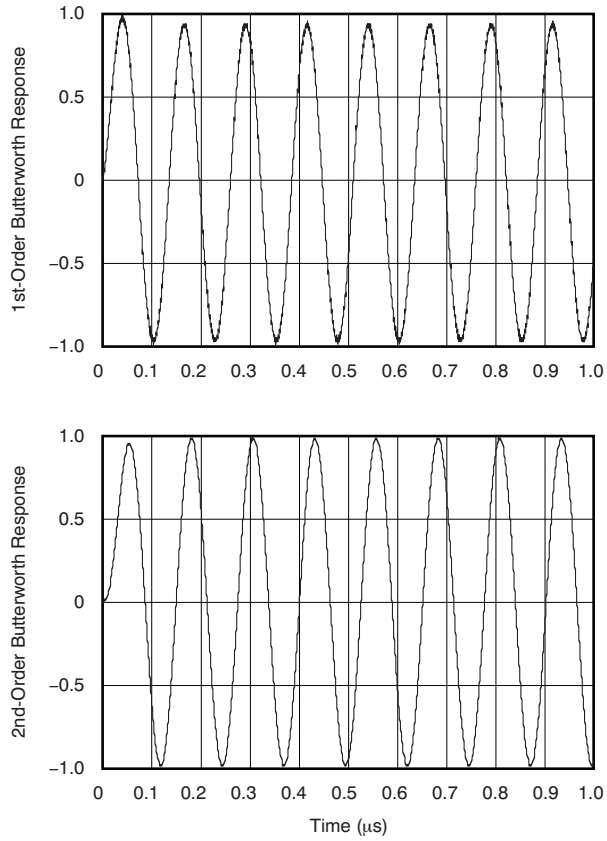

Figure 6. Filtered Modulator Signal

4 Deriving Carrier Signal Parameters

The carrier frequency can be calculated from Equation 1:

$$f_{CARRIER} = \frac{f_{CLK}}{(N_{CDIV} \cdot N_{PAT})} \quad (1)$$

where:

- $f_{CARRIER}$ is the carrier frequency for the resolver stator
- f_{CLK} is the master clock frequency
- N_{CDIV} is the clock divider parameter, programmed by bits SD3–SDO0 in the Clock Divider Register
- N_{PAT} is the length of the pattern, programmed by bits PC9–PC0 in the Control Register

Equation 1 shows that the carrier frequency depends on both the clock frequency and the programmed values of N_{CDIV} and N_{PAT}. This dependence means that only certain carrier frequencies can be achieved for any given master clock frequency. The N_{CDIV} variable can divide down the master clock frequency by any integer value from 1 to 16, and the N_{PAT} variable can hold any value from 1 to 1024. However, as mentioned in Section 3, it is desirable to run the digital carrier pattern as fast as possible. To achieve this fast operation, a single cycle of the carrier frequency should use as much of the pattern length as feasible, thereby making N_{PAT} as close to the maximum 1024 as can be tolerated. Consideration must be taken when designing the system to be sure that the clock frequency is an integer multiple of the carrier frequency needed.

For the example discussed in this application report, these variables will be set to the following values:

- $f_{CARRIER}$ = 8kHz
- f_{CLK} = 32MHz
- N_{CDIV} = 4
- N_{PAT}= 1000

These values satisfy the conditions for Equation 1. Note that the values N_{PAT} = 500 and N_{CDIV} = 8 would have still satisfied Equation 1; however, the digital carrier pattern bit rate would have decreased by 2, resulting in a decreased filtering effect from the resolver.

5 Deriving Filter Module Parameters

As mentioned previously, the resolver outputs an AM signal where the position of the motor is given by the envelope of the sine and cosine outputs. To interface with the ADS1205, a DC bias must be added to center the AM signals in the middle of the ADS1205 input signal range. This additional bias is easily accomplished by unity-gain buffering the reference output of the ADS1205, and decoupling the reference voltage signals with 5kΩ resistors. See Figure 7 for the schematic.

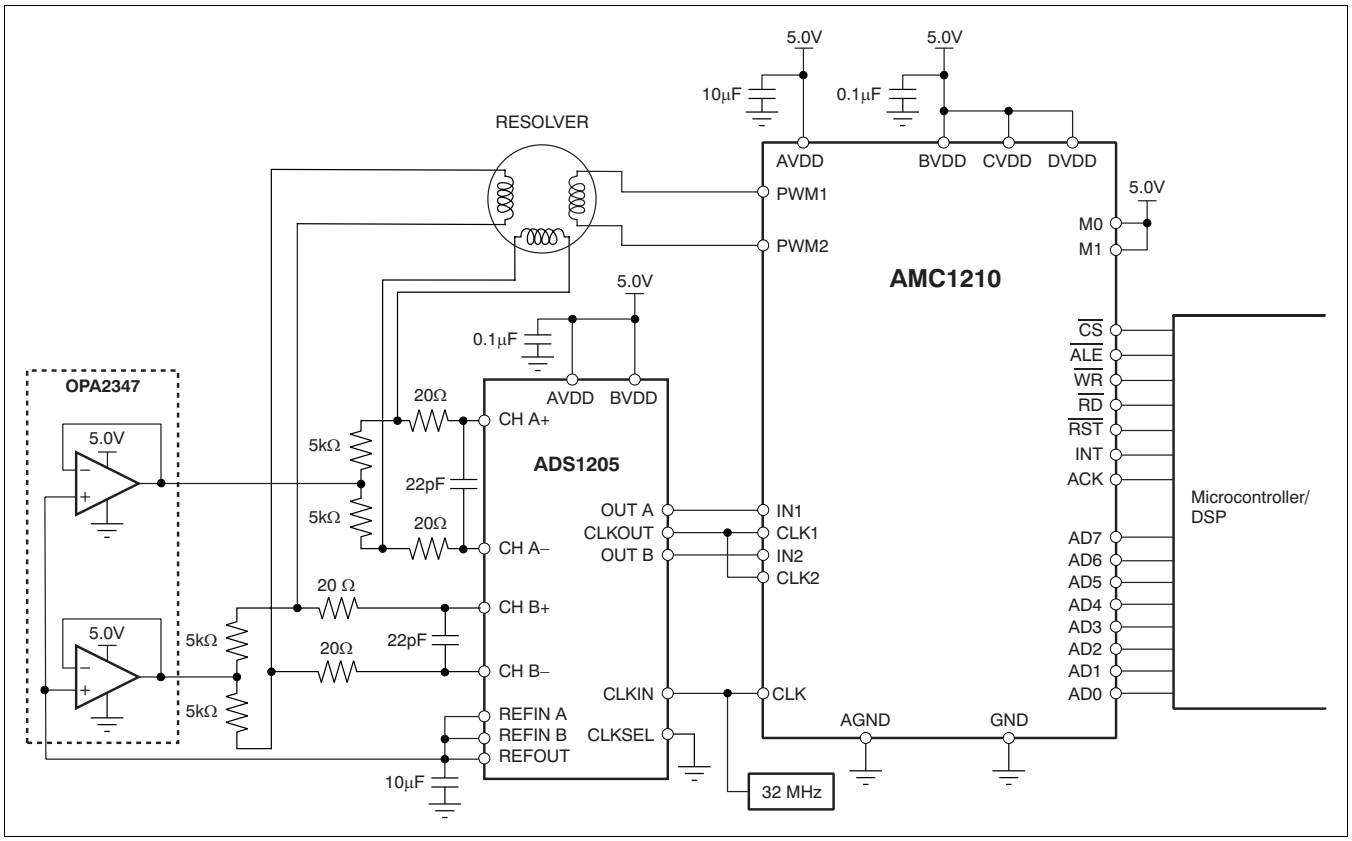

Figure 7. Typical Schematic for Resolver Application

It is recommended that the ADS1205 be driven from the same clock source as the master clock for the AMC1210, if the master clock frequency is less than 32MHz. The modulator rate of the ADS1205 will be half of the clock input rate in external clock mode (pin CLKSEL = 0). The ADS1205 performance is only rated up to 16MHz; therefore, if the AMC1210 master clock rate is greater than 32MHz, a different clock scheme needs to be implemented. In this case, the AMC1210 can drive the ADS1205 clock with the CLKx pin (***x*** = 1–4) . To accomplish this operation, the input mode needs to be set to 3 (Bits [MOD1,MOD0] = [1,1] in the Control Parameter Register). In this mode, the AMC1210 filter module is driven by the external clock. The external clock can then be divided down by any integer number from 1–8, set by bits MD2–MD0 in the Clock Divider Register. This divided clock then drives both the filter module and the ADS1205. The bit CD in the Control Parameter Register also needs to be set to '1', allowing the CLKx pin to become an output.

The example application discussed in this document assumes a 32MHz clock fed directly to both the AMC1210 and ADS1205, giving a modulator rate of 16MHz. It is recommended that the modulator run at the highest rate feasible, to allow a higher oversampling ratio and therefore increased resolution.

Once clock frequencies have been chosen, the oversampling ratios must be determined. The oversampling ratio for the sinc filter (called SOSR) determines both the speed and resolution of the data coming out of the Sinc Filter unit. Figure 8 shows the AMC1205 modulator data after it becomes integrated and decimated through a Sinc^3 filter, with varying values of SOSR.

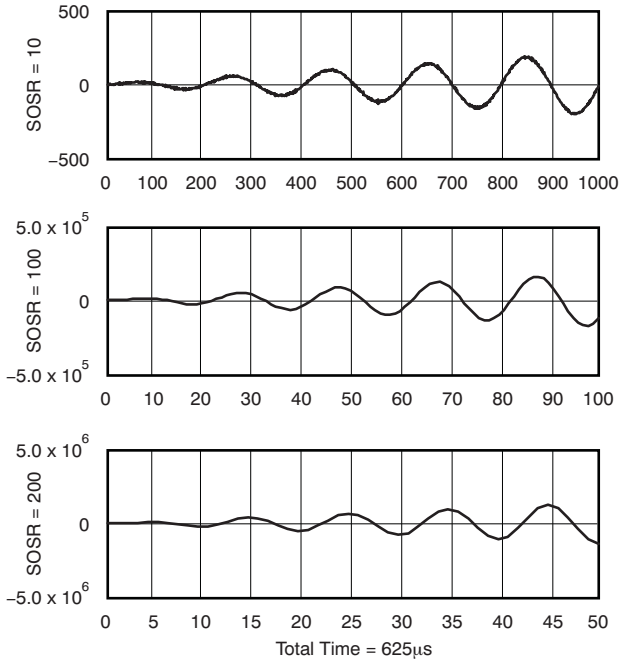

Figure 8. Filtered Modulator Signal with Various Values of SOSR

It is important to note that Figure 8 represents five cycles of an 8kHz carrier signal. This data was filtered from a modulator with a 16MHz data rate. The output data rate of each different configuration is given by Equation 2:

$$f_{SINCDATA} = \frac{f_{MODULATOR}}{SOSR} \quad (2)$$

For a total time window of 625µs, 1000 samples of a filter setup with an SOSR = 10 occur. Likewise, only 50 samples of a filter with an SOSR = 200 are output. Note, however, that the amplitude of the signal increases, giving an increased SOSR value. The total amplitude represents the resolution of the signal; therefore, if a signal is represented by integer values between –500 and +500, its resolution is significantly lower than if that same signal is represented by an amplitude of –5M to +5M.

The data is decimated in a similar manner by the Integrator unit. The Integrator unit, when configured in Oversampling Mode (bit IMOD = 0 in the Integrator Parameter Register), sums a preset number of samples and generates the answer after each summation in the Data Register. The number of samples that the integrator sums is determined by the value IOSR, and can be set from 1 to 128 by bits IOSR6–IOSR0 in the Integrator Parameter Register. The relationship in Equation 3 must be configured to set the correct IOSR.

$$\frac{f_{MODULATOR}}{f_{CARRIER}} = \frac{SOSR \cdot ISOR}{N} \quad (3)$$

where:

- $f_{MODULATOR}$ is the modulator rate of the ADS1205
- $f_{CARRIER}$ is the carrier frequency
- SOSR is the oversampling ratio of the Sinc filter
- IOSR is the oversampling ratio of the Integrator
- N is the number of carrier cycles that the integrator averages. This number can be any integer multiple of 0.5 (that is, 0.5, 1.0, 1.5 and so on).

The combination of SOSR, IOSR and N determine the frequency of the AMC1210 output data. In the case where N = 1, the data coming out of the AMC1210 should equal the carrier frequency. If N = 0.5, the integrator would then sum every half of a carrier cycle, and the output rate would double. This relationship is described in Equation 4:

$$f_{DATA\_OUT} = \frac{f_{MODULATOR}}{SOSR \cdot IOSR \cdot N} \quad (4)$$

where:

- f_{DATA_OUT} is the rate at which data from the integrator is refreshed

A common application averages over one cycle of the carrier signal (N = 1). When placed in Equation 3, we get the following result:

$$\frac{f_{MODULATOR}}{f_{DATA\_OUT}} = SOSR \cdot ISOR = 2000 \quad (5)$$

A value for SOSR must be chosen to achieve the desired resolution from the modulator. Figure 9 shows the effective number of bits (ENOB) versus OSR for the ADS1205.

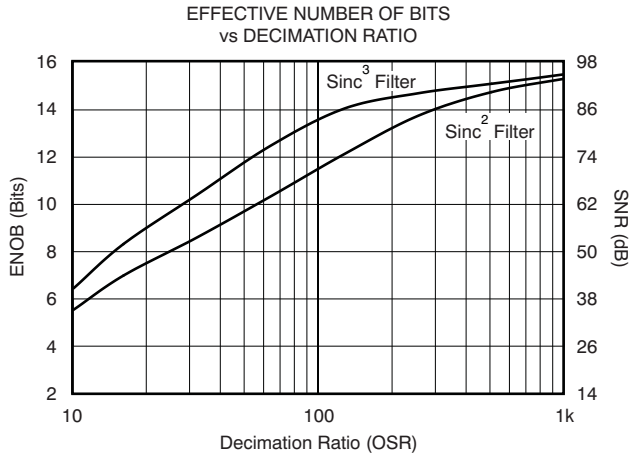

Figure 9. ADS1205 ENOB vs OSR Performance

From Figure 9, it makes sense to choose a $Sinc^3$ filter with a high SOSR to achieve the maximum possible ENOB. Note that the increase in ENOB drops off after an SOSR of 120, therefore making an SOSR = 125 a good option. This value then gives Equation 6:

$$IOSR = \frac{2000}{SOSR} = 16 \quad (6)$$

Now all the parameters necessary to program the AMC1210 have been established.

To review, the configuration defined in this paper has the following parameters:

- f_{CLK} = 32MHz (master clock frequency)
- $f_{CARRIER}$ = 8kHz (frequency of resolver input [carrier] signal)
- N_{CDIV} = 4 (clock divider for signal generator output)
- N_{PAT}= 1000 (length of signal generator pattern)
- SOSR = 125 (sinc filter decimation ratio)
- IOSR = 16 (integrator decimation ratio)

Table 1 gives an overview of the register map and the values that need to be set in each register to configure the device as described here. This configuration applies to Filter Module 1. The same values should be repeated for the other selected Filter Module. Refer to the AMC1210 data sheet for a more detailed description of each bit in the register map.

Table 1. AMC1210 Programmed Register Map

Address	Programmed Value (Hex)	Register Description	Programmed Bits
0x00	Output	Interrupt Register	
0x01	0x0000	Control Parameter Register for Filter Module 1	CD = '0' SHS = '0' TM = N/A MOD1-0 = '00'
0x02	0x0F7C	Sinc Filter Parameter Register for Filter Module 1	SST = '11' AE = '1' FEN = '1' SOSR7-0 = '01111100'
0x03	0x070F	Integrator Parameter Register for Filter Module 1	SH4-0 = N/A(1) DR = '1'(1) DEN = '1' IEN = '1' IMOD = '0' IOSR6-0 = '0001111'
0x04	–	High-level Threshold Register for Filter Module 1	
0x05	–	Low-level Threshold Register for Filter Module 1	
0x06	–	Comparator Parameter Register for Filter Module 1	
0x19	0x03E7	Control Register	PC9–0 = '1111100111'
0x1A	0x0XXX(2)	Pattern Register	SP15–0 = 'XXXXXXXXXXXXXXX'(2)
0x1B	0x1403	Clock Divider Register	HBE = '1' MFE = '1' SGE = '1' PCAL = '0'(3) SCS1 = '00' MD2–0 = '000' SD3–0 = '0011'
0x1C	Output	Status Register	
0x1D	Output	Data Register for Filter Unit 1	
0x1E	Output	Time Register for Filter Unit 1	

(1) Output bits. The programmed value does not affect the state of these bits.
(2) These bits are programmed at start-up according to the generated signal pattern data.
(3) This bit should be set to '1' when performing calibration. It will return a '0' if calibration was successful.

6 Loading the Carrier Pattern

The carrier pattern must be loaded into the AMC1210 correctly for the signal generator to function properly. MATLAB and DOS software is available on the web to generate a delta-sigma modulated sine wave to be used as the carrier signal pattern. The software will take a total pattern length as an input (PC_VAL) and output 64 16-bit words. The words represent a modulator pattern PC_VAL bits long, and zeroes for the remaining bits. The 64 words should be loaded into the AMC1210, one word at a time, starting with the first word. A write to the Pattern Register (bits SP15–SP0) must be performed for each 16-bit word until the entire pattern is loaded.

Figure 10 shows the proper procedures to follow to load the pattern correctly.

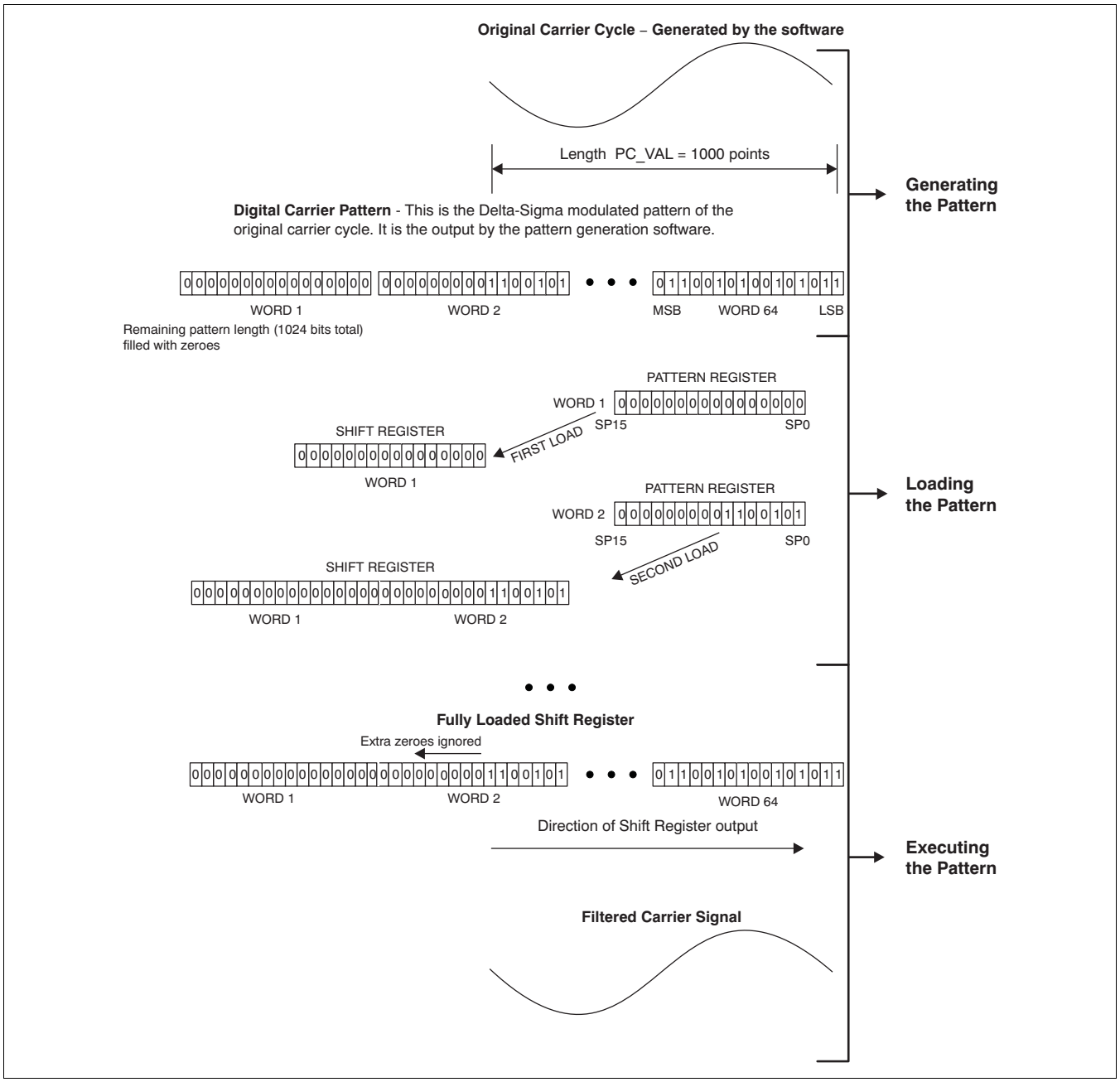

Figure 10. Loading the Pattern Register

7 Calibrating the AMC1210

An undetermined amount of phase shift occurs between the output of the PWM1/2 pins and the filtered delta-sigma modulator signal coming out of the $Sinc^3$ filter. For the demodulation to work properly, these two signals must be in phase with each other. To correct for this phase shift, the AMC1210 has a built-in calibration mechanism. To enable this calibration, the bit PCAL in the Clock Divider Register must be set to '1' while the system is running in a steady-state condition.

The calibration mechanism attempts to align a positive edge zero-crossing on the sinc filtered data with the start of the signal generator pattern. The mechanism assumes that the signal generator pattern is loaded with a single sine wave, in the order described in Section 6. An internal counter counts the number of signal generator clock cycles until the zero-crossing occurs. When the counter finds a zero-crossing, the calibration shifts the start of the signal generator pattern by the corresponding number of clock cycles, and sets bit PCAL to '0' to signal that calibration has occurred.

In addition to performing calibration, the integrators in the sine and cosine channels must be synchronized to each other, so that they are integrating at the same time. Synchronization can be done by setting the bit MFE in the Clock Divider Register to '0', then to '1'. This toggling resets the Sinc filter units, then simultaneously enables them all (assuming the bit FEN is set to '1' for each individual filter). By completing the reset, the integrators will also start simultaneously.

8 16-bit Shift Mode

Some applications may require only 16-bit output for processing. The AMC1210 has an option that allows the user to shift the output data in the integrator such that a specified number of least significant bits are *shifted out*, or removed from the output data, leaving only the most significant bits. For more information, see the ***16-bit Data Shifting*** section in the AMC1210 data sheet.

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