Using the ADSDeSer-50EVM to Deserialize ADS527x 10-bit Data Outputs

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ABSTRACT

The ADSDeSer-50EVM provides an direct means of examining the serialized 10-bit data output from the ADS527x families of serialized low voltage differential signal (LVDS) data converters by deserializing the data and converting to a parallel data port. This application report discusses the process of reading deserialized 10-bit data outputs from the ADS527x family using the ADSDeSer50-EVM. Unless otherwise specified, all references to the ADS527x indicate any member of the ADS5270/71 and ADS5275/76/77 families.

1.1 ADS Output Patterns

The ADSDeSer-50EVM is an evaluation fixture designed to interface to the TI LVDS output data converters with an operating frequency of up to 50MHz and up to eight simultaneous data channels. Since there is no clock embedded, a synchronous clock output is provided separately, along with the eight channels of data.

The ADSDeSer-50EVM was originally developed as a means to deserialize the ADS5270/71 family of 12-bit data converters. One of the design goals for the ADS5275/76/77 family of 10-bit devices was to develop a product group that could use the same deserializer as the 12-bit version. This was accomplished in part by having the 10-bit devices shift out 10 bits of serial data and two pad bits, for a total of 12 bits. The two pad bits are in the LSB positions, and each has a value of zero. This configuration means that the 10-bit output is MSB-justified with respect to the 12 total bits of data. Figure 1-1 shows the two different bit patterns, one from the 12-bit family and one from the 10-bit family of converters.
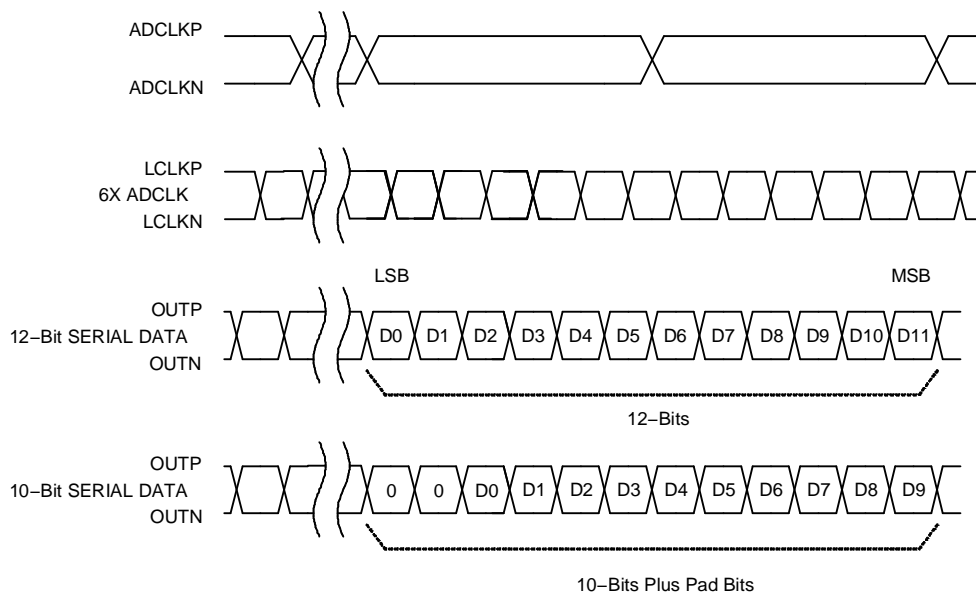

Figure 1-1. 10-Bit and 12-Bit Output Pattern Comparison

When using the ADSDeSer-50EVM (the deserializer) with the 10-bit family of converters, the set-up is the same as that required for the 12-bit converters. The default setting of the ADS527x device output data is LSB first. With the default settings of the ADS527xEVM, the 10 bits appear in the pattern shown in Figure 1-2 on the parallel output pins of the deserializer:
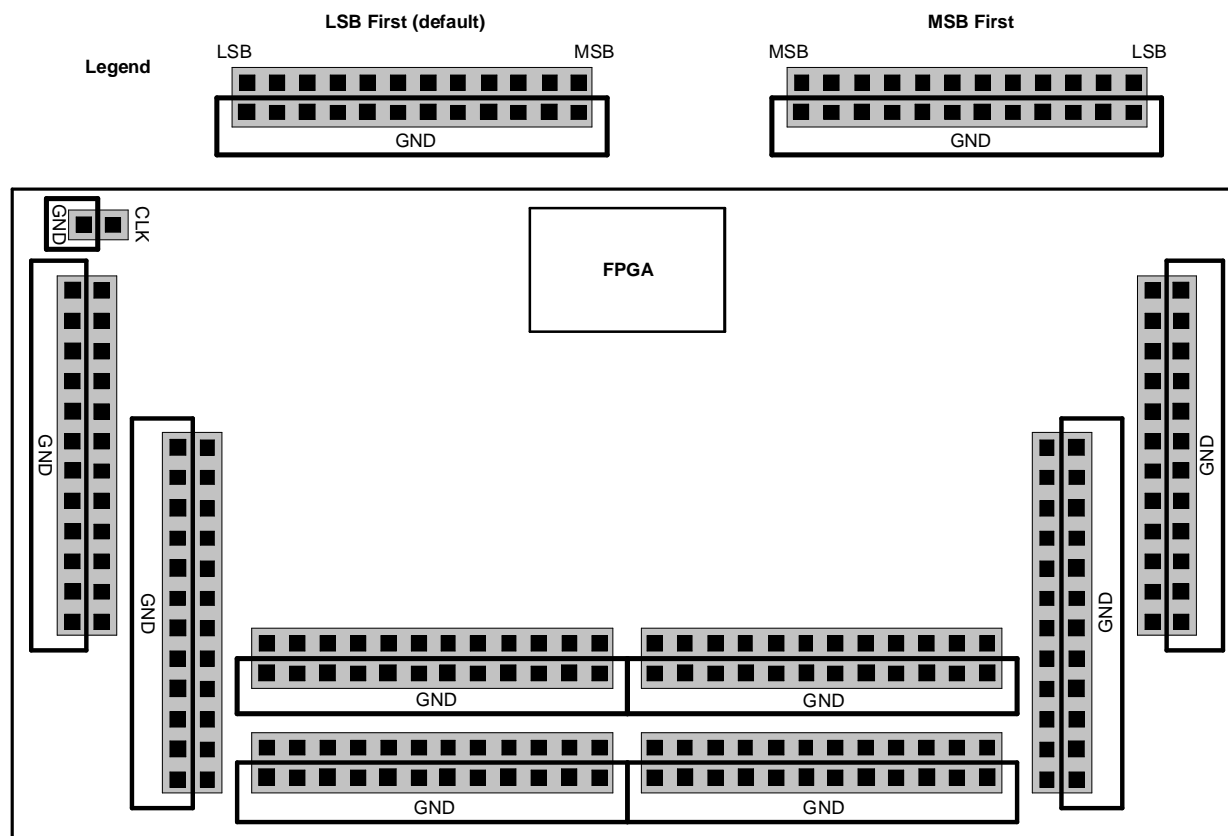

Figure 1-2. 10-Bit Output from ADSDeSer-50EVM

Reading the output data from the ADSDeSer-50 while it is connected to a 10-bit device is fairly straightforward. Confusion occurs when one decides to output data MSB first. When using the MSB first option, data is output MSB first instead of the default setting of LSB first. This configuration means that the data appearing on the parallel output pins of the deserializer is reversed from the default position. See Figure 1-3 for further clarification.
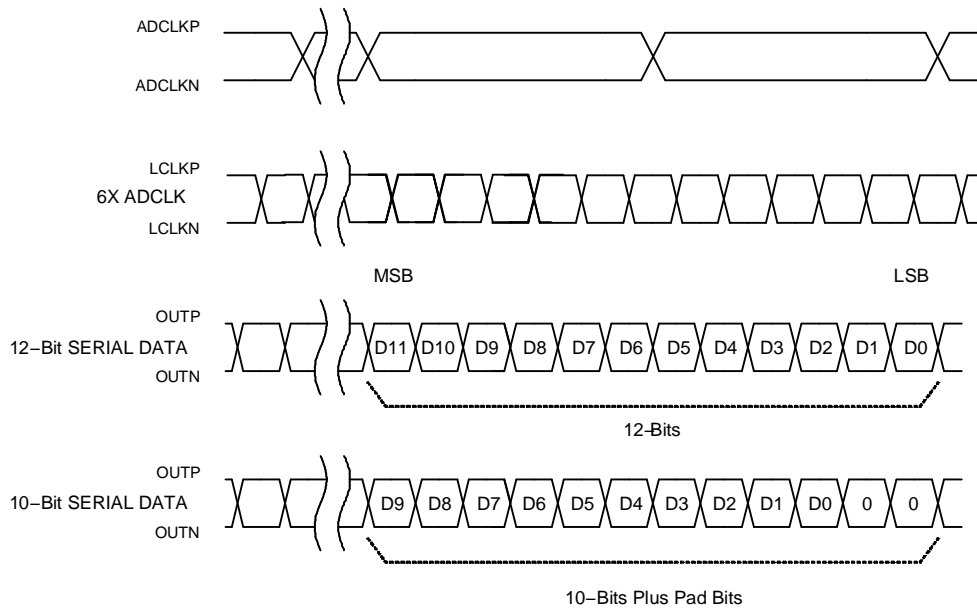
Figure 1-3. Reversed 10-Bit and 12-Bit Deserializer Output Patterns

Even though the order of the output data is reversed, the 10-bit data is still MSB-justified.

Reading 10-bit data with a 12-bit deserializer is a straightforward process when the default device settings are used for normal operation. When one deviates from the default settings, however, confusion can occur. Following the procedures described in this application report should eliminate any potential confusion and assist the user with properly reading a10-bit output from the ADS527x.

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