Combining the ADS1202 with an FPGA Digital Filter for Current Measurement in Motor Control Applications

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ABSTRACT

The ADS1202 is a precision, 80dB dynamic range, delta-sigma (ΔΣ) modulator operating from a single +5V supply. The differential inputs are ideal for direct connections to transducers or low-level signals, such as shunt resistors. With the appropriate digital filter and modulator rate, the device can be used to achieve 15-bit analog-to-digital (A/D) conversion with no missing codes. This application report describes how to combine the ADS1202 with appropriate filtering techniques for current measurement in motor control.

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Introduction

This document provides information on the operation and use of the ADS1202 ΔΣ (delta-sigma) modulator and a detailed description of the digital filter design implemented in the Xilinx field programmable gate array (FPGA). The latest information, along with the FPGA files and software, can be found on the Texas Instruments web site at www.ti.com.

For this specific application, the ADS1202 and FPGA communicate with a DSP board via two SPI™ ports. The user-interface software controls graphical display and analysis. The filter configuration and data retrieval are set up by switches directly on the board. A complete description of the hardware and software features of the digital filter implemented in the FPGA for the ADS1202 is given in this application report.

1.2 ADS1202 Description

The ADS1202 is a single-channel, second-order, delta-sigma modulator operating from a single +5V supply, as shown in Figure 1.

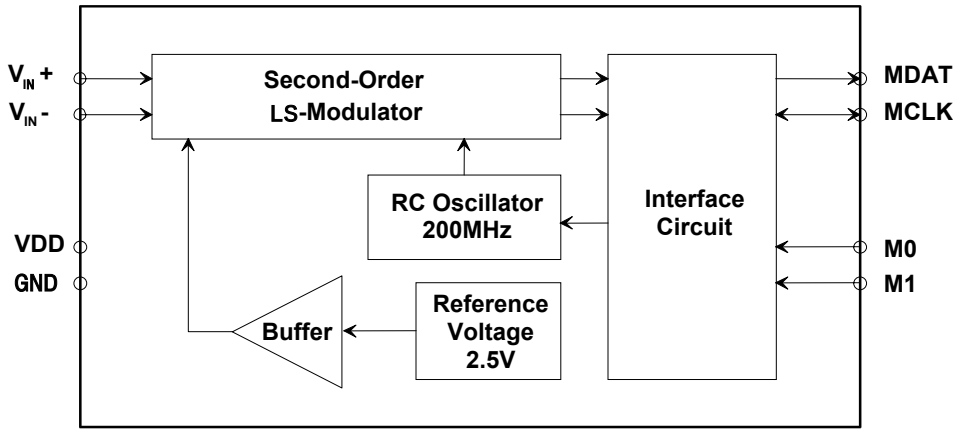


Figure 1. ADS1202 Block Diagram

The delta-sigma modulator converts an analog signal into a digital data stream of 1s and 0s. The 1s density of the output data stream is proportional to the input analog signal. Oversampling and noise shaping are used to reduce the quantization noise in the frequency band of interest. This delta-sigma modulator, with 16-bit performance, can be used with a digital filter for wide dynamic range A/D conversion of up to its full resolution.

The primary purpose of the digital filter is to filter the noise in the signal. The secondary purpose is to convert the 1-bit data stream at high sampling rates into a higher resolution data stream at a lower rate (decimation).

For evaluation purposes, the ASD1202 operates in mode 3. In this mode, input control signals M0 and M1 are HIGH; this disables the internal RC oscillator. Input signal MCLK provides a conversion clock to the modulator. The source for output signal MDAT is the signal arriving directly from the delta-sigma modulator. The MCLK input can have a frequency from 500kHz to 20MHz with a fixed duty cycle around 50%. In this mode, output MDAT is read on every second falling edge of the MCLK input, as shown in Figure 2.

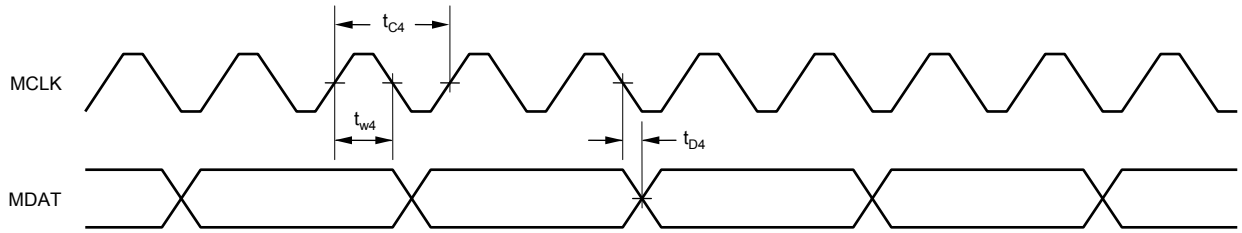


Figure 2. ADS1202 Output Read Operation

The collected output of the modulator is then passed through a digital low-pass filter. The resulting output word is decimated and truncated to the desired data rate and effective resolution, respectively. The combination of the delta-sigma modulator and the digital decimation filter forms a delta-sigma A/D converter. For more detailed information and specifications concerning the ADS1202 modulator, refer to the ADS1202 data sheet (located at www.ti.com).

The MDAT signal is a digitized representation of the analog input. Unlike the MCLK signal, it does not have a fixed frequency or duty cycle. The duty cycle is a function of the input analog signal, as shown in Figure 3.

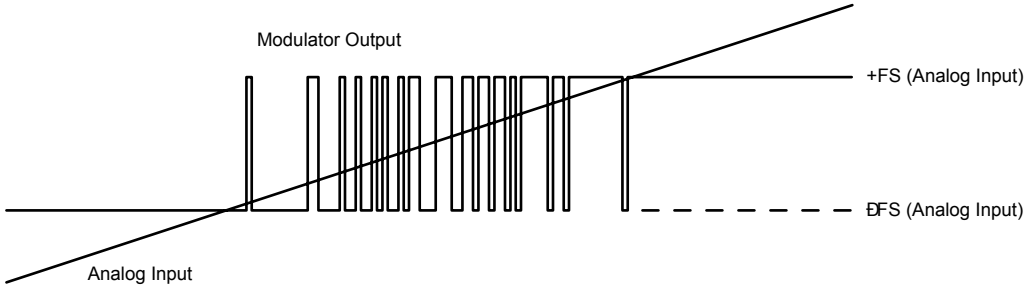


Figure 3. Analog Input versus Modulator Output of the ADS1202

2 ΔΣ Modulator Characteristics

The modulator sampling frequency f_S can operate over a range of a few MHz to 12MHz, when the ADS1202 is in mode 3. The input frequency of MCLK can be adjusted with the clock requirements of the application. The MCLK input must have the double modulator frequency, $2f_S$. When ADS1202 operates in other modes, the modulator sampling frequency f_S has a nominal value of 10MHz and is determined by the internal oscillator.

The modulator topology is a second-order, charge-balancing A/D converter, such as the one conceptualized in Figure 4. The analog input voltage and the output of the 1-bit Digital-to-Analog Converter (DAC) are subtracted, providing an analog voltage at X2 and X3. The voltages at X2 and X3 are then presented to their individual integrators. The output of these integrators progresses in either a negative or a positive direction. When the value of the signal at X4 equals the comparator reference voltage, the output of the comparator switches from negative to positive or positive to negative, depending on its original state. When the output value of the comparator switches from HIGH to LOW or vice-versa, the 1-bit DAC responds on the next clock pulse by changing its analog output voltage at X6, causing the integrators to progress in the opposite direction. The feedback of the modulator to the front end of the integrators forces the value of the integrator output to track the average of the input.

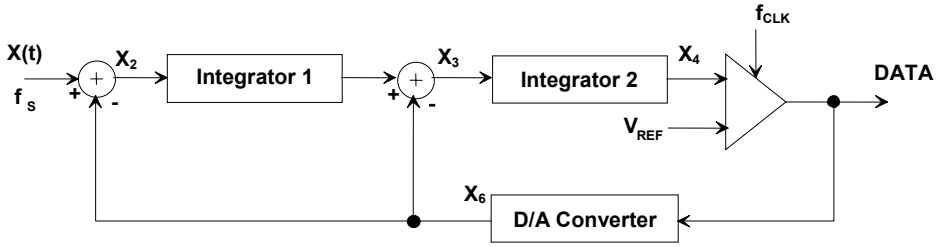


Figure 4. Block Diagram of the 2nd-Order Modulator

The process of converting an analog signal, which has infinite resolution, into a finite range number system introduces an error signal that depends on how the signal is being approximated. The noise transfer function of the delta-sigma modulator can be described by following equation:

$$Q(f) = \frac{V_{LSB}}{\sqrt{12 \cdot f_S}} \cdot \left(2 \cdot \sin \pi \frac{f}{f_S} \right)^K \qquad (1)$$

K represents the implemented order of the delta-sigma modulator. f_S is the sampling frequency, and V_{LSB} is the value of the least significant bit of the converter. Figure 5 presents quantization noise for first- and second-order delta-sigma modulators up to the Nyquist frequency of the modulator.

Digital low-pass filters can remove the high-frequency quantization noise without affecting the input signal characteristics residing in base-band. For both types of modulators, the noise increases with frequency. The greater the order of the modulator, the closer that quantization approaches the Nyquist frequency.

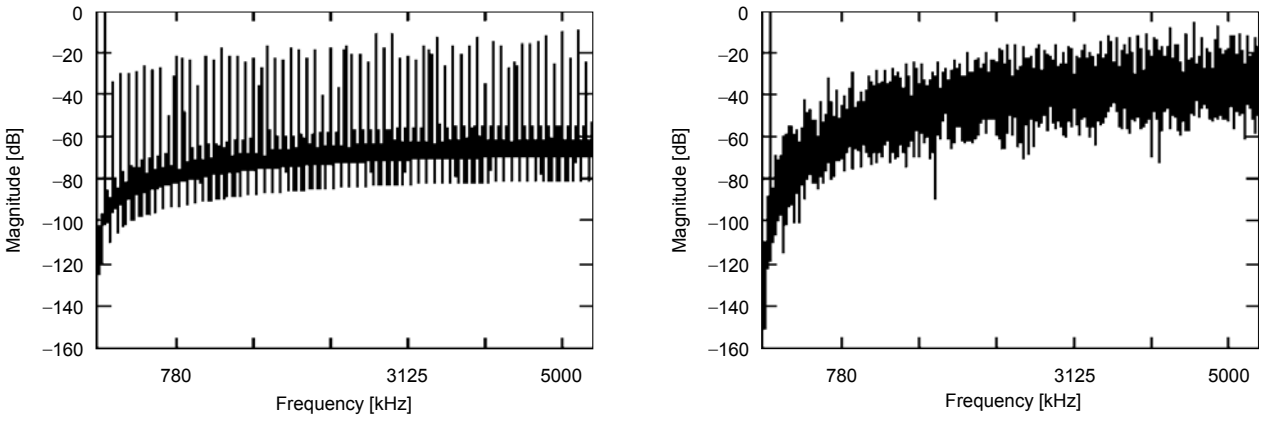


Figure 5. 1st and 2nd Order ΔΣ Modulator Modulation Noise

If we introduce the over-sampling ratio *M*, or a decimation ratio that will be implemented on the output signal from the delta-sigma modulator, the maximum bandwidth of the input signal can be specified as:

$$B = \frac{f_S}{2 \cdot M} \tag{2}$$

The RMS quantization noise present in a bandwidth of interest *B* can now be calculated combining equation 1 and 2:

$$V_{Qe,RMS} = \sqrt{2 \cdot \int_0^B \frac{V_{LSB}^2}{12 \cdot f_S} \cdot \left[2 \cdot \sin \pi \frac{f}{f_S}\right]^{2K}} \tag{3}$$

Solving equation 3, the RMS noise in bandwidth *B* can be written as:

$$V_{Qe,RMS} = \frac{V_{LSB}}{\sqrt{12}} \cdot \frac{\pi^K}{\sqrt{2 \cdot K + 1}} \cdot \frac{1}{M^{K+1/2}} \tag{4}$$

The ADS1202 has implemented a second-order modulator; thus, replacing *K* with 2 in equation 4, we can calculate the RMS noise in bandwidth *B* as:

$$V_{Qe,RMS} = \frac{V_{LSB}}{\sqrt{12}} \cdot \frac{\pi^2}{\sqrt{5}} \cdot \frac{1}{M^{5/2}} \tag{5}$$

Finally, we can calculate the theoretical, or ideal, delta-sigma modulator signal to noise ratio using Equation 6.

$$SNR_{ideal} = 20 \cdot \log \frac{V_P / \sqrt{2}}{V_{Qe,RMS}} = 6.02 \cdot N + 1.76 - 20 \cdot \log \left[\frac{\pi^K}{\sqrt{2 \cdot K + 1}} \right] + (20 \cdot K + 10) \cdot \log M \quad (6)$$

Applying Equation 6 for a different order of modulator and a different decimation ratio (over-sampling), it is possible to show that the theoretically achievable SNR is within the function of this parameter. (See Table 1.) Now it is relatively easy to determine the effective number of bits (ENOB) for the same conditions.

Table 1. Ideal SNR and ENOB of 2nd Order ΔΣ Modulator for Different Decimation Ratios

Decimation Ratio (M)	Ideal SNR (dB)	Ideal ENOB (bits)
4	24.99	3.9
8	40.04	6.4
16	55.09	8.9
32	70.14	11.4
64	85.19	13.9
128	100.24	16.4
256	115.30	18.9

As previously mentioned, ADS1202 has a second-order modulator. Ideally, for 64-bit over-samples, the SNR is -85dB, and the effective number of bits is 13.9.

3 Digital Filter Design

The total quantization energy is very high for the delta-sigma modulator, because the number of bits per sample is extremely low. It is left to the decimator to filter unwanted noise in the spectrum above the Nyquist band, so that the noise is not aliased into the base-band by the decimation process.

Decimation by the integer factor M, in principle, will reduce the sampling frequency by the same number. Figure 6 presents the basic block diagram of the filter.

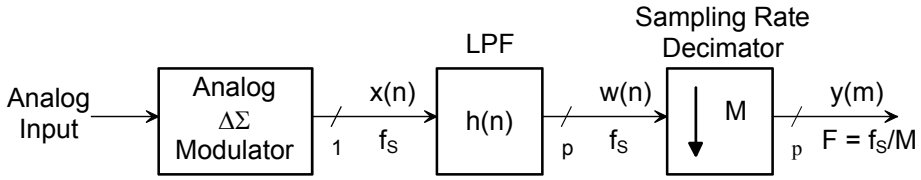


Figure 6. Basic Block Diagram of Decimation for ΔΣ Converter

The signal coming from the delta-sigma modulator x(n) is a bit stream with the frequency f_S. The signal x(n) is first digitally filtered by a low-pass filter h(n) with digital cut off frequency of π/M, where π is the normalized (radian) frequency corresponding to the Nyquist frequency, or half of the sampling frequency f_S. The filter h(n) removes all energy from signal x(n) above the frequency π/M, and avoids aliasing in the decimation process when the signal w(n) is re-sampled by the sampling rate decimator. This process is typically performed by using only one out of every M outputs of the digital filter, as shown by Equation 7.

$$y(m) = \sum_{k=-\infty}^{\infty} h(k) \cdot x(Mm - k) \qquad (7)$$

This equation shows that the input signal x(n) is shifted by M samples for each new computed output.

To keep costs low, the most important design criteria is the efficiency with which the decimator operation can be implemented. This is directly related to the type, order and architecture of the digital filter used in the implementation. The order of the low-pass filter, in turn, is directly related to a function of the required characteristics of ripple in the pass-band and stop-band as the ratio of the cut-off frequency to the stop band frequency.

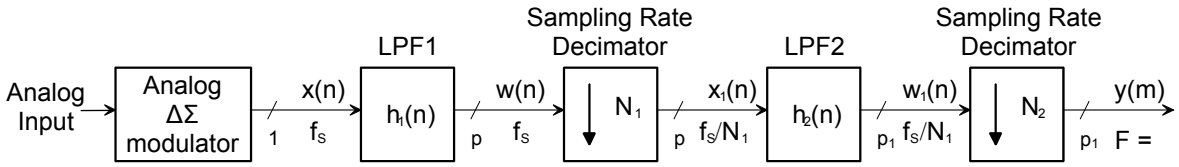


Figure 7. Simple Example of a Two-Stage Network for Decimation by a Factor of N_1N_2

The combined filter order of the two-stage decimation network from Figure 7 is several times smaller than the one-stage decimation network from Figure 6. Practical considerations of implementing more than two stages, however, may lead to the conclusion that a two-stage design is best.

The most popular filter architecture for delta-sigma conversion entails the combination of a $Sinc^K$ filter at the high sampling rate and a finite-impulse response (FIR) or infinite-impulse response (IIR) filter operating at intermediate and low sampling rates (see Figure 8). The suggested design will break the decimation process into a $Sinc^K$ filter stage that decimates by a large factor N_1 (typically 64), followed by an FIR (or IIR) narrow-band filtering stage that decimates by a small factor N_2 (for example, 2-8).

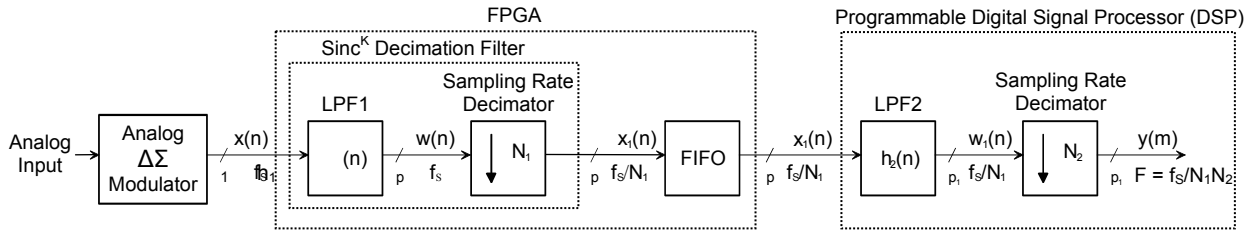


Figure 8. Multistage Decimator Incorporating Programmable DSP with FIFO Between Stages

The hardware structure that implements a $Sinc^K$ filter can be a very simple architecture composed of adders and registers. Such structures consume relatively little chip area. This design will be discussed in Section 4.

4 Sinc^K Filter

One of the most effective illustrations of matching design simplicity with the previously specified criteria is given by the use of a Sinc^K filter for high rate stage of decimation. These filters are very attractive for hardware implementation because they do not require the use of digital multipliers. They are more efficiently implemented by cascading *K* stages of accumulators operating at the high sample rate (sampling frequency f_S), followed by *K* stages of cascaded differentiators operating at the lower sample rate, f_S/N_1. This architecture utilizes wrap-around arithmetic and is inherently stable. The block diagram of the third-order Sinc filter (a Sinc^3) is presented in Figure 9.

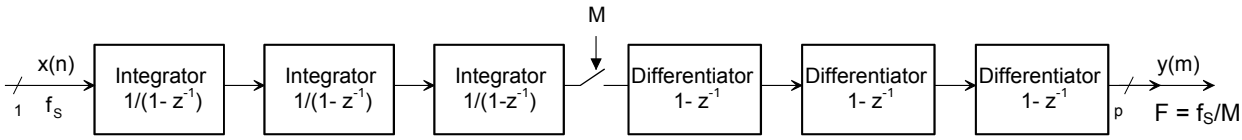


Figure 9. Sinc^3 Digital Filter Topology

Equation 8 describes the transfer function of a Sinc^K filter, where *M* is the decimation ratio of the sampling rate compressor.

$$H(z) = \left(\frac{1}{M} \cdot \frac{1 - z^{-M}}{1 - z^{-1}} \right)^K \qquad (8)$$

Substituting *Z* by e^{-j}, the frequency response obtained is:

$$\left| H(e^{j\omega}) \right| = \left(\frac{1}{M} \cdot \frac{\sin(\omega M / 2)}{\sin(\omega / 2)} \right)^K \qquad (9)$$

where:

$$\omega = 2\pi \frac{f}{f_S} \qquad (10)$$

Figure 10 illustrates an example of the frequency response of a Sinc^3 filter, from Figure 9, having a decimation factor of M = 16. The spectral zeroes are at frequencies that are multiples of the decimated sampling frequency.

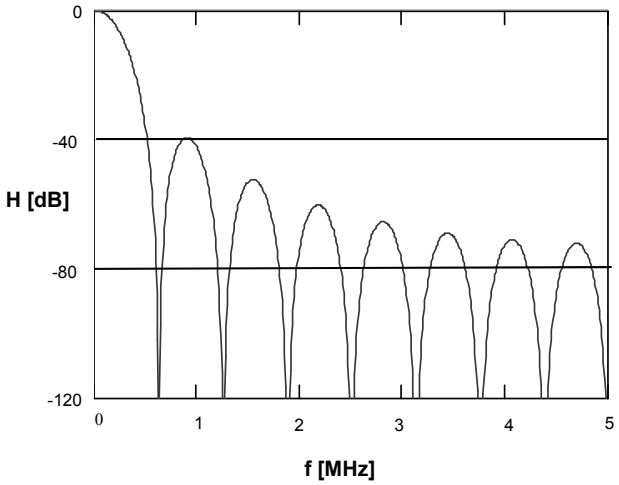


Figure 10. Frequency Response of the Sinc^3 Filter with M = 16

The relationship between the modulator clock (or sampling frequency f_S), output data rate (or first notch frequency), and the decimation ratio *M* is given by:

$$\text{DataRate} = \frac{f_S}{M} \qquad (11)$$

Therefore, data rate can be used to place a specific notch frequency in the digital filter response.

In the choice of the order of the Sinc filter, it is necessary to know the order of the delta-sigma modulator that will provide data. The order *K* of the Sinc^K filter should be at least 1 plus the order of the delta-sigma modulator in order to prevent excessive aliasing of out-of-band noise from the modulator from entering the base-band.

$$K \geq 1 + (\text{order\_}\Delta\Sigma) \qquad (12)$$

The output word size from the Sinc^K filter is larger than the input by a factor *p*, which is a function of decimation factor *M* and filter order *K*.

$$p = K \cdot \log_2 M \qquad (13)$$

Using Equation 9, it is possible to find the –3dB Sinc^K filter response point. This point is more dependent upon the filter order *K* and less dependent on the decimation ratio *M*. A Sinc^3 filter response point is 0.262 times the data rate.

For a sampling frequency of the delta-sigma modulator f_S = 10MHz, applying Equations 7 through 13, it is possible to summarize the results for a Sinc^3 filter and decimation ratio from 4 to 256, as shown in Table 2.

Table 2. Summary of the Sinc^3 Filter Applied to the ADS1202

Decimation	Data Rate (kHz)	Output Word Size (bits)	Filter Response f-3dB (kHz)
4	2,500.0	6	655
8	1,250.0	9	327.5
16	625.0	12	163.7
32	312.5	15	81.8
64	156.2	18	40.9
128	78.1	21	20.4
256	39.1	24	10.2

5 Sinc^3 Filter Implementation

The digital filter structure chosen to decode the output of the ADS1202 second-order delta-sigma modulator is a Sinc^3 digital filter. The function of the Sinc^3 digital filter is to output *M* word samples after each input, which represents a weighted average of the last *3(M-1)+1* input samples. This filter can also be implemented in software using a straight linear convolution from Equation 14:

$$y(k) = \sum_{n=0}^{3\cdot M-1} h(n)\cdot x(k-n) \qquad (14)$$

where *x(i)* denotes the input data stream made up of ones and zeros, *h(n)* are the filter coefficients, *y(k)* represents the decimated output data words and *M* is the decimation ratio. The coefficients of the digital filter, *h(n)*, are calculated based on the desired decimation ratio as follows:

$$h(n) = \frac{n\cdot(n+1)}{2} \qquad 0 \le n \le M-1 \qquad (15)$$

$$h(n) = \frac{M\cdot(M+1)}{2} + (n+M)\cdot(2\cdot M-1-n) \qquad M \le n \le 2\cdot M-1 \qquad (16)$$

$$h(n) = \frac{(3\cdot M-n-1)\cdot(3\cdot M-n)}{2} \qquad 2\cdot M \le n \le 3\cdot M-1 \qquad (17)$$

The filter transfer function in Equation 8 can be implemented using a cascading series of three integrators and three differentiators, as shown in Figure 10. The three integrators operate at the high modulator clock frequency f_S. The output from the third integrator is decimated down by M and fed to the input of the first differentiator. The three differentiators operate at the low clock frequency of f_S /M, where M is the decimation ratio. Figure 11 and Figure 12 show the detailed schematic of the Sinc^3 digital filter, as implemented in the Xilinx FPGA.

The gain of the $Sinc^3$ filter at dc is described by Equation 18. This means, for example, that for third order filter and decimation 64, the input will be multiplied by 262,144. In this case, the result from the filter, prior to scaling, is 18 bit.

$$Gain_{DC} = M^K \quad (18)$$

In each added filter order, the output word size is increased by $\log_2 M$. If the input is 1 bit, the output from the first-order filter (for decimation 64) will be a 6-bit word. A second-order filter will add another 6 bits; its output will be 13-bit, and so on. The internal bus of the Sinc filter, integrators and differentiators, needs to have a bus width that is one bit wider than the filter's dc gain (see Equation 19). The results for a $Sinc^3$ filter and a decimation ratio from 4 up to 256 are presented in Table 3.

$$Bus\_Width = 1 + K \cdot \log_2 M \quad (19)$$

Table 3. Output Word Size from Different Integrators in $Sinc^3$ Filter for 1-Bit Input Word

	$Sinc^3$		
Decimation Ratio (M)	**$Gain_{DC}$**	**$Gain_{DC}$ (bits)**	**Bus Width (bits)**
4	64	6	7
8	512	9	10
16	4,096	12	13
32	32,768	15	16
64	262,144	18	19
128	2,097,152	21	22
256	16,777,216	24	25

The evaluation board has the capacity to implement up to 256 decimations on the output signal coming from ADS1202. The 25-bit word on the filter output is latched into the output data register and transferred to a FIFO buffer. Eight words at a time will be later transferred to the DSP via the SPI port.

Figure 11 shows the implementation of a single integrator in the Xilinx FPGA. The 25-bit wide incoming data is continuously added to the previously accumulated result.

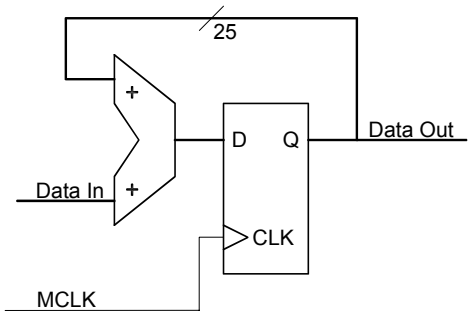


Figure 11. Xilinx Integrator Implementation

Figure 12 shows the implementation of a single differentiator. The 25-bit wide incoming data is latched onto the D flip-flop array while being subtracted from the previously latched result.

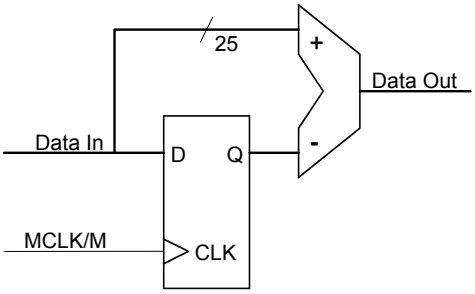


Figure 12. Xilinx Differentiator Implementation

Integrating Figure 11 and Figure 12 into Figure 9, we can present the implemented block diagram of the sinc^3 filter into the Xilinx FPGA.

Figure 13 presents the final implementation of the filter as described by VHDL code shown in Appendix A.

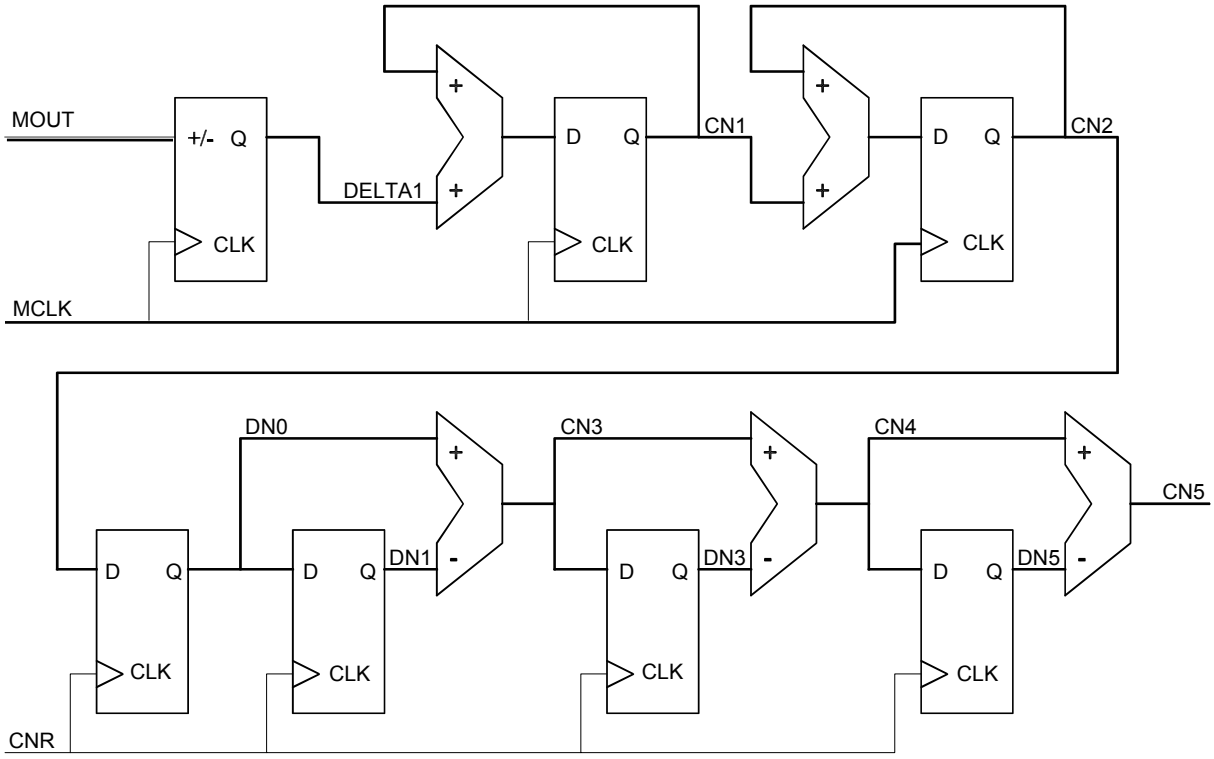


Figure 13. Xilinx Sinc^3 Filter Implementation

The Sinc^3 filter circuit from Figure 13 was simulated in an Excel spreadsheet. Appendix B presents results for a decimation ratio of 4. Appendix C presents results for a decimation ratio of 16.

The decimation ratio of the implemented Sinc^3 is set up by a switch on the evaluation board. The 3-bit input data is passed to a configuration register inside the FPGA and used to program the modulator clock frequency divider (MCLK), as shown in Figure 14. The divided clock, CNR, will be use to update differentiators in the Sinc^3 filter as well as moving this result into the FIFO buffer. After this, the output data rate is calculated and the appropriate values are programmed into the configuration and decimation registers inside the FPGA. For the third-order Sinc filter, the step function response will require three clock periods. Table 4 presents the input code of the clock divider, decimation ratio, data rate and filter response.

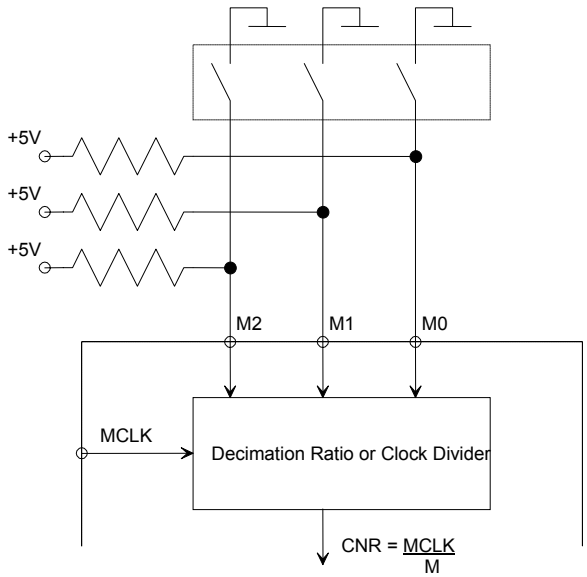


Figure 14. Clock Divider Inputs

Table 4. Decimation Ratio and Filter Response for Different Clock Divider Inputs

Clock Divider Inputs			Decimation Ratio (M)	Data Rate (kHz)	Filter Response (μs)
M2	M1	M0			
0	0	0	4	2,500.0	1.2
0	0	1	8	1,250.0	2.4
0	1	0	16	625.0	4.8
0	1	1	32	312.5	9.6
1	0	0	64	156.2	19.2
1	0	1	128	78.1	38.4
1	1	0	256	39.1	76.7

Appendix D presents the filter response on the input step function for decimation ratios of 4, 8, 16, and 32.

6 Conclusion

The ADS1202 is designed for current measurement in motor control applications. The current loop regulator typically works between 1 and 4 kHz. The signal used for this control loop must contain information from 10 up to 40kHz, with a required resolution from 12- to 16-bits. This application note provides designers of motor control systems with a solution for the easy implementation of the third-order Sinc filter. Table 5 presents an overview of the different parameters in the function of over-sampling or decimation ratio.

Table 5. Third-Order Sinc Filter Characteristics

Decimation Ratio (M)	Ideal SNR (dB)	Ideal ENOB (Bits)	Data Rate (kHz)	Filter Response f-3dB (kHz)	Filter Response (μs)	$gain_{DC}$ (Bits)
4	24.99	3.9	2,500.0	655	1.2	6
8	40.04	6.4	1,250.0	327.5	2.4	9
16	55.09	8.9	625.0	163.7	4.8	12
32	70.14	11.4	312.5	81.8	9.6	15
64	85.19	13.9	156.2	40.9	19.2	18
128	100.24	16.4	78.1	20.4	38.4	21
256	115.30	18.9	39.1	10.2	76.7	24

Appendix A.

VHDL code of implemented Sinc^3 filter from Figure 13.

```
library IEEE;
use IEEE.std_logic_1164.all;
use IEEE.std_logic_unsigned.all;


entity FLT is
  port(RESN, MOUT, MCLK, CNR : in std_logic;
       CN5                   : out std_logic_vector(24 downto 0));
end FLT;

architecture RTL of FLT is

 signal DN0, DN1, DN3, DN5 : std_logic_vector(24 downto 0);
 signal CN1, CN2, CN3, CN4 : std_logic_vector(24 downto 0);
 signal DELTA1             : std_logic_vector(24 downto 0);
begin


  process(MCLK, RESn)
  begin
    if RESn = '0' then
      DELTA1 <= (others => '0');
    elsif MCLK'event and MCLK = '1' then
      if MOUT = '1' then
        DELTA1 <= DELTA1 + 1;
      end if;
    end if;
  end process;


  process(RESN, MCLK)
  begin
    if RESN = '0' then
      CN1 <= (others => '0');
      CN2 <= (others => '0');
    elsif MCLK'event and MCLK = '1' then
      CN1 <= CN1 + DELTA1;
      CN2 <= CN2 + CN1;
    end if;
  end process;


  process(RESN, CNR)
  begin
    if RESN = '0' then
      DN0 <= (others => '0');
      DN1 <= (others => '0');
      DN3 <= (others => '0');
      DN5 <= (others => '0');
    elsif CNR'event and CNR = '1' then
      DN0 <= CN2;
      DN1 <= DN0;
      DN3 <= CN3;
      DN5 <= CN4;
    end if;
  end process;


  CN3 <= DN0 - DN1;
  CN4 <= CN3 - DN3;
  CN5 <= CN4 - DN5;

end RTL;
```

Appendix B.

The responses of the Sinc^3 filter circuit from Figure 13 for decimation ratio 4.

	Data In				MCLK/M							Data Out
K	MOUT	Delta1	CN1	CN2	CNR	DN0	DN1	CN3	DN3	CN4	DN5	CN5
0	0	0	0	0	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	0	0	0	0	0
2	0	0	0	0	0	0	0	0	0	0	0	0
3	0	0	0	0	0	0	0	0	0	0	0	0
4	0	0	0	0	0	0	0	0	0	0	0	0
5	1	1	0	0	1	0	0	0	0	0	0	0
6	1	2	1	0	1	0	0	0	0	0	0	0
7	1	3	3	1	1	0	0	0	0	0	0	0
8	1	4	6	4	1	0	0	0	0	0	0	0
9	1	5	10	10	2	4	0	4	0	4	0	4
10	1	6	15	20	2	4	0	4	0	4	0	4
11	1	7	21	35	2	4	0	4	0	4	0	4
12	1	8	28	56	2	4	0	4	0	4	0	4
13	1	9	36	84	3	56	4	52	4	48	4	44
14	1	10	45	120	3	56	4	52	4	48	4	44
15	1	11	55	37	3	56	4	52	4	48	4	44
16	1	12	66	92	3	56	4	52	4	48	4	44
17	1	13	78	30	4	92	56	36	52	112	48	64
18	1	14	91	108	4	92	56	36	52	112	48	64
19	1	15	105	71	4	92	56	36	52	112	48	64
20	1	16	120	48	4	92	56	36	52	112	48	64
21	1	17	8	40	5	48	92	84	36	48	112	64
22	1	18	25	48	5	48	92	84	36	48	112	64
23	1	19	43	73	5	48	92	84	36	48	112	64
24	1	20	62	116	5	48	92	84	36	48	112	64
25	1	21	82	50	6	116	48	68	84	112	48	64
26	1	22	103	4	6	116	48	68	84	112	48	64
27	1	23	125	107	6	116	48	68	84	112	48	64
28	1	24	20	104	6	116	48	68	84	112	48	64
29	1	25	44	124	7	104	116	116	68	48	112	64
30	1	26	69	40	7	104	116	116	68	48	112	64
31	1	27	95	109	7	104	116	116	68	48	112	64
32	1	28	122	76	7	104	116	116	68	48	112	64
33	1	29	22	70	8	76	104	100	116	112	48	64
34	1	30	51	92	8	76	104	100	116	112	48	64
35	1	31	81	15	8	76	104	100	116	112	48	64
36	1	32	112	96	8	76	104	100	116	112	48	64
37	1	33	16	80	9	96	76	20	100	48	112	64
38	1	34	49	96	9	96	76	20	100	48	112	64
39	1	35	83	17	9	96	76	20	100	48	112	64
40	1	36	118	100	9	96	76	20	100	48	112	64

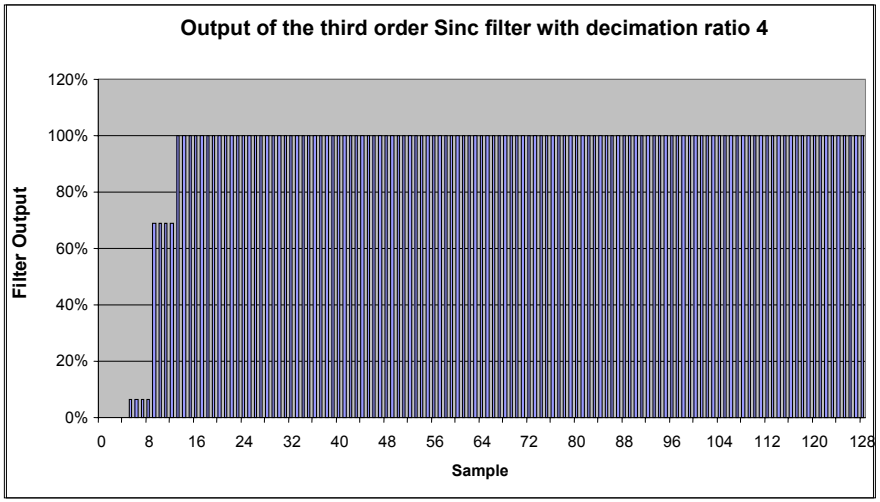
Appendix C.

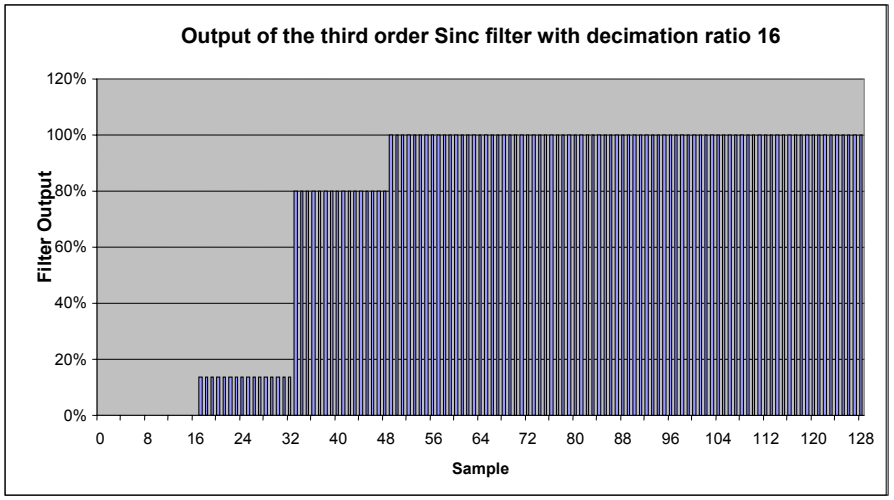
The responses of the Sinc^3 filter circuit from Figure 13 for decimation ratio 8.

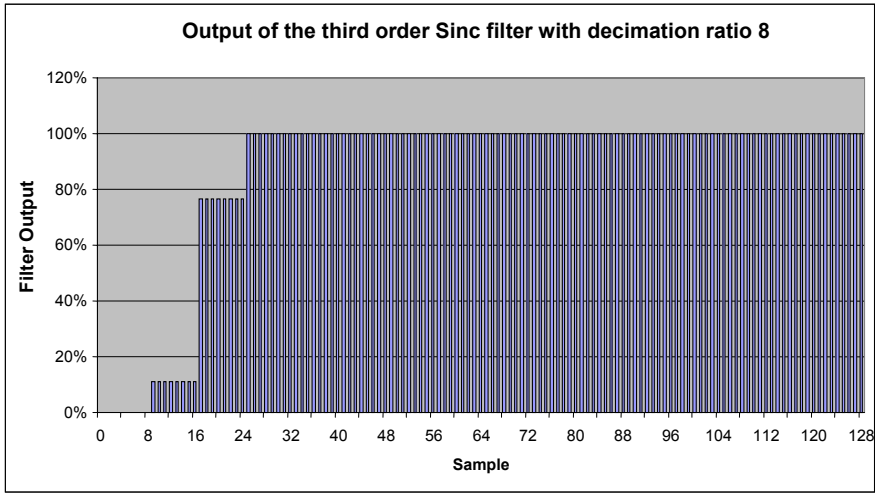
	Data In				MCLK/M							Data Out
K	MOUT	Delta1	CN1	CN2	CNR	DN0	DN1	CN3	DN3	CN4	DN5	CN5
0	0	0	0	0	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	0	0	0	0	0
2	0	0	0	0	0	0	0	0	0	0	0	0
3	0	0	0	0	0	0	0	0	0	0	0	0
4	0	0	0	0	0	0	0	0	0	0	0	0
5	1	1	0	0	0	0	0	0	0	0	0	0
6	1	2	1	0	0	0	0	0	0	0	0	0
7	1	3	3	1	0	0	0	0	0	0	0	0
8	1	4	6	4	0	0	0	0	0	0	0	0
9	1	5	10	10	1	4	0	4	0	4	0	4
10	1	6	15	20	1	4	0	4	0	4	0	4
11	1	7	21	35	1	4	0	4	0	4	0	4
12	1	8	28	56	1	4	0	4	0	4	0	4
13	1	9	36	84	1	4	0	4	0	4	0	4
14	1	10	45	120	1	4	0	4	0	4	0	4
15	1	11	55	165	1	4	0	4	0	4	0	4
16	1	12	66	220	1	4	0	4	0	4	0	4
17	1	13	78	286	2	220	4	216	4	212	4	208
18	1	14	91	364	2	220	4	216	4	212	4	208
19	1	15	105	455	2	220	4	216	4	212	4	208
20	1	16	120	560	2	220	4	216	4	212	4	208
21	1	17	136	680	2	220	4	216	4	212	4	208
22	1	18	153	816	2	220	4	216	4	212	4	208
23	1	19	171	969	2	220	4	216	4	212	4	208
24	1	20	190	116	2	220	4	216	4	212	4	208
25	1	21	210	306	3	116	220	920	216	704	212	492
26	1	22	231	516	3	116	220	920	216	704	212	492
27	1	23	253	747	3	116	220	920	216	704	212	492
28	1	24	276	1000	3	116	220	920	216	704	212	492
29	1	25	300	252	3	116	220	920	216	704	212	492
30	1	26	325	552	3	116	220	920	216	704	212	492
31	1	27	351	877	3	116	220	920	216	704	212	492
32	1	28	378	204	3	116	220	920	216	704	212	492
33	1	29	406	582	4	204	116	88	920	192	704	512
34	1	30	435	988	4	204	116	88	920	192	704	512
35	1	31	465	399	4	204	116	88	920	192	704	512
36	1	32	496	864	4	204	116	88	920	192	704	512
37	1	33	528	336	4	204	116	88	920	192	704	512
38	1	34	561	864	4	204	116	88	920	192	704	512
39	1	35	595	401	4	204	116	88	920	192	704	512
40	1	36	630	996	4	204	116	88	920	192	704	512

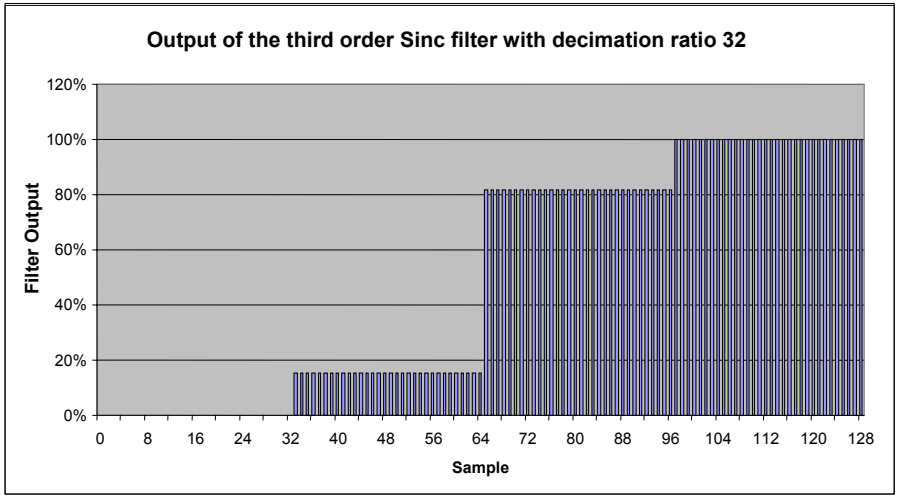
Appendix D.

Third-order Sinc filter response on the step function for different decimation ratios.









References

ADS1202 Product Data Sheet (SBAS275A)

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