Application Report
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Overclocking the ADS1240 and ADS1241

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ABSTRACT

The ADS1240 and ADS1241 are precision, wide dynamic range, delta-sigma (ΔΣ) Analog-to-Digital Converters (ADCs) with 24-bit resolution. These devices are very competitively priced. Considering their low speed and low current consumption parameters, designers may find it advantageous to know that both devices are capable of running considerably faster while maintaining performance at the expense of current consumption.

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Theory of Operation

In order to run the ADS1240 or ADS1241 converter at speeds above those specified in the product data sheet (SBAS173) while maintaining reasonable performance, extra bias current to the modulator is needed. This additional current can be obtained by adjusting a protected register value. To adjust the value, a special bit pattern must be written to the device and a pin toggled.

Overclocking Procedure

First, substitute the faster crystal, resonator, or oscillator on the board. Then configure the device for your application as usual (including channel selection, PGA setting, digital I/O lines, buffer on/off, etc). To unprotect the special register, raise pin 8 from DGND to DV_{DD}. This pin must be held at DV_{DD} for the modulator to obtain the extra current required; however, to change the configuration of the normal, unprotected registers of this device, this pin must be returned to DGND while WREG and RREG opcodes are issued.

While pin 8 is set to DV_{DD}, input the bit pattern shown in Figure 1. The *xxxx* placeholder stands for 4 *don't care* bits which may be any value. The *nnnnn* placeholder is 00000 for a default setting, but the normal operating analog current usually corresponds to a higher code. Note that the code is considerably higher for higher PGA settings. As analog current increases, performance improvements can be observed. Figure 2 shows how INL improves with higher current at various master clock frequencies.

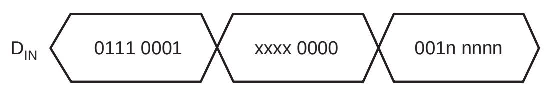

Figure 1. Input Waveform to Change Current Consumption

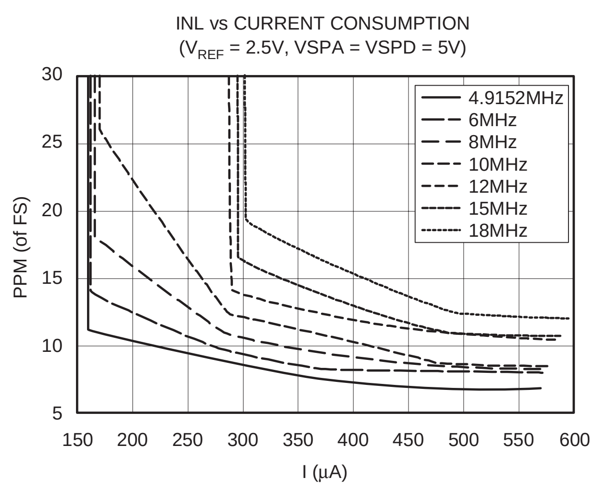

Figure 2. Typical Integral Nonlinearity versus Current Consumption at Various Standard Clock Frequencies

Once an appropriate value for *nnnnn* is selected and input, the current will increase and remain at this higher level until one of the following conditions are met: the part is reset; a new value of *nnnnn* is input; pin 8 is set back to DGND; or the bit pattern shown in Figure 3 is applied.

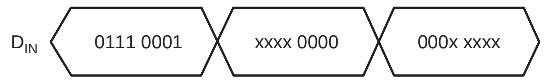

Figure 3. Input Waveform to Reset Current Consumption

Refer to Figure 4 through Figure 7 to select a clock frequency and appropriate code to program for increased current consumption. These figures show nominal current consumtion at the selected frequency, and the results of changing the code in the protected register.

These graphs do not give an indication of performance at the selected code, only the current consumption. It is recommended to start with the lowest overclocking frequency that the application can support. It is also recommended to start with the highest code (for highest current consumption) that the application can support. This will give the best performance under the new conditions. If the performance at these settings is acceptable, try reducing the code or increasing the speed for additional time or current savings.

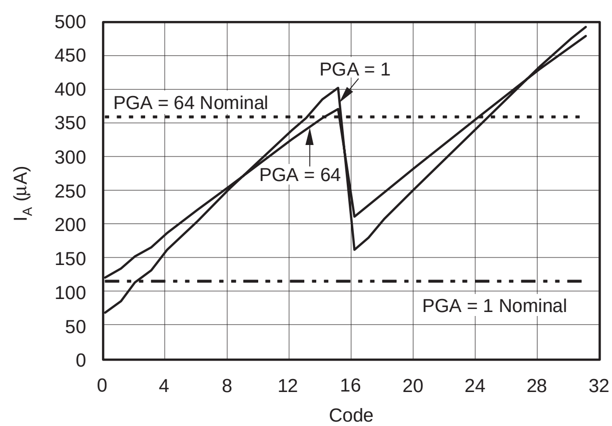

Figure 4. Analog Current Consumption vs Code at 2.4576MHz

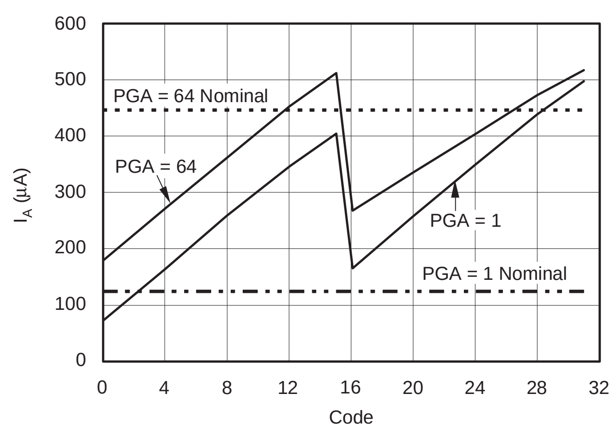

Figure 5. Analog Current Consumption vs Code at 4.9152MHz

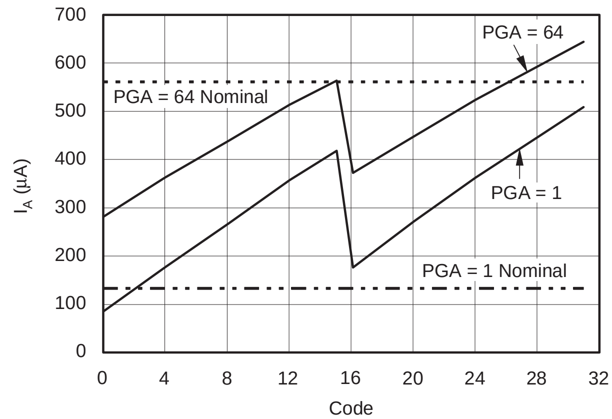

Figure 6. Analog Current Consumption vs Code at 10MHz

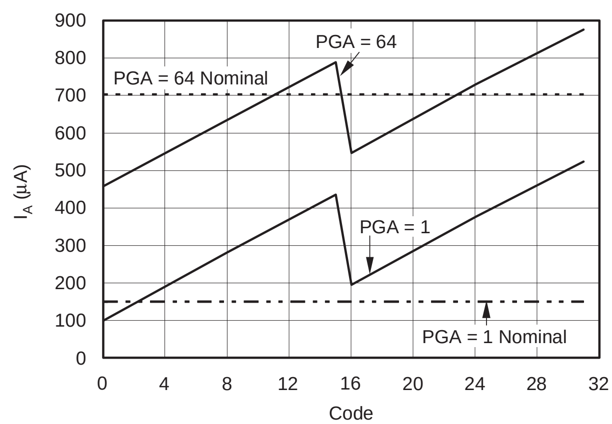

Figure 7. Analog Current Consumption vs Code at 18MHz

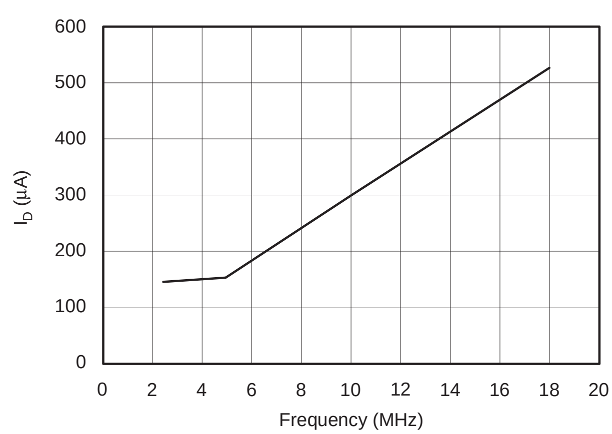

Figure 8. Digital Current Consumption vs Frequency

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