Application Report
SBAA081A–October 2002–Revised May 2015

Using a SAR Analog-to-Digital Converter for Current Measurement in Motor Control Applications

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ABSTRACT

With careful analysis, a designer can get good performance from what may, at first, look like incompatible components in a motor control system. One might assume that for a ±5V output signal from the current sensors, an Analog-to-Digital (A/D) converter using dual, high-voltage supplies (±12V) might be required, when in fact, new, less-expensive converters may work equally well.

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1 Introduction

In a typical motor-control system, as shown in Figure 1, the currents and voltage of the motor phase windings are measured and converted into a digital format for use by a microcontroller (μC) or Digital Signal Processor (DSP). Due to the high voltages on the motor windings, electrically isolated Hall effect closed-loop sensors are used to convert the electric field from motor currents into a voltage within the input voltage range of an A/D converter. Multi-channel Successive Approximation Register (SAR) A/D converters are used for simultaneous sampling to maintain correct phase information. This application report will analyze the application of closed-loop current transducers and how to achieve the best signal-to-noise performance from the A/D converter. In our example, the ADS7864, a 6-channel, 12-bit, 500kHz SAR-type A/D converter, will be used.

2 Hall Effect Closed-loop Current Transducers

An open-loop current transducer will have an output voltage that is an amplified version of V_H, the output voltage of a Hall effect sensor. V_H is proportional to a bias current across the device, the magnetic flux through the device, and a scaling factor that is dependent upon process parameters and temperature (see Figure 2).

The closed-loop transducer, also called a compensation or zero-flux transducer, has an integrated compensation circuit in which the overall performance is improved over that of an uncompensated Hall sensor. The output current is a scaled replica of the motor current and is sensed by the measurement resistor.

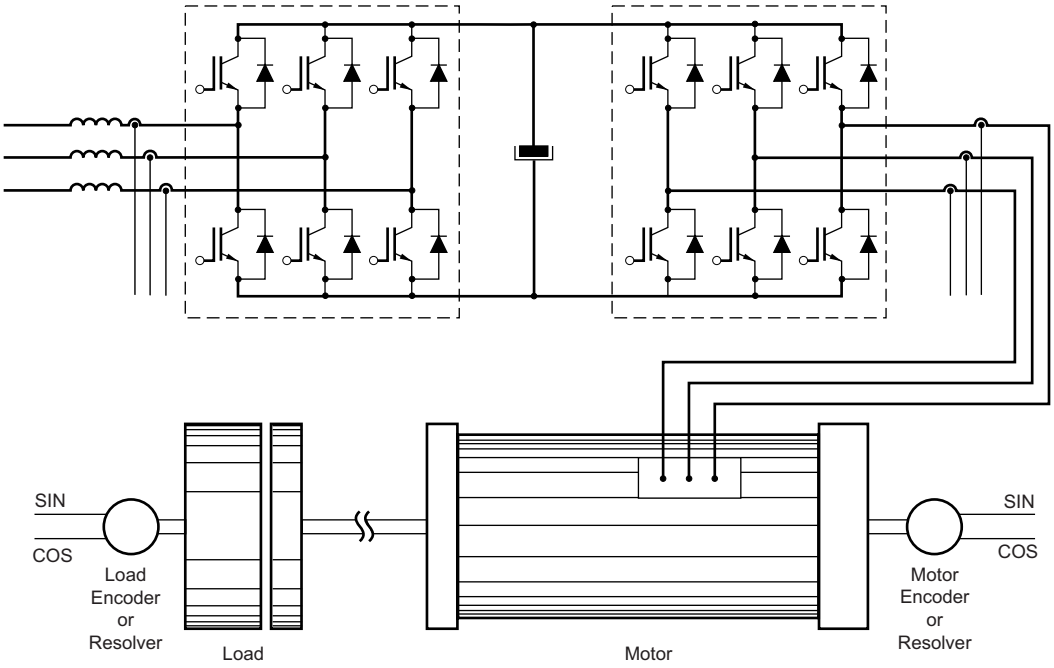

Figure 1. Motor Control System with Measuring Signals

In the closed-loop sensor, Hall sensor voltage VH is applied directly to a transconductance amplifier. Output current from the amplifier is sent through windings wound in such a way that the induced field is opposite to the field caused by the motor current. The high open-loop gain of the transconductance amplifier forces the Hall sensor voltage to be small, and thus, the magnetic field through the Hall sensor must also be very small. Continuing the analogy of op amps and feedback networks, we can call the magnetic flux due to the motor winding ($B_P = I_P \times N_P$), the input signal. The feedback signal would be the magnetic field, due to the output current of the sensor being multiplied by the number of turns of the secondary winding ($B_S = I_S \times N_S$). Secondary current I_S, reduced by the turns ratio, is much lower than I_P because a winding with N_S turns is used to generate the same magnetic flux (ampere-turns). Therefore:

$$N_P \times I_P = N_S \times I_S \quad (1)$$

It is the high open-loop gain of the amplifier that allows the equal sign to be approximated in Equation 1. Therefore, the B_S induction is equivalent to B_P and their respective ampere-turns counter-balance each other; thus, the system operates at nearly zero magnetic flux.

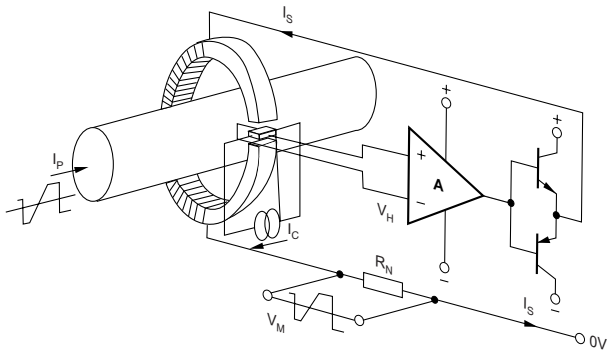

Figure 2. Operating Principle of the Closed-Loop Transducer

Take as an example the measurement of a DC current of 100A. The number of turns N_P = 1, because the conductor leads directly into the magnetic circuit, thereby, constituting a single turn. The secondary winding has N_S = 1000 turns. Therefore, the turns ratio is 1:1000.

As soon as I_P takes a positive value, a B_P induction appears in the air gap of the magnetic core, producing a V_H voltage in the Hall element. This voltage is transformed into a current through the amplifier stage which supplies the I_S current flowing through the secondary winding. The B_S induction is thus created, which compensates the B_P induction. The resulting secondary current is:

$$I_S = \frac{N_P \times I_P}{N_S} = \frac{1 \times 100}{1000} = 100 \text{ mA} \quad (2)$$

Therefore, I_S is a scaled image of I_P. This is the measurement current intended for the user. In the analysis that follows, the Hall effect closed-loop current transducer will be replaced by an ideal current source.

3 Hall Effect Closed-loop Current Transducers Output Signal (Load Resistance)

The output current is shunted through a measuring resistance to develop the output voltage. The range in value of this resistor is constrained by several factors. The value of the measuring resistance must be within the range shown in the Hall effect sensor data sheet: between the $R_{M\ min}$ resistance (determined by power dissipation), and the $R_{M\ max}$ resistance. $R_{M\ max}$ is defined to avoid the electronic saturation of the circuit, taking into account the minimum available supply voltage which determines the maximum measuring range.

It must be noted that the data sheet indicates the R_M values corresponding to the permanent nominal rating and a given measuring range. Other conditions can also determine the choice of value of measuring resistor R_M.

In our example, the LEM LA 55-P closed-loop transducer has the following parameters: I_P = 70A, T_A = 70°C, and V_C = ±15V. The turns ratio of 1:1000 determines the secondary current I_S = 70mA.

The LEM LA 55-P data sheet indicates $R_{M\ max}$ = 90Ω and $R_{M\ min}$ = 50Ω. To set the full-scale output voltage to be ±5V, 71Ω will be used for the measuring resistor. Figure 3 shows the voltage on the measuring resistor in relation to the primary current, I_P.

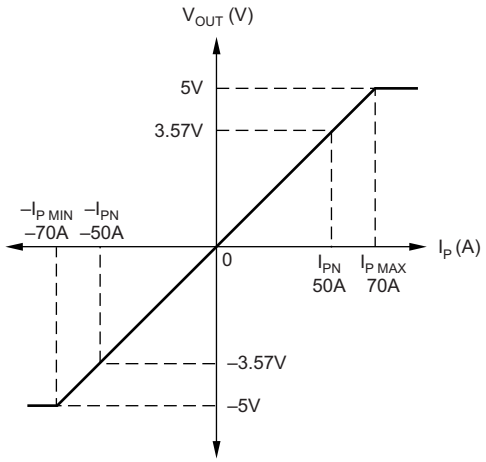

Figure 3. Output Curve of LA 55-P Current Transducer with 71Ω Measuring Resistor

4 SAR-Type A/D Converter

Figure 4 shows an equivalent input stage of the ADS7864; it is a representation of many SAR-type A/D converters. A summary of the operation of these parts is worthwhile in coming to an understanding of their performance limitations.

The measured signal is connected to the positive IN+ and negative IN– inputs. At the beginning of the cycle, switches SW1 and SW2 are closed, while switches SW5 and SW6 remain open, and SW3 is closed to V_{GND}. The comparator is presented with an input differential signal of 0V and a common-mode bias voltage of V_{MID}, and undergoes an auto-zero cycle to eliminate any inherent offset voltage. The sampling process starts from this condition with the closing of input switches SW7 and SW8.

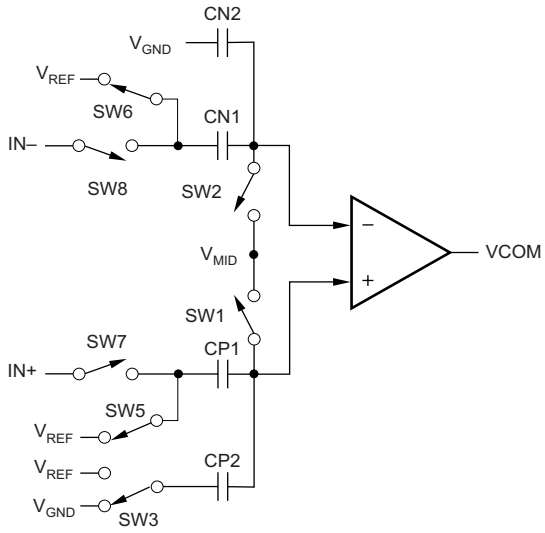

Figure 4. Equivalent Input Circuit of SAR A/D Converter

Since the circuit is symmetrical, we can evaluate the positive input, as shown in Figure 5. After some transitional period of time, the charge on the capacitors will stabilize—this time is the sampling period. Switches SW1 and SW2 are then opened simultaneously. The charge (Q_{PS}) stored on the noninverting comparator input node is described by Equation 3.

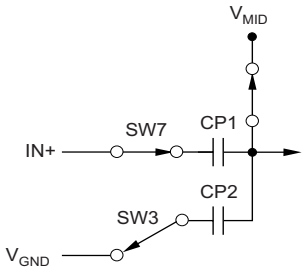

Figure 5. Equivalent Input Circuit During Sampling, Acquisition, Time

$$Q_{PS} = (V_{MID} - V_{IN+}) \times CP1 + (V_{MID} - V_{GND}) \times C_{P2} \quad (3)$$

Similarly, the charge (Q_{NS}) on the inverting node of the comparator, or the charge (Q_{NS}) stored on capacitors C_{N1} and C_{N2} can be describe by Equation 4.

$$Q_{NS} = (V_{MID} - V_{IN-}) \times C_{N1} + (V_{MID} - V_{GND}) \times C_{N2} \quad (4)$$

Now the negative and positive input nodes of the comparator are not tied together anymore and there is no circuit path for charge to accumulate or leave from these nodes. Captured charge Q_{PS} will be held on capacitors C_{P1} and C_{P2} and captured charge Q_{NS} on capacitors C_{N1} and C_{N2}. The next step is to open input switches SW7 and SW8, disconnecting sampling capacitors C_{P1} and C_{N1} from the input signal.

During the conversion cycle, successively smaller fractions of C_{P1} and C_{P2} will be switched between ground and V_{REF} to minimize the voltage on the input nodes of the comparator. The output code represents the resulting size of C_{P1} with respect to the sum of C_{P1} and C_{P2} that, when multiplied by V_{REF}, most closely matches the amplitude of the sampled input voltage.

5 Analysis of A/D Converter Input During sampling Time

Referring to the previous explanation of the input stage of a SAR A/D converter, the equivalent circuit in Figure 6 can be used for analysis. Sampling capacitor C_S has an initial charge of voltage V_0 before switch SW is closed. This is left over from a prior conversion. During acquisition, input switch SW is closed. Sampling capacitor C_S will be charged through source resistor R_{SRC} and switch resistor R_{SW} from the signal source, which during the acquisition period has output voltage E. Equivalent resistance RS is equal to the sum of signal source resistor R_{SRC} and switch resistor R_{SW}. Switch resistor R_{SW} in the case of the ADS7864 is about 20Ω.

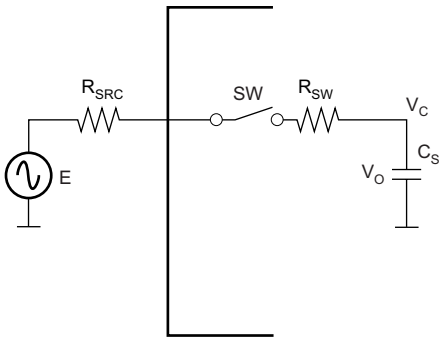

Figure 6. Circuit Describing the Behavior of an A/D Converter During the Sampling of an Input Signal

A plot of Equation 5 describing the voltage on capacitor C_S after switch SW is closed, is shown in Figure 7.

$$V_C(t) = V_0 + (E - V_0) \times \left(1 - e^{\frac{-1}{\tau}}\right) \quad (5)$$

Where $\tau = R_S \times C_S$.

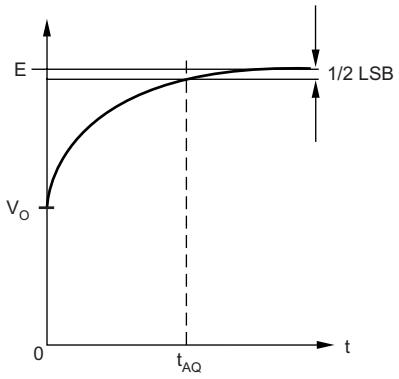

Figure 7. Voltage on the Sampling Capacitor During the Sampling Period

Our goal is to determine the acquisition time needed to charge the input capacitor to the value that is less than 1/2 LSB in error with respect to input signal. This is described in Equation 6.

$$E - V_C(t_{AQ}) \le \frac{1}{2}LSB \tag{6}$$

The analog input signal to the ADS7864 (in single-ended mode) is $\pm V_{REF}$ around V_{REF}. In this case, the reference voltage is an internal reference of 2.5V, so the analog input signal is ±2.5V around 2.5V. The input signal range is from 0V to 5V. The difference between the most positive and most negative analog input of the converter's operating range is Full-Scale Range (FSR) and in this case is 5V. To analyze the worst case, input signal voltage E from the signal source will be equal to the full-scale voltage. The ideal code width of the 12-bit converter or 1LSB will be $E/2^{12}$.

Replacing the value of 1LSB in Equation 6, it is possible to derive the value on which the input capacitor is supposed to be charged at the end of the acquisition time, as shown in Equation 7.

$$V_C(t_{AQ}) \ge E \times \left(1 - \frac{1}{2^{13}}\right) \tag{7}$$

Substituting Equation 7 in Equation 5 and assuming that this condition is satisfied at the end of the acquisition time, we get the following result in Equation 8:

$$E \times \left(1 - \frac{1}{2^{13}}\right) \le V_0 + (E - V_0) \times \left(1 - e^{\frac{-t_{AQ}}{\tau}}\right) \tag{8}$$

Now it is easy to calculate the required value for τ.

$$\tau \le \frac{t_{AQ}}{\ln\left(\frac{E - V_0}{E} \times 2^{13}\right)} \tag{9}$$

The initial charge for different SAR converters is different and can be 0V, V_{REF}, full-scale voltage, etc. The initial charge depends on the internal structure of the converter. See Figure 4 for the ADS7864 input structure. In our case, the initial charge (V_0) of sampling capacitor C_S will be half of the FSR because the V_{MID} (see Figure 4) is half of the supply voltage (or half of FSR) for V_{REF} equal to 2.5V. The acquisition time must be a minimum of 8.32 times the time constant, when replacing V_0 with E/2 in Equation 9.

For a 12-bit A/D converter like the ADS7864, it is good practice that the acquisition time is 9 to 11 time constants. Knowing that internal sampling capacitor C_S of this converter is 15pF, we can determine the maximum value of input resistor R_S. The equivalent input resistance, R_S, is equal to the sum of signal source resistor, R_{SRC}, and switch resistor, R_{SW}.

$$R_S \le \frac{t_{AQ}}{11 \times C_S} = \frac{250\ ns}{11 \times 15\ pF} = 1.515\ k\Omega \tag{10}$$

6 Verification of DC Performance Parameters

For this experiment, the DEM-ADS7864 evaluation board was used. First, one input pair of the A/D converter, positive and negative, is connected to the internal reference voltage of 2.5V. One pair is shown in Figure 8. Ideally, a Gausian Probability Density Function (PDF) should describe a histogram of a large sample of conversion results. In this test, 8192 points were collected.

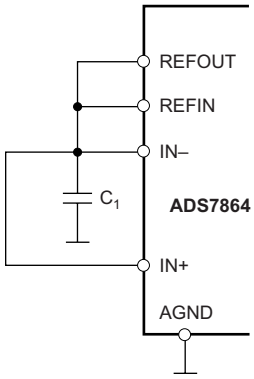

Figure 8. A/D Converter DC Parameter Testing Circuit

The Gausian PDF is defined by specification of a mean (μ) and variance (σ^2). X is a digital output sample of the A/D converter and n is the number of samples.

$$p(x) = \frac{n}{\sigma\sqrt{2\pi}} \times e^{\frac{-(X-\mu)^2}{2\sigma^2}} \tag{11}$$

The mean and variance are estimated from the sample set of data using the following equations:

$$\mu \approx \frac{1}{n}\sum_{i=1}^{n} X_i \tag{12}$$

$$\sigma^2 \approx \frac{\sum_{i=1}^{n} (X_i - \mu)^2}{n-1} \tag{13}$$

The mean (μ) is the expected or average value. It is used to measure offset errors. The variance (σ^2) describes the variability of the distribution about the mean. It is used as a measurement of uncertainty or noise.

The square root of the variance is called standard deviation (σ), and it is a measure of the effective or root mean squared (RMS) noise. The peak-to-peak noise can be determined from the RMS noise value:

Offset Error = μ

RMS Noise = σ

Peak-to-Peak Noise = 6.6 × σ

In measuring dynamic performance, two parameters can be calculated. The ideal SNR of the A/D converter, assuming the only noise source is quantization noise, can be calculated by the following equation:

$$SNR = 6.02\ N + 1.76\ db \tag{14}$$

The “noise floor” is set by the A/D converter’s resolution and the number of samples used in the FFT. The FFT is done using coherent sampling and without windowing.

$$SpotNoise = -6.02 \times N - 1.76 - 10 \times \log\left(\frac{samples}{2}\right) = -110.1\,dB \tag{15}$$

For a 12-bit converter with full-scale voltage range of 5V ($1.768V_{RMS}$), and 8192 samples we can calculate following:

1 LSB = 5 V / 2^{12} = 1.2207 mV

SNR = 6.02 × 12 +1.76 = 74 dB

SpotNoise = –6.02 × 12 – 1.76 – 10 × log(4096) = –110.1 dB

When the noise is random, the FFT and histogram tests should correlate with each other.

$$\text{Noise} = 1.768\ V_{RMS} \times 10^{\left(\frac{-70.853}{20}\right)} = 506.7\ \mu V_{RMS}$$

AverageSpotNoise = –70.853 dB – 10 × log(4096) = –107 dB

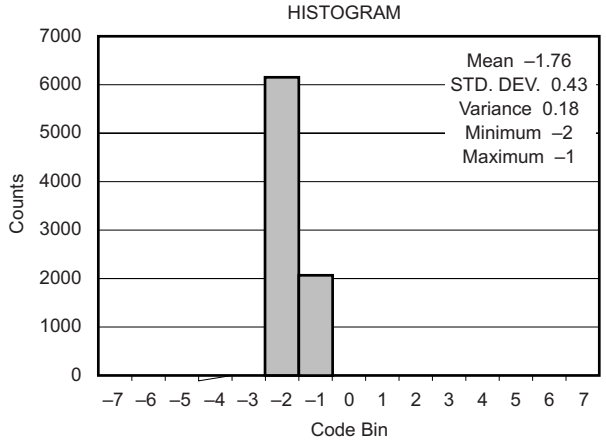

Figure 9. Histogram of 8192 Points with Inputs Connected Together

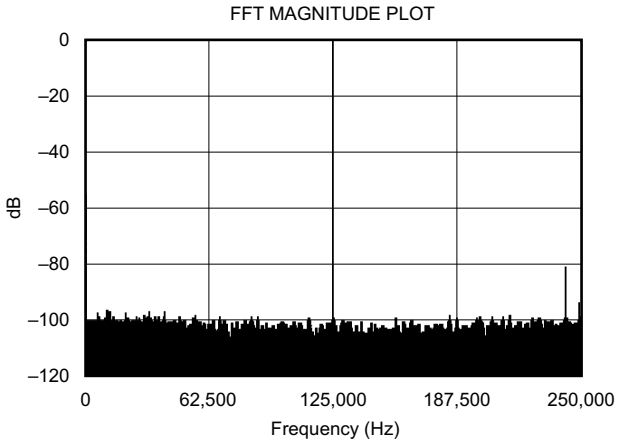

Figure 10. Histogram of 8192 Points with Inputs Connected Together

The results just calculated represent our the best performances we can expect to achieve, as shown in Figures 9 and 10.

From the description of the closed-loop Hall sensor, this is a ±5V output signal connected to A/D converter specified for ±2.5V around 2.5V input signal. The sensor manufacture specification prohibits using a measuring resistor of < 50Ω, so this signal must be atteuated and level-shifted. The negative input is directly connected to internal reference voltage (see Figure 11). The positive input is connected to a proposed resistor network. Referring to Equation 10, resistors R_1 and R_2 are chosen to have 3kΩ values so that Thevinin equivalent resistance on the input to the A/D converter is 1.5kΩ. To verify this worked, the measurements were repeated with the inputs tied to ground.

Again, a histogram and FFT are done using 8192 points and the new results are presented in Figures 12 and 13.

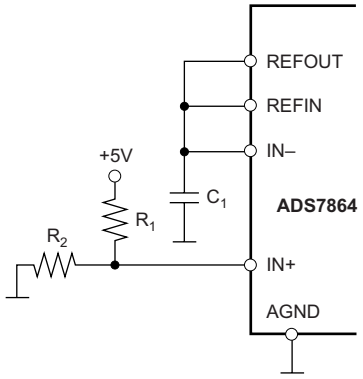

Figure 11. A/D Converter DC Parameter Testing Cirucit with Proposed Resistive Network on the Input

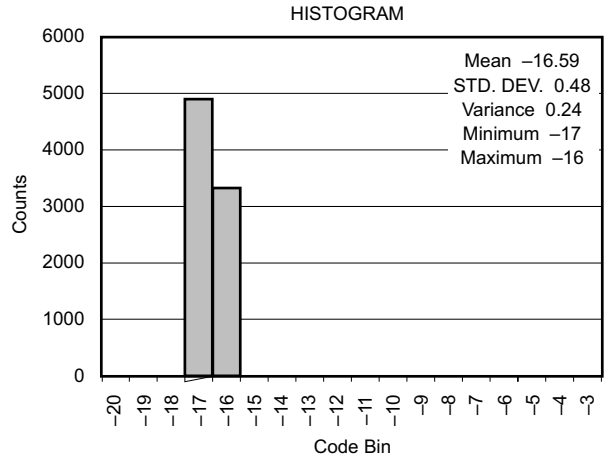

Figure 12. Histogram of 8192 Points with Grounded Resis- tive Network Input

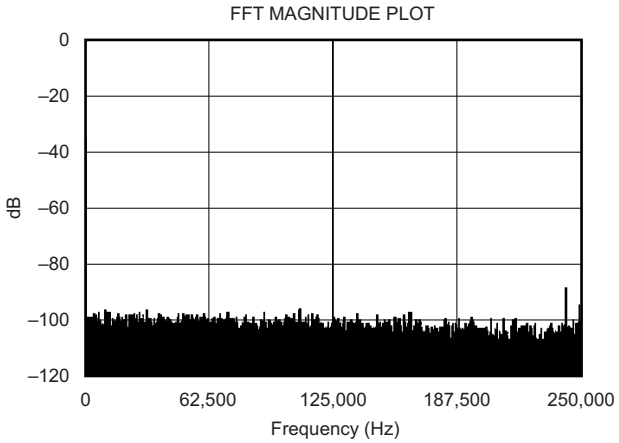

Figure 13. FFT of 8192 Points with Grounded Resistive Network Input

RMS noise and average spot noise are calculated again:

$$\text{Noise} = 1.768\ V_{RMS} \times 10^{\left(\frac{-69.520}{20}\right)} = 590.8\ \mu V_{RMS}$$

AverageSpotNoise = –69.520 dB – 10 × log(4096) = –105.6 dB

The differences between the two sets of measurements show a change in offset and noise caused by the resistive divider on the input of the A/D converter. To balance source impedance and minimize offset, it is good practice to tie the negative input to V_{REF} with a 1.5kΩ resistor, at the expense of a slight increase in noise.

7 Verification of AC Performance Parameters

To verify AC performance, the same configuration is used. The signal source has ±5V output connected to resistor R_2. This is replacing the Hall effect closed-loop current transducer with its measuring resistor on the output, (see Figure 3). The connection diagram is presented in Figure 14. To study the sensitivity of system performance with respect to the sampling, or acquisition time, a series of tests were run sweeping the acquisition time as a parameter. The input signal is approximately 15kHz and full-scale, and there were variations in system clocking frequency and sampling frequency. Results are summarized below

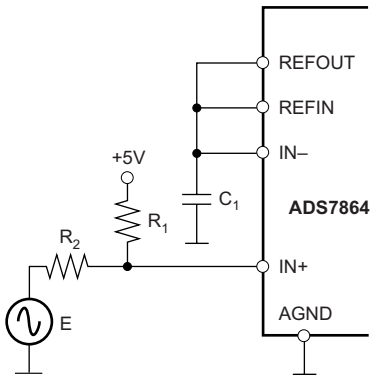

Figure 14. A/D Converter AC Parameter Testing Circuit with Proposed Resistive Network on the Input

The measurements are done for different conditions and different acquisition times. In every measurement, 8192 points are sampled and FFT is calculated. The results are presented in Figures 18 to 27 and Tables II to XI. Table I summarizes the data and present as a function of acquisition time. Data from Table I are presented in Figures 15, 16, and 17.

Table 1. Measured AC Performance as a Function of Acquisition Time

tAQ	(ns)	177	190	210	234	265	309	348	397	447	561
SNR	(dB)	63.1	65.4	68.3	70.4	71.3	71.4	71.4	71.5	71.4	71.7
SND	(dB)	56.8	59.4	63.2	66.7	69.4	70.0	70.5	70.7	70.8	71.0
SFR	(dB)	60.1	62.7	66.7	71.0	76.1	77.5	80.7	82.7	83.5	84.0
THD	(dB)	–58.0	–60.7	–64.8	–69.1	–73.7	–75.6	–77.7	–78.6	–79.2	–79.0
Harmonics											
0	(dB)	–44.2	–42.1	–40.5	–39.9	–39.3	–39.0	–38.9	–38.9	–38.7	–40.0
1	(dB)	–0.2	–0.2	–0.2	–0.2	–0.2	–0.2	–0.2	–0.2	–0.2	–0.2
2	(dB)	–81.2	–82.2	–84.4	–86.8	–89.3	–90.6	–89.8	–91.6	–92.2	–93.0
3	(dB)	–60.1	–62.7	–66.7	–71.0	–76.1	–77.5	–80.7	–82.7	–83.5	–84.5
4	(dB)	–90.5	–90.0	–88.9	–87.8	–87.2	–88.5	–86.8	–86.4	–86.6	–85.1
5	(dB)	–65.0	–67.8	–72.4	–76.7	–81.9	–85.5	–87.2	–87.3	–87.8	–88.3
6	(dB)	–98.3	–95.5	–97.7	–99.3	–100.4	–98.0	–102.6	–102.3	–100.8	–100.3
7	(dB)	–67.8	–70.5	–74.4	–78.5	–81.9	–84.7	–85.7	–85.1	–86.0	–85.1
8	(dB)	–97.2	–96.4	–95.7	–97.8	–98.9	–98.1	–97.6	–97.5	–98.7	–96.2
9	(dB)	–69.9	–72.7	–76.7	–82.5	–88.3	–91.6	–95.3	–99.0	–99.5	–102.9
10	(dB)	–99.0	–99.8	–101.5	–101.3	–103.1	–100.7	–103.0	–101.2	–102.5	–103.0

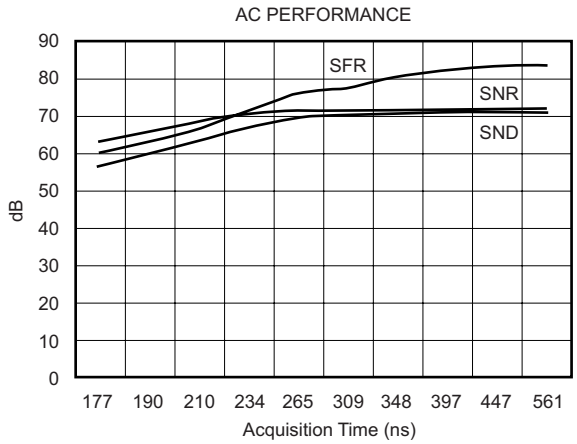

Figure 15. Measured SNR, SND, and SFR as a Function of Acquisition time.

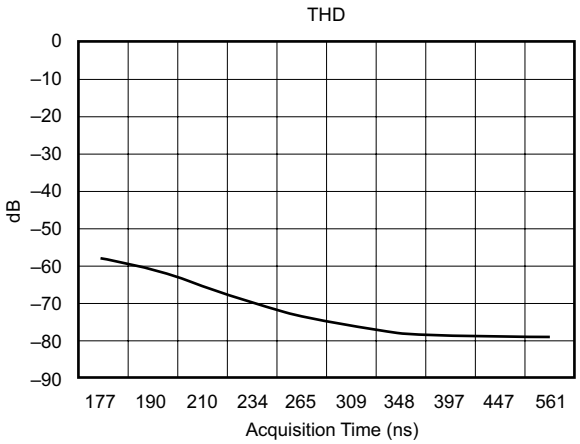

Figure 16. Measured Total Harmonic Distortion as a Function of Acquistion Time

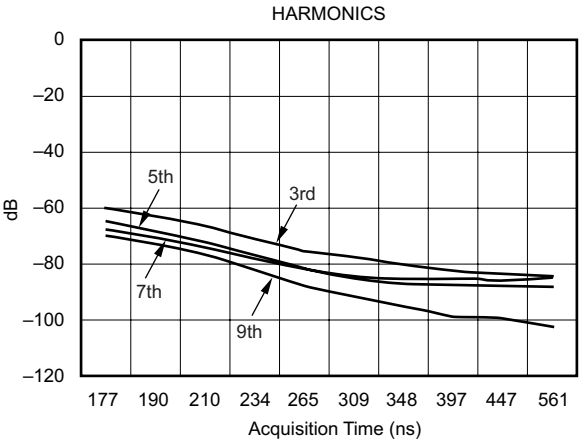

Figure 17. Measured Harmonic as a Function of Acquisition Time

8 Conclusion

The results in Table I and Figures 15-17 show changes in AC performance as a function of acquisition time. The input resistor network was calculated based on the internal sampling capacitor of the A/D converter, which is 15pF, and an acquisition time of 250ns. By increasing the acquisition time from 250ns to 400ns, better performance is obtained without significantly reducing the sampling rate. If the master clock is running at full speed (8MHz), the conversion time is 1.625µs. By changing the acquisition time from 170ns to 420ns, the total conversion time will increase from 2µs to 2.25µs. Making the acquisition time longer allowed the signal-to-noise ratio to increase from 63.1dB to 71.5dB and at the same time, THD will decrease from –58dB to –78.6dB.

9 References

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2. Selecting an A/D Converter, Larry Gaddy, Burr-Brown Application Bulletin AB-098.
3. DSP-Based Testing of Analog and Mixed-Signal Circuits, Matthew Mahoney, IEEE catalog number EH0258-4.
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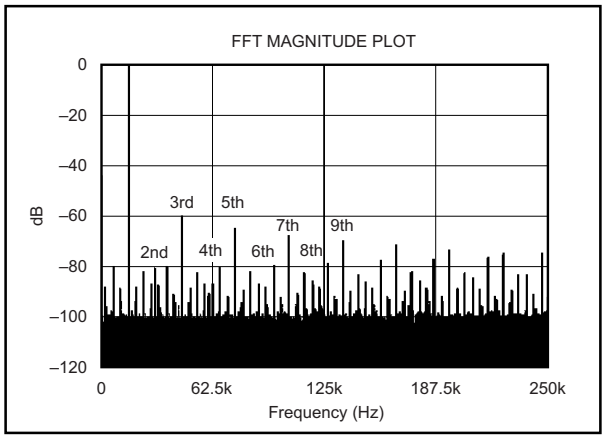
5. BBEval, Version 2.0, Gebhard Haug, Burr-Brown Software Library, 2000.

10 Appendix

Measurement Parameters

Clock Frequency = 8MHz
Sampling Frequency = 500kHz
Sample Size = 8192 points
Input Frequency = 14,953.6133Hz
Number of Cycles = 245 cycles
Acquisition Time = 177ns



SNR = 63.1dB
SND = 56.8dB
SFR = 60.1dB
THD = –58.0dB

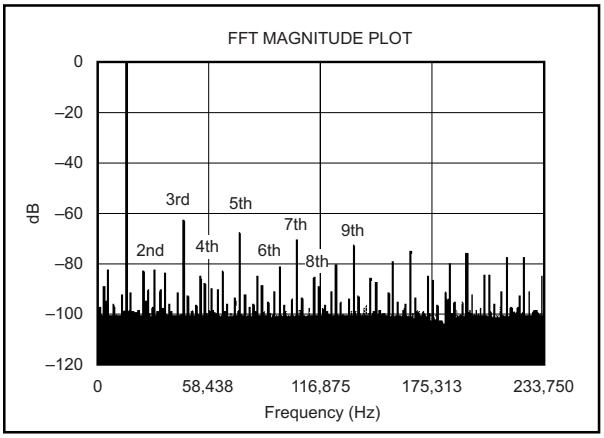
Harmonics for 177ns Acquisition Time

HARMONIC (N)	FREQUENCY (kHz)	AMPLITUDE (dB)
0	0.00	–44.2
1	14.95	–0.2
2	29.91	–81.2
3	44.86	–60.1
4	59.81	–90.5
5	74.77	–65.0
6	89.72	–104.68
7	104.68	–67.8
8	119.63	–97.2
9	134.58	–69.9
10	149.54	–99.0

Figure 18. Acquisition Time of 177ns

Measurement Parameters

Clock Frequency = 7.48MHz
Sampling Frequency = 467.5kHz
Sample Size = 8192 points
Input Frequency = 14,894.7144Hz
Number of Cycles = 261 cycles
Acquisition Time = 190ns



SNR = 65.4dB
SND = 59.4dB
SFR = 62.7dB
THD = –60.7dB

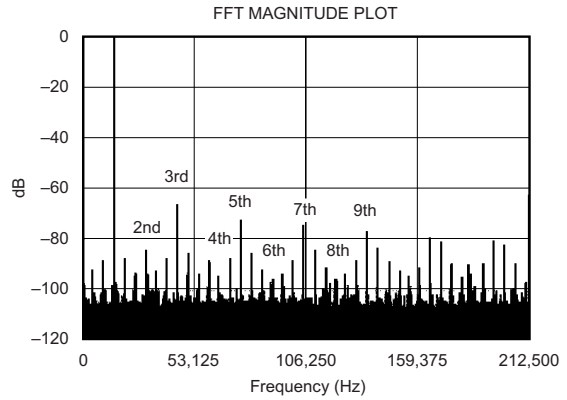
Harmonics for 190ns Acquisition Time

HARMONIC (N)	FREQUENCY (kHz)	AMPLITUDE (dB)
0	0.00	–44.1
1	14.89	–0.2
2	29.79	–82.2
3	44.68	–62.7
4	59.58	–90.0
5	74.47	–67.8
6	89.37	–95.5
7	104.26	–70.5
8	119.16	–96.4
9	134.05	–72.7
10	148.95	–99.8

Figure 19. Acquisition Time of 190ns

Measurement Parameters

Clock Frequency = 6.8MHz
Sampling Frequency = 425kHz
Sample Size = 8192 points
Input Frequency = 14,993.2861Hz
Number of Cycles = 289 cycles
Acquisition Time = 210ns



SNR = 68.3dB
SND = 63.2dB
SFR = 66.7dB
THD = –64.8dB

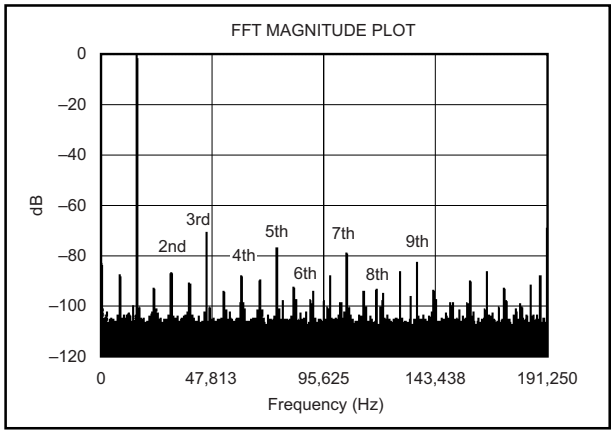
Harmonics for 210ns Acquisition Time

HARMONIC (N)	FREQUENCY (kHz)	AMPLITUDE (dB)
0	0.00	–40.5
1	14.99	–0.2
2	29.99	–84.4
3	44.98	–66.7
4	59.97	–88.9
5	74.97	–72.4
6	89.96	–97.7
7	104.95	–74.4
8	119.95	–95.7
9	134.94	–76.7
10	149.93	–101.5

Figure 20. Acquisition Time of 210ns

Measurement Parameters

Clock Frequency = 6.12MHz
Sampling Frequency = 382.5kHz
Sample Size = 8192 points
Input Frequency = 14,988.0981Hz
Number of Cycles = 321 cycles
Acquisition Time = 234ns



SNR = 70.4dB
SND = 66.7dB
SFR = 71.0dB
THD = –69.1dB

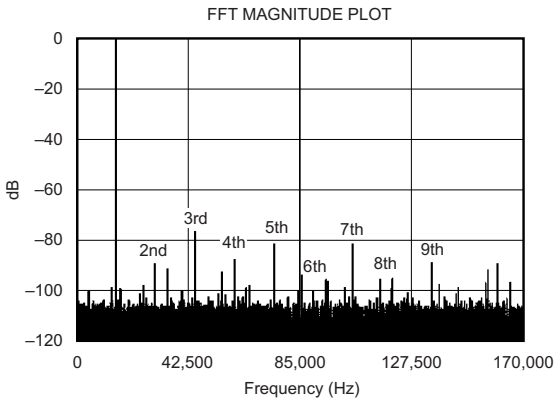
Harmonics for 234ns Acquisition Time

HARMONIC (N)	FREQUENCY (kHz)	AMPLITUDE (dB)
0	0.00	–39.9
1	14.99	–0.2
2	29.98	–86.8
3	44.96	–71.0
4	59.95	–87.8
5	74.94	–76.7
6	89.93	–99.3
7	104.92	–78.5
8	119.90	–97.8
9	134.89	–82.5
10	149.88	–101.3

Figure 21. Acquisition Time of 234ns

Measurement Parameters

Clock Frequency = 5.44MHz
Sampling Frequency = 340kHz
Sample Size = 8192 points
Input Frequency = 14,982.9102Hz
Number of Cycles = 361 cycles
Acquisition Time = 265ns



SNR = 71.3dB
SND = 69.4dB
SFR = 76.1dB
THD = –73.7dB

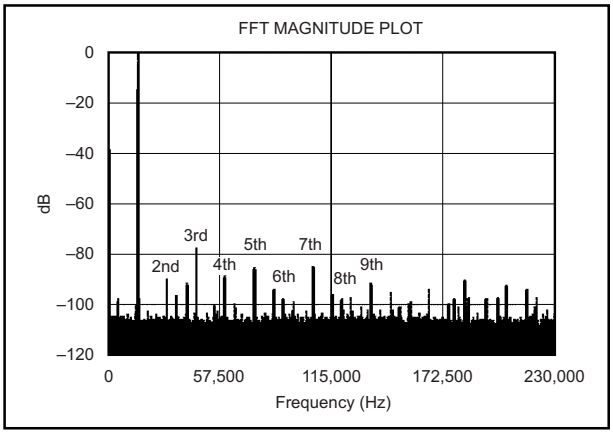
Harmonics for 265ns Acquisition Time

HARMONIC (N)	FREQUENCY (kHz)	AMPLITUDE (dB)
0	0.00	–39.3
1	14.98	–0.2
2	29.97	–89.3
3	44.95	–76.3
4	59.93	–87.2
5	74.91	–81.9
6	89.90	–100.4
7	104.88	–81.9
8	119.86	–98.9
9	134.85	–88.3
10	149.83	–103.1

Figure 22. Acquisition Time of 265ns

Measurement Parameters

Clock Frequency = 7.82MHz
Sampling Frequency = 460kHz
Sample Size = 8192 points
Input Frequency = 14,992.6758Hz
Number of Cycles = 267 cycles
Acquisition Time = 309ns



SNR = 71.4dB
SND = 70.0dB
SFR = 77.5dB
THD = –75.6dB

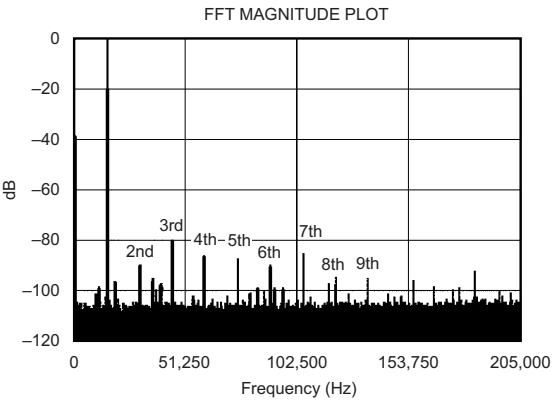
Harmonics for 309ns Acquisition Time

HARMONIC (N)	FREQUENCY (kHz)	AMPLITUDE (dB)
0	0.00	–39.0
1	14.99	–0.2
2	29.99	–90.6
3	44.98	–77.5
4	59.97	–88.5
5	74.96	–85.5
6	89.96	–98.0
7	104.95	–84.7
8	119.94	–98.1
9	134.93	–91.6
10	149.93	–100.7

Figure 23. Acquisition Time of 309ns

Measurement Parameters

Clock Frequency = 6.97MHz
Sampling Frequency = 410kHz
Sample Size = 8192 points
Input Frequency = 14,964.5996Hz
Number of Cycles = 299 cycles
Acquisition Time = 348ns



SNR = 71.4dB
SND = 70.5dB
SFR = 80.7dB
THD = –77.7dB

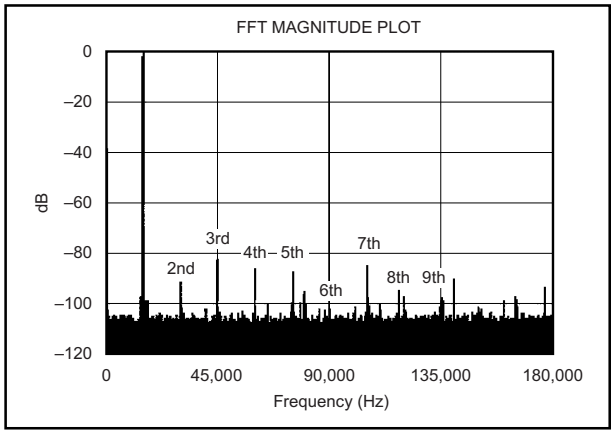
Harmonics for 348ns Acquisition Time

HARMONIC (N)	FREQUENCY (kHz)	AMPLITUDE (dB)
0	0.00	–38.9
1	14.96	–0.2
2	29.93	–89.8
3	44.89	–80.7
4	59.86	–86.8
5	74.82	–87.2
6	89.79	–102.6
7	104.75	–85.7
8	119.72	–97.6
9	134.68	–95.3
10	149.65	–103.0

Figure 24. Acquisition Time of 348ns

Measurement Parameters

Clock Frequency = 6.12MHz
Sampling Frequency = 360kHz
Sample Size = 8192 points
Input Frequency = 14,985.3516Hz
Number of Cycles = 341 cycles
Acquisition Time = 397ns



SNR = 71.5dB
SND = 70.7dB
SFR = 82.7dB
THD = –78.6dB

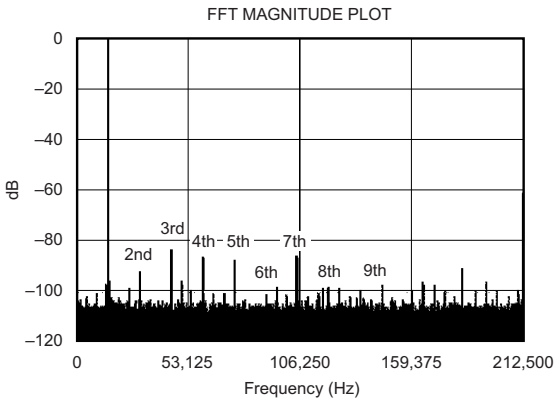
Harmonics for 397ns Acquisition Time

HARMONIC (N)	FREQUENCY (kHz)	AMPLITUDE (dB)
0	0.00	–38.9
1	14.99	–0.2
2	29.97	–91.6
3	44.96	–82.7
4	59.94	–86.4
5	74.93	–87.3
6	89.91	–102.3
7	104.90	–85.1
8	119.88	–97.5
9	134.87	–99.0
10	149.85	–101.2

Figure 25. Acquisition Time of 397ns

Measurement Parameters

Clock Frequency = 7.65MHz
Sampling Frequency = 425kHz
Sample Size = 8192 points
Input Frequency = 14,993.2861Hz
Number of Cycles = 289 cycles
Acquisition Time = 447ns



SNR = 71.4dB
SND = 70.8dB
SFR = 83.5dB
THD = –79.2dB

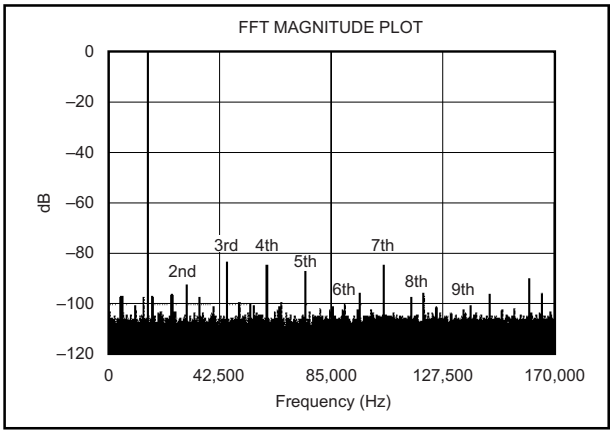
Harmonics for 447ns Acquisition Time

HARMONIC (N)	FREQUENCY (kHz)	AMPLITUDE (dB)
0	0.00	–38.7
1	14.99	–0.2
2	29.99	–92.2
3	44.98	–83.5
4	59.97	–86.6
5	74.97	–87.8
6	89.96	–100.8
7	104.95	–86.0
8	119.95	–98.7
9	134.94	–99.5
10	149.93	–102.5

Figure 26. Acquisition Time of 447ns

Measurement Parameters

Clock Frequency = 6.12MHz
Sampling Frequency = 340kHz
Sample Size = 8192 points
Input Frequency = 14,982.9102Hz
Number of Cycles = 361 cycles
Acquisition Time = 561ns



SNR = 71.7dB
SND = 71.0dB
SFR = 84.0dB
THD = –79.0dB

Harmonics for 561ns Acquisition Time

HARMONIC (N)	FREQUENCY (kHz)	AMPLITUDE (dB)
0	0.00	–40.0
1	14.98	–0.2
2	29.97	–93.0
3	44.95	–84.5
4	59.93	–85.1
5	74.91	–88.3
6	89.90	–100.3
7	104.88	–85.1
8	119.86	–96.2
9	134.85	–102.9
10	149.83	–103.0

Figure 27. Acquisition Time of 447ns

Revision History

Changes from Original (October 2002) to A Revision	Page
• Changed format of entire document to the latest template.	1

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

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