RETRIEVING DATA FROM THE DDC112

by Jim Todsen

This application bulletin explains how to retrieve data from the DDC112. It elaborates on the discussion given in the DDC112 data sheet and provides additional information to allow you more flexibility during retrieval. It is assumed that you have a basic understanding of the DDC112's operation. For a good introduction to the DDC112, see the DDC112's data sheet.

There are three main sections to this bulletin. First, the basic operation of data retrieval is explained for a single DDC112 system. Next, a circuit and timing diagram are discussed that use additional logic circuits to convert the serial bitstream from the DDC112 into multi-bit words for parallel readback. Finally, data retrieval considerations for multiple DDC112 systems are covered.
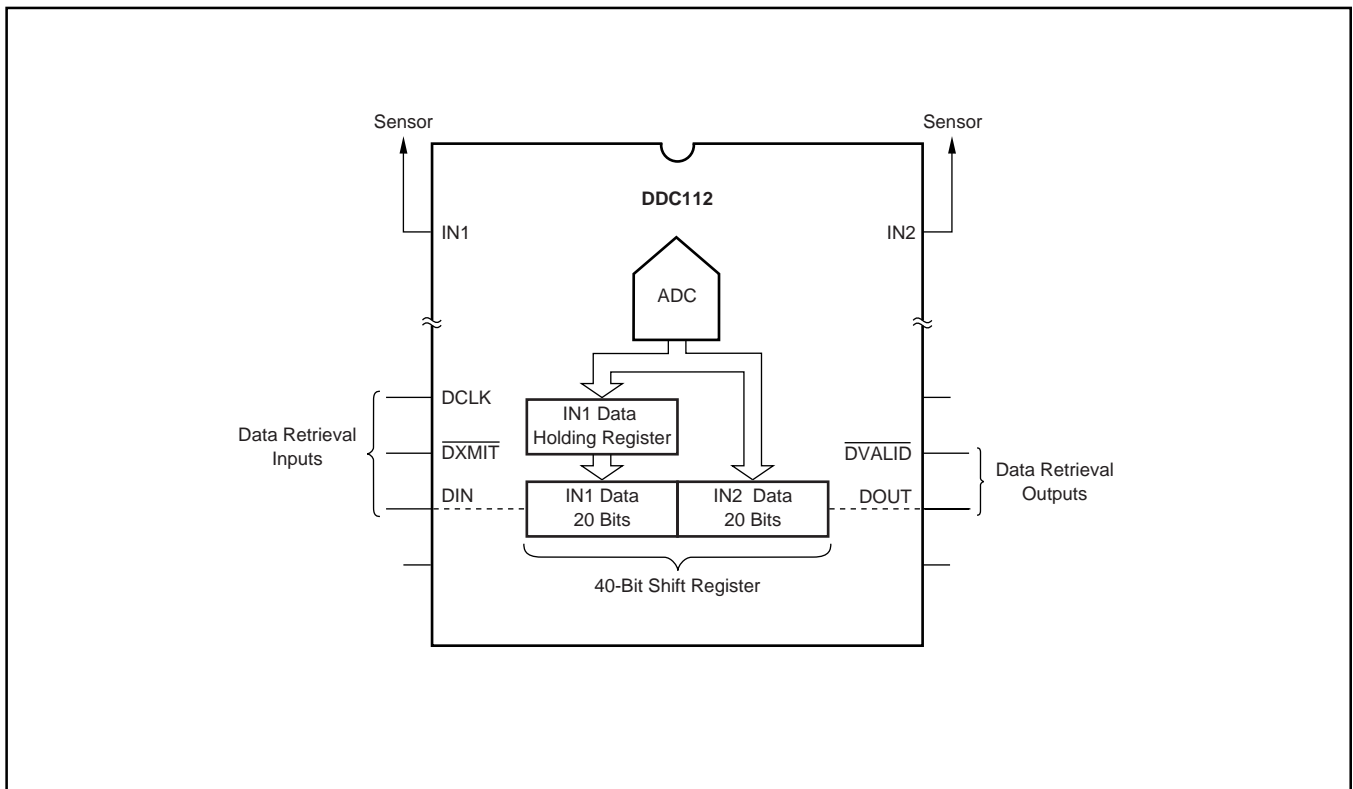

FIGURE 1. Serial Interface Block Diagram.

BASIC OPERATION

The DDC112 uses the same serial interface as used in the DDC101. This interface uses five I/O pins and allows multiple DDC112s to be daisy-chained together in multi-sensor systems. Figure 1 shows a diagram of the data retrieval pins and internal registers. Figure 2 provides the accompanying timing diagram. The DDC112 uses a single analog-to-digital converter (ADC) to measure both IN1 and IN2. A holding register temporarily stores IN1's data while IN2's data is being generated. When IN2 is finished being measured, both IN1 and IN2 data are loaded into the DDC112's 40-bit shift register. You have until the next conversion completes to retrieve the data as the shift register is automatically updated when new data is ready.

The DDC112 indicates data is ready by taking $\overline{\text{DVALID}}$ LO (see Figure 2). When ready to retrieve the data, take $\overline{\text{DXMIT}}$ LO to enable DOUT. $\overline{\text{DVALID}}$ now returns HI. The DDC112 shifts data out on the falling edge of DCLK, therefore, read DOUT on the rising edge of DCLK. When finished retrieving the data, return $\overline{\text{DXMIT}}$ HI. DIN allows daisy-chaining of multiple DDC112s by feeding DOUT from one DDC112 into the next DDC112's DIN. When not used, DIN should be tied to either ground or V_{DD}.

DCLK is completely independent of CLK and is used solely to retrieve data. When not retrieving data, freeze DCLK to reduce digital noise coupling into the front-end integrators. DCLK can be held either HI or LO when not in use. If held HI, it must be returned LO before $\overline{\text{DXMIT}}$ goes LO (t_3 in Figure 2). If this condition is violated, bit 20 (MSB) will be lost and the first bit out will be bit 19.

You can read the data *before*, *after,* or *before and after* CONV toggles as described in the last section on multiple DDC112 systems. Never retrieve data while CONV toggles. That is, make sure the serial interface is inactive at the end and beginning of the integration period to prevent digital noise coupling into the front end.

If you decide not to retrieve the data on a particular conversion, leave $\overline{\text{DXMIT}}$ HI. $\overline{\text{DVALID}}$ will pulse HI for 1.2μs (for CLK = 10MHz) when the data is first ready and then stay LO the remainder of the time. Wait until the next $\overline{\text{DVALID}}$ pulse to begin retrieval when ready.
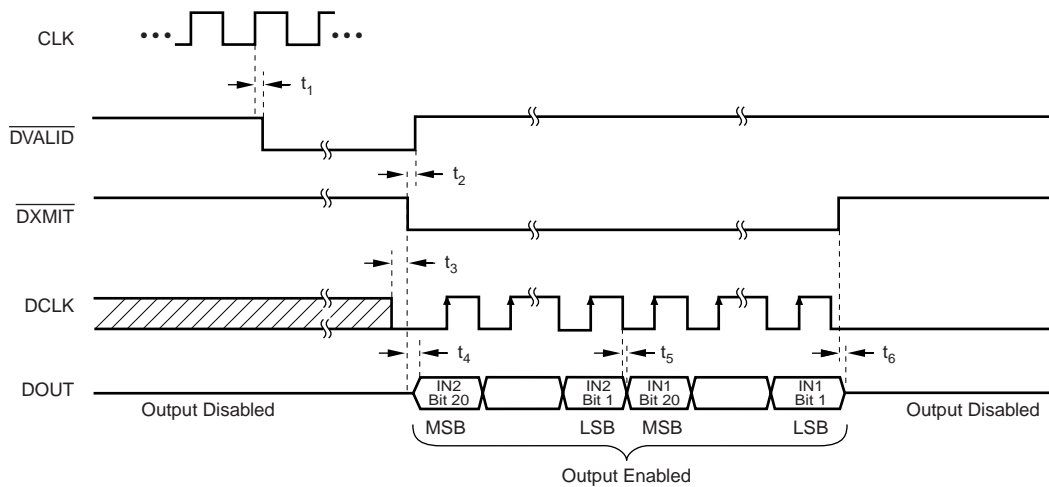
SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNITS
t_1	Propagation Delay from Rising Edge of CLK to $\overline{\text{DVALID}}$ LO	30			ns
t_2	Propagation Delay from $\overline{\text{DXMIT}}$ LO to $\overline{\text{DVALID}}$ HI	30			ns
t_3	Setup Time for DCLK LO Before $\overline{\text{DXMIT}}$ LO		20		ns
t_4	Propagation Delay from $\overline{\text{DXMIT}}$ LO to DOUT Enabled			30	ns
t_5	Hold Time for DOUT After Falling Edge of DCLK	5			ns
t_6	Propagation Delay from $\overline{\text{DXMIT}}$ HI to DOUT Disabled		30		ns

FIGURE 2. Timing Diagram for Data Retrieval.

EXAMPLE OF PARALLEL DATA RETRIEVAL

Sometimes it is desirable to have a parallel interface for retrieving data from the DDC112. This is easy to accomplish with a few additional components. Figure 3 shows one possibility. The circuit loads the serial data from the DDC112 into an 8-bit shift register for parallel retrieval. Five parallel retrievals are then needed to get all 40 bits from the DDC112.

CLK is typically 10MHz and the signal "DX" is generated by the user. $\overline{\text{DVALID}}$ can be monitored to determine when data is ready (it is also possible to determine when data is ready from CONV's status as described in Application Bulletin AB-131). As shown in Figure 4, DX is taken HI by the user once $\overline{\text{DVALID}}$ goes LO. The negative edge of CLK triggers the D flip-flop which sets $\overline{\text{DXMIT}}$ LO. The Q output of the flip-flop enables DCLK via the AND gate. The propagation delay of the inverter and D flip-flop insure that DCLK is LO and glitch-free when $\overline{\text{DXMIT}}$ goes LO to meet setup time t_3 in Figure 2. DCLK clocks both the DDC112 and the 8-bit shift register (a 74HC164 for example). After 8 DCLKs, DX is taken HI to pause the serial shifting. During this pause, the parallel data from the shift register is retrieved. Afterwards, DX is taken LO and another 8 bits are shifted into the register. The cycle continues until all 40 bits are retrieved. R_P pulls up DOUT when disabled to keep it from floating.

$\overline{\text{DXMIT}}$ must be LO for DCLK to shift data in the DDC112s internal 40-bit shift register. If $\overline{\text{DXMIT}}$ is HI, DCLK is then ignored by the DDC112. Though not the case in Figure 3, DCLK could have been left running during the pause used for reading the parallel data.
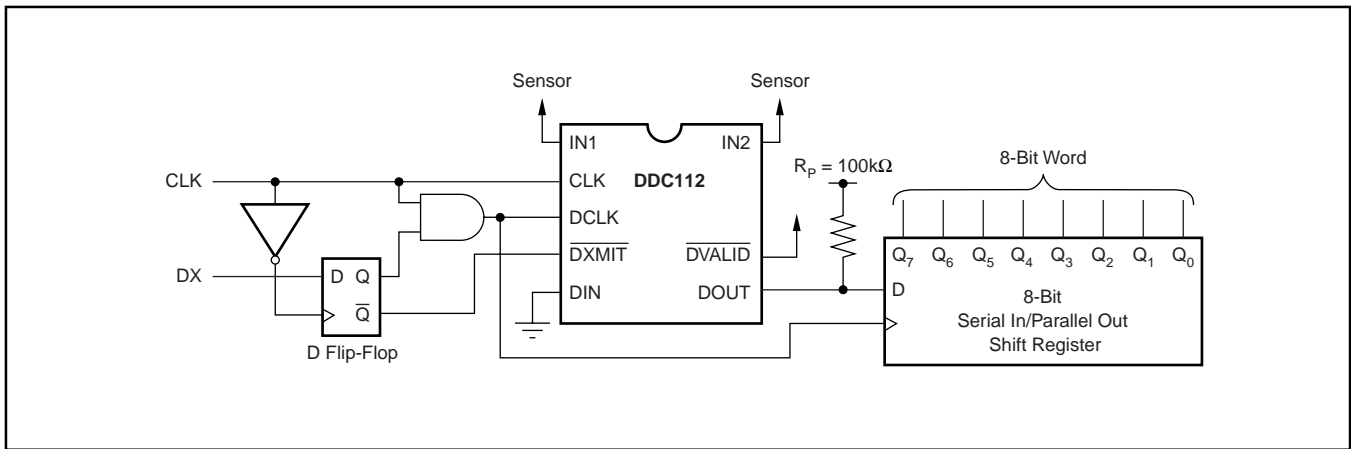

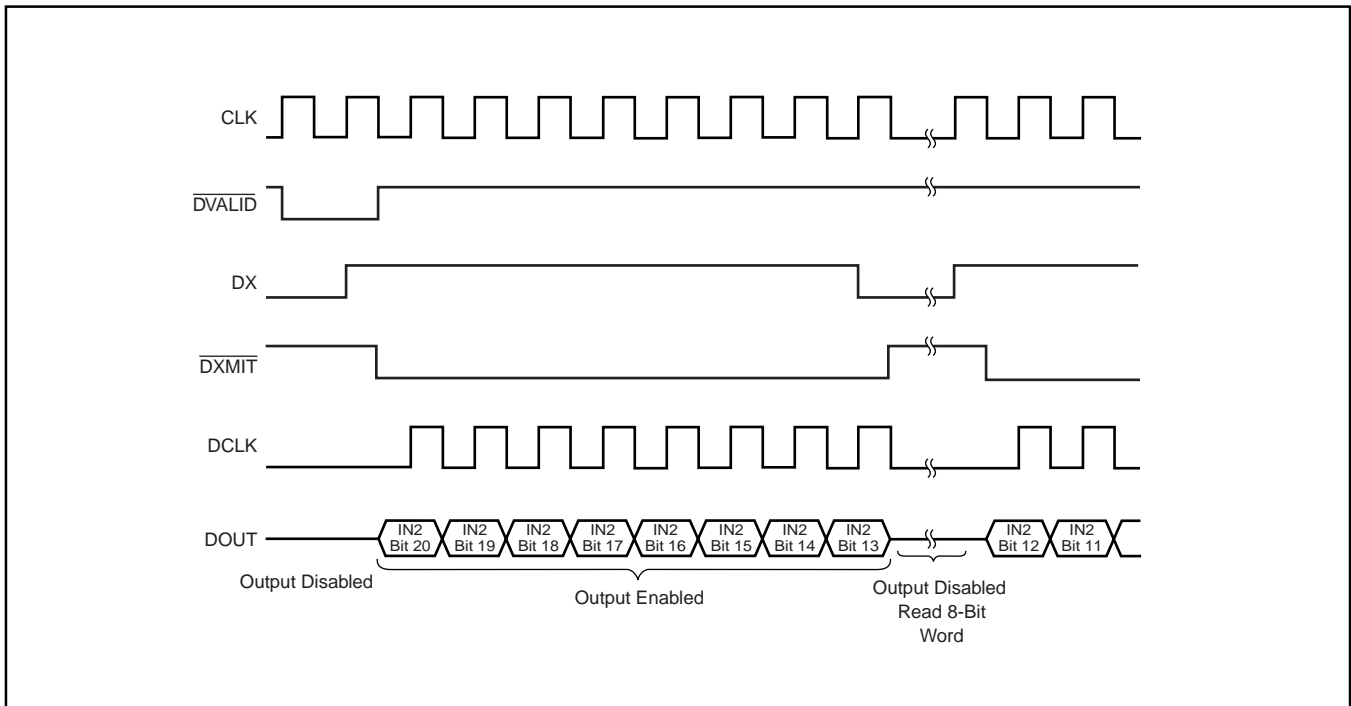FIGURE 3. Example Circuit for Parallel Data Retrieval.

FIGURE 4. Timing Diagram for the Circuit in Figure 3.

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MULTIPLE DDC112 SYSTEMS

The DDC112's serial interface allows daisy-chaining of multiple DDC112s. This is especially useful in systems with lots of sensors requiring lots of DDC112s. Figure 5 shows an example of a 3 DDC112 system used to measure 6 sensors. DOUT from one DDC112 is fed into DIN of the next essentially creating a giant shift register with 120 bits. A pull-up resistor is used on DOUT to prevent it from floating when disabled. As can be seen from Figure 6, the timing diagram for a multiple DDC112 system is very similar to that of a single DDC112 system. All of the timing specifications in Figure 2 apply plus an additional specification: t_7. $\overline{\text{DXMIT}}$ must be HI before new data is loaded. This condition also applies to a single DDC112 system but, is much more likely to be violated in multiple DDC112 systems where more time is needed for data retrieval.

For very large systems, it is possible to have transmission line effects on the digital signals since the traces get lengthy and there is large capacitive loading from the multiple DDC112s. DCLK is particularly sensitive as reflections can cause glitches resulting in unwanted shifting of the data. Make sure to use good digital design techniques to avoid these problems. Consider using multiple DCLK lines to reduce the number of DDC112s connected to a particular DCLK line. Terminating the lines can also help.

The data must not be retrieved while CONV toggles so as to prevent digital noise coupling to the front integrators. For very large systems, the time required can become large and care must be used in deciding when to retrieve. There is no absolute limit on the number of DDC112s that can be daisy-chained together. The maximum number of DDC112s is limited by the time available for data retrieval which depends on the integration time (T_{INT}). The different retrieval options for the continuous mode are discussed below, followed by some considerations for using the noncontinuous mode.
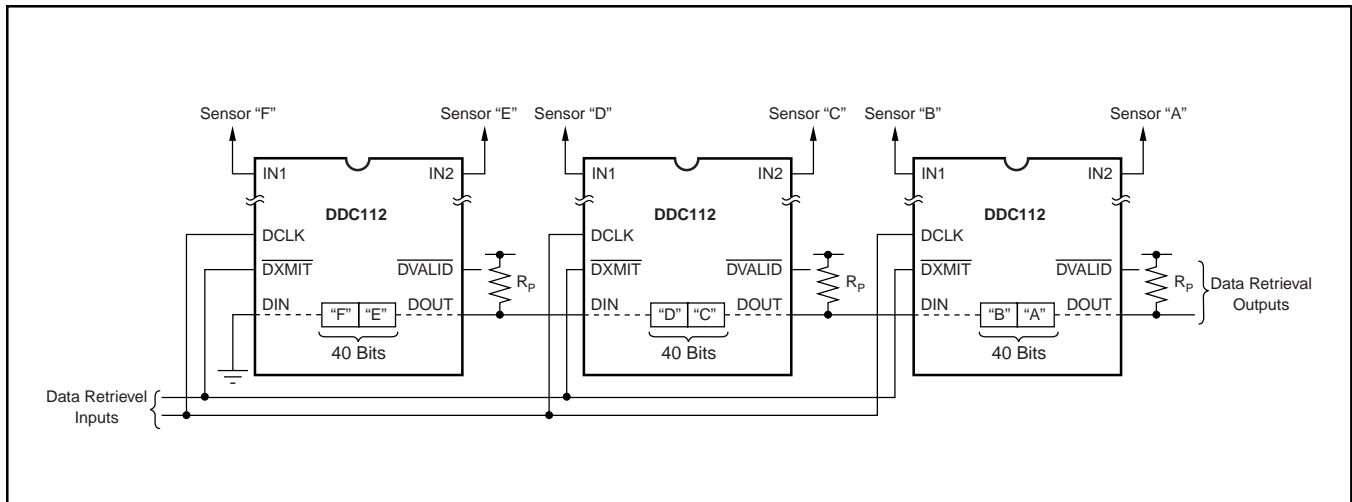
FIGURE 5. Multiple DDC112 Daisy Chain.

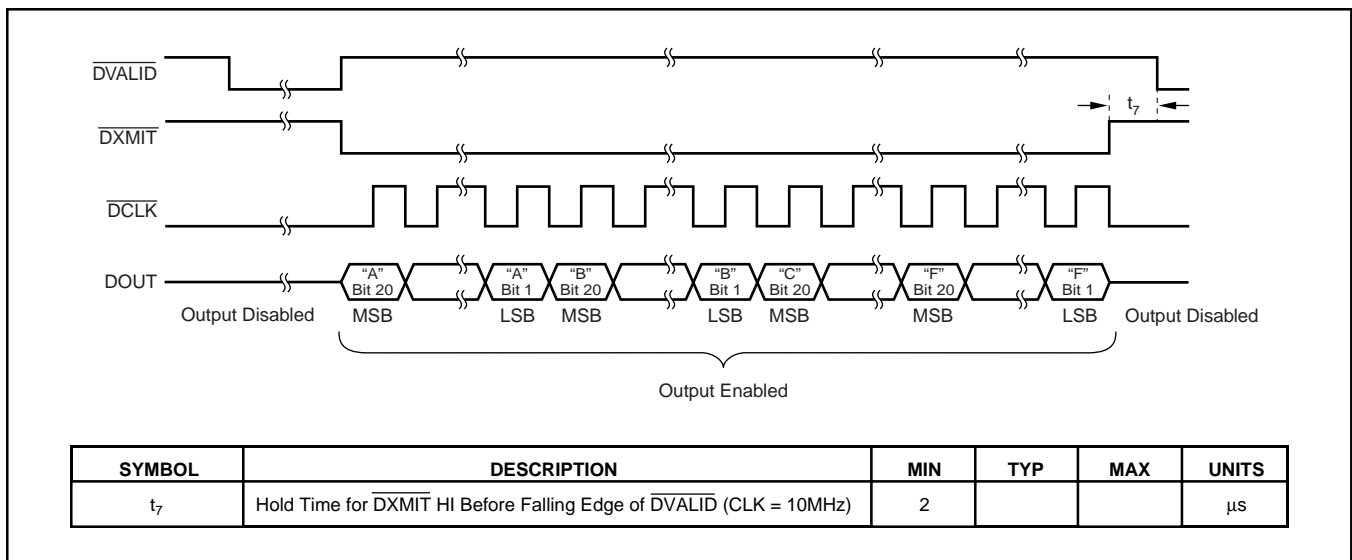| SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNITS
t_7	Hold Time for $\overline{\text{DXMIT}}$ HI Before Falling Edge of $\overline{\text{DVALID}}$ (CLK = 10MHz)	2			µs

FIGURE 6. Timing Diagram for Multiple DDC112 Data Retrieval.

RETRIEVAL *BEFORE* CONV TOGGLES (CONTINUOUS MODE)

This is the most straightforward method. Data retrieval begins soon after $\overline{\text{DVALID}}$ goes LO and finishes before CONV toggles, see Figure 7. For best performance, data retrieval must stop t_9 before CONV toggles. This method is the most appropriate for longer integration times. The maximum time available for readback is $T_{INT} - t_8 - t_9$. For DCLK and CLK = 10MHz, the maximum number of DDC112s that can be daisy-chained together is:

$$\frac{T_{INT} - 431.2\mu s}{40\tau_{DCLK}}$$

Where τ_{DCLK} is the period of the data clock. For example, if $T_{INT} = 1000\mu s$ and DCLK = 10MHz, the maximum number of DDC112s is:

$$\frac{1000\mu s - 431.2\mu s}{(40)(100 ns)} = 142.2 \rightarrow 142 \text{ DDC112s}$$

RETRIEVAL *AFTER* CONV TOGGLES (CONTINUOUS MODE)

For shorter integration times, more time is available if data retrieval begins after CONV toggles and ends before the new data is ready. Data retrieval must wait t_{10} after CONV toggles before beginning. Figure 8 shows an example of this. The maximum time available for retrieval is $t_8 - t_{10} - t_7$ (421.2μs – 10μs – 2μs for CLK = 10MHz), regardless of T_{INT}. The maximum number of DDC112s that can be daisy-chained together is:

$$\frac{409.2\mu s}{40\tau_{DCLK}}$$

For DCLK = 10MHz, the maximum number of DDC112s is 102.

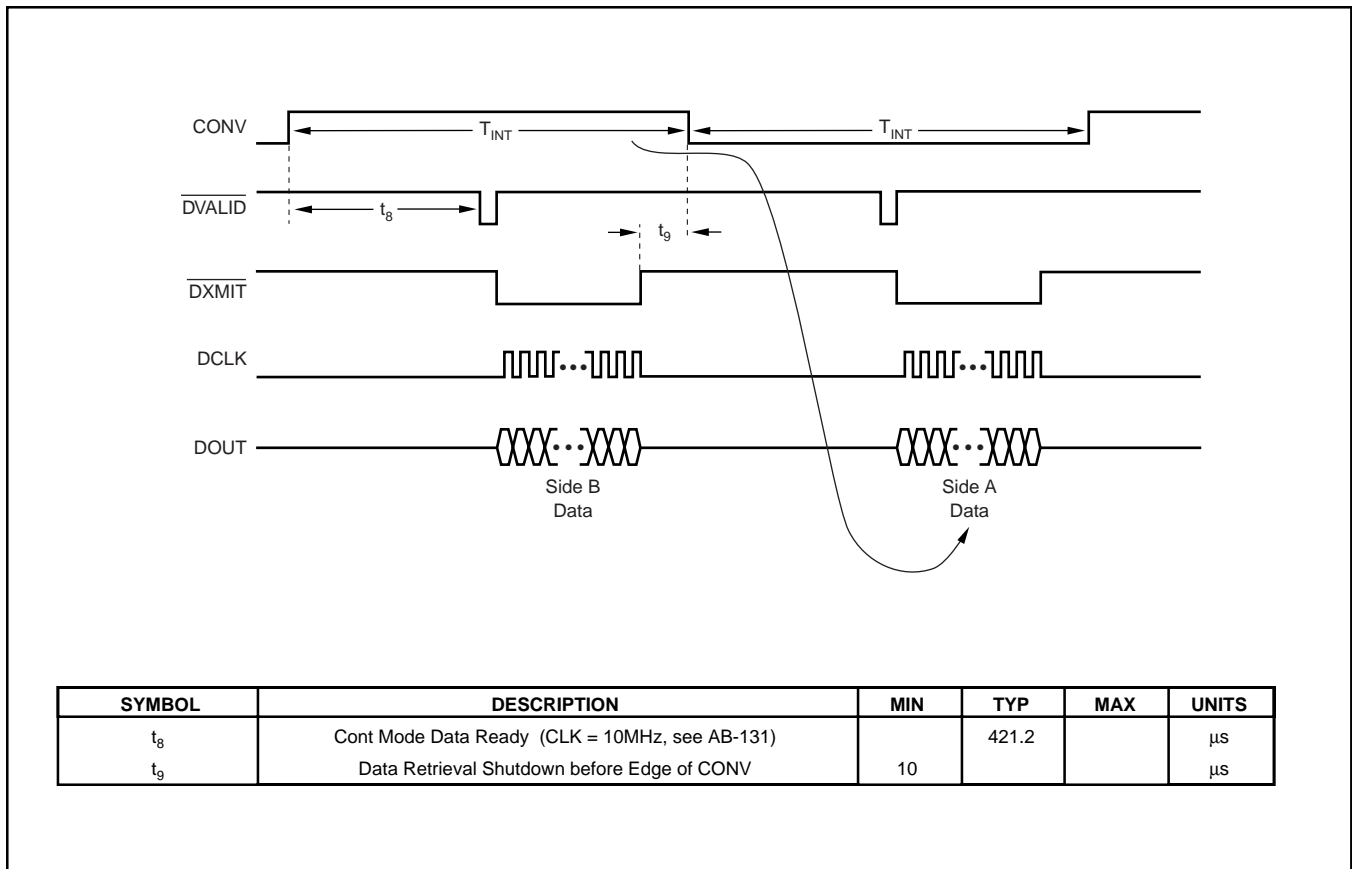| SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNITS
t_8	Cont Mode Data Ready (CLK = 10MHz, see AB-131)		421.2		μs
t_9	Data Retrieval Shutdown before Edge of CONV	10			μs

FIGURE 7. Readback *Before* CONV Toggles.

RETRIEVAL *BEFORE AND AFTER* CONV TOGGLES (CONTINUOUS MODE)

For the absolute maximum time for data retrieval, data can be retrieved *before and after* CONV toggles. Nearly all of T_{INT} is available for data retrieval. Figure 9 illustrates how this is done by combining the two previous methods. You must pause the retrieval during CONV's toggling to prevent digital noise, as discussed previously, and finish before the next data is ready. The maximum number of DDC112s that can be daisy-chained together is:

$$\frac{T_{INT} - 20\mu s - 2\mu s}{40\tau_{DCLK}}$$

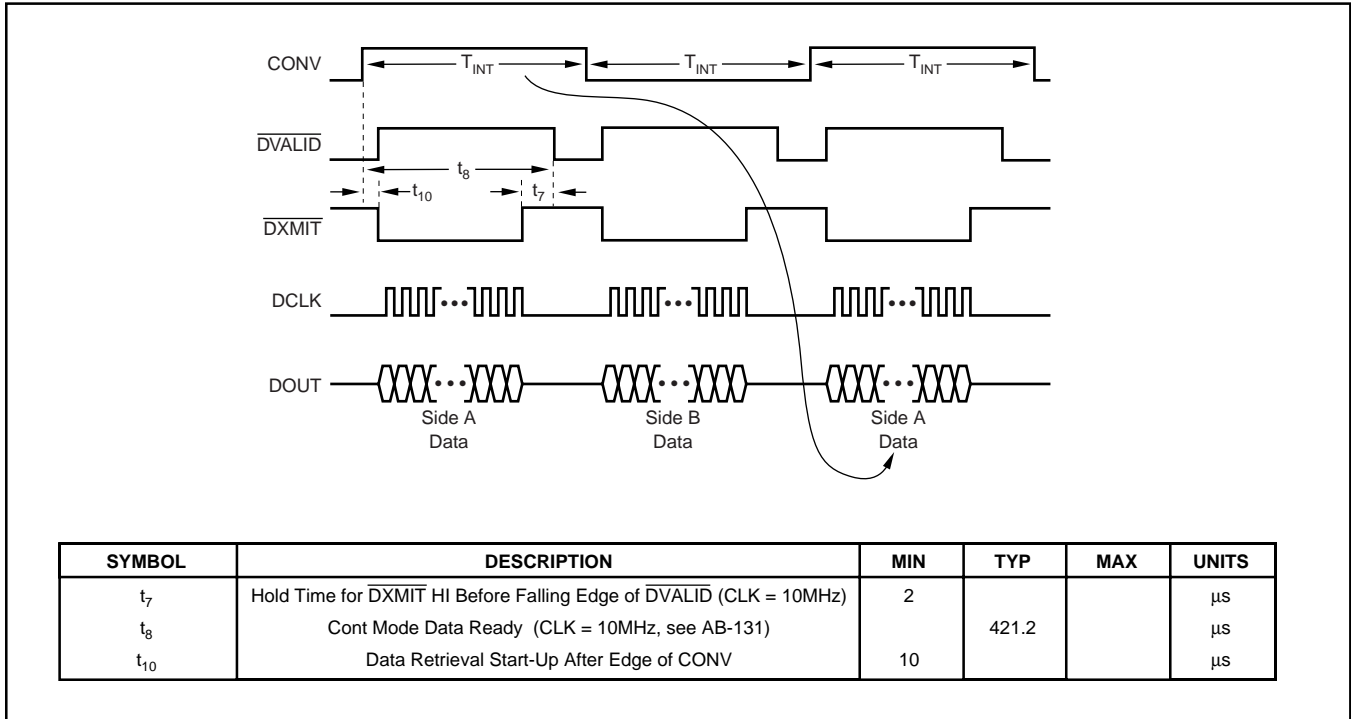For $T_{INT} = 500\mu s$ and DCLK = 10MHz, the maximum number of DDC112s is 119.

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNITS
t_7	Hold Time for $\overline{DXMIT}$ HI Before Falling Edge of $\overline{DVALID}$ (CLK = 10MHz)	2			μs
t_8	Cont Mode Data Ready (CLK = 10MHz, see AB-131)		421.2		μs
t_{10}	Data Retrieval Start-Up After Edge of CONV	10			μs

FIGURE 8. Readback *After* CONV Toggles.

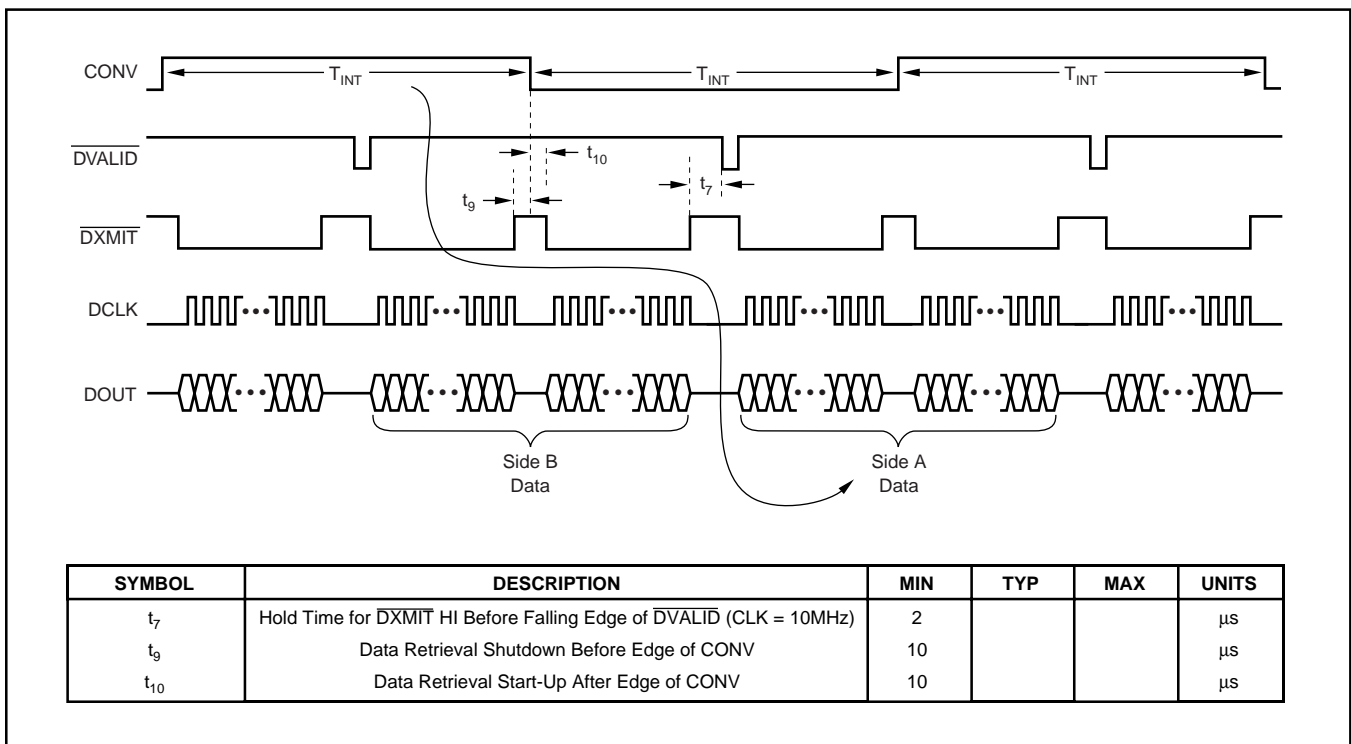| SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNITS
t_7	Hold Time for $\overline{DXMIT}$ HI Before Falling Edge of $\overline{DVALID}$ (CLK = 10MHz)	2			μs
t_9	Data Retrieval Shutdown Before Edge of CONV	10			μs
t_{10}	Data Retrieval Start-Up After Edge of CONV	10			μs

FIGURE 9. Readback *Before and After* CONV Toggles.

RETRIEVAL: NONCONTINUOUS MODE

Retrieving in noncontinuous mode is slightly different as compared with the continuous mode. As shown in Figure 10 and described in detail in Application Bulletin AB-131, $\overline{\text{DVALID}}$ goes LO in time t_{11} after the first integration completes. If T_{INT} is shorter than this time, all of t_{12} is available to retrieve data before the other side's data is ready.

For $T_{INT} > t_{11}$, the first integration's data is ready before the second integration completes. Data retrieval must be delayed until the second integration completes leaving less time available for retrieval. The time available is $t_{12} - (T_{INT} - t_{11})$. The second integration's data must be retrieved before the next round of integrations begin. This time is highly dependent on the pattern used to generate CONV. As with the continuous mode, data retrieval must halt before and after CONV toggles (t_9, t_{10}) and be completed before new data is ready (t_7).

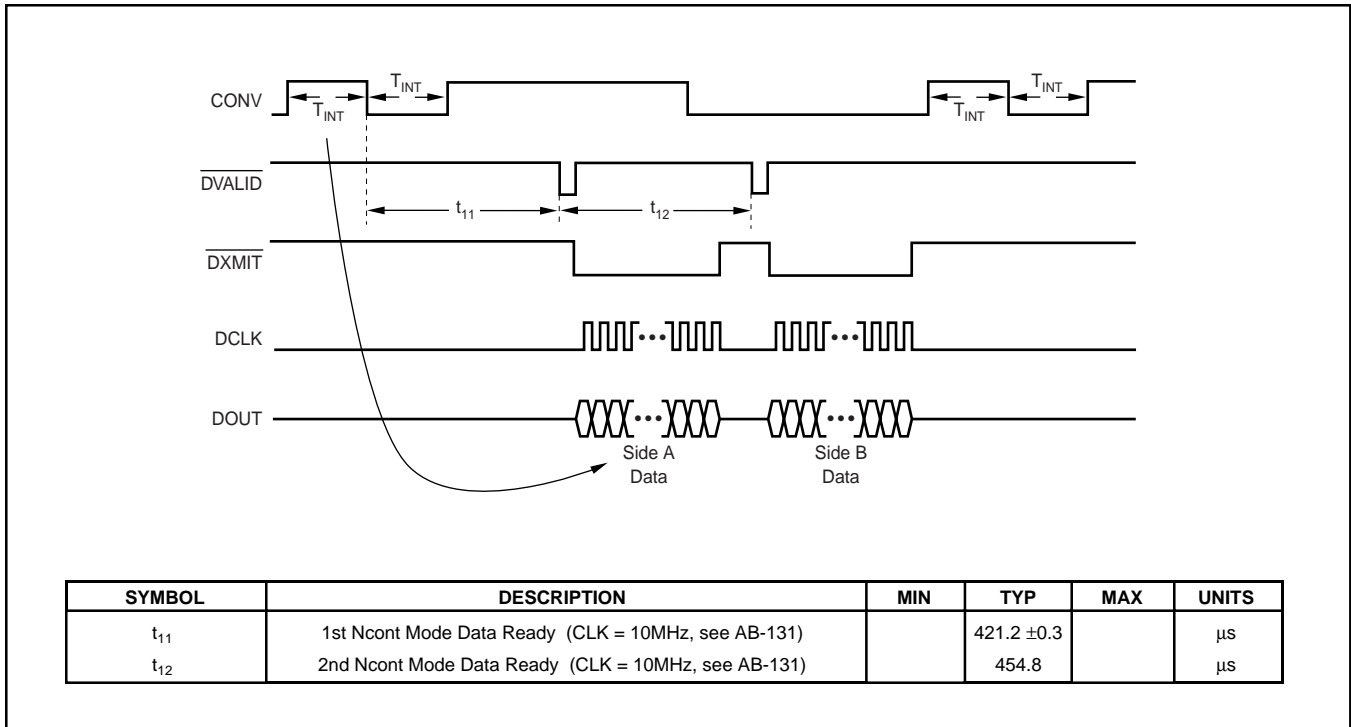| SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNITS
t_{11}	1st Ncont Mode Data Ready (CLK = 10MHz, see AB-131)		421.2 ±0.3		μs
t_{12}	2nd Ncont Mode Data Ready (CLK = 10MHz, see AB-131)		454.8		μs

FIGURE 10. Readback in Noncontinuous Mode.

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