Application Report
DLPA080–August 2017

PCB Design Requirements for TI DLP® Standard TRP Digital Micromirror Devices

ABSTRACT

This application report summarizes the printed-circuit board (PCB) layout and PCB design requirements for systems that use a TRP digital micromirror device (DMD) in combination with any DLPC4422 display controller, the DLPA100 power management device, and the TPS65145 power regulator.

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1 Introduction

NOTE: The information in this document is not a substitute for the specifications listed in the corresponding device data sheets. In the event of a discrepancy, the data sheet supersedes this application report.

CAUTION

Adhere to the design guidelines or the published device specifications to help avoid permanent damage to the devices.

2 Related Documentation

For related documentation, see the following:

- *DLPC4422 DLP® Display Controller* (DLPS074), including DLPC4422
- *DLPA100 Power Management and Motor Driver* (DLPS082)
- *TPS6514x Triple Output LCD Supply With Linear Regulator and Power Good* (SLVS497)
- *DLP660TE 0.66 4K UHD DMD* (DLPS072)
- *DLP470NE 0.47 1080P DMD* (DLPS091)
- *DLP480RE 0.48 WUXGA DMD* (DLPS092)

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3 Connectivity Guidelines

3.1 Dual ASIC DMD Electrical Connections

Figure 1 shows the *DLP660TE 0.66 4K UHD DMD* (DLPS072) and how it is driven in a DLP® projection system.

- The DLPC4422 device provides the data and control.
- The DLPA100 supplies the power for the DLPC4422 and the TPS65145 supplies power for the DMD.

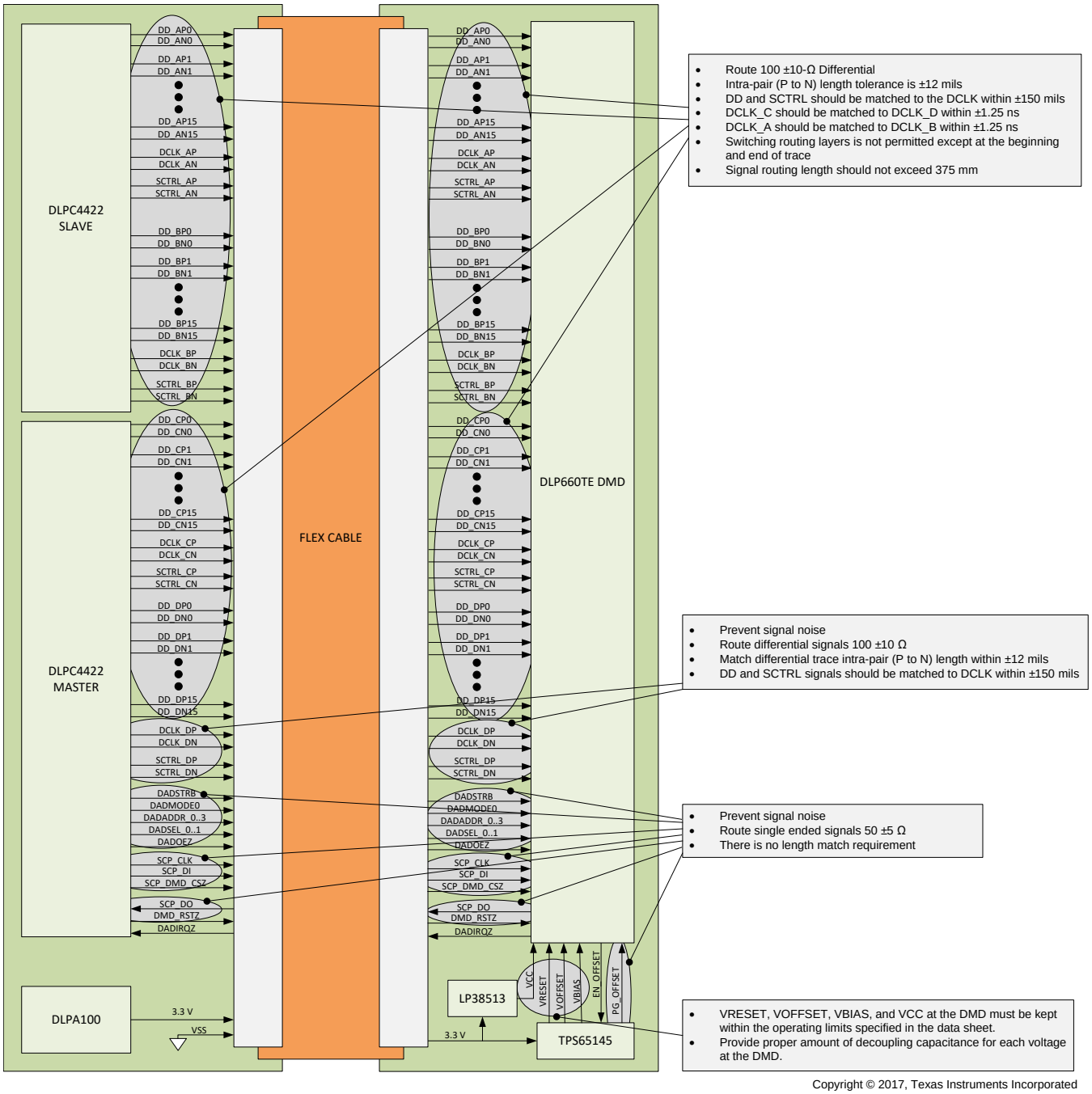

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Figure 1. DLP660TE 4K UHD DMD Projection System

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3.2 Single ASIC DMD Electrical Connections

Figure 2 shows the *DLP470NE 1080p DMD* and how it is driven in a DLP projection system. The *DLP480RE WUXGA DMD* is also driven in the same manner.

- The DLPC4422 device provides the data and control.
- The DLPA100 supplies the power for the DLPC4422 and the TPS65145 supplies power for the DMD.

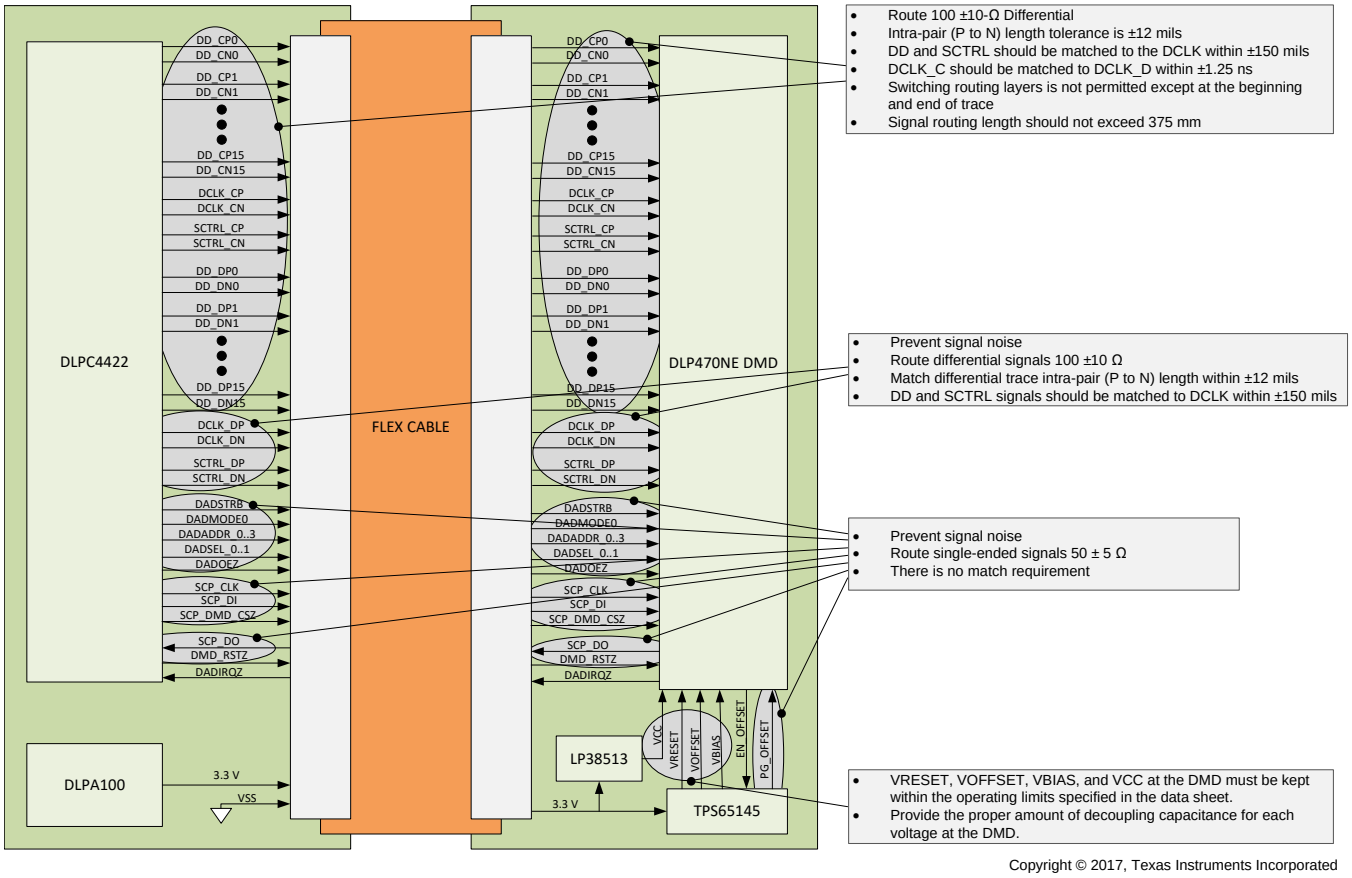

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Figure 2. DLP470NE 1080p DMD DLP Projection System

The guidelines shown in Figure 1 and Figure 2 are summaries taken from *DLPC4422 DLP® Display Controller* (DLPC4422), *DLPA100 Power Management and Motor Driver* (DLPS082), and *TPS6514x Triple Output LCD Supply With Linear Regulator and Power Good* (SLVS497F).

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3.3 Power Connections

- VOFFSET, VBIAS, VRESET, VCC, and VCCI power rails must be kept within the specified operating range; *this includes effects from ripple and DC error*.
  - To accommodate power supply transient current requirements, adequate decoupling capacitance must be placed near the DMD VOFFSET, VBIAS, VRESET, VCC, and VCCI pins.
- Do not swap DMDs while the DMD is still powered on (this is called hot swapping). All DMD power supply rails and signals must be 0 volts (not driven) before connecting or disconnecting the DMD physical interface.
- Do not allow power to be applied to the DMD when one or more signal pins are not being driven.
- Decoupling capacitor consideration: some layout consideration for the decoupling capacitors is to ensure the device is as close as possible to the DMD. The pads of the capacitors should be connected to at least two or three vias to get a low impedance to ground, shown in Figure 3. Furthermore, the capacitor should be in the flow of the power trace as it goes to the input of the DMD.
- Adhere to the power-up and power-down procedures specified in the DMD data sheet and in this document, and do not allow the DMD power-supply levels to be outside of the recommended operating conditions specified in the DMD data sheet.

Figure 3. Decoupling Capacitor Example

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3.4 Signal Noise Definition

During operation, it is critical to prevent the coupling of noise or intermittent power connections onto the following signals because *irreversible DMD micromirror array damage* or lesser effects of image disruption can occur:

- SCTRL_DN, STRL_DP
- DCLK_DN, DCLK_DP
- SCPCLK
- SCPDI
- SCP_DMD_CSZ
- DADADDR_0, DADADDR1_1, DADADDR_2, DADADDR_3
- DADMODE0
- DADSEL_0, DADSEL_1, DADSEL_2, DADSEL_3
- DADSTRB
- DMD_RSTZ
- DADOEZ
- PG_OFFSET

In this context, the following conditions are considered noise:

- Shorting to another signal
- Shorting to power
- Shorting to ground
- Intermittent connection (includes hot swapping)
- An electrical open condition
- An electrical floating condition
- Inducing electromagnetic interference that is strong enough to affect the integrity of the signals
- Unstable inputs (conditions outside of the specified operating range) to any of the device power rails
- Voltage fluctuations on the device ground pins

4 DMD Power Up and Power Down

The manner in which the DMD is powered up and powered down is critical to its proper operation. Any variation in control signals or voltages outside the specified parameters has a high probability of causing irreversible DMD micromirror array damage. The TPS65145 and DLPA100 devices are designed to provide the required power-up and power-down sequences, provided that the conditions listed in Section 4.1 and Section 4.2 are met.

4.1 DMD Power Supply Power-Up Procedure

- VCC and VCCI must always start and settle before VOFFSET, VBIAS, and VRESET voltages are applied to the DMD. The LVCMOS input pins shall not be driven high until after VCC and VCCI have settled at operating voltages listed in the DMD data sheet.
- VBIAS and VOFFSET have a strict delta voltage requirement that should never exceed 10.5 V.
- There is no requirement for the relative timing of VRESET with respect to VBIAS.

Power supply slew rates during power up are flexible, provided that the transient voltage levels do not exceed the absolute maximum ratings. Always follow the supply voltage delta requirements, and always follow the power-up sequence requirements listed in the DMD data sheet.

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4.2 DMD Power Supply Power-Down Procedure

- VCC and VCCI must be supplied after VOFFSET, VBIAS, and VRESET voltages are discharged within the specified limit of ground in the DMD data sheet.
- VBIAS and VOFFSET have a strict delta voltage requirement that should not exceed 10.5 V.
- There is no requirement for the relative timing of VRESET with respect to VBIAS.
- LVCMOS input pins must be less than specified in the recommended operating conditions listed in the DMD data sheet.

Power supply slew rates during power down are flexible, provided that the transient voltage levels do not exceed the absolute maximum ratings. Always follow the supply voltage delta requirements, and always follow the power-down sequence requirements listed in the DMD data sheet.

5 Manufacturing Best Practices

To prevent possible DMD failures during system manufacturing, see the following best practices.

- Any device electrically interfacing to the DMD must follow all of the guidelines specified in this document and in the applicable data sheets; this includes cabling, test electronics, power distribution, on and off procedures, DMD connect and disconnect, and more.
- All connectors have an insertion and removal life. Insertion and removal cycles for connectors between the DLPC4422 and the DMD should not exceed the manufacturers stated lifetime maximum.
- Any and all Flexible Printed Circuits (FPCs) used in the factory should be designed in accordance with the guidelines specified in this document and the applicable data sheets.
- Optical engine production is typically a manual process requirement a human operator to connect the DMD, power on, assemble and test, power down, and disconnect. Every time this cycle is performed, there is a possibility of an operator error, such as:
  - Power on before connecting the DMD (hot plug).
  - Disconnecting the DMD before powering down (hot unplug).
  - Not fully mating the DMD to the test electronics.
  - Shorting or opening DMD control signals during active operation.

Texas Instruments™ Incorporated recommends to keep the number of assembly and test stations where the DMD is power cycled to a minimum; this reduces the probability of damage to the DMD due to operator error.

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Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Date	Revision	Description
August 2017	*	Initial release

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