Introduction to ±12 Degree Orthogonal Digital Micromirror Devices (DMDs)

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This document describes the basic structure and operation of digital micromirror devices (DMDs) which have ±12 degree tilt angle states organized in an orthogonal micromirror array.

1.1 Overview

A DMD is an optical micro-electrical-mechanical system (MEMS) that contains an array of highly reflective aluminum micromirrors. This document describes how one mirror, or pixel, works. It also explains how rows, blocks, or frames of data can be loaded to an entire DMD array. This information specifically applies to DMDs with ±12 degree tilt angle states organized in an orthogonal micromirror array that are part of the Advanced Light Control portfolio of DLP products. These DLP chips are often used for high speed industrial, medical, and advanced display applications.

Mirror (Pixel)

The DMD pixel (mirror) is both an opto-mechanical element and an electro-mechanical element.

2.1 Bi-stable Operation (±12 Degrees)

The DMD pixel is an electro-mechanical element in that there are two stable micromirror states (+12° and –12° for most current DMDs) that are determined by geometry and electrostatics of the pixel during operation.

The DMD pixel is an opto-mechanical element in that these two positions determine the direction that light is deflected. In particular, the DMD is a spatial light modulator. By convention, the positive (+) state is tilted toward the illumination and is referred to as the "on" state. Similarly, the negative (–) state is tilted away from the illumination and is referred to as the "off" state. Figure 2-1 shows two pixels, one in the on and one in the off state. These are the only operational states of the micromirror.

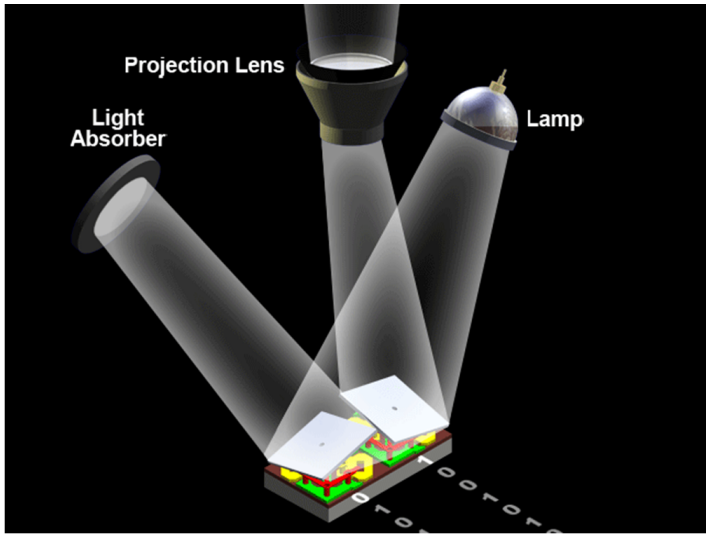


Figure 2-1. Pixels in On and Off State

2.2 Mechanical

Mechanically the pixel is comprised of a micromirror attached by means of a via to a hidden torsional hinge. The underside of the micromirrors make contact with the spring tips shown in Figure 2-2. The diagram shows a micromirror in the **unpowered** state. The two electrodes shown are used in holding the micromirror in the two operational positions (+12° and –12°).

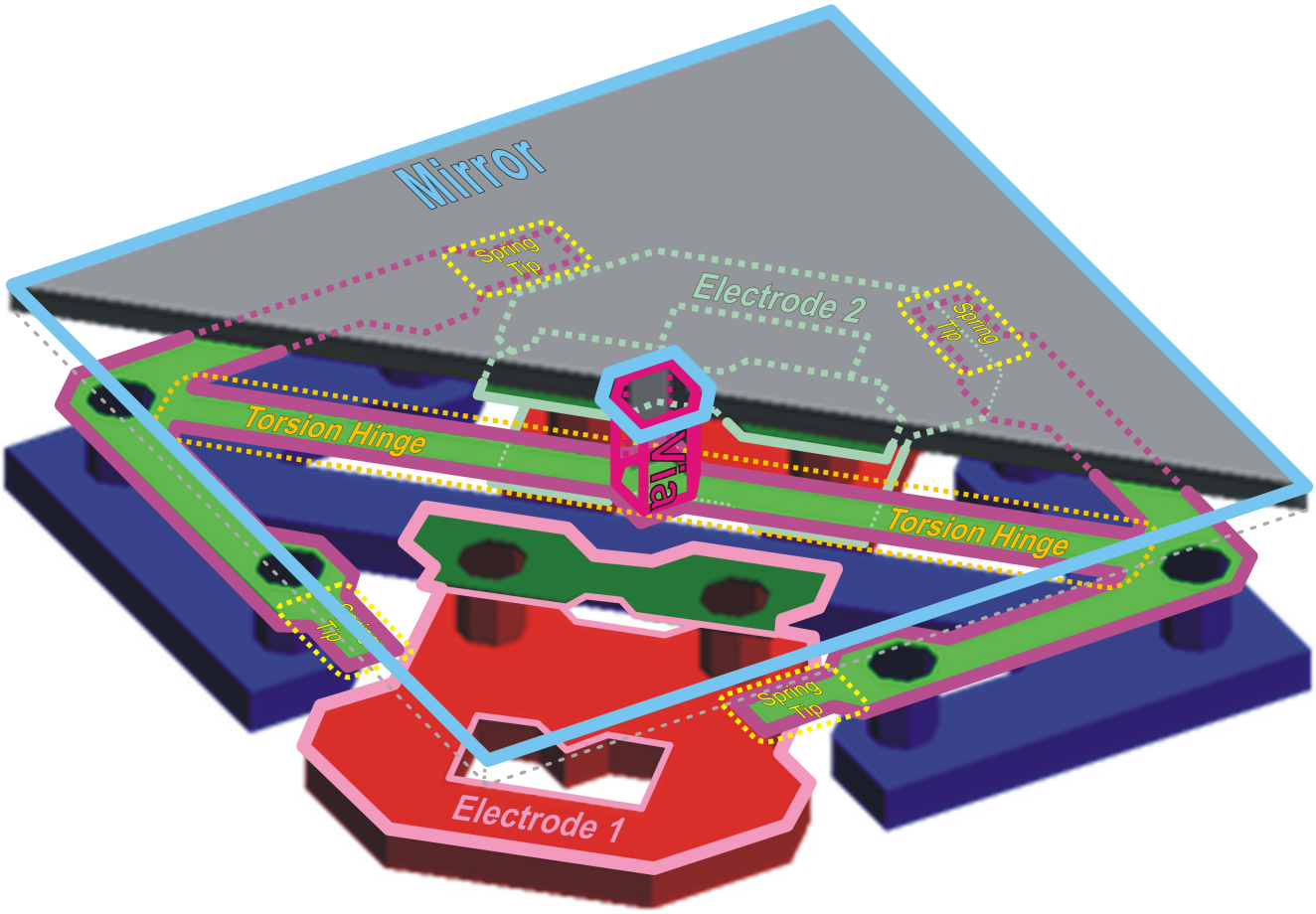


Figure 2-2. Pixel With Labeled Parts

2.3 Electrical

2.3.1 Dual CMOS Memory

Below each micromirror is a memory cell formed from dual CMOS memory elements as depicted in Figure 2-3. The state of the two memory elements are not independent, but are always complimentary. If one element is logical 1, then the other element is logical 0, and vice versa. The state of the pixel memory cell plays a part in the mechanical position of the micromirror, however, loading the memory cell does not automatically change the mechanical state of the micromirror.

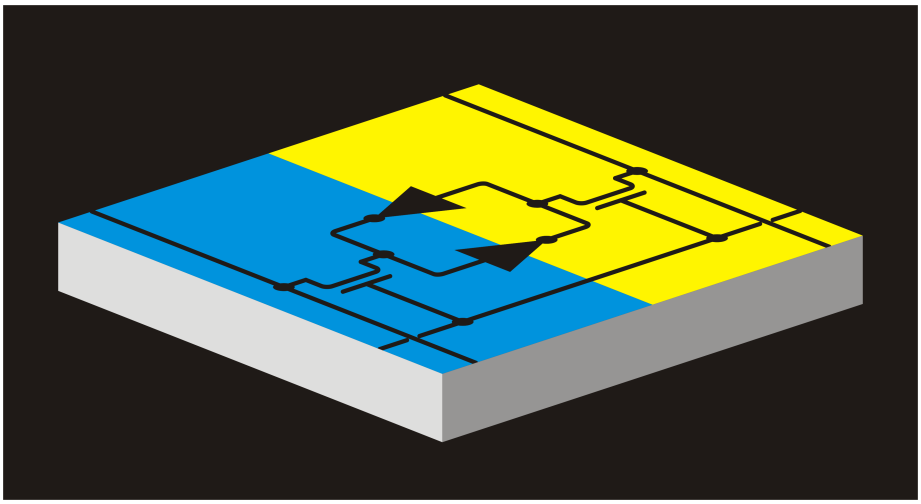


Figure 2-3. Dual CMOS Pixel Memory

2.3.2 Memory State versus Micromirror State

Although the state of the dual CMOS cell plays a part in determining the state of the micromirror, it is not the sole factor. Once the micromirror has landed, changing the state of the memory cells will not cause the micromirror to flip to the other state. Therefore, memory state and micromirror state are not directly linked together.

2.3.3 Mirror Clocking Pulse – Transferring Memory State to Mirror State

In order for the state of the CMOS memory to be transferred to the mechanical position of the micromirror, the pixel must receive a "mirror clocking pulse" (formerly referred to as a “reset”). This mirror clocking pulse momentarily releases the micromirror and then re-lands it based on the state of the CMOS memory below. Therefore, it is important that the memory cell is not overwritten during a mirror clocking pulse operation. The various DMD data sheets specify the time before and after a mirror clocking pulse occurs that data cannot be loaded to the pixel CMOS memory.

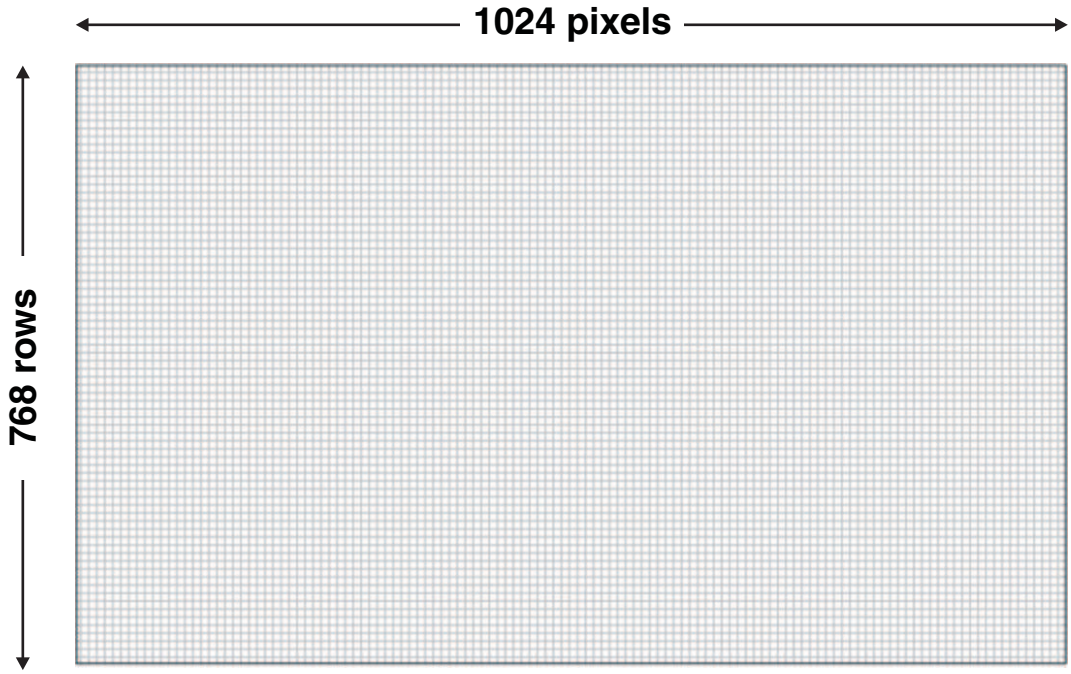
This allows the memory of groups of pixels to be pre-loaded and their mechanical position to be changed simultaneously with a mirror clocking pulse.

2.3.4 Power Up and Power Down

When a DMD is “powered up” or “powered down”, there are prescribed operations that are necessary to ensure proper operation of the micromirrors. These operations land the micromirrors during power up and release them during power down. Specific details are described in the various DLP controller and DMD data sheets.

DMD Array Operations

A DMD is an array of individual pixels, the array dimensions being determined by the resolution of the particular DMD. For example, consider a DMD with an XGA resolution of 1024 columns by 768 rows.



The CMOS memory array consists of 768 rows of 1024 pixels long. 1 = on, 0 = off

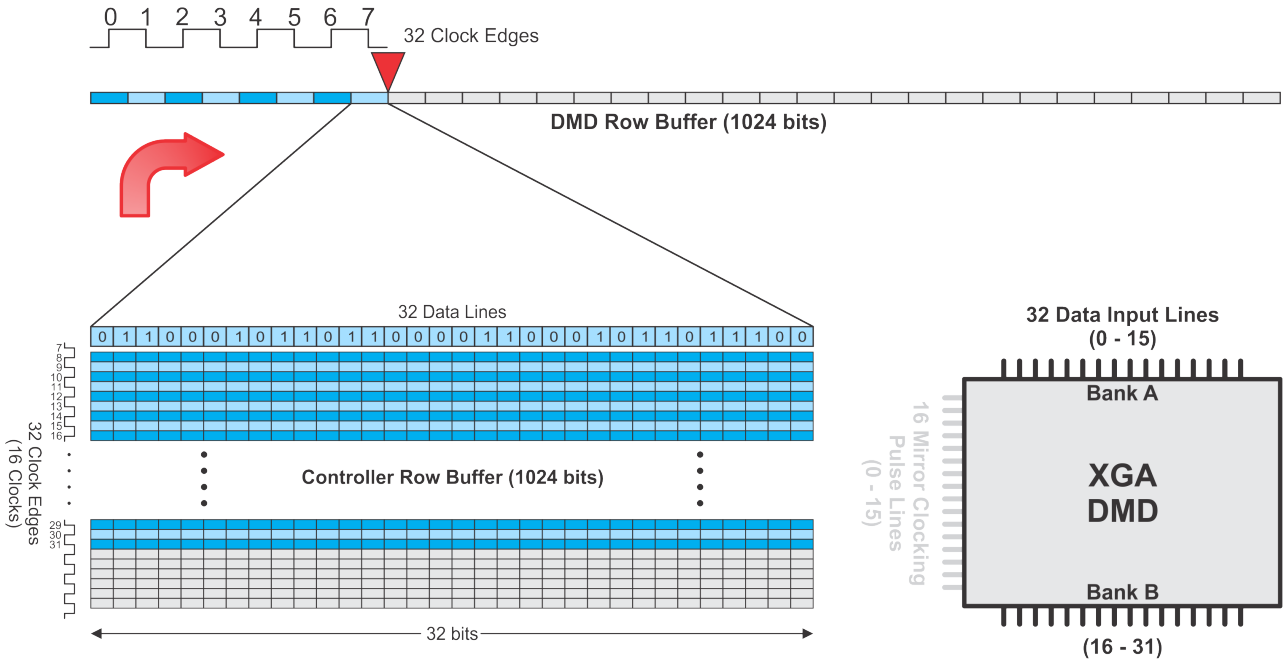
Each row is randomly or sequentially addressable (automatic counter).

Figure 3-1. DMD Array

The DMD memory is loaded by row. An entire row must be loaded even if only one pixel in the row needs to be changed.

3.1 Row Load

Loading a row is accomplished via a parallel bus of 16 or 32 bits. Current 2xLVDS XGA type A devices use a 32-bit wide bus. This data is loaded on both rising and falling edges of the data clock (known as dual data rate [DDR]). For the XGA device, 32 clock edges (16 clock cycles) over the 32 bit wide bus are needed to load the 1024 bits of a complete a row. Figure 3-2 shows a row load. Note: The 2xLVDS 1080p type A device uses two 32-bit wide buses.



Row data is loaded 32 bits per clock over 32 edges (1024 bits per row) for the 2xLVDS XGA Type A DMD.

Figure 3-2. Row Load

3.2 Row Addressing

Rows can be addressed sequentially by way of an automatic counter or randomly by row address.

3.2.1 Sequential Mode (Automatic Counter)

Sequential addressing means that when row (n) is loaded, the DMD internally increments the row address pointer to (n + 1).

NOTE: The pointer does not automatically reset to zero when the last row is loaded. An explicit command to set the row pointer to zero must be issued.

This mode is useful when it is expected that most of the data in the image will change each time the device is loaded. Further, it does not require the user to keep track of the row address pointer.

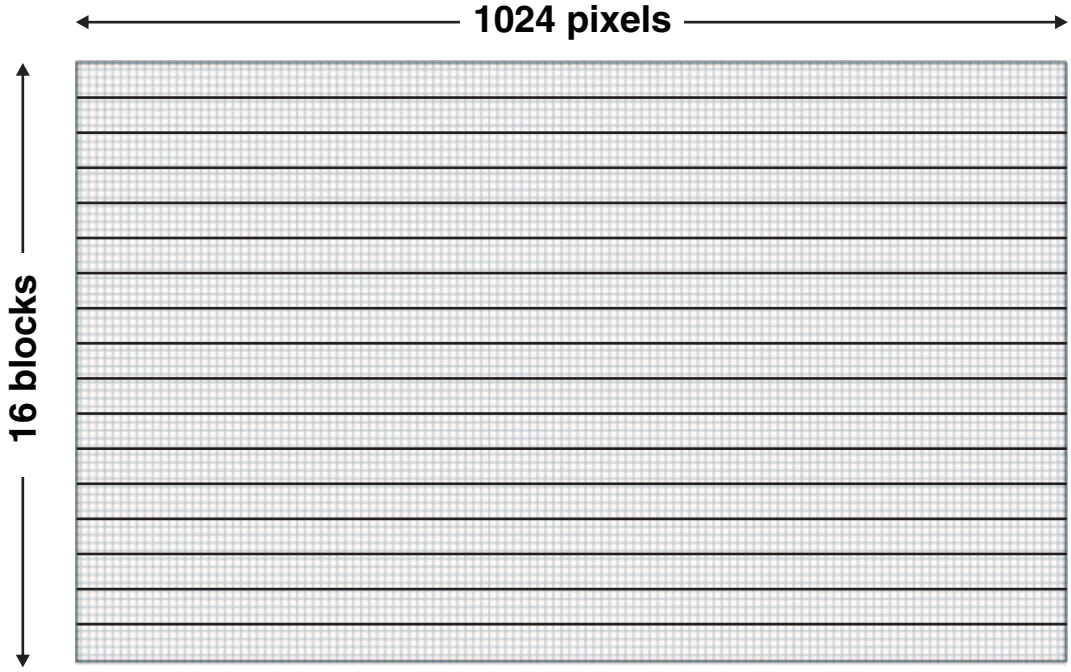
3.2.2 Random Mode

Random addressing means that as row data is supplied a row address (n) must also be supplied. The DMD will then load the row data to row (n) specified by the row address.

This mode is useful when it is expected that the data in the image will only change in a subset of rows. However, it does require the user to keep track of the row address pointer and supply the row address during each row load.

Block Operations

For the purpose of mirror clocking pulses and quickly clearing data, the DMD is divided into blocks. 2xLVDS XGA type A devices are divided into 16 blocks of 48 rows each. Figure 4-1 illustrates the blocks. Note: 2xLVDS 1080p type A devices are divided into 15 blocks of 72 rows each.



The XGA array is divided into 16 blocks of 48 rows.

Figure 4-1. DMD Blocks

4.1 Mirror Clocking Pulses

Previously it was noted that loading the CMOS memory does not cause the micromirrors to change their mechanical state, and that in order for the loaded memory to change the mechanical position of the mirrors, a “mirror clocking pulse” must be applied.

A mirror clocking pulse is issued to a block. The pixels in that block whose data has changed moves to the opposite mechanical position and those whose data did not change will remain in the same mechanical position. These operations are referred to as “cross-over” transitions and “same-side” transitions respectively.

NOTE: Memory cannot be loaded in a block that is undergoing a mirror clocking pulse. However, memory can be loaded in a block that is not undergoing a mirror clocking pulse. However, there is a minimum time that must transpire after a mirror clocking pulse is sent to a block before new data can be loaded to that block. This wait time is referred to as the “mirror settle time”.

The DMD has 16 mirror clocking pulse input lines, one for each block as illustrated in Figure 4-2.

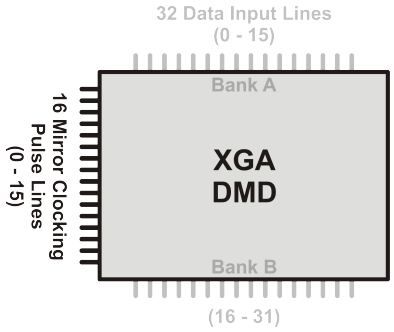


Figure 4-2. DMD Mirror Clocking Pulse Lines

There are four mirror clocking pulse modes that determine which blocks receive a mirror clocking pulse when issued:

- Single block mode
- Dual block mode
- Quad block mode
- Global mode

4.1.1 Single Block Mode

In single block mode, a single block can be loaded and sent a mirror clocking pulse. After a block's memory is loaded, it is sent a mirror clocking pulse to transfer the information to the mechanical state of the mirrors (that is, display the data). These blocks can be sent a mirror clocking pulse in any order.

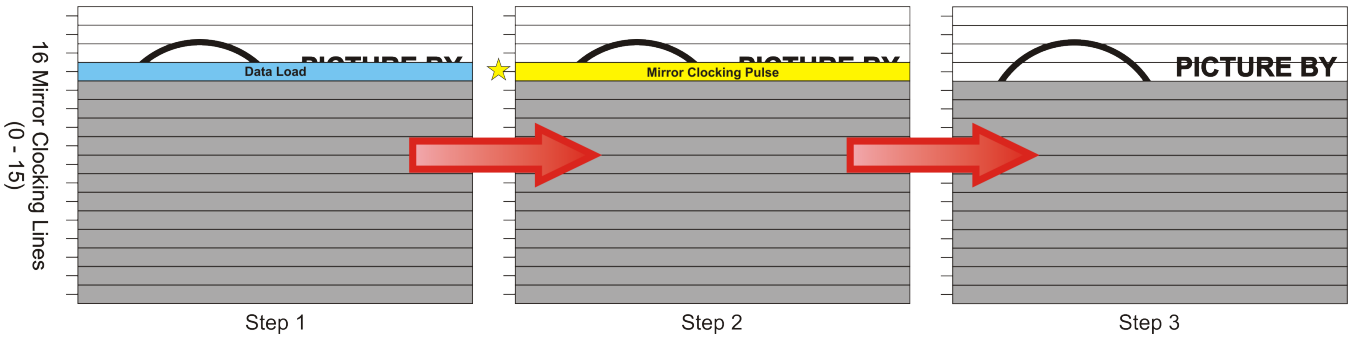


Figure 4-3. Single Block Mirror Clocking Pulse

4.1.2 Dual Block Mode

In dual block mode mirror clocking pulse, blocks are paired together as follows: (0-1), (2-3), (4-5) . . . (14-15). After data is loaded, a pair can be sent a mirror clocking pulse to transfer the information to the mechanical state of the mirrors. These pairs can be sent a mirror clocking pulse in any order.

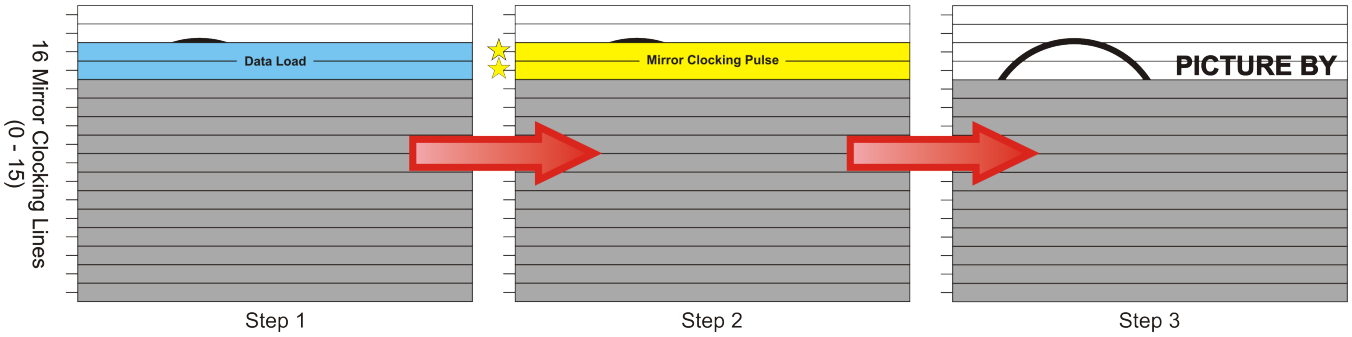


Figure 4-4. Dual Block Mirror Clocking Pulse

4.1.3 Quad Block Mode

In quad block mode mirror clocking pulse, blocks are grouped together in fours as follows: (0-3), (4-7), (8-11), and (12-15). After a quad group is loaded, it can be sent a mirror clocking pulse to transfer the information to the mechanical state of the mirrors. Each quad group can be sent a mirror clocking pulse in any order.

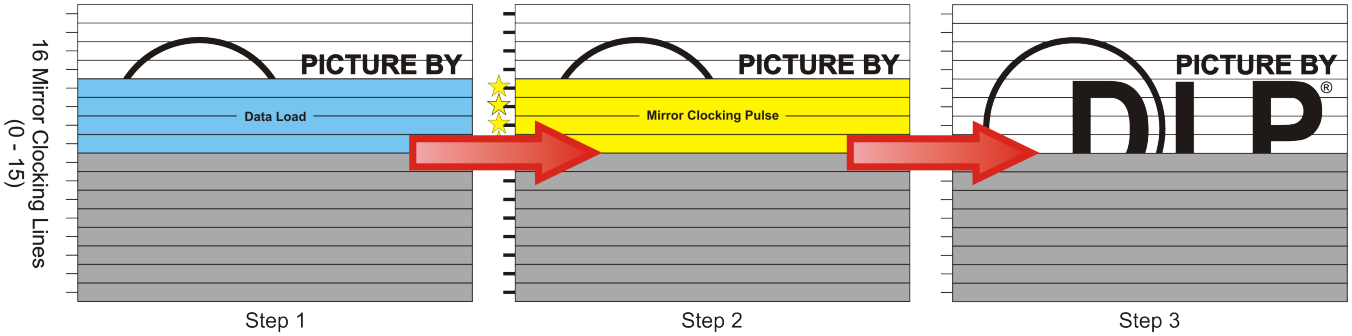


Figure 4-5. Quad Block Mirror Clocking Pulse

4.1.4 Global Mode

In global mode, all mirror clocking pulse blocks are grouped together. Therefore, the entire DMD must be loaded with the desired data before issuing a global mirror clocking pulse to transfer the information to the mechanical state of the mirrors.

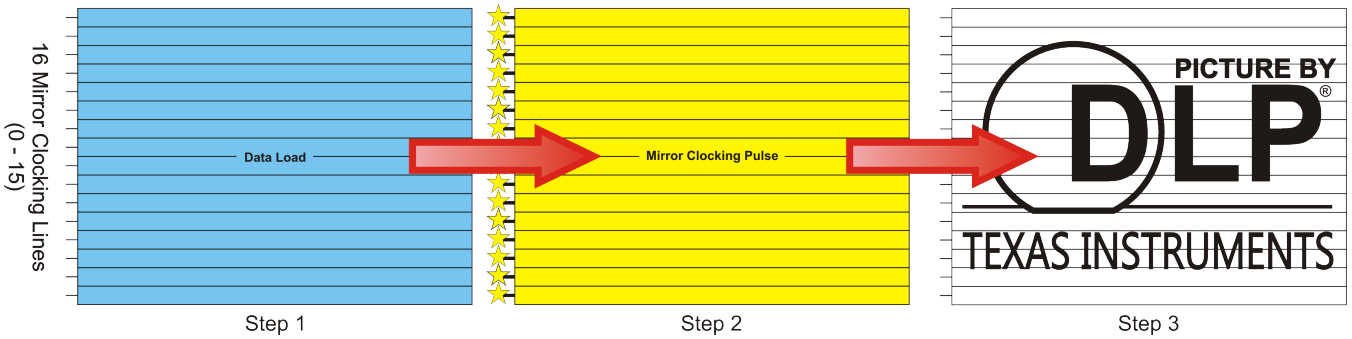


Figure 4-6. Global Mirror Clocking Pulse

4.2 Block Clear

Although memory can be “cleared” by loading all zeros into a block, a special block function known as a “block clear” can be issued instead. Loading 48 rows would require 48 × 16 (768) clock cycles, but a block clear command causes the DMD to load all zero’s into the specified block. For a 2xLVDS XGA type A DMD a block clear command takes the same amount of time as one row load operation. Thus, in the time it takes to load a row of data (16 clock cycles) an entire block can be loaded with zeros. Therefore, it is possible to clear the entire XGA DMD memory in less time than it would take to load a single block (48 times faster than loading zeros using row loads). This function is useful when short display times are desired with continuous illumination sources.

NOTE: The 2xLVDS 1080p type A devices require a block clear command followed by two no operation (NoOp) row cycles to clear a block (24 times faster than using row loads).

Block clear commands (including any subsequent NoOps) and row load operations cannot be executed simultaneously, even if the row is not in the block to be cleared.

4.3 Phased Operation

4.3.1 Motivation

For some applications, it is desirable to display a given image (binary frame) for a short period of time.

If a global mirror clocking pulse is used, the array cannot begin loading data even with a block clear command, until the mirror settle time is satisfied.

A shorter effective display time can be achieved by loading a subset of blocks during the mirror settle time of another subset of blocks. This can be done in a cascading fashion down the surface of the DMD until the entire image has been briefly displayed. The result is that the mirror settle time is allowed to occur or while other blocks are loading. This in effect removes the mirror settle time from the time it takes to display one binary frame.

This operation is analogous to the way a focal plane shutter works in a modern SLR camera to achieve high shutter speeds.

NOTE: In 2xLVDS XGA type A parts (at 400 MHz clock), the load time of one block is shorter than the required mirror settle time. Therefore, in practice, two consecutive blocks are loaded before returning to clear the initial blocks. This is the example shown in Figure 4-7.

4.3.2 How it is Done

A phased operation uses both block operations (mirror clocking pulse and block clear) to achieve short effective display times.

Several steps of a phased mirror clocking pulse operation for a 2xLVDS XGA type A part (at 400 MHz) are illustrated in Figure 4-7.

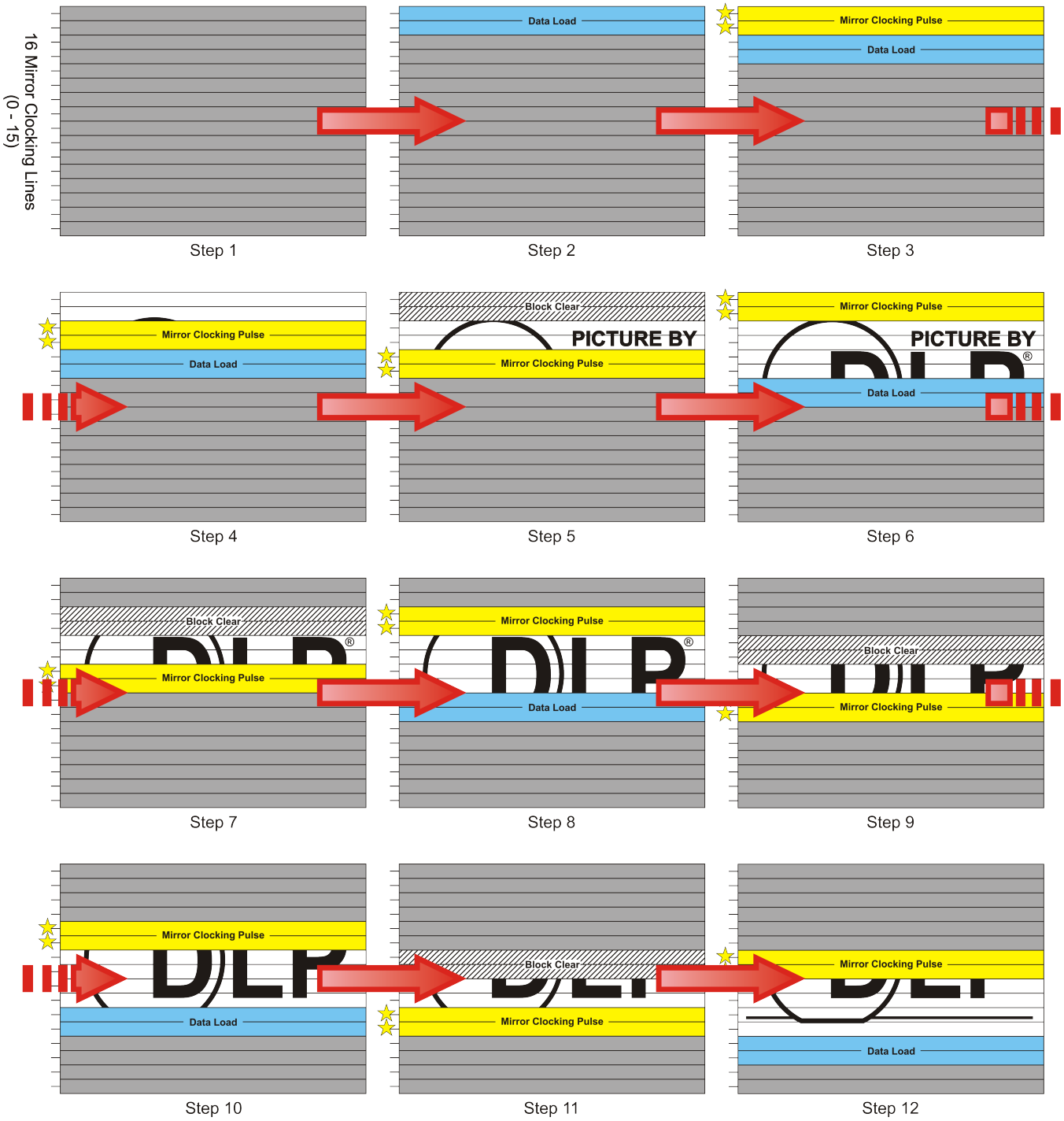


Figure 4-7. Phased Mirror Clocking Pulse Steps

In this sequence, a “window” of two displayed blocks sweeps down the surface of the DMD. The image is effectively displayed for the time that it takes to load two blocks. When the bottom of the DMD is reached, the next frame of data can begin a sweep immediately since the blocks at the top of the DMD have already satisfied the mirror settle time.

Note: The entire image is not displayed simultaneously, therefore, sufficient exposure time is needed to integrate the image.

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from A Revision (October 2013) to B Revision	Page
• Applied grammatical and formatting edits throughout the document to improve clarity and follow TI documentation standards	1

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