SN65HVS885 34-V Digital-Input Serializer for 5-V Systems

1 Features

- Eight Digital Sensor Inputs
  - High Input Voltage up to 34 V
  - Selectable Debounce Filters From 0 ms to 3 ms
  - Flexible Input Current-Limited – 0.2 mA to 5.2 mA
  - Field Inputs Protected to 15-kV ESD
- Single 5-V Supply
- Output Drivers for External Status LEDs
- Cascadable for More Inputs in Multiples of Eight
- SPI-Compatible Interface
- Overtemperature Indicator

2 Applications

- Industrial PCs
- Digital I/O Cards
- High Channel Count Digital Input Modules
- Decentralized I/O Modules

3 Description

The SN65HVS885 is an eight channel, digital-input serializer for high-channel density digital input modules in industrial and building automation. Operating from a 5-V supply the device accepts field input voltages of up to 34 V. In combination with galvanic isolators the device completes the interface between the high voltage signals on the field-side and the low-voltage signals on the controller side. Inputs signals are current limited and then validated by internal debounce filters.

With the addition of few external components, the input switching characteristic can be configured in accordance with IEC61131-2 for Type 1, 2 and 3 sensor switches.

Upon the application of load and clock signals, input data is latched in parallel into the shift register and afterwards clocked out serially.

Cascading of multiple devices is possible by connecting the serial output of the leading device with the serial input of the following device, enabling the design of high-channel count input modules. Multiple devices can be cascaded through a single serial port, reducing both the isolation channels and controller inputs required.

Input status can be visually indicated via constant current LED outputs. The current limit on the inputs is set by a single, external, precision resistor. An on-chip temperature sensor provides diagnostic information for graceful shutdown and system safety.

The SN65HVS885 is available in a 28-pin PWP PowerPAD™ package, allowing for efficient heat dissipation. The device is specified for operation at temperatures from –40°C to 125°C.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
SN65HVS885	HTSSOP (28)	9.70 mm × 4.40 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Simplified I/O Structure

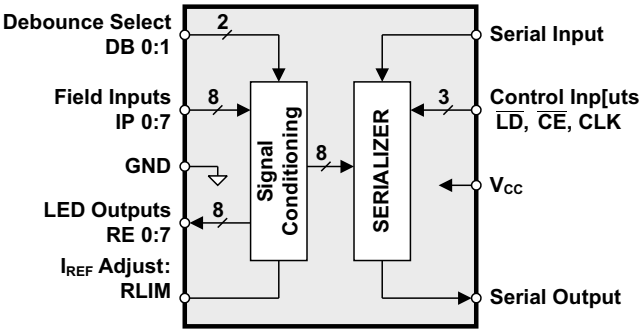


Table of Contents

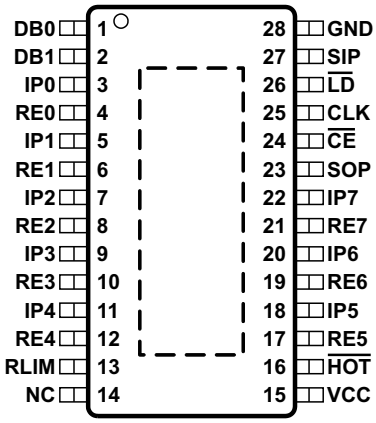
4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (January 2009) to Revision A	Page
• Added *Pin Configuration and Functions* section, *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section	1

5 Pin Configuration and Functions

PWP Package
28-Pin HTSSOP With Exposed Thermal Pad
Top View



Pin Functions

PIN		DESCRIPTION
NAME	NO.	
$\overline{CE}$	24	Clock Enable Input
CLK	25	Serial Clock Input
DB0	1	Debounce select inputs
DB1	2	
GND	28	Device Ground
$\overline{HOT}$	16	Over-Temperature Flag
IPx	3, 5, 7, 9, 11, 18, 20, 22	Input Channel x
$\overline{LD}$	26	Load Pulse Input
NC	14	Not Connected
REx	4, 6, 8, 10, 12, 17, 19, 21	Return Path x (LED drive)
RLIM	13	Current Limiting Resistor
SIP	27	Serial Data Input
SOP	23	Serial Data Output
V_{CC}	15	5 V Device Supply

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

			MIN	MAX	UNIT
V_{CC}	Device power input	V_{CC}	–0.5	6	V
V_{IPx}	Field digital inputs	IPx	–0.3	36	V
V_{ID}	Voltage at any logic input	DB0, DB1, CLK, SIP, $\overline{CE}$, $\overline{LD}$	–0.5	6	V
I_O	Output current	$\overline{HOT}$, SOP	–8	8	mA
P_{TOT}	Continuous total power dissipation		See *Thermal Information*		
T_J	Junction temperature			170	°C
T_{stg}	Storage temperature			150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	All pins	±4000	V
			IPx	±15000	
		Charged-device model (CDM), per JEDEC specification JESD22-C101 (2)		±1000	
		Machine model (MM) (3)		±100	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.
(3) JEDEC Standard 22, Method A115-A

6.3 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Device supply voltage	4.5	5	5.5	V
V_{IPL}	Field input low-state input voltage	0		4	V
V_{IPH}	Field input high-state input voltage	5.5		34	V
V_{IL}	Logic low-state input voltage	0		0.8	V
V_{IH}	Logic high-state input voltage	2.0		5.5	V
R_{LIM}	Current limiter resistor	17	25	500	kΩ
f_{IP} (1)	Input data rate	0		1	Mbps
T_A	Device	–40		125	°C
T_J	Junction Temperature			150	°C

(1) Maximum data rate corresponds to 0 ms debounce time, (DB0 = open, DB1 = GND), and R_{IN} = 0 Ω

6.4 Thermal Information

THERMAL METRIC (1)			SN65HVS885 PWP (HTSSOP) 28 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	High-K thermal resistance	35	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance		4.27	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance		15	°C/W
ψ_{JT}	Junction-to-top characterization parameter		0.6	°C/W
ψ_{JB}	Junction-to-board characterization parameter		15.9	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

Thermal Information (continued)

THERMAL METRIC[1]		SN65HVS885 PWP (HTSSOP) 28 PINS	UNIT
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	2.4	°C/W

6.5 Electrical Characteristics

over full-range of recommended operating conditions (unless otherwise noted) all voltages measured against device ground, see Figure 9

PARAMETER		TERMINAL	TEST CONDITIONS		MIN	TYP	MAX	UNIT
FIELD INPUTS								
$V_{TH-(IP)}$	Low-level device input threshold voltage	IP0–IP7	R_{LIM} = 25 kΩ		4	4.3		V
$V_{TH+(IP)}$	High-level device input threshold voltage					5.2	5.5	V
$V_{HYS(IP)}$	Device input hysteresis					0.9		V
$V_{TH-(IN)}$	Low-level field input threshold voltage	Measured at field side of R_{IN}	4.5 V < V_{CC} < 5.5 V, R_{IN} = 1.2 kΩ ± 5%, R_{LIM} = 25 kΩ, T_A ≤ 125°C		6	8.4		V
$V_{TH+(IN)}$	High-level field input threshold voltage					9.4	10	V
$V_{HYS(IN)}$	Field input hysteresis					1		V
R_{IP}	Input resistance	IP0–IP7	3 V < V_{IPx} < 6 V, R_{LIM} = 25 kΩ		0.2	0.63	1.1	kΩ
I_{IP-LIM}	Input current limit	IP0–IP7	R_{LIM} = 25 kΩ		3.15	3.6	4	mA
t_{DB}	Debounce times of input channels	IP0–IP7	DB0 = open, DB1 = GND			0		ms
			DB0 = GND, DB1 = open			1		
			DB0 = DB1 = open			3		
I_{RE-on}	RE on-state current	RE0–RE7	R_{LIM} = 25 kΩ, RE_X = GND		2.8	3.15	3.5	mA
DEVICE SUPPLY								
$I_{CC(VCC)}$	Supply current	V_{CC}	IP0 to IP7 = 24V, RE_X = GND, All logic inputs open			6.5	10	mA
LOGIC INPUTS AND OUTPUTS								
V_{OL}	Logic low-level output voltage	SOP, $\overline{HOT}$	I_{OL} = 20 µA				0.4	V
V_{OH}	Logic high-level output voltage		I_{OH} = –20 µA		4			V
I_{IL}	Logic input leakage current	DB0, DB1, $\overline{SIP}$, $\overline{LD}$, $\overline{CE}$, CLK			–50		50	µA
T_{OVER}	Over-temperature indication					150		°C
T_{SHDN}	Shutdown temperature					170		°C
POWER DISSIPATION								
P_D	Power Dissipation		V_{CC} = 5 V, R_{IN} = 0Ω, R_{LIM} = 25 kΩ, RE0 – RE7 = GND, f_{CLK} = 100 MHz	IP0-IP7 = 34 V		1100		mW
				IP0-IP7 = 24 V				
				IP0-IP7 = 20 V				
				IP0-IP7 = 12 V				

6.6 Timing Requirements

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
t_{W1}	CLK pulse width	See Figure 6	4			ns
t_{W2}	$\overline{LD}$ pulse width	See Figure 4	6			ns

Timing Requirements (continued)

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
t_{SU1}	SIP to CLK setup time	See Figure 7	4			ns
t_{H1}	SIP to CLK hold time	See Figure 7	2			ns
t_{SU2}	Falling edge to rising edge ($\overline{CE}$ to CLK) setup time	See Figure 8	4			ns
t_{REC}	$\overline{LD}$ to CLK recovery time	See Figure 5	2			ns
f_{CLK}	Clock pulse frequency	See Figure 6	DC		100	MHz

6.7 Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH1}, t_{PHL1}	CLK to SOP	C_L = 15 pF, see Figure 6			10	ns
t_{PLH2}, t_{PHL2}	$\overline{LD}$ to SOP	C_L = 15 pF, see Figure 4			14	ns
t_r, t_f	Rise and fall times	C_L = 15 pF, see Figure 6			6	ns

6.8 Typical Characteristics

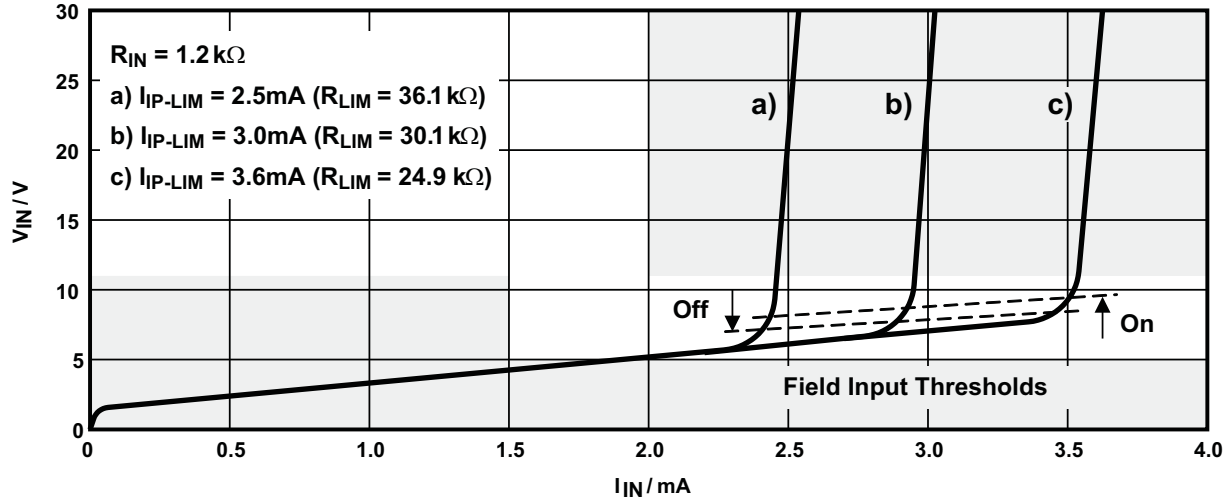


Figure 1. Typical Input Characteristics

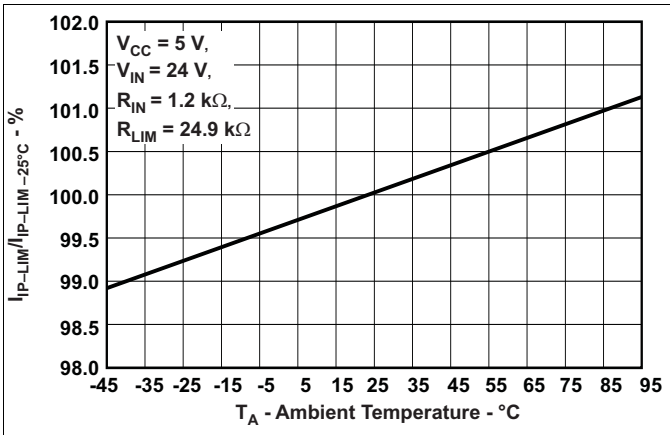


Figure 2. Typical Current Limiter Variation vs Ambient Temperature

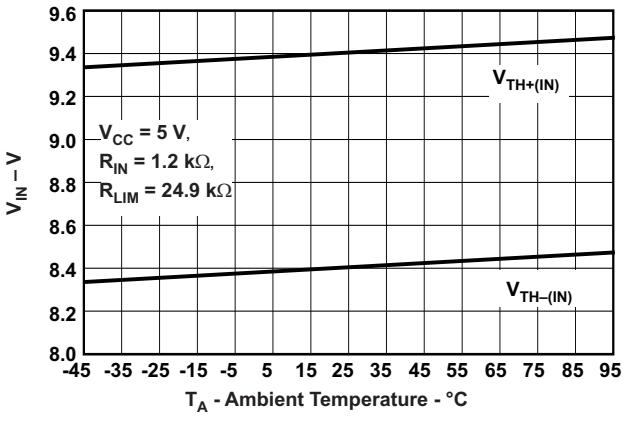


Figure 3. Typical Limiter Threshold Voltage Variation vs Ambient Temperature

7 Parameter Measurement Information

7.1 Waveforms

For the complete serial interface timing, refer to Figure 17.

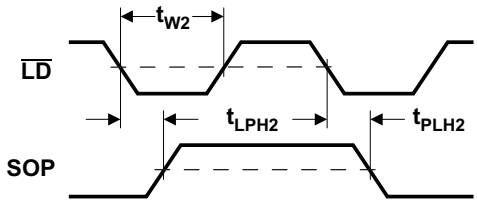


Figure 4. Parallel – Load Mode

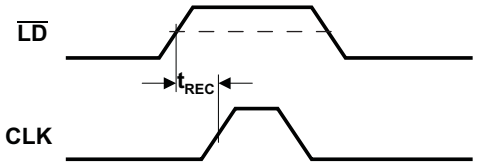


Figure 5. Serial – Shift Mode

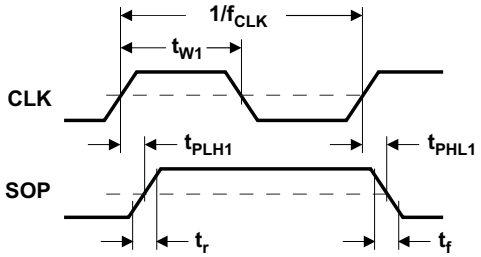


Figure 6. Serial – Shift Mode

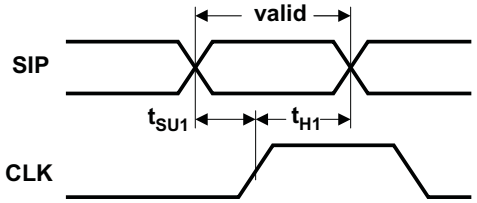


Figure 7. Serial – Shift Mode

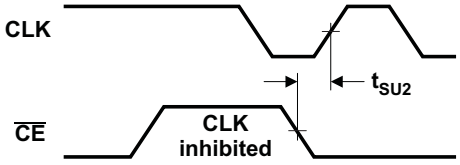


Figure 8. Serial – Shift Mode

7.2 Signal Conventions

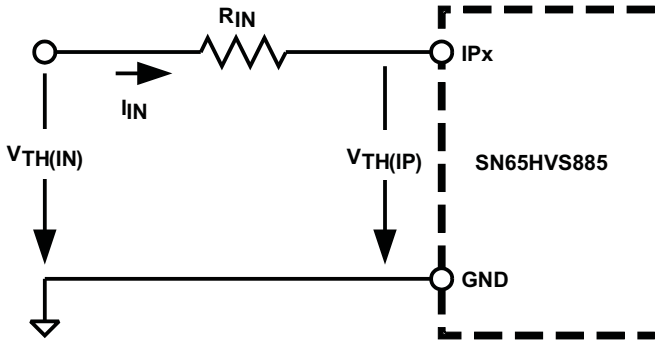


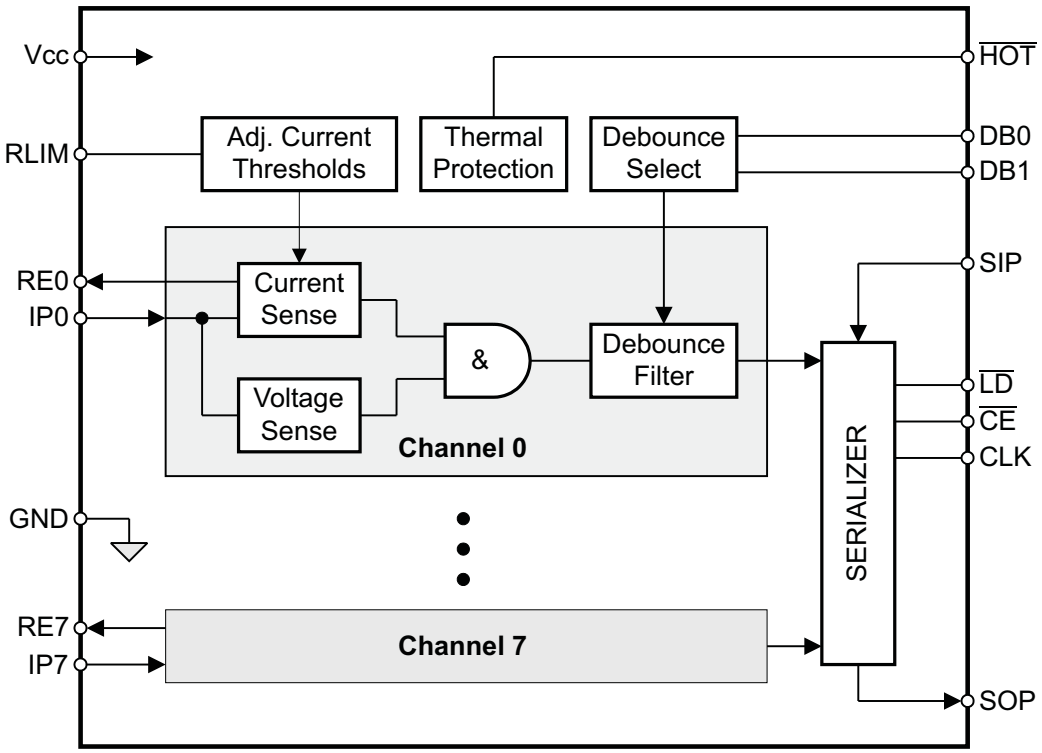
Figure 9. On/Off Threshold Voltage Measurements

8 Detailed Description

8.1 Overview

The SN65HVS885 is an 8 channel, digital input serializer which operates from a 5 V supply and accepts digital inputs of up to 34 V on the 8 channels (IP0-IP7). The device provides a serially shifted digital output with reduced voltage ranges of 0-5 V for applications in industrial and building automation systems. The SN65HVS885 meets JEDEC standards for ESD protection (refer to ESD Ratings), and is SPI compatible for interfacing with standard microcontrollers. The serializer operates in 2 fundamental modes: Load Mode and Shift mode. In Load mode, information from the field inputs is allowed to latch into the shift register. In Shift mode, the information stored in the parallel shift register can be serially shifted to the serial output (SOP). A detailed description of the functional modes is available in the *Device Functional Modes* section.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Digital Inputs

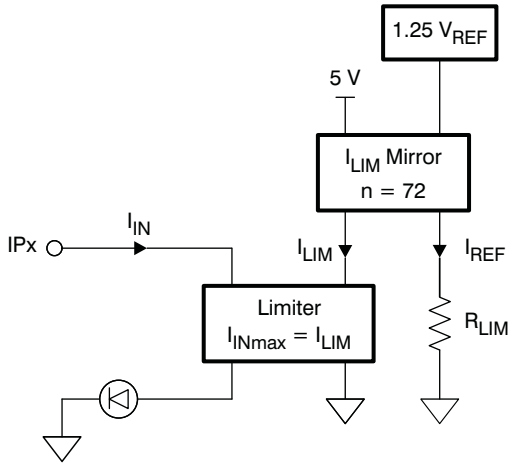


Figure 10. Digital Input Stage

Each digital input operates as a controlled current sink limiting the input current to a maximum value of I_{LIM}. The current limit is derived from the reference current via $I_{LIM} = n \times I_{REF}$, and I_{REF} is determined by $I_{REF} = V_{REF}/R_{LIM}$. Thus, changing the current limit requires the change of R_{LIM} to a different value via: $R_{LIM} = n \times V_{REF}/I_{LIM}$.

Inserting the actual values for n and V_{REF} gives: $R_{LIM} = 90\ V / I_{LIM}$.

While the device is specified for a current limit of **3.6 mA**, (via R_{LIM} = 25 kΩ), it is easy to lower the current limit to further reduce the power consumption. For example, for a current limit of **2.5 mA** simply calculate:

$$R_{LIM} = \frac{90\ V}{I_{LIM}} = \frac{90\ V}{2.5\ mA} = 36\ k\Omega \quad (1)$$

8.3.2 Debounce Filter

The HVS885 applies a simple analog/digital filtering technique to remove unintended signal transitions due to contact bounce or other mechanical effects. Any new input (either low or high) must be present for the duration of the selected debounce time to be latched into the shift register as a valid state.

The logic signal levels at the control inputs, DB0 and DB1 of the internal Debounce-Select logic determine the different debounce times listed in the following truth table.

Table 1. Debounce Times

DB1	DB0	FUNCTION
Open	Open	3 ms delay
Open	GND	1 ms delay
GND	Open	0 ms delay (Filter bypassed)
GND	GND	Reserved

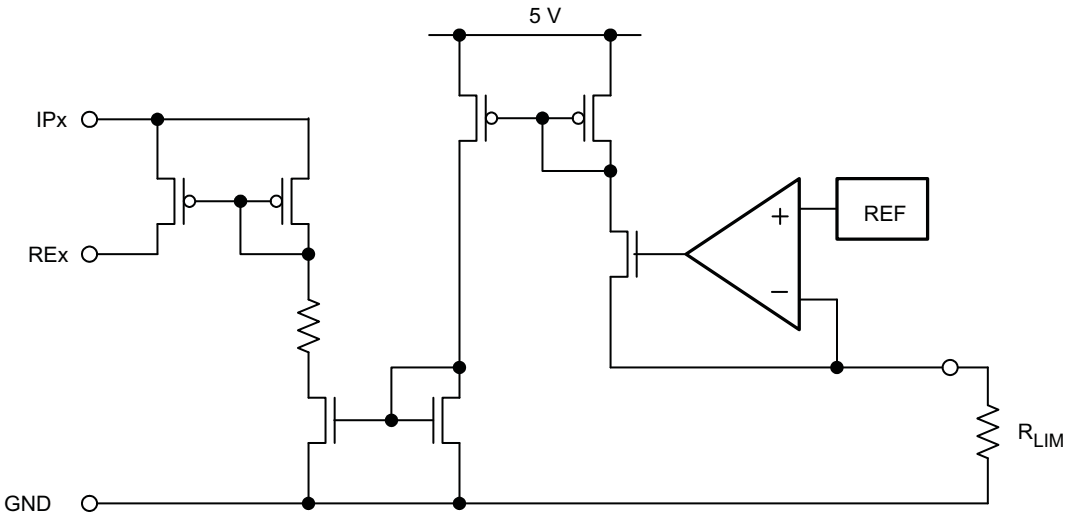


Figure 11. Equivalent Input Diagram

8.3.3 Shift Register

The conversion from parallel input to serial output data is performed by an eight-channel, parallel-in serial-out shift register. Parallel-in access is provided by the internal inputs, PIP0–PIP7, that are enabled by a low level at the load input ($\overline{LD}$). When clocked, the latched input data shift towards the serial output (SOP). The shift register also provides a clock-enable function.

Clocking is accomplished by a low-to-high transition of the clock (CLK) input while $\overline{LD}$ is held high and the clock enable ($\overline{CE}$) input is held low. Parallel loading is inhibited when $\overline{LD}$ is held high. The parallel inputs to the register are enabled while $\overline{LD}$ is low independently of the levels of the CLK, $\overline{CE}$, or serial (SIP) inputs.

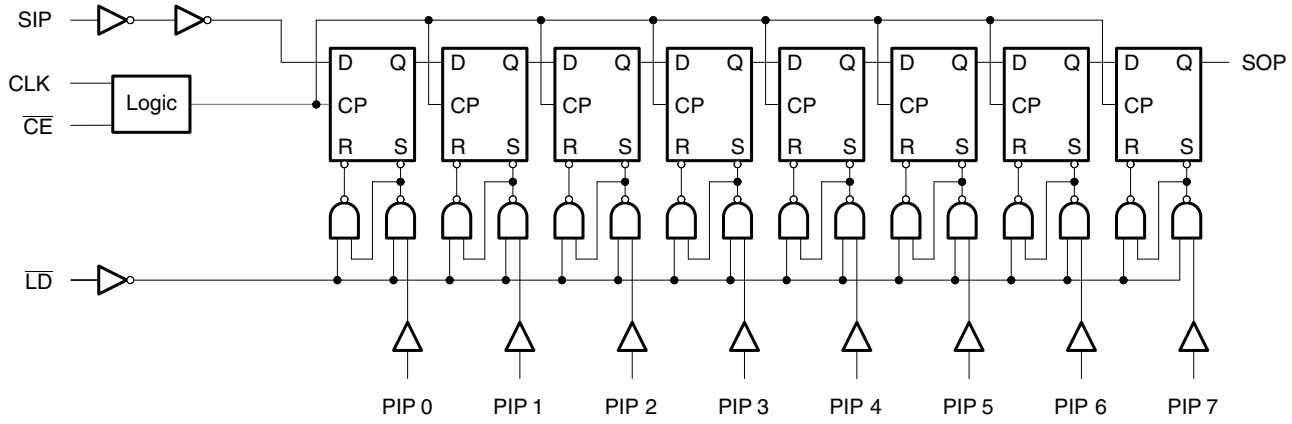


Figure 12. Shift Register Logic Structure

Table 2. Function Table

INPUTS			FUNCTION
$\overline{LD}$	CLK	$\overline{CE}$	
L	X	X	Parallel load
H	X	H	No change
H	↑	L	Shift(1)

(1) Shift = content of each internal register shifts towards serial outputs. Data at SIP is shifted into first register.

8.3.4 Temperature Sensor

An on-chip temperature sensor monitors the device temperature and signals a fault condition if the temperature exceeds a first trip point at 150°C by pulling the HOT output low. If the junction temperature continues to rise, passing a second trip point at 170 °C, all device outputs assume high impedance state.

A special condition occurs when the chip temperature exceeds the second temperature trip point due to an output short; the HOT output buffer becomes high impedance, thus separating the buffer from the external circuitry. An internal 100-kΩ pulldown resistor, connecting the HOT-pin to ground, is used as a "cooling down" resistor, which continues to provide a logic low level to the external circuitry.

8.4 Device Functional Modes

The 2 functional modes of operation are Load mode and Shift mode. Load mode enables information from the field inputs to latch into the shift register. To enter load mode, the LD pin must be held low, and the device will remain in load mode regardless of the CLK, CE, or serial (SIP) input levels. A high level at the LD pin switches the device into Shift mode. When the device is in Shift mode, a low level at the CE pin will cause the data stored in the parallel shift register to be serially shifted to the serial output (SOP) on the rising edge of CLK. A high level at the CE pin inhibits the serial shifting, which is demonstrated in Figure 17. After 8 consecutive CLK pulses, the serial output (SOP) will remain at the level of the serial input (SIP) which is internally pulled to logic high. A logic high at the CE pin is required to signify the end of the serial data output. In the case of a daisy chained configuration, the serial output (SOP) of the SN65HVS885 can be connected to the serial input (SIP) of a following device, and additional clock pulses are required to shift the additional data out of the chain. The number of consecutive clock pulses will equal 8 times the number of devices in the chain. See Figure 18 for an example of a cascaded chain of 4x SN65HVS885.

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

9.1.1 System-Level EMC

The SN65HVS885 is designed to operate reliably in harsh industrial environments. At a system level, the device is tested according to several international electromagnetic compatibility (EMC) standards.

In addition to the device internal ESD structures, external protection circuitry shown in Figure 13, can be used to absorb as much energy from burst- and surge-transients as possible.

R_{IN}	1.2 kΩ, 1/4 W MELF Resistor
C_{IN}	220 nF, 60 V Ceramic Capacitor
C_S	4.7 nF, 2 kV Ceramic Capacitor

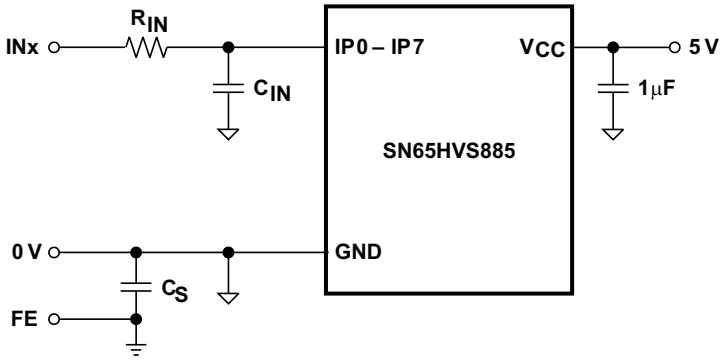


Figure 13. Typical EMC Protection Circuitry for Supply and Signal Inputs

9.1.2 Input Channel Switching Characteristics

The input stage of the HVS885 is so designed, that for an input resistor R_{IN} = 1.2 kΩ the trip point for signaling an ON-condition is at 9.4 V at 3.6 mA. This trip point satisfies the switching requirements of IEC61131-2 Type 1 and Type 3 switches.

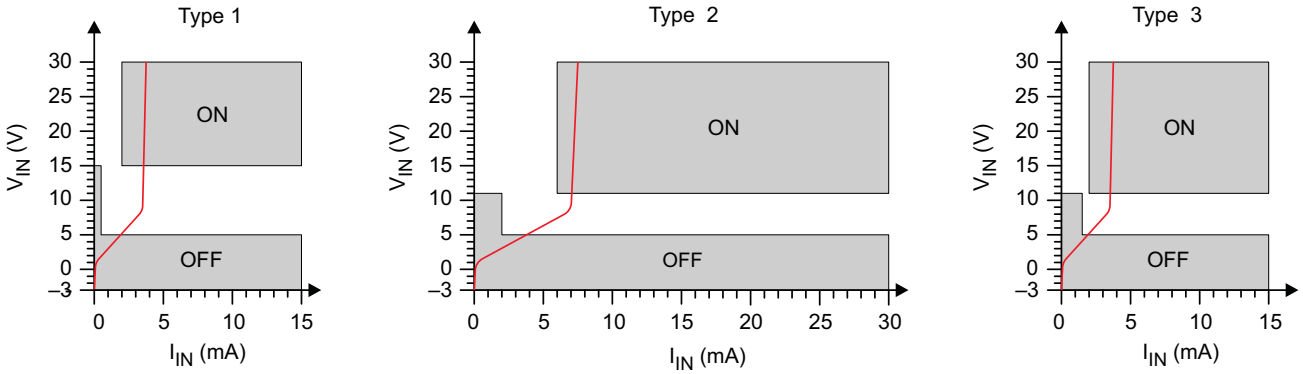


Figure 14. Switching Characteristics for IEC61131-2 Type 1, 2, and 3 Proximity Switches

For a Type 2 switch application, two inputs are connected in parallel. The current limiters then add to a total maximum current of 7.2 mA. While the return-path (RE-pin), of one input might be used to drive an indicator LED, the RE-pin of the other input channel should be connected to ground (GND).

Application Information (continued)

Paralleling input channels reduces the number of available input channels from an octal Type 1 or Type 3 input to a quad Type 2 input device. Note, that in this configuration output data of an input channel is represented by two shift register bits.

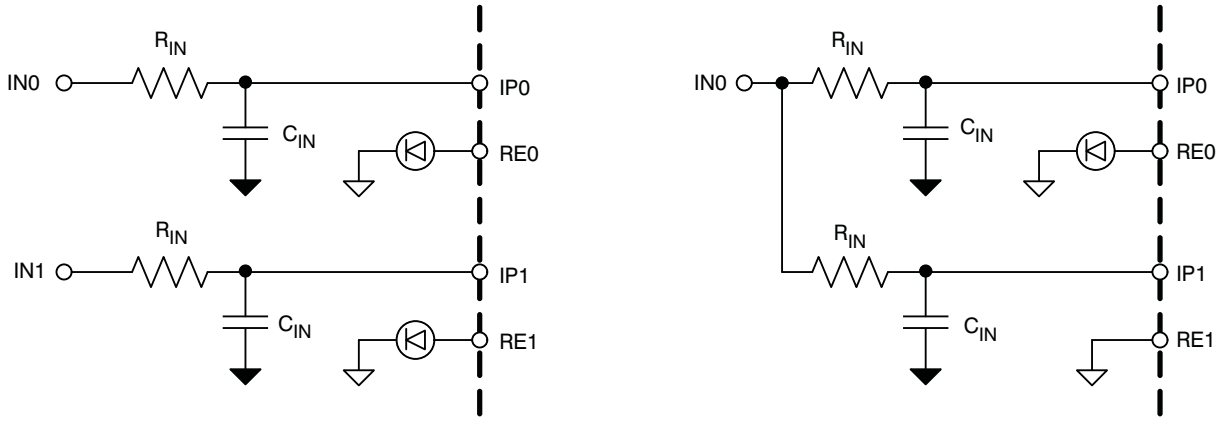


Figure 15. Paralleling Two Type 1 or Type 3 Inputs Into One Type 2 Input

9.1.3 Digital Interface Timing

The digital interface of the SN65HVS885 is SPI compatible and interfaces, isolated or non-isolated, to a wide variety of standard micro controllers.

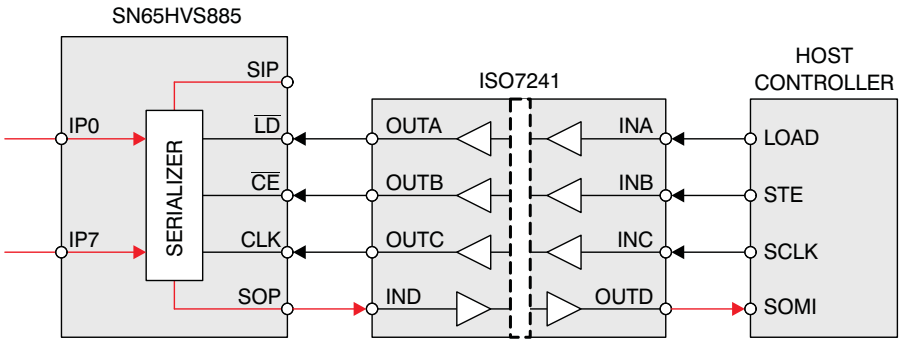


Figure 16. Simple Isolation of the Shift Register Interface

Upon a low-level at the load input, $\overline{LD}$, the information of the field inputs, IP0 to IP7 is latched into the shift register. Taking /LD high again blocks the parallel inputs of the shift register from the field inputs. A low-level at the clock-enable input, $\overline{CE}$, enables the clock signal, CLK, to serially shift the data to the serial output, SOP. Data is clocked at the rising edge of CLK. Thus after eight consecutive clock cycles all field input data have been clocked out of the shift register and the information of the serial input, SIP, appears at the serial output, SOP.

Application Information (continued)

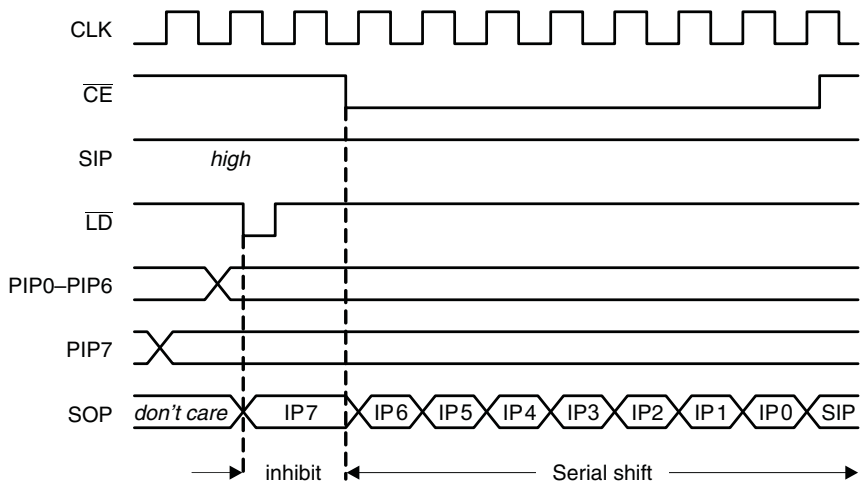


Figure 17. Interface Timing for Parallel-Load and Serial-Shift Operation of the Shift Register

9.1.4 Cascading for High Channel Count Input Modules

Designing high-channel count modules require cascading multiple SN65HVS885 devices. Simply connect the serial output (SOP) of a leading device with the serial input (SIP) of a following device without changing the processor interface.

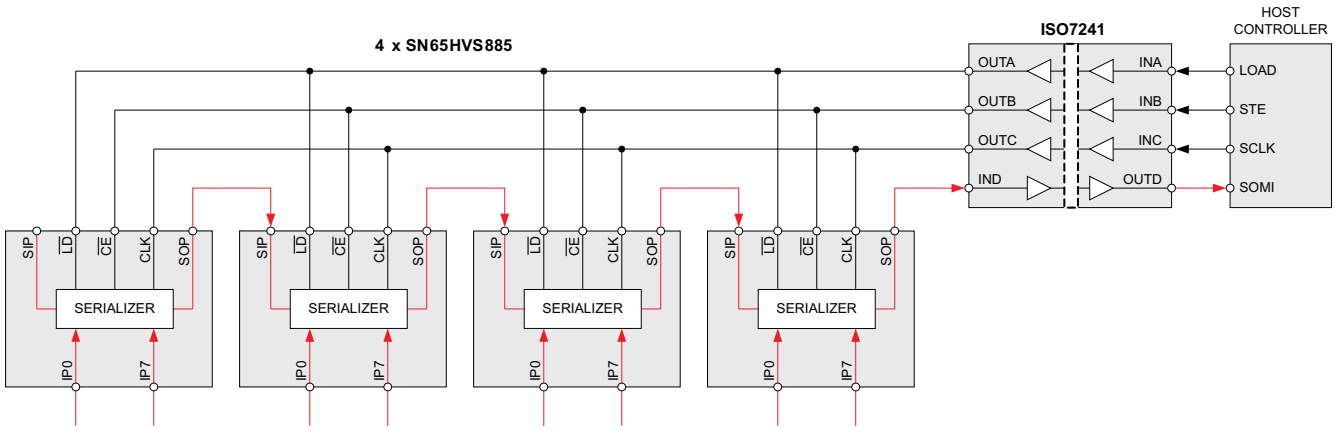


Figure 18. Cascading Four SN65HVS885 for a 32-Channel Input Module

9.2 Typical Application

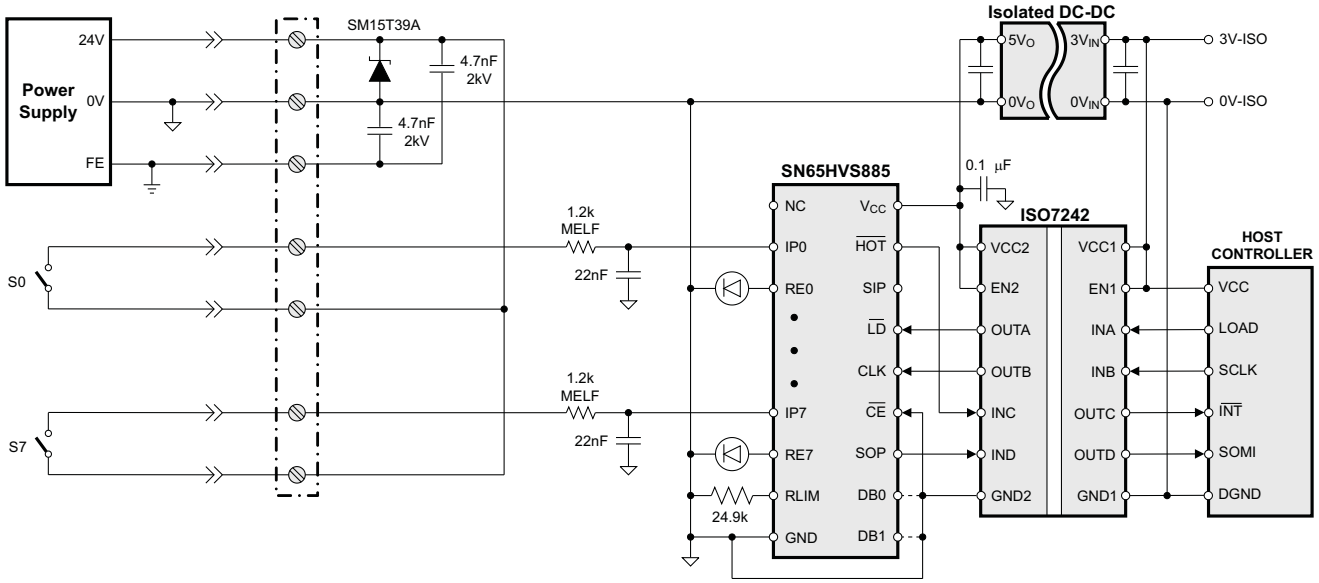


Figure 19. Typical Digital Input Module Application

9.2.1 Design Requirements

The simplified schematic in Figure 19 demonstrates a typical application of the SN65HVS885 for sensing the state of digital switches with 24-V high logic levels. In this application, a 3.3-V host controller must receive the state of 8 switches as a serial input, while remaining isolated from the high voltage power supply.

9.2.2 Detailed Design Procedure

9.2.2.1 Input Stage

Selection of the current limiting resistor R_{LIM} sets the input current limit I_{LIM} for the device. *Digital Inputs* includes necessary equations for choosing the limiting resistor.

The On/Off voltage thresholds at the device pin $V_{TH(IP+)}$ and $V_{TH(IP-)}$ are fixed to 5.2 V and 4.3 V respectively, however the On/Off voltage thresholds of the field input $V_{TH(IN+)}$ and $V_{TH(IN-)}$ are determined by the value of the series resistor RIN placed between the field input and the device. The threshold voltage $V_{TH(IN+)}$ is determined with the following equation:

$$V_{TH(IN+)} = I_{IN} \times R_{IN} + V_{TH(IP+)} \quad (2)$$

Substituting Equation 1 from section 8.3.1, and solving for R_{IN} produces an equation for R_{IN} given a desired on-threshold.

$$R_{IN} = \frac{(V_{TH(IN+)} - 5.2V) \times R_{LIM}}{90V} \quad (3)$$

The following equation can be used to calculate the off-threshold voltage given a value for R_{IN}

$$V_{TH(IN-)} = \frac{90V \times R_{IN}}{R_{LIM}} + V_{TH(IP-)} \quad (4)$$

Figure 20 contains an example input characteristic:

Typical Application (continued)

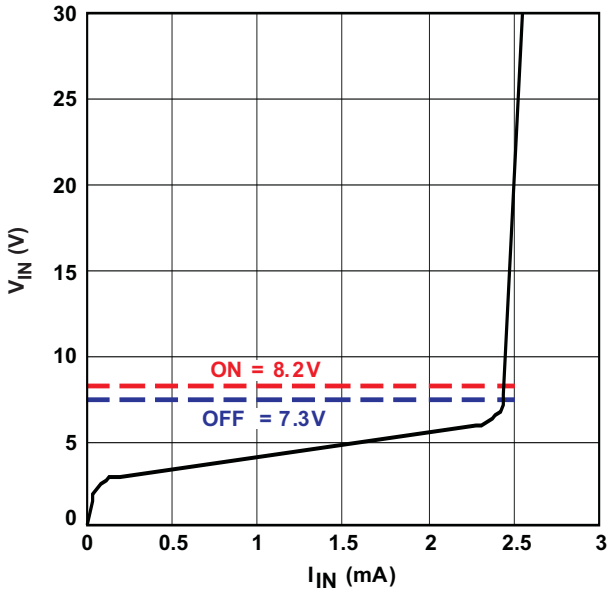


Figure 20. SN65HVS885 Example Input Characteristic

9.2.2.2 Setting Debounce Time

The logic signals at the DB0 and DB1 pins determine the denounce times for the device according to the table in section 6.5. The DB0 and DB1 pins are internally pulled high. Connecting the pins to GND in different configurations allows for selection of 0, 1, or 3ms debounce times. In noisy environments, it is recommended that unused DB pins should be connected externally to a 5 V supply.

9.2.2.3 Using the HOT Indicator

The HOT pin can be used as a visual health indicator for the device. To use the HOT pin as a health indicator, a green LED can be connected (with a series resistor) between the HOT pin and ground. If the device exceeds recommended operating temperature, the LED will turn off. Alternatively, the HOT pin can be connected to the MCU to trigger an interrupt if temperature limits are exceeded.

9.2.2.4 Example: High-Voltage Sensing Application

For the high-voltage sensing application in Figure 19, inputs from each switch (S0-S7) are connected to the 8 parallel inputs (IP0-IP7) of the SN65HVS885 through 1.2kΩ MELF resistors. Small capacitors (22nF) are tied to ground at each input to provide noise protection for the signals. A resistor is added between the R_{LIM} pin and GND to provide a device current limit according to the equation I_{LIM} = 90 V / R_{LIM}. In this example, with a 24.9kΩ resistor, the current limit for the device is set to 3.6mA. LEDs are placed between pins RE0-RE7 to allow for external status observation of the parallel inputs. Finally the SN65HVS885 is connected through a digital isolation device to the host controller to provide galvanic isolation to the external interfaces and to allow for communication between the 5 V SN65HVS885 logic and the 3.3-V host controller. The host controller manages mode switching and clocking of the SN65HVS885 through the digital isolation device.

Typical Application (continued)

9.2.3 Application Curve

The application traces acquired in Figure 21 demonstrate typical behavior for the SN65HVD885. The trace names in descending order are: Clock Signal (CE), Clock Enable Input (CE), Load Pulse Input (LD), and Serial Data Output (SOP).

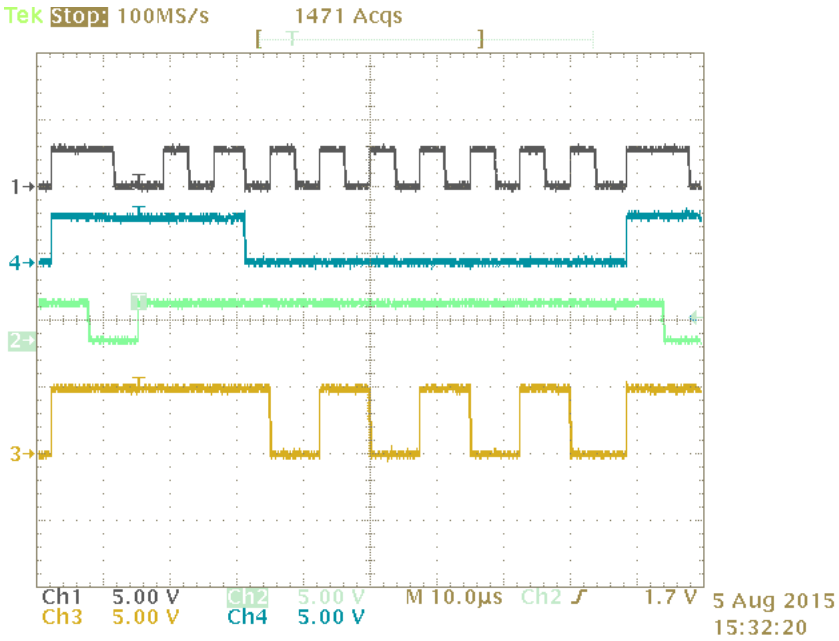


Figure 21. SN65HVD885 Application Measurements

10 Power Supply Recommendations

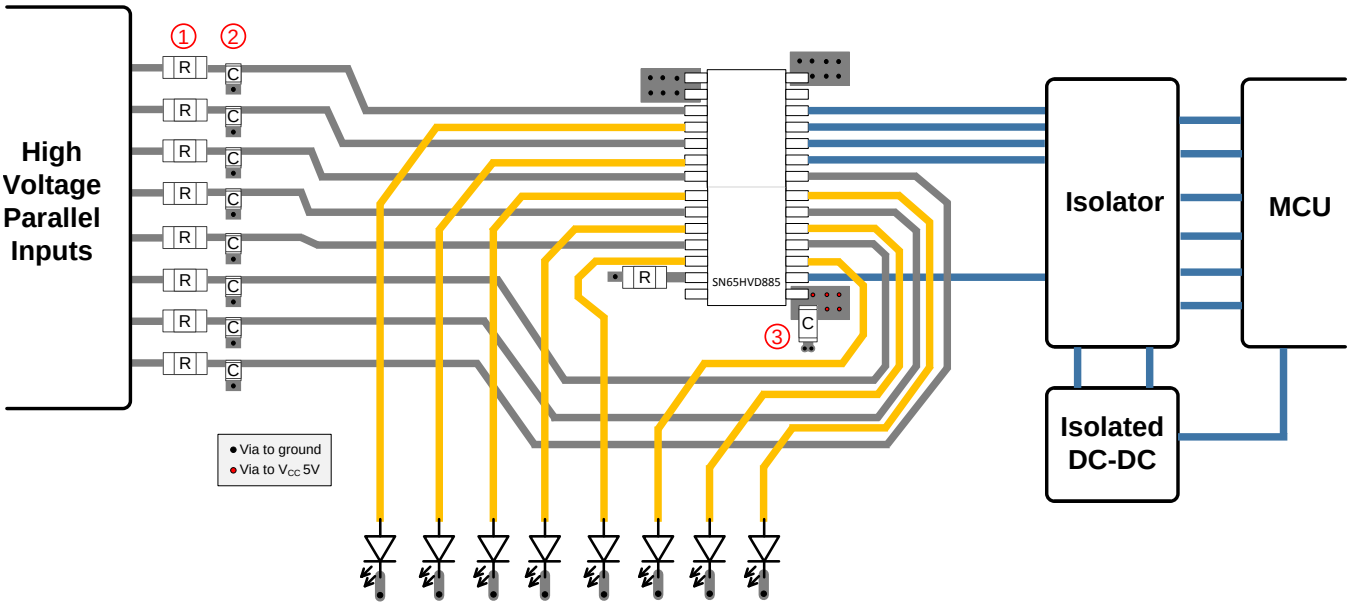
The SN65HVD885 operates within a recommended supply voltage range from 4.5 V to 5.5 V. A 0.1 µF or larger capacitor should be placed between V_{CC} and ground to improve power supply noise immunity. A current limiting resistor can be used to reduce overall power consumption as described in *Digital Inputs*. The high voltage parallel field inputs can accept voltages ranging from 0 V to 34 V, however all other inputs must remain between 0 V to 5 V. Refer to the *Recommended Operating Conditions* table for more detailed voltage suggestions. High voltage field inputs should be buffered as shown in Figure 19 to improve input noise immunity.

11 Layout

11.1 Layout Guidelines

1. Place series MELF resistors between the field inputs and the device input pins.
2. Place small ~22 nF capacitors close to the field input pins to reduce noise.
3. Place a supply buffering 0.1-µF capacitor around as close to the V_{CC} pin as possible.

11.2 Layout Example



12 Device and Documentation Support

12.1 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.2 Trademarks

PowerPAD, E2E are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

12.3 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN65HVS885PWPR	Active	Production	HTSSOP (PWP) | 28	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	HVS885
SN65HVS885PWPR.A	Active	Production	HTSSOP (PWP) | 28	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	HVS885

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

GENERIC PACKAGE VIEW

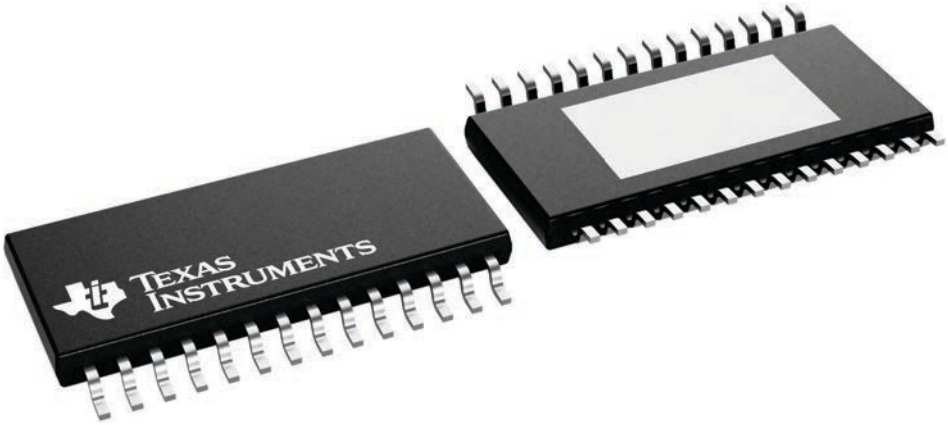
PWP 28

PowerPAD™ TSSOP - 1.2 mm max height

4.4 x 9.7, 0.65 mm pitch

SMALL OUTLINE PACKAGE

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4224765/B

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265