CDCE(L)913: Flexible Low Power LVCMOS Clock Generator With SSC Support for EMI Reduction

1 Features

- Member of programmable clock generator family
  - CDCE913/CDCEL913: 1-PLL, 3 outputs
  - CDCE925/CDCEL925: 2-PLL, 5 outputs
  - CDCE937/CDCEL937: 3-PLL, 7 outputs
  - CDCE949/CDCEL949: 4-PLL, 9 outputs
- In-system programmability and EEPROM
  - Serial programmable volatile register
  - Nonvolatile EEPROM to store customer settings
- Flexible input clocking concept
  - External crystal: 8MHz to 32MHz
  - On-chip VCXO: pull range ±150ppm
  - Single-ended LVCMOS Up to 160MHz
- Free selectable output frequency up to 230 MHz
- Low-noise PLL core
  - PLL loop filter components integrated
  - Low period jitter (typical 50ps)
- Separate output supply pins
  - CDCE913: 3.3V and 2.5V
  - CDCEL913: 1.8V
- Flexible clock driver:
  - Three user-definable control inputs [S0/S1/S2], for example, SSC selection, frequency switching, output enable, or power down
  - Generates highly accurate clocks for video, audio, USB, IEEE1394, RFID, Bluetooth®, WLAN, Ethernet™, and GPS
  - Generates common clock frequencies used with TI- DaVinci™, OMAP™, DSPs
  - Programmable SSC modulation
  - Enables 0PPM clock generation
- 1.8V device power supply
- Wide temperature range: –40°C to 85°C
- Packaged in TSSOP
- Development and programming kit for easy PLL design and programming (TI Pro-Clock™)

2 Applications

- Digital Televisions (D-TVs)
- Set-Top Boxes (STBs)
- IP-STBs
- DVD players
- DVD recorders
- Printers

3 Description

The CDCE913 and CDCEL913 devices are modular PLL-based, low-cost, high-performance, programmable clock synthesizers. The devices generate up to three output clocks from a single input frequency. Each output can be programmed in-system for any clock frequency up to 230MHz, using the integrated configurable PLL.

The CDCx913 has separate output supply pins, V_{DDOUT}, which is 1.8V for CDCEL913 and 2.5V to 3.3V for CDCE913.

The input accepts an external crystal or LVCMOS clock signal. A selectable on-chip VCXO allows synchronization of the output frequency to an external control signal.

The PLL supports SSC (spread-spectrum clocking) for better electromagnetic interference (EMI) performance.

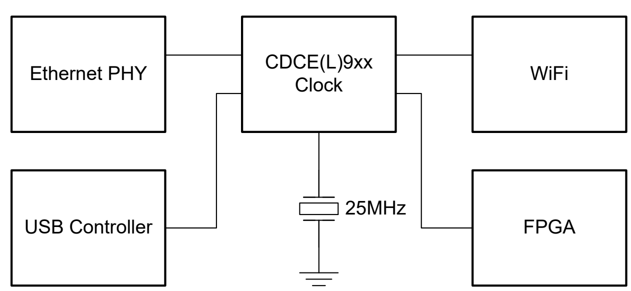
The device supports nonvolatile EEPROM programming for easy customization of the device to the application. All device settings are programmable through the SDA/SCL bus, a 2-wire serial interface.

The CDCx913 operates in a 1.8V environment and operates in a temperature range of –40°C to 85°C.

Package Information

PART NUMBER	PACKAGE (1)	PACKAGE SIZE(2)
CDCE913 CDCEL913	PW (TSSOP, 14)	5mm × 6.4mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Typical Application Schematic

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4 Pin Configuration and Functions

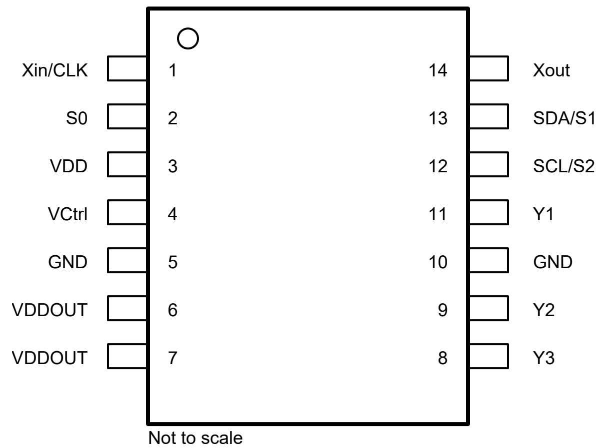


Figure 4-1. PW Package 14-Pin TSSOP Top View

Table 4-1. Pin Functions

PIN		Type[1]	DESCRIPTION
NAME	NO.		
GND	5, 10	G	Ground
SCL/S2	12	I	**SCL:** serial clock input LVCMOS (default configuration), internal pullup 500 kΩ or **S2:** user-programmable control input; LVCMOS inputs; 500-kΩ internal pullup
SDA/S1	13	I/O or I	**SDA:** bidirectional serial data input/output (default configuration), LVCMOS internal pullup; or **S1:** user-programmable control input; LVCMOS inputs; 500-kΩ internal pullup
S0	2	I	User-programmable control input S0; LVCMOS inputs; 500-kΩ internal pullup
VCtrl	4	I	VCXO control voltage (leave open or pull up when not used)
VDD	3	P	1.8-V power supply for the device
VDDOUT	6, 7	P	**CDCE913:** 3.3-V or 2.5-V supply for all outputs
			CDCEL913: 1.8-V supply for all outputs
Xin/CLK	1	I	Crystal oscillator input or LVCMOS clock Input (selectable through SDA/SCL bus)
Xout	14	O	Crystal oscillator output (leave open or pull up when not used)
Y1	11	O	LVCMOS outputs
Y2	9	O	LVCMOS outputs
Y3	8	O	LVCMOS outputs

1. In = Input, O = Output, I/O = Input or Output G = Ground, P = Power

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{DD}	Supply voltage		–0.5	2.5	V
V_{DDOUT}	Output clocks supply voltage	CDCEL913	–0.5	V_{DD}	V
		CDCE913	–0.5	3.6 + 0.5	
V_I	Input voltage(2) (3)		–0.5	V_{DD} + 0.5	V
V_O	Output voltage(2)		–0.5	V_{DDOUT} + 0.5	V
I_I	Input current (V_I < 0, V_I > V_{DD})			20	mA
I_O	Continuous output current			50	mA
T_J	Maximum junction temperature			125	°C
T_{stg}	Storage temperature		–65	150	

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime
(2) The input and output negative voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
(3) SDA and SCL can go up to 3.6 V as stated in the *Recommended Operating Conditions* table.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
V_{DD}	Device supply voltage	1.7	1.8	1.9	V
V_O	Output Yx supply voltage for CDCE913, V_{DDOUT}	2.3		3.6	V
	Output Yx supply voltage for CDCEL913, V_{DDOUT}	1.7		1.9	
V_{IL}	Low-level input voltage, LVCMOS			0.3 × V_{DD}	V
V_{IH}	High-level input voltage, LVCMOS	0.7 × V_{DD}			V
$V_{I\ (thresh)}$	Input voltage threshold, LVCMOS		0.5 × V_{DD}		V
$V_{I(S)}$	Input voltage range, S0	0		1.9	V
	Input voltage range S1, S2, SDA, SCL; $V_{I(thresh)}$ = 0.5 V_{DD}	0		3.6	
$V_{I(CLK)}$	Input voltage range CLK	0		1.9	V
I_{OH} /I_{OL}	Output current (V_{DDOUT} = 3.3 V)			±12	mA
	Output current (V_{DDOUT} = 2.5 V)			±10	
	Output current (V_{DDOUT} = 1.8 V)			±8	
C_L	Output load, LVCMOS			15	pF
T_A	Operating free-air temperature	–40		85	°C
RECOMMENDED CRYSTAL/VCXO SPECIFICATIONS (1)					
f_{Xtal}	Crystal input frequency range (fundamental mode)	8	27	32	MHz
ESR	Effective series resistance			100	Ω
f_{PR}	Pulling range (0 V ≤ V_{Ctrl} ≤ 1.8 V)(2)	±120	±150		ppm
	Frequency control voltage, V_{Ctrl}	0		V_{DD}	V

		MIN	NOM	MAX	UNIT
C_0/C_1	Pullability ratio			220	
C_L	On-chip load capacitance at Xin and Xout	0		20	pF

(1) For more information about VCXO configuration, and crystal recommendation, see *VCXO Application Guideline for CDCE(L)9xx Family* (application note).
(2) Pulling range depends on crystal type, on-chip crystal load capacitance, and PCB stray capacitance; pulling range of minimum ±120 ppm applies for crystal listed in *VCXO Application Guideline for CDCE(L)9xx Family* (application note).

5.4 Thermal Information

over operating free-air temperature range (unless otherwise noted)

THERMAL METRIC[(1)] [(2)] [(3)]			CDCEx913 PW [TSSOP] 14 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	Airflow 0 lfm	106	°C/W
		Airflow 150 lfm	93	
		Airflow 200 lfm	92	
		Airflow 250 lfm	90	
		Airflow 500 lfm	85	
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance		1.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance		66	°C/W
Ψ_{JT}	Junction-to-top characterization parameter		1.35	°C/W
Ψ_{JB}	Junction-to-board characterization parameter		61.83	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance		62	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application note.
(2) The package thermal impedance is calculated in accordance with JESD 51 and JEDEC2S2P (high-K board).
(3) For the most-current package and ordering information, see the *Package Option Addendum* at the end of this document, or see the TI website at www.ti.com.

5.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

		TEST CONDITIONS		MIN	TYP[(1)]	MAX	UNIT
OVERALL PARAMETER							
I_{DD}	Supply current (see Figure 5-1)	All outputs off, f_{CLK} = 27 MHz, f_{VCO} = 135 MHz; f_{OUT} = 27 MHz	All PLLS on		11		mA
			Per PLL		9		
$I_{DD(OUT)}$	Supply current (see Figure 5-2 and Figure 5-3)	No load, all outputs on, f_{OUT} = 27 MHz	V_{DDOUT} = 3.3 V		1.3		mA
			V_{DDOUT} = 1.8 V		0.7		
$I_{DD(PD)}$	Power-down current. Every circuit powered down except SDA/SCL	f_{IN} = 0 MHz, V_{DD} = 1.9 V			30		µA
$V_{(PUC)}$	Supply voltage V_{dd} threshold for power-up control circuit			0.85		1.45	V
f_{VCO}	VCO frequency range of PLL			80		230	MHz
f_{OUT}	LVCMOS output frequency	V_{DDOUT} = 3.3 V				230	MHz
		V_{DDOUT} = 1.8 V				230	
LVCMOS PARAMETER							
V_{IK}	LVCMOS input voltage	V_{DD} = 1.7 V; I_I = –18 mA				–1.2	V
I_I	LVCMOS input current	V_I = 0 V or V_{DD}; V_{DD} = 1.9 V				±5	µA
I_{IH}	LVCMOS input current for S0/S1/S2	V_I = V_{DD}; V_{DD} = 1.9 V				5	µA
I_{IL}	LVCMOS input current for S0/S1/S2	V_I = 0 V; V_{DD} = 1.9 V				–4	µA

over recommended operating free-air temperature range (unless otherwise noted)

		TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
C_I	Input capacitance at Xin/Clk	V_{IClk} = 0 V or V_{DD}		6		pF
	Input capacitance at Xout	V_{IXout} = 0 V or V_{DD}		2		
	Input capacitance at S0/S1/S2	V_{IS} = 0 V or V_{DD}		3		
CDCE913 - LVCMOS PARAMETER FOR V_{DDOUT} = 3.3 V – MODE						
V_{OH}	LVCMOS high-level output voltage	V_{DDOUT} = 3 V, I_{OH} = –0.1 mA	2.9			V
		V_{DDOUT} = 3 V, I_{OH} = –8 mA	2.4			
		V_{DDOUT} = 3 V, I_{OH} = –12 mA	2.2			
V_{OL}	LVCMOS low-level output voltage	V_{DDOUT} = 3 V, I_{OL} = 0.1 mA			0.1	V
		V_{DDOUT} = 3 V, I_{OL} = 8 mA			0.5	
		V_{DDOUT} = 3 V, I_{OL} = 12 mA			0.8	
t_{PLH}, t_{PHL}	Propagation delay	PLL bypass		3.2		ns
t_r/t_f	Rise and fall time	V_{DDOUT} = 3.3 V (20%–80%)		0.6		ns
$t_{jit(cc)}$	Cycle-to-cycle jitter(2) (3)	1 PLL switching, Y2-to-Y3		50	70	ps
$t_{jit(per)}$	Peak-to-peak period jitter(3)	1 PLL switching, Y2-to-Y3		60	100	ps
$t_{sk(o)}$	Output skew (4), See Table 7-2	f_{OUT} = 50 MHz; Y1-to-Y3			60	ps
odc	Output duty cycle (5)	f_{VCO} = 100 MHz; Pdiv = 1	45%		55%	
CDCE913 – LVCMOS PARAMETER for V_{DDOUT} = 2.5 V – MODE						
V_{OH}	LVCMOS high-level output voltage	V_{DDOUT} = 2.3 V, I_{OH} = –0.1 mA	2.2			V
		V_{DDOUT} = 2.3 V, I_{OH} = –6 mA	1.7			
		V_{DDOUT} = 2.3 V, I_{OH} = –10 mA	1.6			
V_{OL}	LVCMOS low-level output voltage	V_{DDOUT} = 2.3 V, I_{OL} = 0.1 mA			0.1	V
		V_{DDOUT} = 2.3 V, I_{OL} = 6 mA			0.5	
		V_{DDOUT} = 2.3 V, I_{OL} = 10 mA			0.7	
t_{PLH}, t_{PHL}	Propagation delay	PLL bypass		3.6		ns
t_r/t_f	Rise and fall time	V_{DDOUT} = 2.5 V (20%–80%)		0.8		ns
$t_{jit(cc)}$	Cycle-to-cycle jitter(2) (3)	1 PLL switching, Y2-to-Y3		50	70	ps
$t_{jit(per)}$	Peak-to-peak period jitter(3)	1 PLL switching, Y2-to-Y3		60	100	ps
$t_{sk(o)}$	Output skew(4) , See Table 7-2	f_{OUT} = 50 MHz; Y1-to-Y3			60	ps
odc	Output duty cycle(5)	f_{VCO} = 100 MHz; Pdiv = 1	45%		55%	
CDCEL913 — LVCMOS PARAMETER for V_{DDOUT} = 1.8 V – MODE						
V_{OH}	LVCMOS high-level output voltage	V_{DDOUT} = 1.7 V, I_{OH} = –0.1 mA	1.6			V
		V_{DDOUT} = 1.7 V, I_{OH} = –4 mA	1.4			
		V_{DDOUT} = 1.7 V, I_{OH} = –8 mA	1.1			
V_{OL}	LVCMOS low-level output voltage	V_{DDOUT} = 1.7 V, I_{OL} = 0.1 mA			0.1	V
		V_{DDOUT} = 1.7 V, I_{OL} = 4 mA			0.3	
		V_{DDOUT} = 1.7 V, I_{OL} = 8 mA			0.6	
t_{PLH}, t_{PHL}	Propagation delay	PLL bypass		2.6		ns
t_r/t_f	Rise and fall time	V_{DDOUT} = 1.8 V (20%–80%)		0.7		ns
$t_{jit(cc)}$	Cycle-to-cycle jitter(2) (3)	1 PLL switching, Y2-to-Y3		80	110	ps
$t_{jit(per)}$	Peak-to-peak period jitter(3)	1 PLL switching, Y2-to-Y3		100	130	ps
$t_{sk(o)}$	Output skew(4), See Table 7-2	f_{OUT} = 50 MHz; Y1-to-Y3			50	ps
odc	Output duty cycle(5)	f_{VCO} = 100 MHz; Pdiv = 1	45%		55%	
SDA/SCL PARAMETER						
V_{IK}	SCL and SDA input clamp voltage	V_{DD} = 1.7 V; I_I = –18 mA			–1.2	V
I_{IH}	SCL and SDA input current	V_I = V_{DD}; V_{DD} = 1.9 V			±10	μA
V_{IH}	SDA/SCL input high voltage(6)		0.7 × V_{DD}			V
V_{IL}	SDA/SCL input low voltage(6)				0.3 × V_{DD}	V
V_{OL}	SDA low-level output voltage	I_{OL} = 3 mA, V_{DD} = 1.7 V			0.2 × V_{DD}	V

over recommended operating free-air temperature range (unless otherwise noted)

		TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
C_I	SCL/SDA input capacitance	V_I = 0 V or V_{DD}		3	10	pF

(1) All typical values are at respective nominal V_{DD}.
(2) 10,000 cycles.
(3) Jitter depends on configuration. Jitter data is for input frequency = 27 MHz, f_{VCO} = 108 MHz, f_{OUT} = 27 MHz (measured at Y2).
(4) The tsk(o) specification is only valid for equal loading of each bank of outputs, and the outputs are generated from the same divider.
(5) odc depends on output rise and fall time (t_r/t_f); data sampled on rising edge (t_r)
(6) SDA and SCL pins are 3.3-V tolerant.

5.6 EEPROM Specification

		MIN	TYP	MAX	UNIT
EEcyc	Programming cycles of EEPROM	100	1000		cycles
EEret	Data retention	10			years

5.7 Timing Requirements: CLK_IN

over recommended ranges of supply voltage, load, and operating free-air temperature

			MIN	NOM	MAX	UNIT
f_{CLK}	LVCMOS clock input frequency	PLL bypass mode	0		160	MHz
		PLL mode	8		160	
t_r / t_f	Rise and fall time CLK signal (20% to 80%)				3	ns
	Duty cycle CLK at V_{DD}/2		40%		60%	

5.8 Timing Requirements: SDA/SCL (1)

		STANDARD MODE		FAST MODE		UNIT
		MIN	MAX	MIN	MAX	
f_{SCL}	SCL clock frequency	0	100	0	400	kHz
$t_{su(START)}$	START setup time (SCL high before SDA low)	4.7		0.6		µs
$t_{h(START)}$	START hold time (SCL low after SDA low)	4		0.6		µs
$t_{w(SCLL)}$	SCL low-pulse duration	4.7		1.3		µs
$t_{w(SCLH)}$	SCL high-pulse duration	4		0.6		µs
$t_{h(SDA)}$	SDA hold time (SDA valid after SCL low)	0	3.45	0	0.9	µs
$t_{su(SDA)}$	SDA setup time	250		100		ns
t_r	SCL/SDA input rise time		1000		300	ns
t_f	SCL/SDA input fall time		300		300	ns
$t_{su(STOP)}$	STOP setup time	4		0.6		µs
t_{BUS}	Bus free time between a STOP and START condition	4.7		1.3		µs

(1) See Figure 7-8

5.9 Typical Characteristics

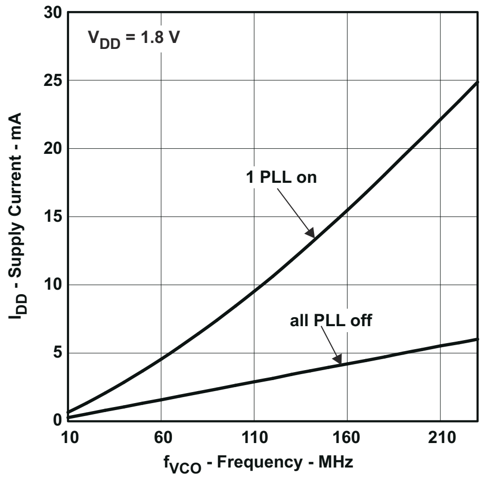


Figure 5-1. CDCE913, CDCEL913 Supply Current vs PLL Frequency

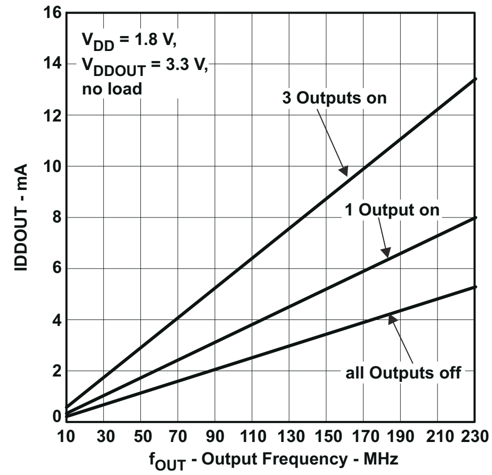


Figure 5-2. CDCE913 Output Current vs Output Frequency

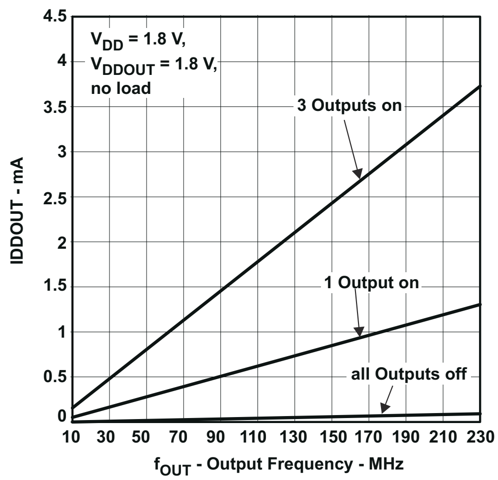


Figure 5-3. CDCEL913 Output Current vs Output Frequency

6 Parameter Measurement Information

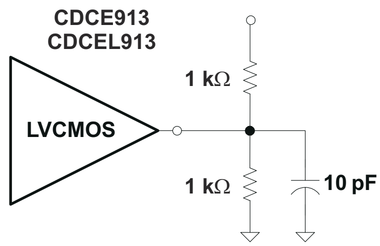


Figure 6-1. Test Load

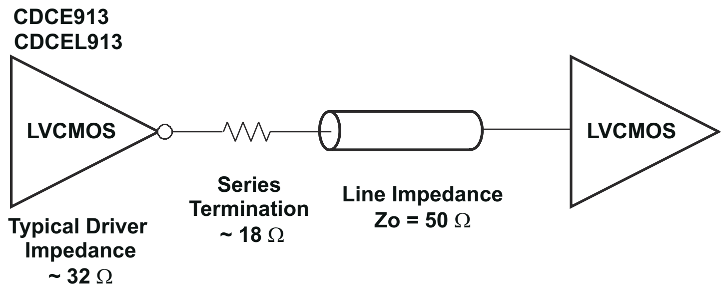


Figure 6-2. Test Load for 50-Ω Board Environment

7 Detailed Description

7.1 Overview

The CDCE913 and CDCEL913 devices are modular PLL-based, low-cost, high-performance, programmable clock synthesizers, multipliers, and dividers. The devices generate up to three output clocks from a single input frequency. Each output can be programmed in-system for any clock frequency up to 230 MHz, using the integrated configurable PLL.

The CDCx913 has separate output supply pins, V_{DDOUT}, which is 1.8 V for CDCEL913 and 2.5 V to 3.3 V for CDCE913.

The input accepts an external crystal or LVCMOS clock signal. If an external crystal is used, an on-chip load capacitor is adequate for most applications. The value of the load capacitor is programmable from 0 to 20 pF. Additionally, a selectable on-chip VCXO allows synchronization of the output frequency to an external control signal, that is, the PWM signal.

The deep M/N divider ratio allows the generation of zero-ppm audio/video, networking (WLAN, Bluetooth, Ethernet, GPS) or interface (USB, IEEE1394, memory stick) clocks from, for example, a 27-MHz reference input frequency.

The PLL supports spread-spectrum clocking (SSC). SSC can be center-spread or down-spread clocking, which is a common technique to reduce electromagnetic interference (EMI).

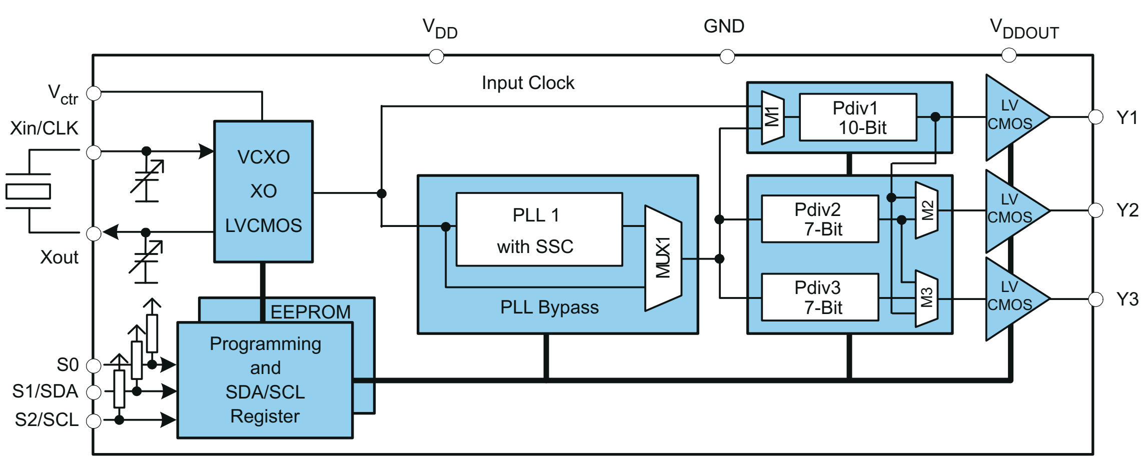
Based on the PLL frequency and the divider settings, the internal loop filter components are automatically adjusted to achieve high stability and optimized jitter transfer characteristics.

The device supports nonvolatile EEPROM programming for easy customization of the device to the application. The device is preset to a factory default configuration (see *Default Device Configuration*) that can be reprogrammed to a different application configuration before PCB assembly, or reprogrammed by in-system programming. All device settings are programmable through the SDA/SCL bus, a 2-wire serial interface.

Three programmable control inputs, S0, S1, and S2, can be used to select different frequencies, change SSC setting for lowering EMI, or control other features like outputs disable to low, outputs 3-state, power down, PLL bypass, and so forth).

The CDCx913 operates in a 1.8-V environment. The device operates in a temperature range of –40° C to 85° C.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Control Terminal Configuration

The CDCE913 or CDCEL913 has three user-definable control terminals (S0, S1, and S2), which allow external control of device settings. The devices can be programmed to any of the following functions:

- Spread-spectrum clocking selection → spread type and spread amount selection
- Frequency selection → switching between any of two user-defined frequencies
- Output state selection → output configuration and power-down control

The user can predefine up to eight different control settings. Table 7-1 and Table 7-2 explain these settings.

Table 7-1. Control Terminal Definition

EXTERNAL CONTROL BITS	PLL1 SETTING			Y1 SETTING
Control function	PLL frequency selection	SSC selection	Output Y2/Y3 selection	Output Y1 and power-down selection

Table 7-2. PLLx Setting (Can Be Selected for Each PLL Individually) (1)

SSCx [3 Bits]			CENTER	DOWN
SSC SELECTION (CENTER/DOWN)				
0	0	0	0% (off)	0% (off)
0	0	1	±0.25%	–0.25%
0	1	0	±0.5%	–0.5%
0	1	1	±0.75%	–0.75%
1	0	0	±1.0%	–1.0%
1	0	1	±1.25%	–1.25%
1	1	0	±1.5%	–1.5%
1	1	1	±2.0%	–2.0%

(1) Center-spread/down-spread, Frequency0/Frequency1 and State0/State1 are user-definable in PLLx configuration register.

Table 7-3. PLLx Setting, Frequency Selection (Can Be Selected for Each PLL Individually) (1)

FSx	FUNCTION
0	Frequency0
1	Frequency1

(1) Frequency0 and Frequency1 can be any frequency within the specified f_{VCO} range.

Table 7-4. PLLx Setting, Output Selection (1) (Y2 ... Y3)

YxYx	FUNCTION
0	State0
1	State1

(1) State0/State1 selection is valid for both outputs of the corresponding PLL module and can be power down, 3-state, low, or active.

Table 7-5. Y1 Setting (1)

Y1 SELECTION	
Y1	**FUNCTION**
0	State 0
1	State 1

(1) State0 and State1 are user definable in the generic configuration register and can be power down, 3-state, low, or active.

S1/SDA and S2/SCL pins of the CDCE913 or CDCEL913 are dual-function pins. In the default configuration, the pins are defined as SDA/SCL for the serial programming interface. The pins can be programmed as control pins (S1/S2) by setting the appropriate bits in the EEPROM. Changes to the control register (Bit **[6]** of byte **02h**) have no effect until the pins are written into the EEPROM.

After the S1/SDA and S2/SCL pins are set as control pins, the serial programming interface is no longer available. However, if V_{DDOUT} is forced to GND, the two control pins, S1 and S2, temporally act as serial programming pins (SDA/SCL).

S0 is **not** a multi-use pin. S0 is a control pin only.

7.3.2 Default Device Configuration

The internal EEPROM of the CDCE913 or CDCEL913 is preconfigured with a factory default configuration, as shown in Figure 7-1 (The input frequency is passed through the output as a default). This preconfiguration allows the device to operate in default mode without the extra production step of programming. The default setting appears after power is supplied or after a power-down–power-up sequence, until the device is reprogrammed by the user to a different application configuration. A new register setting is programmed through the serial SDA/SCL interface.

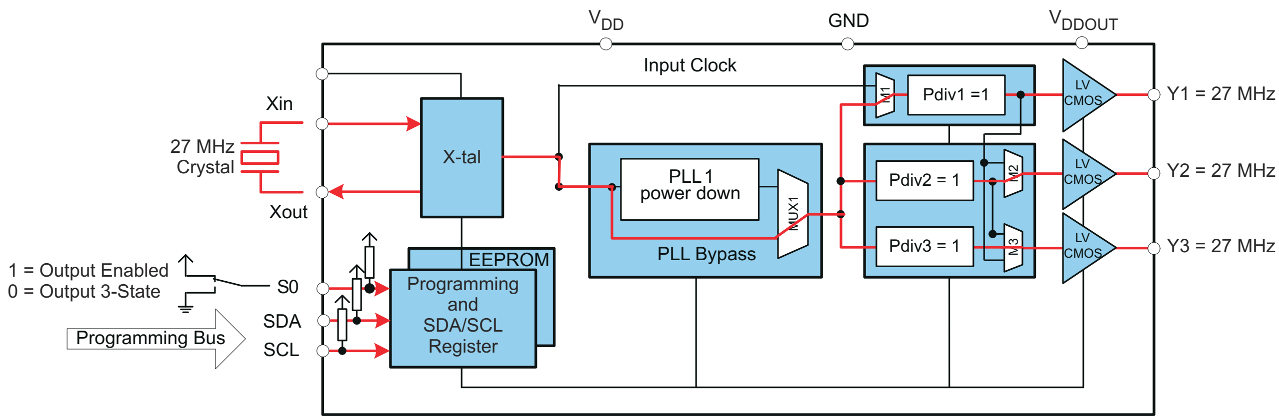


Figure 7-1. Default Configuration

Table 7-6 shows the factory default setting for the Control Terminal register. Though eight different register settings are possible, in the default configuration, only the first two settings (0 and 1) can be selected with S0, as S1 and S2 are configured as programming pins in default mode.

Table 7-6. Factory Default Setting for Control Terminal Register (1)

			Y1	PLL1 SETTINGS		
EXTERNAL CONTROL PINS			OUTPUT SELECTION	FREQUENCY SELECTION	SSC SELECTION	OUTPUT SELECTION
S2	*S1*	**S0**	**Y1**	*FS1*	*SSC1*	**Y2Y3**
SCL (I^2C)	SDA (I^2C)	**0**	3-state	f_{VCO1_0}	off	**3-state**
SCL (I^2C)	SDA (I^2C)	**1**	**Enabled**	f_{VCO1_0}	off	**Enabled**

(1) In default mode or when programmed respectively, S1 and S2 act as serial programming interface, SDA/SCL. S1 and S2 do not have any control-pin function but are internally interpreted as if S1 = 0 and S2 = 0. S0, however, is a control pin, which in the default mode switches all outputs ON or OFF (as previously predefined).

7.3.3 SDA/SCL Serial Interface

The CDCE913 or CDCEL913 operates as a target device of the 2-wire serial SDA/SCL bus, compatible with the popular SMBus or I^2C specification. The devices operate in the standard-mode transfer (up to 100 kbps) and fast-mode transfer (up to 400 kbps) and supports 7-bit addressing.

The S1/SDA and S2/SCL pins of the CDCE913 and CDCEL913 are dual function pins. In the default configuration, the pins are used as the SDA/SCL serial programming interface. The pins can be reprogrammed as general-purpose control pins, S1 and S2, by changing the corresponding EEPROM setting, byte **02h**, bit [**6**].

7.3.4 Data Protocol

The device supports *Byte Write and Byte Read* and *Block Write and Block Read* operations.

For *Byte Write/Read* operations, the system controller can individually access addressed bytes.

For *Block Write/Read* operations, the bytes are accessed in sequential order from lowest to highest byte (with most-significant bit first) with the ability to stop after any complete byte has been transferred. The numbers of bytes read out are defined by Byte Count in the generic configuration register. At the *Block Read* instruction, all bytes defined in Byte Count must be read out to finish the read cycle correctly.

After a byte has been sent, the byte is written into the internal register and is effective immediately. This applies to each transferred byte, regardless of whether this is a *Byte Write* or a *Block Write* sequence.

If the EEPROM write cycle is initiated, the internal registers are written into the EEPROM. Data can be read out during the programming sequence (*Byte Read* or *Block Read*). The programming status can be monitored by *EEPIP*, byte 01h–bit 6. Before beginning EEPROM programming, pull CLKIN LOW. CLKIN must be held LOW for the duration of EEPROM programming. After initiating EEPROM programming with *EEWRITE*, byte 06h-bit 0, do not write to the device registers until *EEPIP* is read back as a 0.

The offset of the indexed byte is encoded in the command code, as described in Table 7-8.

Table 7-7. Target Receiver Address (7 Bits)

DEVICE	A6	A5	A4	A3	A2	A1(1)	A0(1)	R/ $\overline{W}$
CDCE913/CDCEL913	**1**	**1**	**0**	**0**	**1**	**0**	**1**	**1/0**
CDCE925/CDCEL925	1	1	0	0	1	0	0	1/0
CDCE937/CDCEL937	1	1	0	1	1	0	1	1/0
CDCE949/CDCEL949	1	1	0	1	1	0	0	1/0

(1) Address bits A0 and A1 are programmable through the SDA/SCL bus (byte **01**, bits [**1:0**]. This allows addressing up to 4 devices connected to the same SDA/SCL bus. The least-significant bit of the address byte designates a write or read operation.

7.4 Device Functional Modes

7.4.1 SDA/SCL Hardware Interface

Figure 7-2 shows how the CDCE913 or CDCEL913 clock synthesizer is connected to the SDA/SCL serial interface bus. Multiple devices can be connected to the bus, but reducing the speed (400 kHz is the maximum) can be necessary if many devices are connected.

Note that the pullup resistors (R_P) depend on the supply voltage, bus capacitance, and number of connected devices. The recommended pullup value is 4.7 kΩ. The pullup value must meet the minimum sink current of 3 mA at V_{OL}max = 0.4 V for the output stages (for more details see the SMBus or I^2C Bus specification).

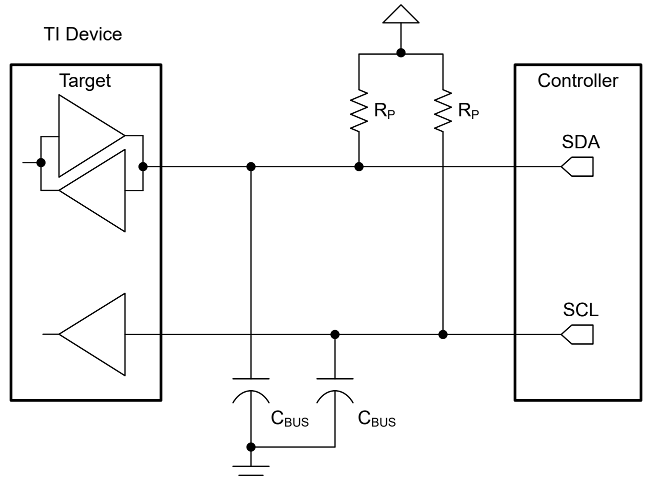


Figure 7-2. SDA / SCL Hardware Interface

7.5 Programming

Table 7-8. Command Code Definition

BIT	DESCRIPTION
7	0 = *Block Read* or *Block Write* operation 1 = *Byte Read* or *Byte Write* operation
(6:0)	Byte offset for *Byte Read*, *Block Read*, *Byte Write*, and *Block Write* operations

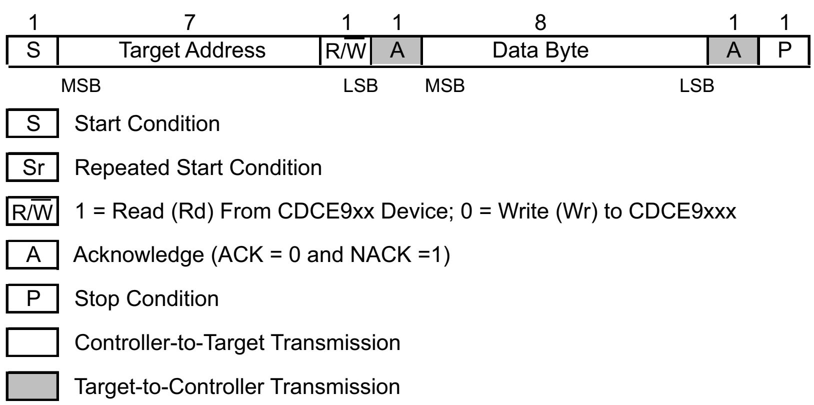


Figure 7-3. Generic Programming Sequence

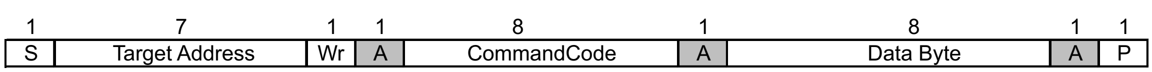


Figure 7-4. Byte Write Protocol

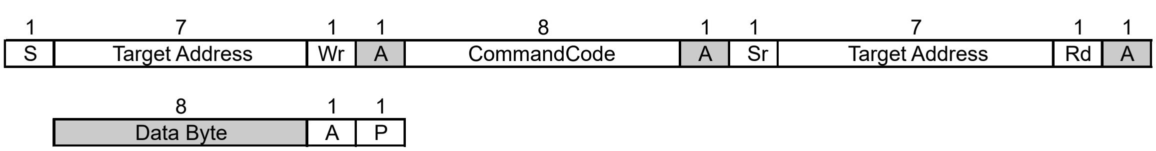


Figure 7-5. Byte Read Protocol

1	7	1	1	8	1	8	1
S	Target Address	Wr	A	CommandCode	A	Byte Count = N	A

8	1	8	1		8	1	1
Data Byte 0	A	Data Byte 1	A	...	Data Byte N-1	A	P

A. Data byte 0 bits [7:0] is reserved for Revision Code and Vendor Identification. Also, Data byte 0 is used for internal test purpose and must not be overwritten.

Figure 7-6. Block Write Protocol

1	7	1	1	8	1	1	7	1	1
S	Target Address	Wr	A	CommandCode	A	Sr	Target Address	Rd	A

8	1	8	1		8	1	1
Byte Count N	A	Data Byte 0	A	...	Data Byte N-1	A	P

Figure 7-7. Block Read Protocol

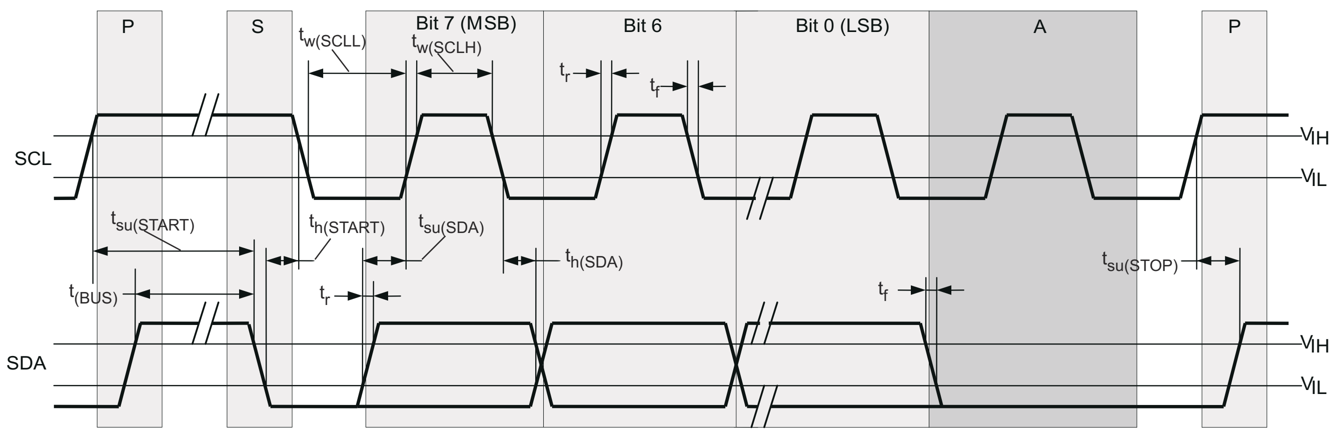


Figure 7-8. Timing Diagram for SDA/SCL Serial Control Interface

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The CDCE913 device is an easy-to-use high-performance, programmable CMOS clock synthesizer. The device can be used as a crystal buffer, clock synthesizer with separate output supply pin. The CDCE913 features an on-chip loop filter and Spread-spectrum modulation. Programming can be done through I^2C, pin-mode, or using on-chip EEPROM. This section shows some examples of the CDCE913 in various applications.

8.2 Typical Application

Figure 8-1 shows the use of the CDCEL913 in an audio/video application using a 1.8-V single supply.

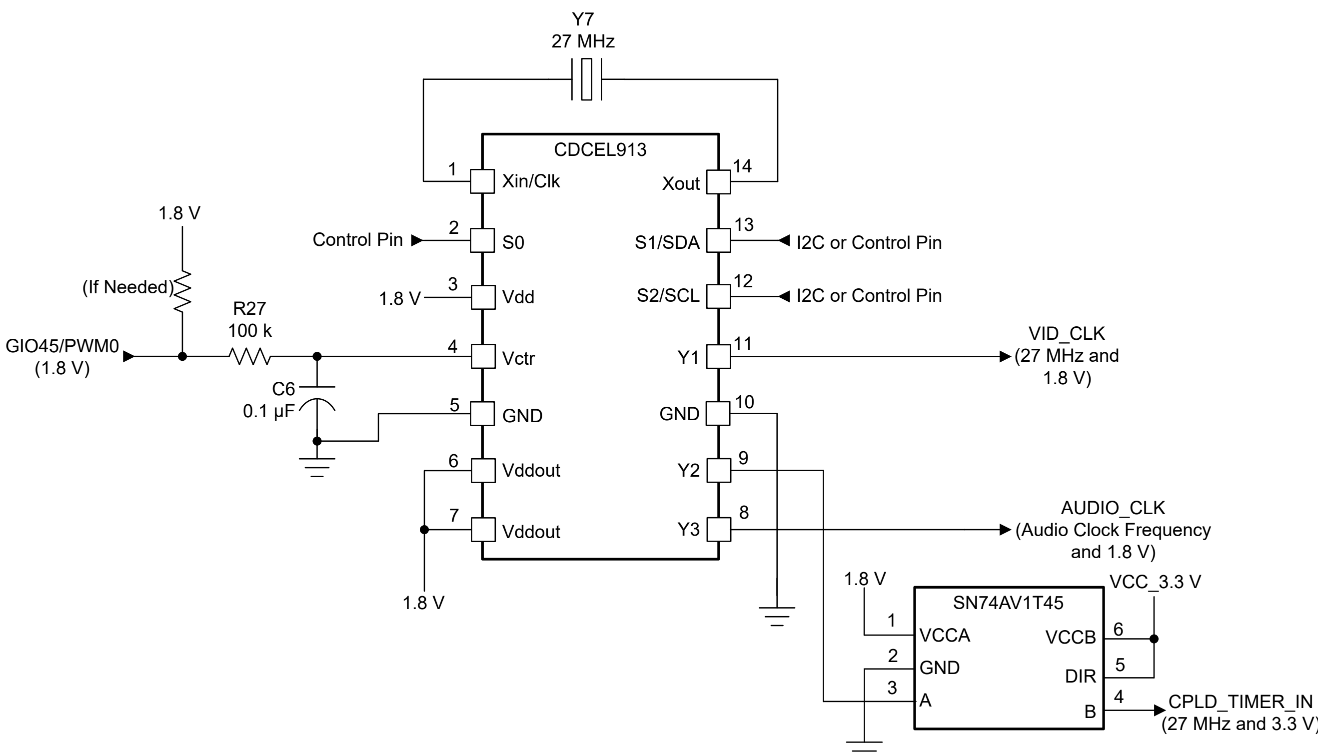


Figure 8-1. Single-Chip Solution Using CDCE913 for Generating Audio/Video Frequencies

8.2.1 Design Requirements

CDCE913 supports spread spectrum clocking (SSC) with multiple control parameters:

- Modulation amount (%)
- Modulation frequency (>20 kHz)
- Modulation shape (triangular, Hershey, and others)
- Center spread / down spread (± or –)

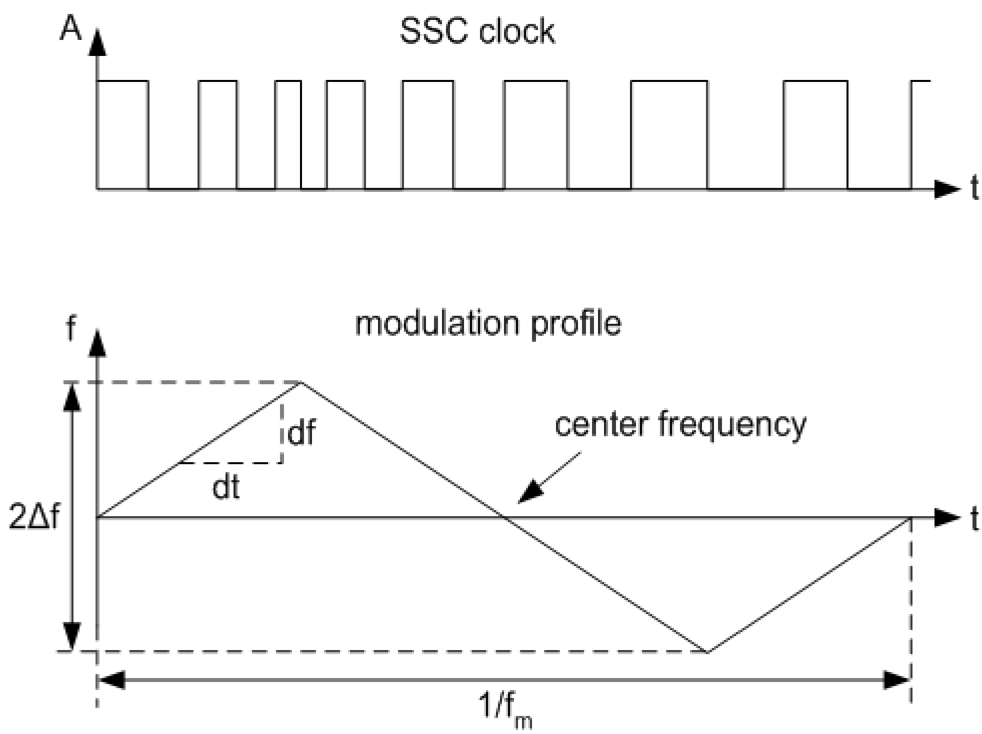


Figure 8-2. Modulation Frequency (fm) and Modulation Amount

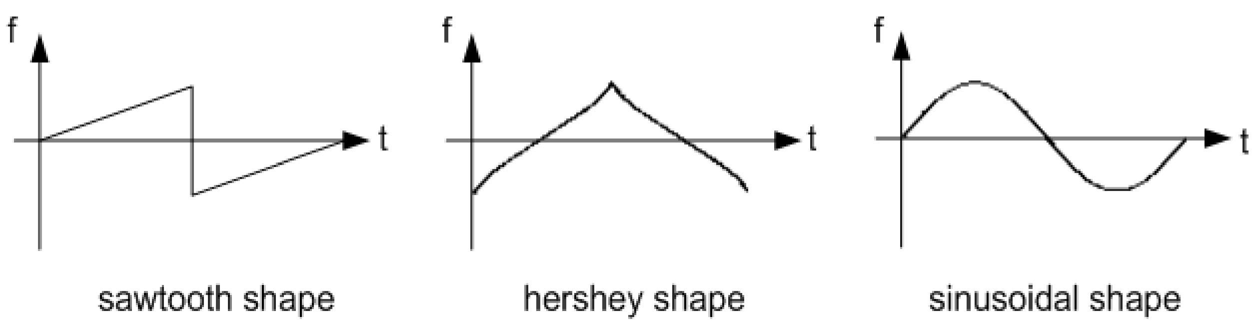
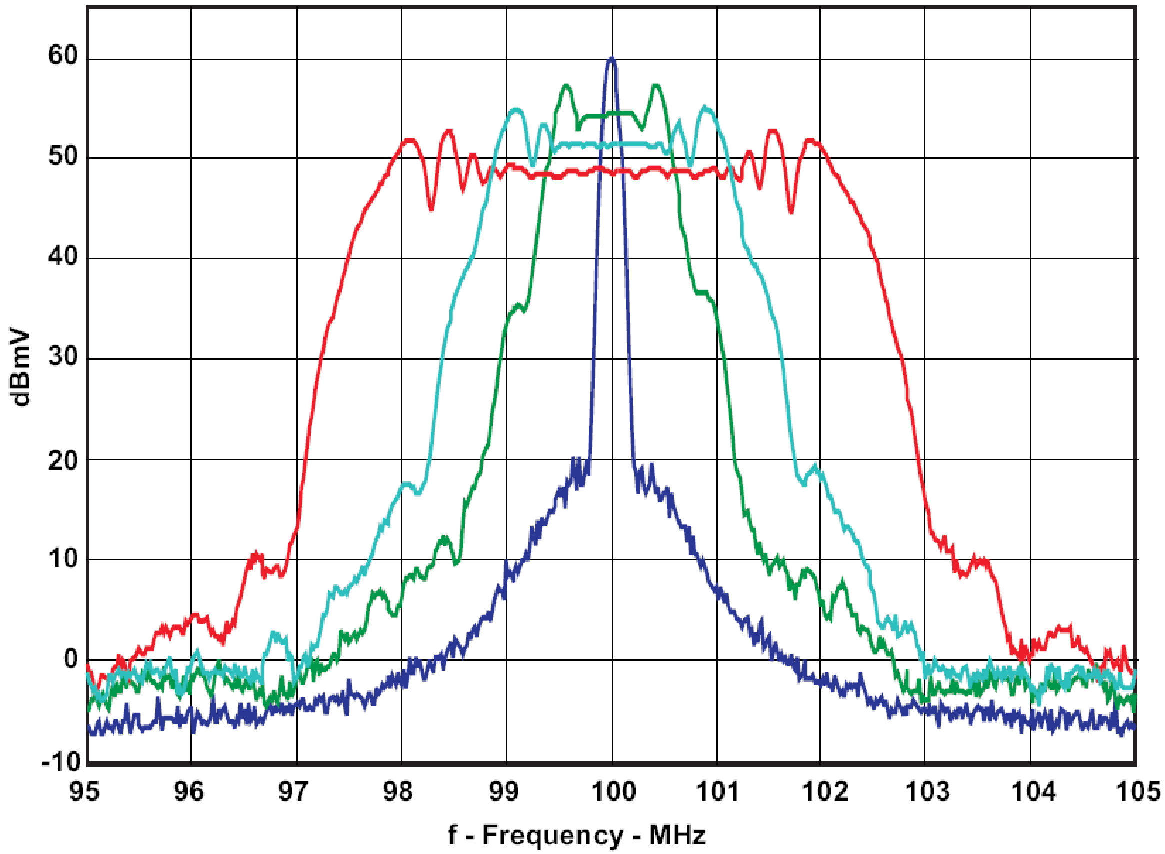


Figure 8-3. Spread Spectrum Modulation Shapes

8.2.2 Detailed Design Procedure

8.2.2.1 Spread-Spectrum Clock (SSC)

Spread-spectrum modulation is a method to spread emitted energy over a larger bandwidth. In clocking, spread spectrum can reduce Electromagnetic Interference (EMI) by reducing the level of emission from clock distribution network.



CDCS502 with a 25-MHz Crystal, FS = 1, Fout = 100 MHz, and 0%, ±0.5, ±1%, and ±2% SSC

Figure 8-4. Comparison Between Typical Clock Power Spectrum and Spread-Spectrum Clock

8.2.2.2 PLL Frequency Planning

At a given input frequency (f_{IN}), use Equation 1 to calculate the output frequency (f_{OUT}) of the CDCE913 or CDCEL913 device.

$$f_{OUT} = \frac{f_{IN}}{Pdiv} \times \frac{N}{M} \quad (1)$$

where

- M (1 to 511) and N (1 to 4095) are the multiplier/divide values of the PLL
- Pdiv (1 to 127) is the output divider

Use Equation 2 to calculate the target VCO frequency (f_{VCO}) of each PLL.

$$f_{VCO} = f_{IN} \times \frac{N}{M} \quad (2)$$

The PLL internally operates as fractional divider and requires the following multiplier/divider settings:

- N
- P = 4 – int($\log_2$N/M; if P < 0 then P = 0
- Q = int(N′/M)
- R = N′ – M × Q

where

$N' = N \times 2^P$

$N \geq M$;

$80\ MHz \leq f_{VCO} \leq 230\ MHz$

$16 \leq Q \leq 63$

$0 \leq P \leq 4$

$0 \leq R \leq 51$

Example:

for f_{IN} = 27 MHz; M = 1; N = 4; Pdiv = 2

→ f_{OUT} = 54 MHz

→ f_{VCO} = 108 MHz

→ P = 4 – int($log_2 4$) = 4 – 2 = 2

→ N' = 4 × 2^2 = 16

→ Q = int(16) = 16

→ R = 16 – 16 = 0

for f_{IN} = 27 MHz; M = 2; N = 11; Pdiv = 2

→ f_{OUT} = 74.25 MHz

→ f_{VCO} = 148.50 MHz

→ P = 4 – int($log_2 5.5$) = 4 – 2 = 2

→ N' = 11 × 2^2 = 44

→ Q = int(22) = 22

→ R = 44 – 44 = 0

The values for P, Q, R, and N' are automatically calculated when using TI Pro-Clock™ software.

8.2.2.3 Crystal Oscillator Start-up

When the CDCE913 or CDCEL913 is used as a crystal buffer, crystal oscillator start-up dominates the start-up time compared to the internal PLL lock time. The following diagram shows the oscillator start-up sequence for a 27-MHz crystal input with an 8-pF load. The start-up time for the crystal is in the order of approximately 250 µs compared to approximately 10 µs of lock time. In general, lock time is an order of magnitude less compared to the crystal start-up time.

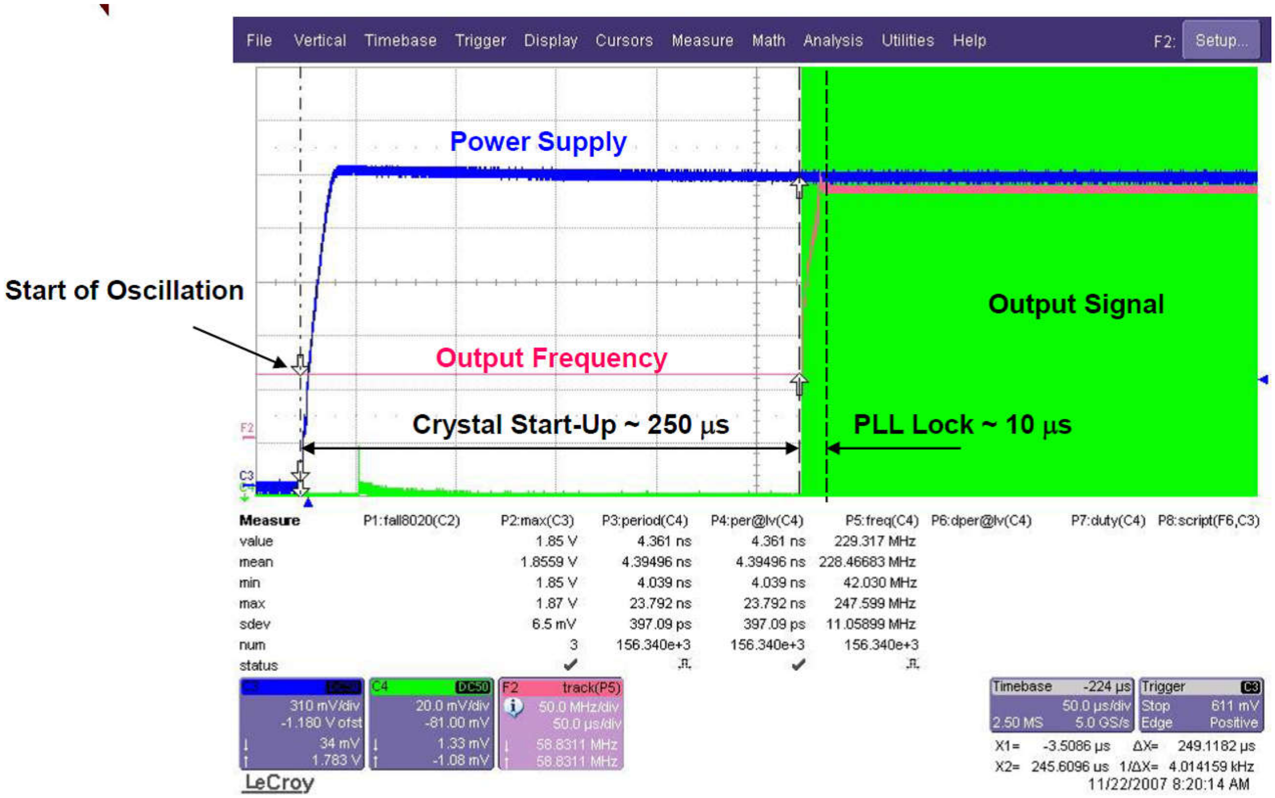


Figure 8-5. Crystal Oscillator Start-Up vs PLL Lock Time

8.2.2.4 Frequency Adjustment with Crystal Oscillator Pulling

The frequency for the CDCE913 or CDCEL913 is adjusted for media and other applications with the VCXO control input V_{Ctrl}. If a PWM-modulated signal is used as a control signal for the VCXO, an external filter is needed.

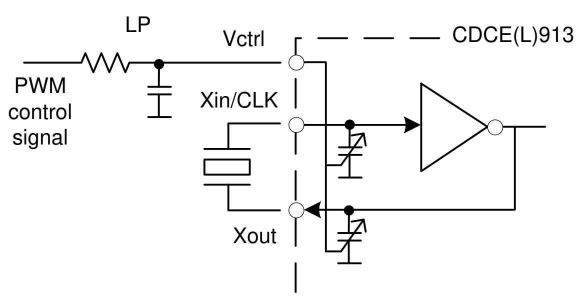


Figure 8-6. Frequency Adjustment Using PWM Input to the VCXO Control

8.2.2.5 Unused Inputs/Outputs

If VCXO pulling functionality is not required, V_{Ctrl} must be left floating. All other unused inputs must be set to GND. Unused outputs must be left floating.

If one output block is not used, TI recommends disabling the block. However, TI always recommends providing the supply for the second output block even if the block is disabled.

8.2.2.6 Switching Between XO and VCXO Mode

When the CDCE(L)913 is in crystal oscillator or in VCXO configuration, the internal capacitors require different internal capacitance. The following steps are recommended to switch to VCXO mode when the configuration for the on-chip capacitor is still set for XO mode. To center the output frequency to 0 ppm:

1. While in XO mode, put Vctrl = Vdd/2
2. Switch from X0 mode to VCXO mode
3. Program the internal capacitors to obtain 0 ppm at the output.

8.2.3 Application Curves

Figure 8-7, Figure 8-8, Figure 8-9, and Figure 8-10 show CDCE913 measurements with the SSC feature enabled. Device Configuration: 27-MHz input, 27-MHz output.

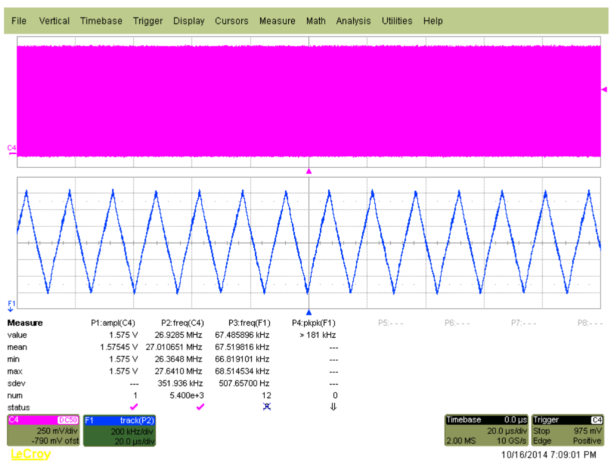


Figure 8-7. f_{OUT} = 27 MHz, VCO Frequency < 125 MHz, SSC (2% Center)

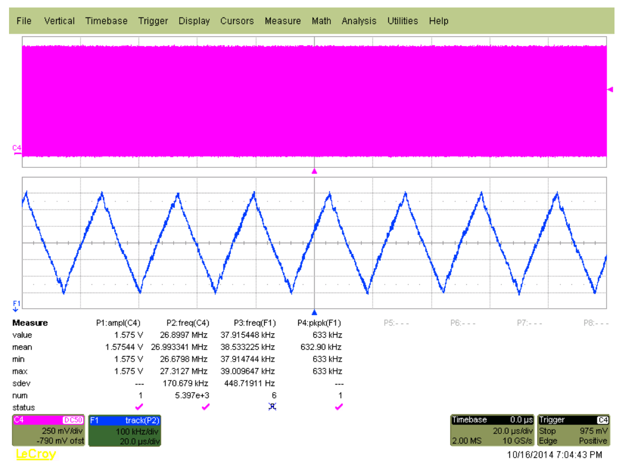


Figure 8-8. f_{OUT} = 27 MHz, VCO Frequency > 175 MHz, SSC (1%, Center)

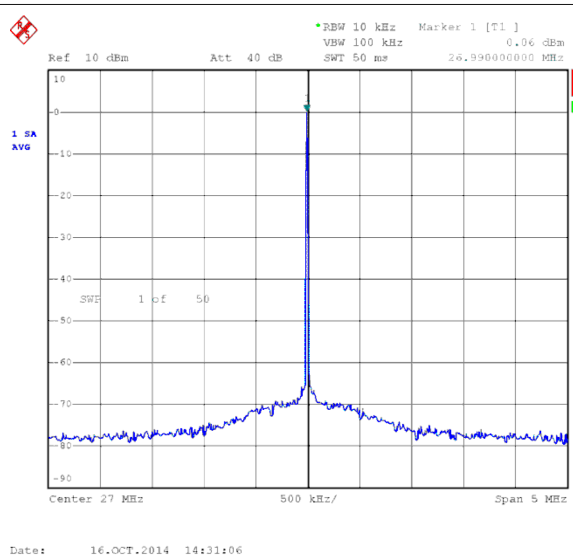


Figure 8-9. Output Spectrum With SSC Off

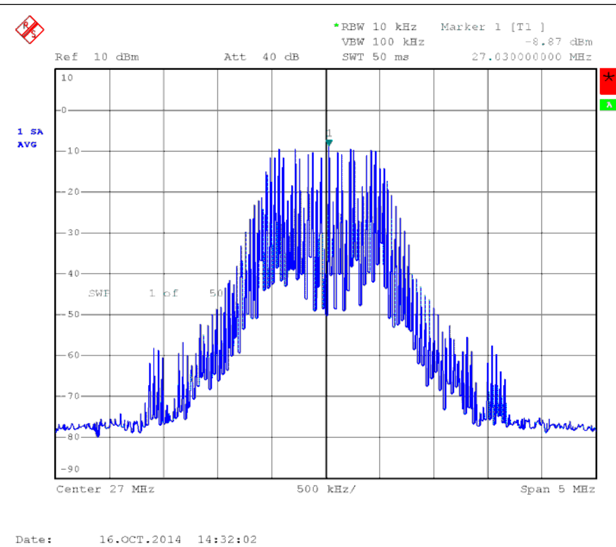


Figure 8-10. Output Spectrum With SSC On, 2% Center

8.3 Power Supply Recommendations

When using an external reference clock, XIN/CLK must be driven before V_{DD} ramps to avoid risk of unstable output. If V_{DDOUT} is applied before V_{DD}, TI recommends keeping V_{DD} pulled to GND until V_{DDOUT} is ramped. In case the V_{DDOUT} is powered while V_{DD} is floating, there is a risk of high current flowing on the V_{DDOUT}.

The device has a power-up control that is connected to the 1.8-V supply. This disables the entire device until the 1.8-V supply reaches a sufficient voltage level. Then, the device switches on all internal components, including the outputs. If there is a 3.3-V V_{DDOUT} available before the 1.8-V, the outputs stay disabled until the 1.8-V supply reaches a certain level.

8.4 Layout

8.4.1 Layout Guidelines

When the CDCE913 is used as a crystal buffer, any parasitics across the crystal affects the pulling range of the VCXO. Therefore, take care placing the crystal units on the board. Crystals must be placed as close to the device as possible, verifying that the routing lines from the crystal terminals to XIN and XOUT have the same length.

If possible, cut out both ground plane and power plane under the area where the crystal and the routing to the device are placed. In this area, always avoid routing any other signal line to avoid adding a source of noise coupling.

Additional discrete capacitors can be required to meet the load capacitance specification of certain crystal. For example, a 10.7-pF load capacitor is not fully programmable on the chip, because the internal capacitor can range from 0 pF to 20 pF with steps of 1 pF. The 0.7-pF capacitor therefore can be discretely added on top of an internal 10-pF capacitor.

To minimize the inductive influence of the trace, TI recommends placing this small capacitor as close to the device as possible and symmetrically with respect to XIN and XOUT.

Figure 8-11 shows a conceptual layout detailing recommended placement of power supply bypass capacitors. For component side mounting, use 0402 body size capacitors to facilitate signal routing. Keep the connections between the bypass capacitors and the power supply on the device as short as possible. Ground the other side of the capacitor using a low-impedance connection to the ground plane.

8.4.2 Layout Example

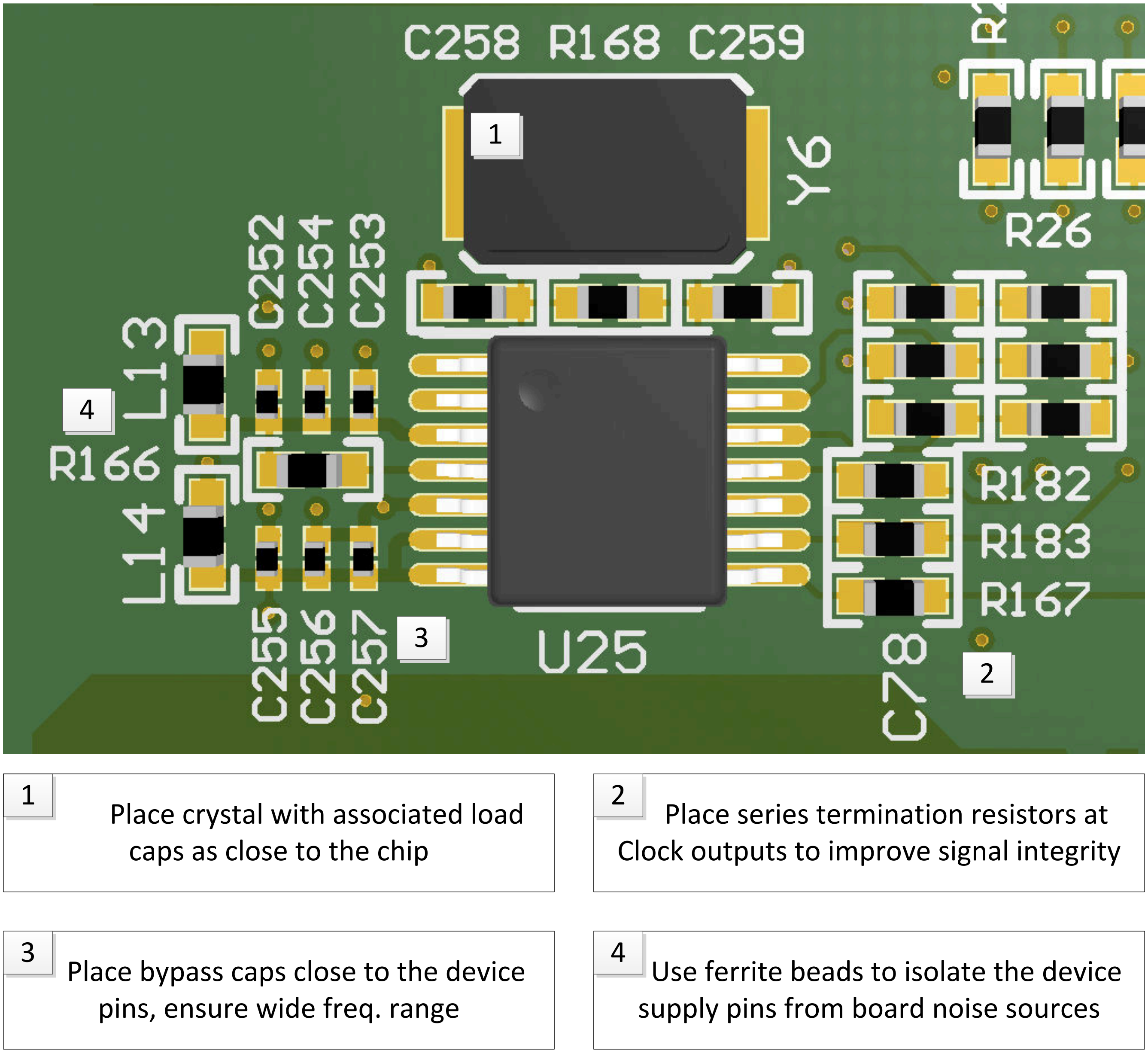


Figure 8-11. Annotated Layout

9 Register Maps

9.1 SDA/SCL Configuration Registers

The clock input, control pins, PLLs, and output stages are user configurable. The following tables and explanations describe the programmable functions of the CDCE913 or CDCEL913. All settings can be manually written into the device through the SDA/SCL bus or easily programmed by using the TI Pro-Clock™ software. TI Pro-Clock™ software allows the user to quickly make all settings and automatically calculates the values for optimized performance at lowest jitter.

Table 9-1. SDA/SCL Registers

ADDRESS OFFSET	REGISTER DESCRIPTION	TABLE
00h	Generic configuration register	Table 9-3
10h	PLL1 configuration register	Table 9-4

The grey-highlighted bits, described in the configuration register tables in the following pages, belong to the control terminal register. The user can predefine up to eight different control settings. These settings then can be selected by the external control pins, S0, S1, and S2. See *Control Terminal Configuration* .

Table 9-2. Configuration Register, External Control Terminals

				Y1	PLL1 Settings		
	EXTERNAL CONTROL PINS			OUTPUT SELECTION	FREQUENCY SELECTION	SSC SELECTION	OUTPUT SELECTION
	S2	S1	S0	Y1	FS1	SSC1	Y2Y3
0	0	0	0	Y1_0	FS1_0	SSC1_0	Y2Y3_0
1	0	0	1	Y1_1	FS1_1	SSC1_1	Y2Y3_1
2	0	1	0	Y1_2	FS1_2	SSC1_2	Y2Y3_2
3	0	1	1	Y1_3	FS1_3	SSC1_3	Y2Y3_3
4	1	0	0	Y1_4	FS1_4	SSC1_4	Y2Y3_4
5	1	0	1	Y1_5	FS1_5	SSC1_5	Y2Y3_5
6	1	1	0	Y1_6	FS1_6	SSC1_6	Y2Y3_6
7	1	1	1	Y1_7	FS1_7	SSC1_7	Y2Y3_7
	Address offset(1)			04h	13h	10h–12h	15h

(1) Address offset refers to the byte address in the configuration register in Table 9-3 and Table 9-4.

Table 9-3. Generic Configuration Register

OFFSET (1)	BIT(2)	ACRONYM	DEFAULT(3)	DESCRIPTION
00h	7	E_EL	Xb	Device identification (read-only): 1 is CDCE913 (3.3 V out), 0 is CDCEL913 (1.8 V out)
	6:4	RID	Xb	Revision identification number (read-only)
	3:0	VID	1h	Vendor identification number (read-only)
01h	7	–	0b	Reserved – always write 0
	6	EEPIP	0b	EEPROM programming Status4:(4) (read-only) — 0 – EEPROM programming is completed. 1 – EEPROM is in programming mode.
	5	EELOCK	0b	Permanently lock EEPROM data(5) — 0 – EEPROM is not locked. 1 – EEPROM is permanently locked.
	4	PWDN	0b	Device power down (overwrites S0/S1/S2 setting; configuration register settings are unchanged) Note: PWDN can not be set to 1 in the EEPROM. 0 – Device active (PLL1 and all outputs are enabled) 1 – Device power down (PLL1 in power down and all outputs in 3-state)
	3:2	INCLK	00b	Input clock selection: 00 – Xtal; 10 – LVCMOS; 01 – VCXO; 11 – Reserved
	1:0	TARGET_ADR	01b	Address bits A0 and A1 of the target receiver address
02h	7	M1	1b	Clock source selection for output Y1: 0 – Input clock; 1 – PLL1 clock
	6	SPICON	0b	Operation mode selection for pin 12/13(6) 0 – Serial programming interface SDA (pin 13) and SCL (pin 12) 1 – Control pins S1 (pin 13) and S2 (pin 12)
	5:4	Y1_ST1	11b	Y1-State0/1 definition 00 – Device power down (all PLLs in power down and all outputs in 3-State) 01 – Y1 disabled to 3-state 10 – Y1 disabled to low 11 – Y1 enabled
	3:2	Y1_ST0	01b	
	1:0	Pdiv1 [9:8]	001h	10-bit Y1-output-divider Pdiv1: 0 – Divider reset and stand-by 1 to 1023 – Divider value
03h	7:0	Pdiv1 [7:0]		
04h	7	Y1_7	0b	Y1_x State Selection(7) — 0 – State0 (predefined by Y1_ST0) 1 – State1 (predefined by Y1_ST1)
	6	Y1_6	0b	
	5	Y1_5	0b	
	4	Y1_4	0b	
	3	Y1_3	0b	
	2	Y1_2	0b	
	1	Y1_1	1b	
	0	Y1_0	0b	
05h	7:3	XCSEL	0Ah	Crystal load capacitor selection(8) — 00h – 0 pF 01h – 1 pF 02h – 2 pF :14h to 1Fh – 20 pF
	2:0		0b	Reserved – do not write other than 0
06h	7:1	BCOUNT	20h	7-bit byte count (defines the number of bytes which is sent from this device at the next *Block Read* transfer); all bytes must be read out to finish the read cycle correctly.
	0	EEWRITE	0b	Initiate EEPROM write cycle (4) (9) — 0– No EEPROM write cycle 1 – Start EEPROM write cycle (internal registers are saved to the EEPROM)
07h-0Fh		—	0h	Unused address range

(1) Writing data beyond ‘20h can affect device function.
(2) All data transferred with the MSB first
(3) Unless customer-specific setting
(4) During EEPROM programming, no data is allowed to be sent to the device through the SDA/SCL bus until the programming sequence is completed. Data, however, can be read out during the programming sequence (*Byte Read* or *Block Read*).
(5) If this bit is set to high in the EEPROM, the actual data in the EEPROM is permanently locked. No further programming is possible. Data, however can still be written through the SDA/SCL bus to the internal register to change device function on the fly, but new data can no longer be saved to the EEPROM. EELOCK is effective only if written into the EEPROM.
(6) Selection of *control pins* is effective only if written into the EEPROM. After the pins are written into the EEPROM, the serial programming pins are no longer available. However, if V_{DDOUT} is forced to GND, the two control pins, S1 and S2, temporarily act as serial programming pins (SDA/SCL), and the two target receiver address bits are reset to A0 = 0 and A1 = 0.

(7) These are the bits of the control terminal register (see Table 9-2). The user can predefine up to eight different control settings. These settings then can be selected by the external control pins, S0, S1, and S2.

(8) The internal load capacitor (C1, C2) must be used to achieve the best clock performance. External capacitors must be used only to finely adjust C_L by a few picofarads. The value of C_L can be programmed with a resolution of 1 pF for a crystal load range of 0 pF to 20 pF. For C_L > 20 pF, use additional external capacitors. The device input capacitance value must be considered, which always adds 1.5 pF (6 pF//2 pF) to the selected C_L. For more about VCXO configuration and crystal recommendation, see the *VCXO Application Guideline for CDCE(L)9xx Family* application note.

(9) The EEPROM WRITE bit must be sent last. This verifies that the content of all internal registers are stored in the EEPROM. The EEWRITE cycle is initiated with the rising edge of the EEWRITE bit. A static level-high does not trigger an EEPROM WRITE cycle. The EEWRITE bit must be reset to low after the programming is completed. The programming status can be monitored by reading out EEPIP. If EELOCK is set to high, no EEPROM programming is possible.

Table 9-4. PLL1 Configuration Register

OFFSET[1]	BIT[2]	ACRONYM	DEFAULT[3]	DESCRIPTION
10h	7:5	SSC1_7 [2:0]	000b	SSC1: PLL1 SSC selection (modulation amount). [4] **Down** / **Center** 000 (off) / 000 (off) 001 – 0.25% / 001 ± 0.25% 010 – 0.5% / 010 ± 0.5% 011 – 0.75% / 011 ± 0.75% 100 – 1.0% / 100 ± 1.0% 101 – 1.25% / 101 ± 1.25% 110 – 1.5% / 110 ± 1.5% 111 – 2.0% / 111 ± 2.0%
	4:2	SSC1_6 [2:0]	000b	
	1:0	SSC1_5 [2:1]	000b	
11h	7	SSC1_5 [0]		
	6:4	SSC1_4 [2:0]	000b	
	3:1	SSC1_3 [2:0]	000b	
	0	SSC1_2 [2]	000b	
12h	7:6	SSC1_2 [1:0]		
	5:3	SSC1_1 [2:0]	000b	
	2:0	SSC1_0 [2:0]	000b	
13h	7	FS1_7	0b	FS1_x: PLL1 frequency selection [4] 0 – f_{VCO1_0} (predefined by PLL1_0 – multiplier/divider value) 1 – f_{VCO1_1} (predefined by PLL1_1 – multiplier/divider value)
	6	FS1_6	0b	
	5	FS1_5	0b	
	4	FS1_4	0b	
	3	FS1_3	0b	
	2	FS1_2	0b	
	1	FS1_1	0b	
	0	FS1_0	0b	
14h	7	MUX1	1b	PLL1 multiplexer: 0 – PLL1 1 – PLL1 bypass (PLL1 is in power down)
	6	M2	1b	Output Y2 multiplexer: 0 – Pdiv1 1 – Pdiv2
	5:4	M3	10b	Output Y3 Multiplexer: 00 – Pdiv1-divider 01 – Pdiv2-divider 10 – Pdiv3-divider 11 – Reserved
	3:2	Y2Y3_ST1	11b	Y2, Y3-State0/1definition: 00 – Y2/Y3 disabled to 3-state (PLL1 is in power down) 01 – Y2/Y3 disabled to 3-State 10–Y2/Y3 disabled to low 11 – Y2/Y3 enabled
	1:0	Y2Y3_ST0	01b	
15h	7	Y2Y3_7	0b	Y2Y3_x output state selection. [4] 0 – State0 (predefined by Y2Y3_ST0) 1 – State1 (predefined by Y2Y3_ST1)
	6	Y2Y3_6	0b	
	5	Y2Y3_5	0b	
	4	Y2Y3_4	0b	
	3	Y2Y3_3	0b	
	2	Y2Y3_2	0b	
	1	Y2Y3_1	1b	
	0	Y2Y3_0	0b	

Table 9-4. PLL1 Configuration Register (continued)

OFFSET[1]	BIT[2]	ACRONYM	DEFAULT[3]	DESCRIPTION	
16h	7	SSC1DC	0b	PLL1 SSC down/center selection:	0 – Down 1 – Center
	6:0	Pdiv2	01h	7-bit Y2-output-divider Pdiv2:	0 – Reset and stand-by 1 to 127 – Divider value
17h	7	—	0b	Reserved – do not write others than 0	
	6:0	Pdiv3	01h	7-bit Y3-output-divider Pdiv3:	0 – Reset and stand-by 1 to 127 – Divider value
18h	7:0	PLL1_0N [11:4]	004h	PLL1_0[5]: 30-bit multiplier/divider value for frequency f_{VCO1_0} (for more information, see the *PLL Multiplier/Divider Definition* paragraph).	
19h	7:4	PLL1_0N [3:0]			
	3:0	PLL1_0R [8:5]	000h		
1Ah	7:3	PLL1_0R[4:0]			
	2:0	PLL1_0Q [5:3]	10h		
1Bh	7:5	PLL1_0Q [2:0]			
	4:2	PLL1_0P [2:0]	010b		
	1:0	VCO1_0_RANGE	00b	f_{VCO1_0} range selection:	00 – f_{VCO1_0} < 125 MHz 01 – 125 MHz ≤ f_{VCO1_0} < 150 MHz 10 – 150 MHz ≤ f_{VCO1_0} < 175 MHz 11 – f_{VCO1_0} ≥ 175 MHz
1Ch	7:0	PLL1_1N [11:4]	004h	PLL1_1[5]: 30-bit multiplier/divider value for frequency f_{VCO1_1} (for more information see the *PLL Multiplier/Divider Definition*).	
1Dh	7:4	PLL1_1N [3:0]			
	3:0	PLL1_1R [8:5]	000h		
1Eh	7:3	PLL1_1R[4:0]			
	2:0	PLL1_1Q [5:3]	10h		
1Fh	7:5	PLL1_1Q [2:0]			
	4:2	PLL1_1P [2:0]	010b		
	1:0	VCO1_1_RANGE	00b	f_{VCO1_1} range selection:	00 – f_{VCO1_1} < 125 MHz 01 – 125 MHz ≤ f_{VCO1_1} < 150 MHz 10 – 150 MHz ≤ f_{VCO1_1} < 175 MHz 11 – f_{VCO1_1} ≥ 175 MHz

(1) Writing data beyond 20h can adversely affect device function.
(2) All data is transferred MSB-first.
(3) Unless a custom setting is used.
(4) The user can predefine up to eight different control settings. In normal device operation, these settings can be selected by the external control pins, S0, S1, and S2.
(5) PLL settings limits: $16 \le q \le 63$, $0 \le p \le 7$, $0 \le r \le 511$, $0 < N < 4096$.

10 Device and Documentation Support

10.1 Documentation Support

10.1.1 Related Documentation

For related documentation, see the following:

Texas Instruments, *VCXO Application Guideline for CDCE(L)9xx Family* application note

10.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

10.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

10.4 Trademarks

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10.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.6 Glossary

TI Glossary — This glossary lists and explains terms, acronyms, and definitions.

11 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision H (February 2024) to Revision I (August 2024) — **Page**

- Included links to Applications list... 1
- Updated footnote language to conform to updated TI Datasheet Guidelines throughout the Specifications section... 4
- Updated Power Supply Recommendations section with correct power sequence... 22

Changes from Revision G (October 2016) to Revision H (February 2024) — **Page**

- Updated the numbering format for tables, figures, and cross-references throughout the document................. 1
- Changed all instances of legacy terminology to controller and target where I^2C is mentioned......................... 1
- Changed *Device Information* table to *Package Information* 1
- Changed unit kbit/s to kbps... 12
- Added information on allowable data inputs during the EEPROM write cycle in *Data Protocol* 13

Changes from Revision F (April 2015) to Revision G (October 2016)	Page
• Changed data sheet title from: *CDCEx913 Programmable 1-PLL VCXO Clock Synthesizer With 1.8-V, 2.5-V, and 3.3-V Outputs* to: *CDCE(L)913: Flexible Low Power LVCMOS Clock Generator With SSC Support for EMI Reduction*	1

Changes from Revision E (March 2010) to Revision F (April 2015)	Page
• Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section	1
• Added in Figure 9, second S to Sr	14
• Changed 100 MHz < f_{VCO} > 200 MHz; TO 80 MHz ≤ f_{VCO} ≤ 230 MHz; and changed 0 ≤ p ≤ 7 TO 0 ≤ p ≤ 4	18
• Changed under Example, fifth row, N", 2 places TO N'	18

Changes from Revision D (October 2009) to Revision E (March 2010)	Page
• Added PLL settings limits: 16≤q≤63, 0≤p≤7, 0≤r≤511 to PLL Multiplier/Divider Definition Section	18
• Added PLL settings limits: 16≤q≤63, 0≤p≤7, 0≤r≤511, 0<N<4096 foot to PLL1 Configure Register Table	24

Changes from Revision C (August 2007) to Revision D (October 2009)	Page
• Deleted sentence - A different default setting can be programmed upon customer request. Contact Texas Instruments sales or marketing representative for more information	12

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
CDCE913PW	Active	Production	TSSOP (PW) | 14	90 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CDCE913
CDCE913PW.B	Active	Production	TSSOP (PW) | 14	90 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CDCE913
CDCE913PWG4	Active	Production	TSSOP (PW) | 14	90 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CDCE913
CDCE913PWR	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CDCE913
CDCE913PWR.B	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CDCE913
CDCE913PWRG4	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CDCE913
CDCEL913PW	Active	Production	TSSOP (PW) | 14	90 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CKEL913
CDCEL913PW.B	Active	Production	TSSOP (PW) | 14	90 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CKEL913
CDCEL913PWR	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CKEL913
CDCEL913PWR.B	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CKEL913
CDCEL913PWRG4.B	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CKEL913

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF CDCE913, CDCEL913 :

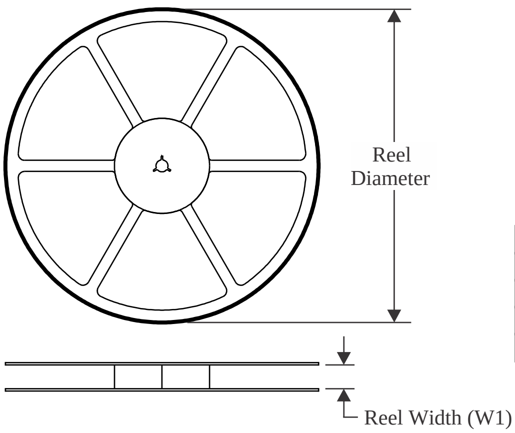
- Automotive : CDCE913-Q1, CDCEL913-Q1

NOTE: Qualified Version Definitions:

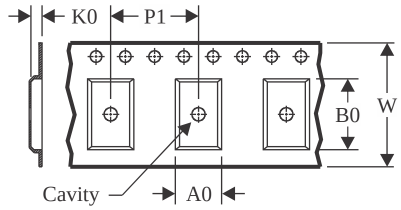
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

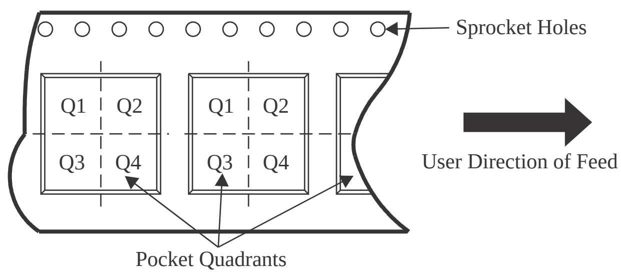


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

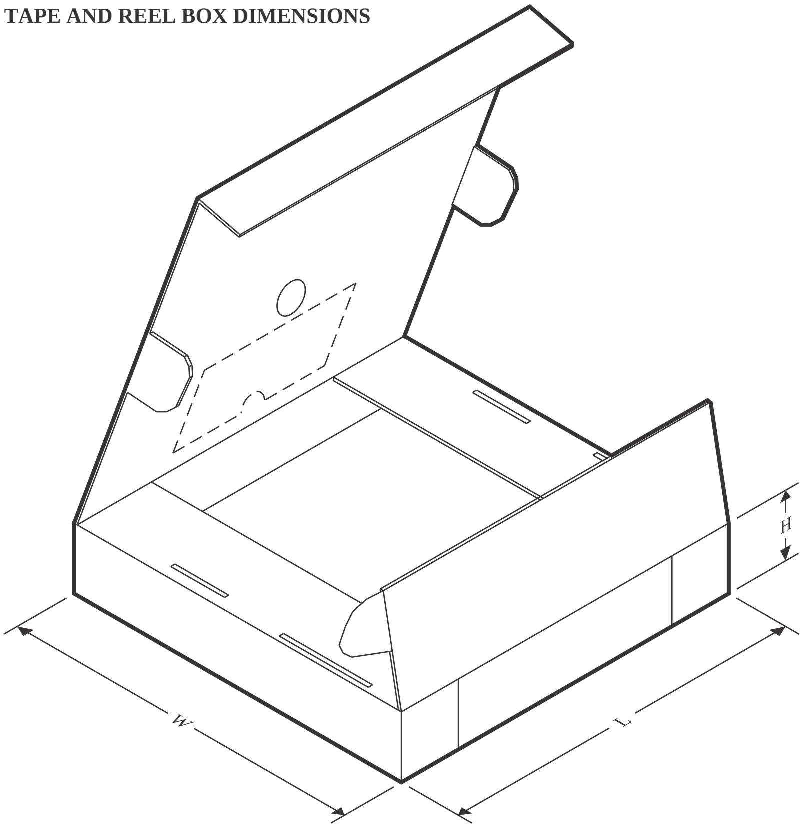
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CDCE913PWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
CDCEL913PWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

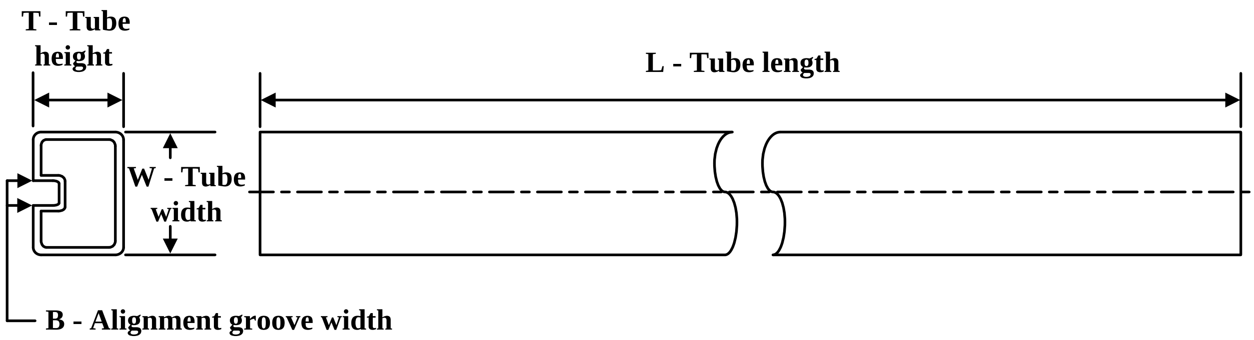
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

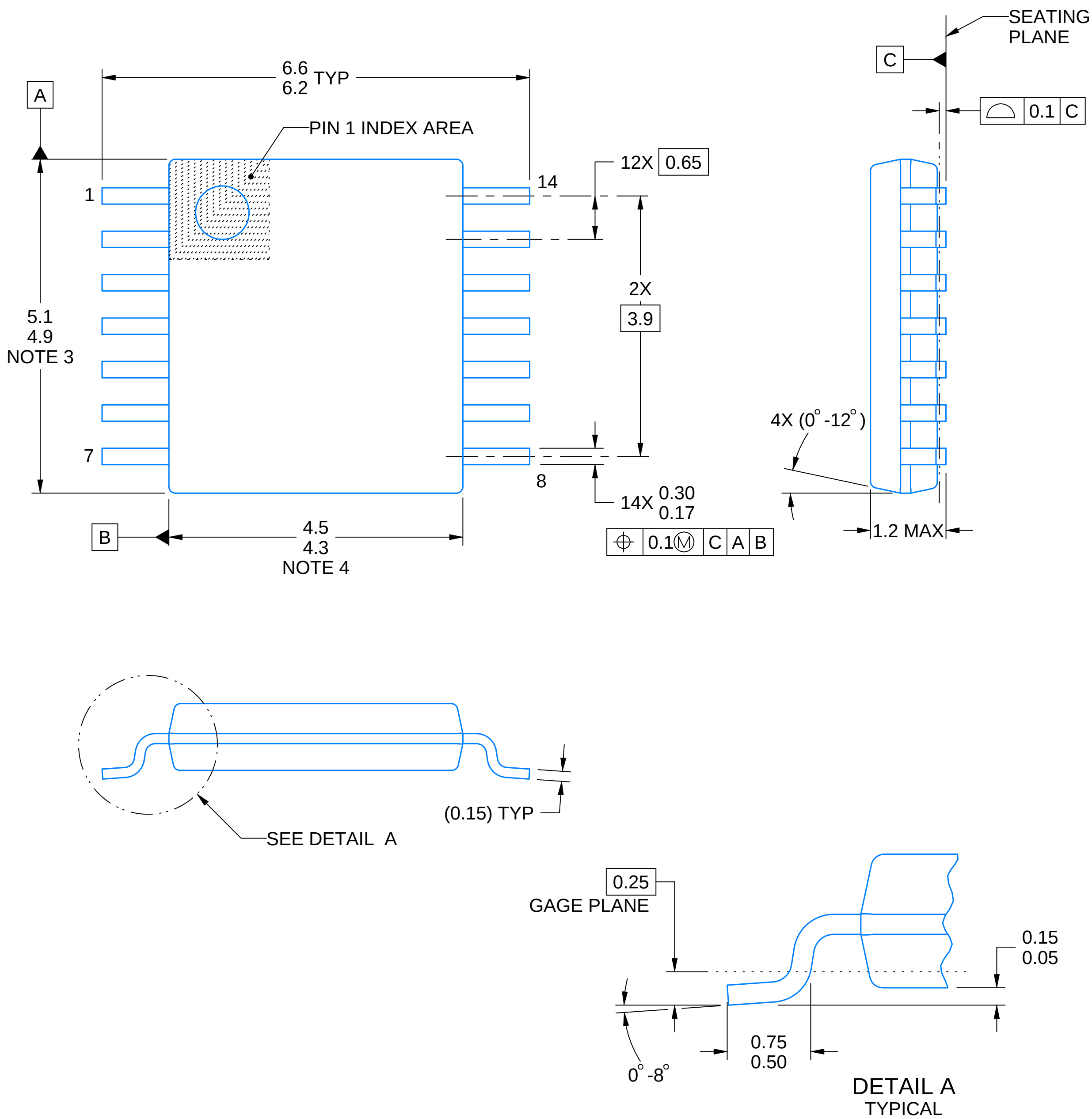
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CDCE913PWR	TSSOP	PW	14	2000	356.0	356.0	35.0
CDCEL913PWR	TSSOP	PW	14	2000	367.0	367.0	35.0

TUBE



*All dimensions are nominal

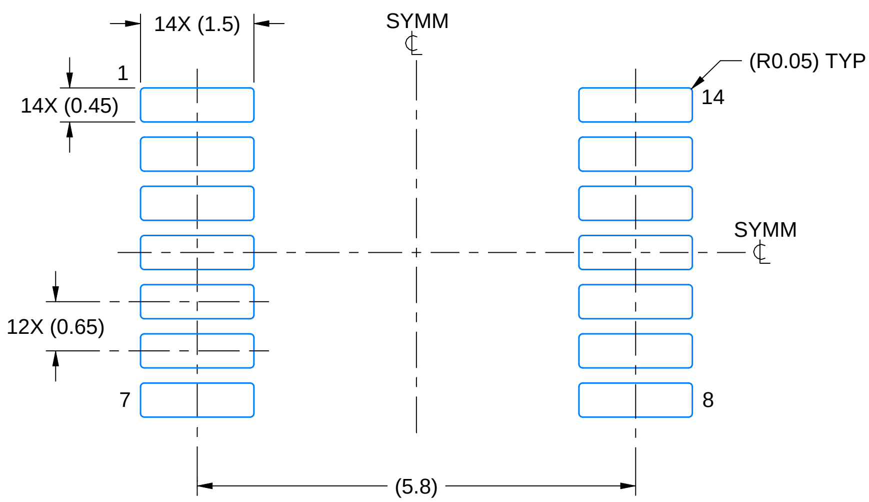
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
CDCE913PW	PW	TSSOP	14	90	530	10.2	3600	3.5
CDCE913PW.B	PW	TSSOP	14	90	530	10.2	3600	3.5
CDCE913PWG4	PW	TSSOP	14	90	530	10.2	3600	3.5
CDCEL913PW	PW	TSSOP	14	90	530	10.2	3600	3.5
CDCEL913PW.B	PW	TSSOP	14	90	530	10.2	3600	3.5



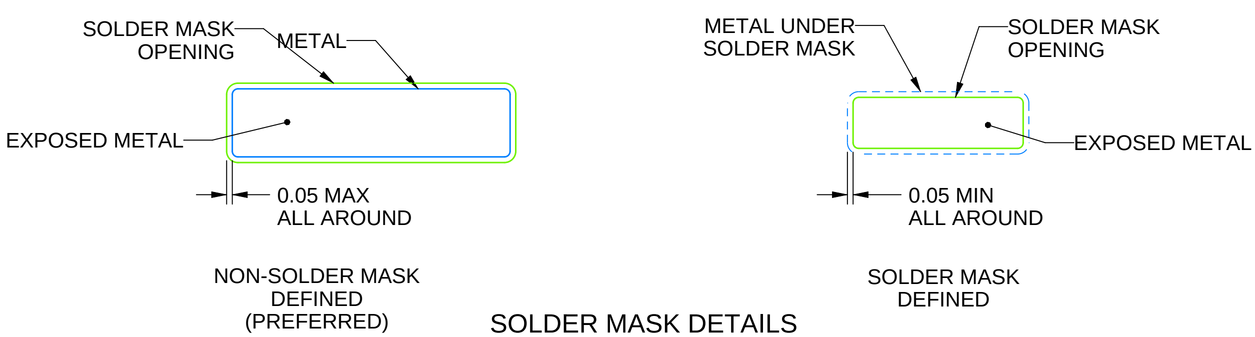
4220202/B 12/2023

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

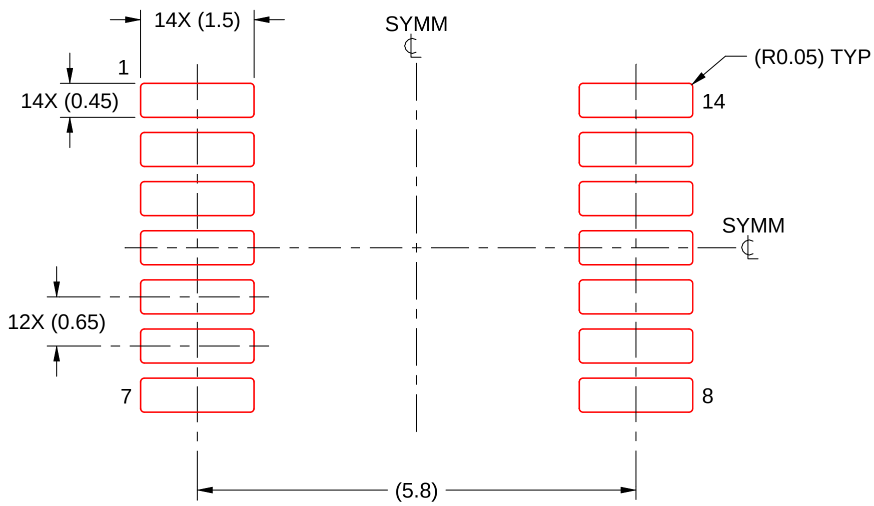


SOLDER MASK DETAILS

4220202/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220202/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.