# Digital Power Controllers

**Check for Samples: UCD3040, UCD3028, UCD3020**

## FEATURES

- Digital Control of up to Four Voltage Feedback Loops
- Up to Eight High-Resolution Digital Pulsewidth Modulated (DPWM) Outputs for Supporting a Wide Range of Offline, Isolated and Non-Isolated DC-to-DC Topologies
  - 250-ps DPWM Pulse-Width Resolution
  - 4-ns DPWM Frequency Resolution
  - Adjustable Phase Shift Between DPWM Outputs
  - Adjustable Dead Band Between Each DPWM Pair
  - Active-High or -Low DPWM Polarity
  - Up to 2-MHz DPWM Switching Frequency
- Dedicated High-Speed Error Analog-to-Digital Converter (EADC) for Each Feedback Loop With Sense Resolution of up to 1 mV
- On-Chip 10-Bit D and A Converter (DAC) for Setting EADC Reference Voltage
- Dedicated Hardware Accelerated Digital Compensators or Control Law Accelerators (CLA)
  - Three-Pole, Three-Zero Configurable Compensator
  - Features Non-Linear Digital Control
  - Multiple Programmable Coefficient Registers for Adaptive Digital Compensation
- Up to 15-Channel, 12-Bit, 200-ksps, Analog-to-Digital Converter (ADC)
- Multiple Levels of Fault Protection
  - Four High-Speed Analog Comparators
  - External Fault Inputs
  - 12-Bit ADC
- Configurable for Voltage-Mode, Average-Current-Mode, and Resonant-Mode Control
- Allows Synchronization of DPWM Waveforms Between Multiple UCD3040, UCD3020 and UCD3028 (UCD30xx) Devices
- Adjustable DPWM Pulse Width Enables Support for Current Balancing in a Multiphase Application.
- High-Performance 31.25-MHz, 32-Bit ARM7 Processor
- 32-KByte Program Flash and 2-KByte Data Flash Memory With Error Correction Code (ECC)
- 4-KByte Data RAM
- 4-KByte Boot ROM
- Communication Peripherals
  - PMBus
  - UART
  - SPI
  - JTAG (Not Available in the UCD3028)
- Single-Supply Solution: Internal Regulator Controls External Pass Element
- Internal Temperature Sensor
- Up to Five Additional Timers
- Built-In Watchdog, BOD, and POR
- 80-Pin QFP (PFC), 64-Pin QFN (RGC), 48-Pin QFN (RGZ), and 40-Pin QFN (RHA and RMH) Package Offerings
- Operating Temperature Range: –40°C to 125°C

## APPLICATIONS

- Isolated AC-to-DC and DC-to-DC Power Supplies
- Power-Factor Correction
- Non-Isolated DC-to-DC Power Supplies

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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## DESCRIPTION

The UCD30xx devices are members of a family of digital PWM controllers from Texas Instruments providing a single-chip control solution for digital power-conversion applications. These devices allow digital control implementation of a high-performance, high-frequency power supply with flexible configuration of parameters, supervisory, monitoring, and communication functions.

The UCD30xx are fully programmable solutions that are configurable to support a wide range of isolated and non-isolated topologies in single- or multiphase configurations. Some examples include interleaved PFC, isolated forward, half-bridge, phase-shifted full bridge, active clamp, and resonant LLC.

At the core of the UCD30xx controllers are the digital control-loop peripherals, also known as Fusion Digital Power™ peripherals (FDPP). Each FDPP implements a high-speed digital control loop consisting of a dedicated error analog-to-digital converter (EADC), a three-pole/three-zero (3p, 3z) digital compensator, and two DPWM outputs with 250-ps pulse-width resolution. The device also contains a 12-bit, 200-ksps general-purpose ADC with up to 15 channels, timers, interrupt controls, and communications ports such as PMBus, SCI, and SPI. The device is based on a 32-bit ARM7 RISC CPU that performs real-time monitoring, configures peripherals, and manages communications. The CPU executes its program out of programmable flash memory as well as ROM.

The UCD30xx is supported by Texas Instruments' Code Composer Studio™ software development environment.

### ORDERING INFORMATION

| OPERATING TEMPERATURE RANGE, $T_A$ | ORDERABLE PART NUMBER | PIN COUNT | SUPPLY | PACKAGE | TOP-SIDE MARKING |
|---|---|---|---|---|---|
| –40°C to 125°C | UCD3028RHAR | 40 | Reel of 2500 | QFN | UCD3028 |
| | UCD3028RHAT | 40 | Reel of 250 | QFN | UCD3028 |
| | UCD3028RMHR | 40 | Reel of 2500 | QFN | 3028RMH |
| | UCD3028RMHT | 40 | Reel of 250 | QFN | 3028RMH |
| | UCD3020RGZR | 48 | Reel of 2500 | QFN | UCD3020 |
| | UCD3020RGZT | 48 | Reel of 250 | QFN | UCD3020 |
| | UCD3040RGCR | 64 | Reel of 2000 | QFN | UCD3040 |
| | UCD3040RGCT | 64 | Reel of 250 | QFN | UCD3040 |
| | UCD3040PFCR | 80 | Reel of 1000 | QFP | UCD3040 |
| | UCD3040PFC | 80 | Tray of 119 | QFP | UCD3040 |


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## PRODUCT SELECTION MATRIX

| FEATURE | UCD3040 PFC Package | UCD3040 RGC Package | UCD3020 RGZ Package | UDC3028 RHA Package | UDC3028 RMH Package |
|---|---|---|---|---|---|
| ARM7 core processor | 31.25 MHz | 31.25 MHz | 31.25 MHz | 31.25 MHz | 31.25 MHz |
| High-resolution DPWM outputs (250-ps resolution) | 8 | 8 | 6 | 8 | 8 |
| Number of high-speed independent feedback loops (number of regulated output voltages) | 4 | 4 | 2 | 2 | 2 |
| 12-bit, 200-ksps, general-purpose ADC channels | 15 | 11 | 9 | 9 | 9 |
| Digital comparators at ADC outputs | 6 | 6 | 6 | 6 | 6 |
| Flash memory (program) | 32 KB | 32 KB | 32 KB | 32 KB | 32 KB |
| Flash memory (data) | 2 KB | 2 KB | 2 KB | 2 KB | 2 KB |
| Flash security | √ | √ | √ | √ | √ |
| RAM | 4 KB | 4 KB | 4 KB | 4 KB | 4 KB |
| DPWM switching frequency | Up to 2 MHz | Up to 2 MHz | Up to 2 MHz | Up to 2 MHz | Up to 2 MHz |
| Programmable fault inputs | 8 | 8 | 6 | 2 | 2 |
| High-speed analog comparators | 4 | 4 | 4 | 4 | 4 |
| UART (SCI) | 1 | 1 | 1 | 1 (1) | 1 (1) |
| PMBus | √ | √ | √ | √ | √ |
| Timers | 4 (16-bit) and 1 (24-bit) | 4 (16- bit) and 1 (24-bit) | 4 (16-bit) and 1 (24-bit) | 4 (16-bit) and 1 (24-bit) | 4 (16-bit) and 1 (24-bit) |
| Timer PWM outputs | 4 | 4 | 2 | 2 | 2 |
| Timer compare outputs | 1 | 1 (2) | 1 (2) | 0 | 0 |
| Timer capture inputs | 2 | 2 (2) | 2 (2) | 0 | 0 |
| Watchdog | √ | √ | √ | √ | √ |
| On-chip oscillator | √ | √ | √ | √ | √ |
| Power-on reset and brownout reset | √ | √ | √ | √ | √ |
| JTAG | √ | √ | √ | | |
| Package offering | 80-pin QFP (14 mm × 14 mm) | 64-pin QFN (9 mm × 9 mm) | 48-pin QFN (7 mm × 7 mm) | 40-pin QFN (6 mm × 6 mm) | 40-pin QFN (6 mm × 6 mm) |
| On-chip voltage-regulator control (external-pass element) | √ | √ | √ | √ | √ |
| Sync IN and sync OUT functions | √ | √ (2) | √ (2) | √ (1) | √ (1) |
| Total GPIO (includes all pins with multiplexed functions, such as DPWM, fault inputs, SCI, SPI, etc.) | 33 | 26 | 21 | 20 | 20 |
| External Vref for 12-bit ADC | √ | | √ | | |
| External interrupts | 2 | 2 (2) | 2 (2) | | |
| SPI | 1 | 1 (1) | 1 (1) | | |

(1) Multiplexed pins with SYNC_IN, SYNC_OUT, and SCI
(2) Multiplexed pins with JTAG

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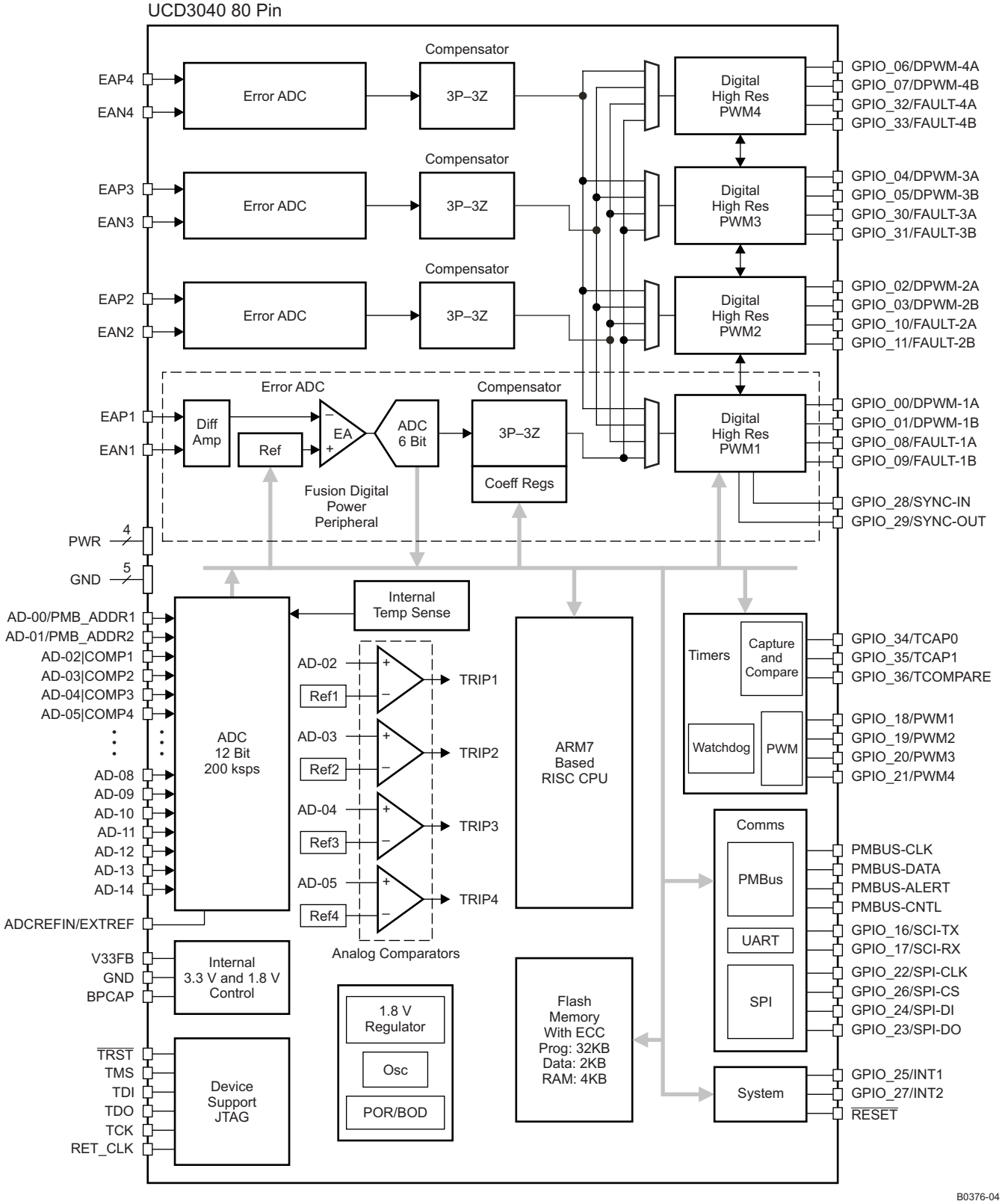
## FUNCTIONAL BLOCK DIAGRAMS





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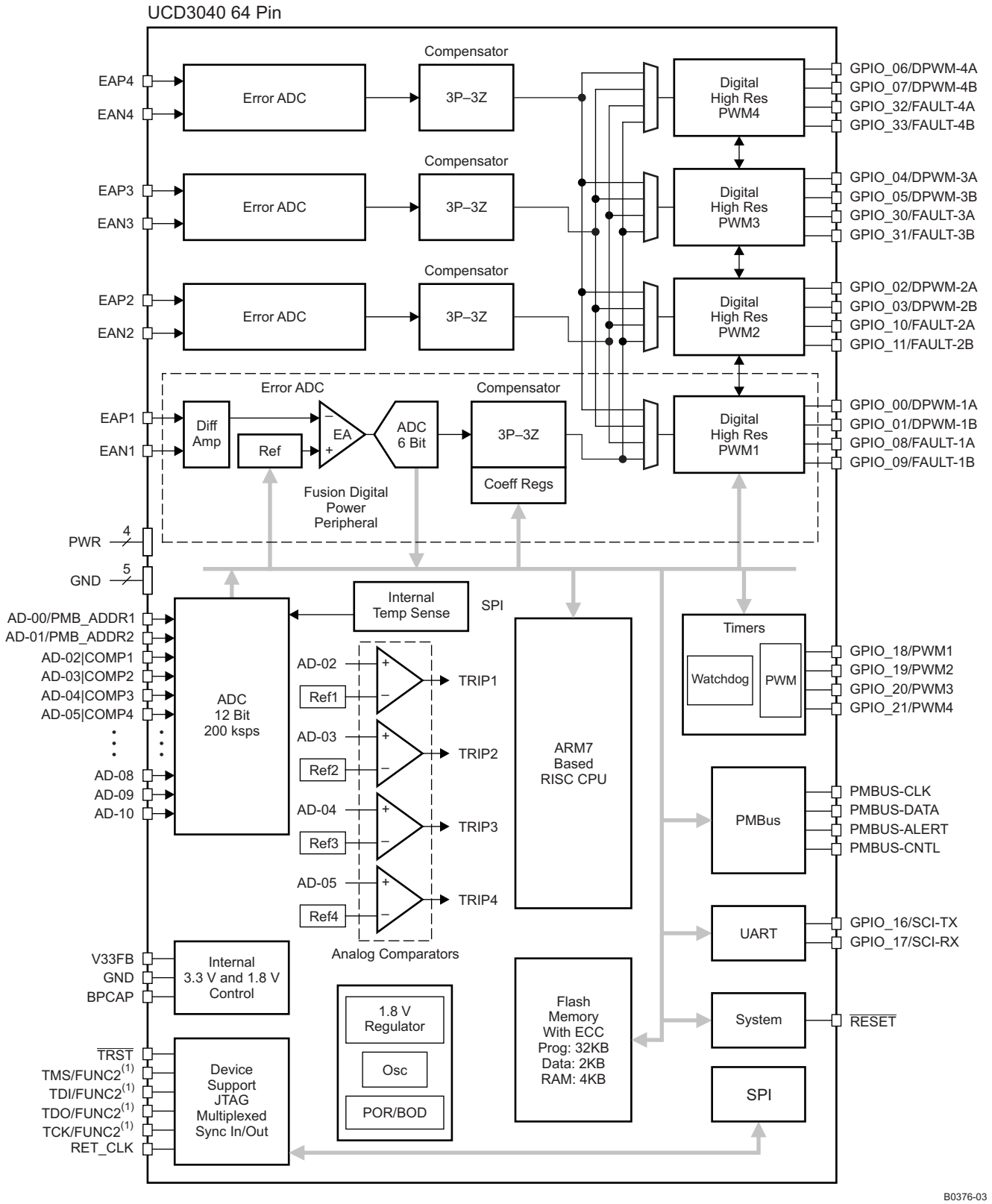
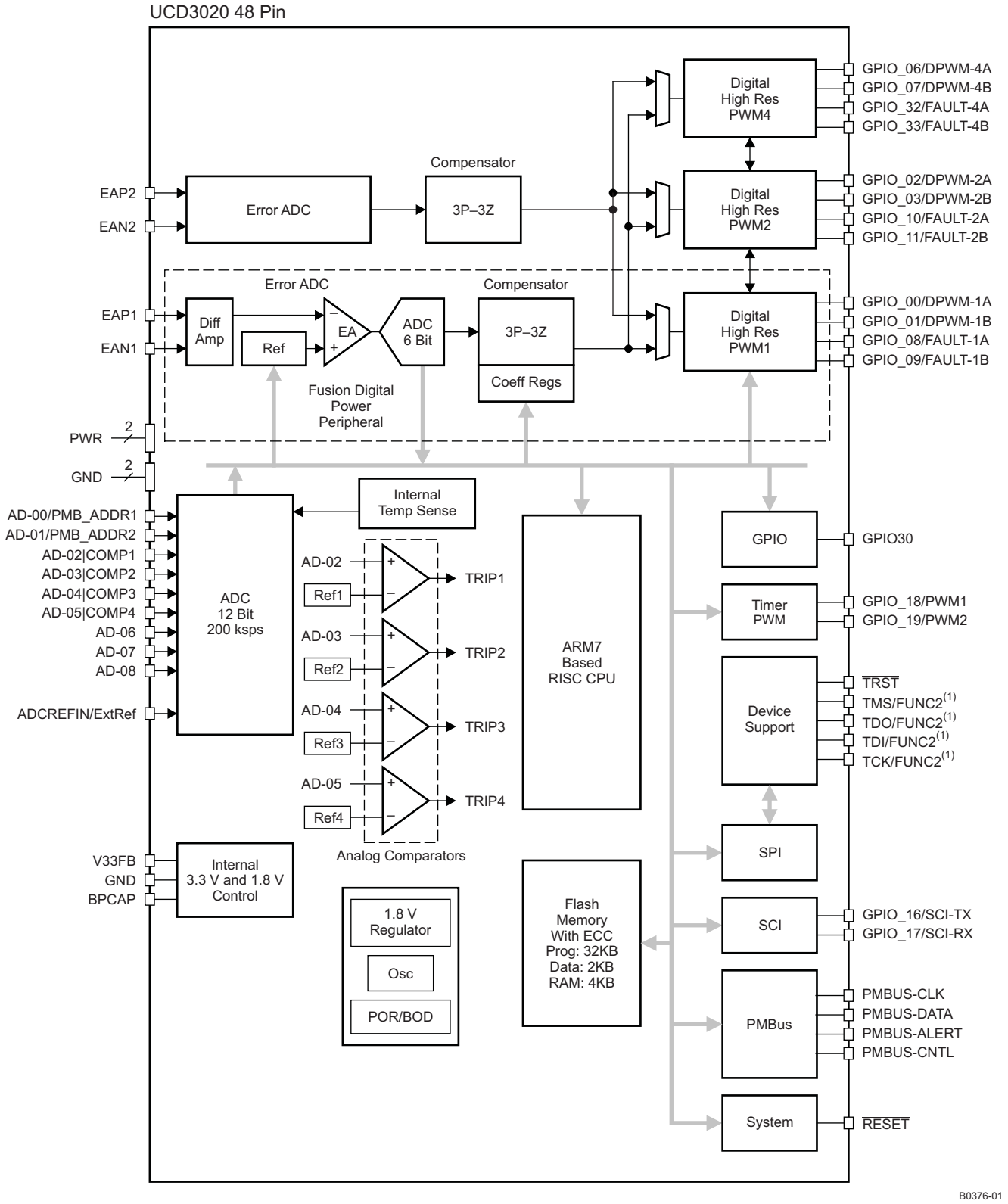



(1) FUNC2 for the four pins TMS, TDI, TDO, and TCK indicates secondary functions available on these pins. These are configurable by the IO_FUNC_MODE bits in the I/O Functional Multiplexer Control register (IOMUXCTRL).




(1) FUNC2 for the four pins TMS, TDI, TDO, and TCK indicates secondary functions available on these pins. These are configurable the by IO_FUNC_MODE bits in the I/O Functional Multiplexer Control register (IOMUXCTRL).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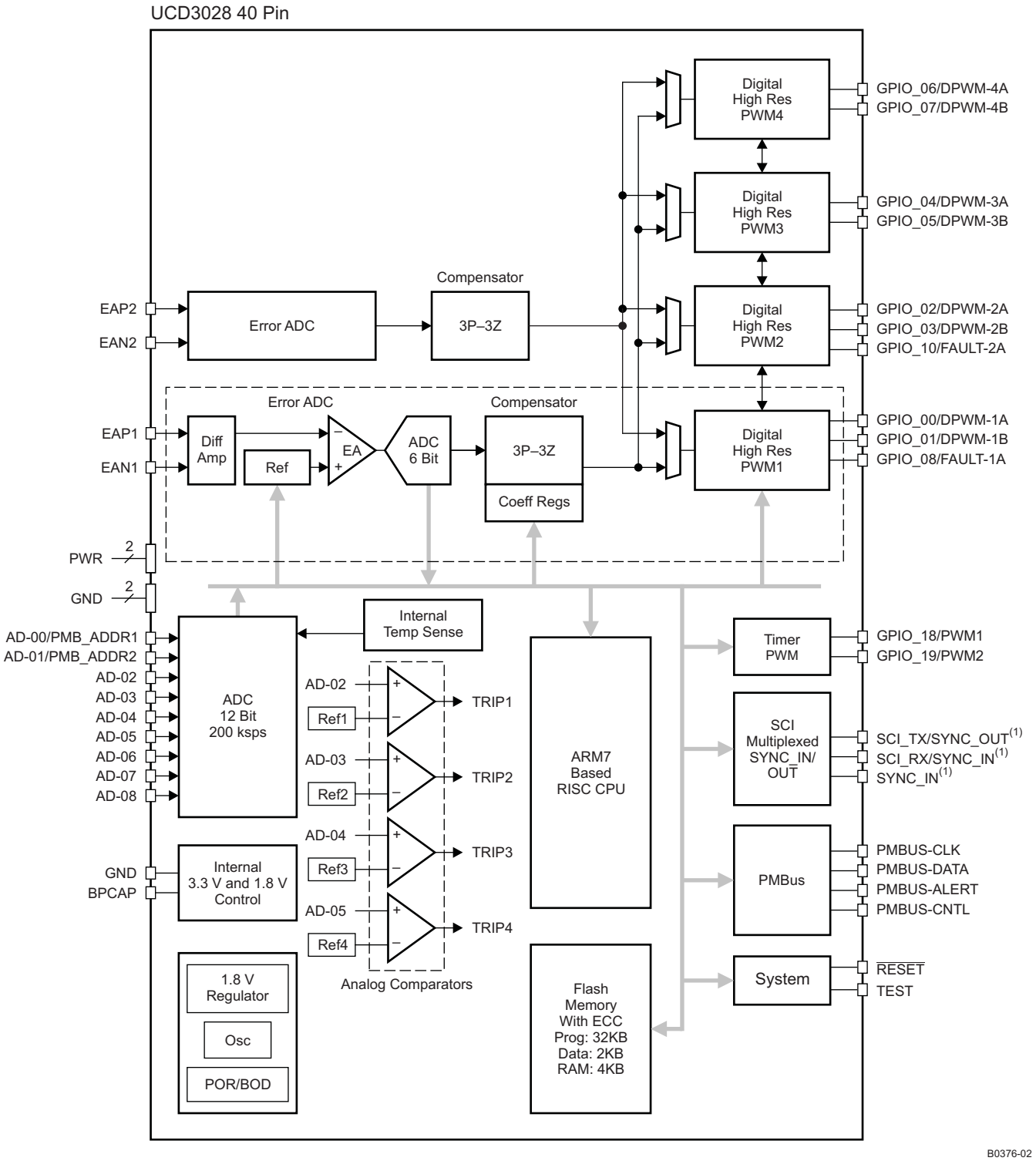
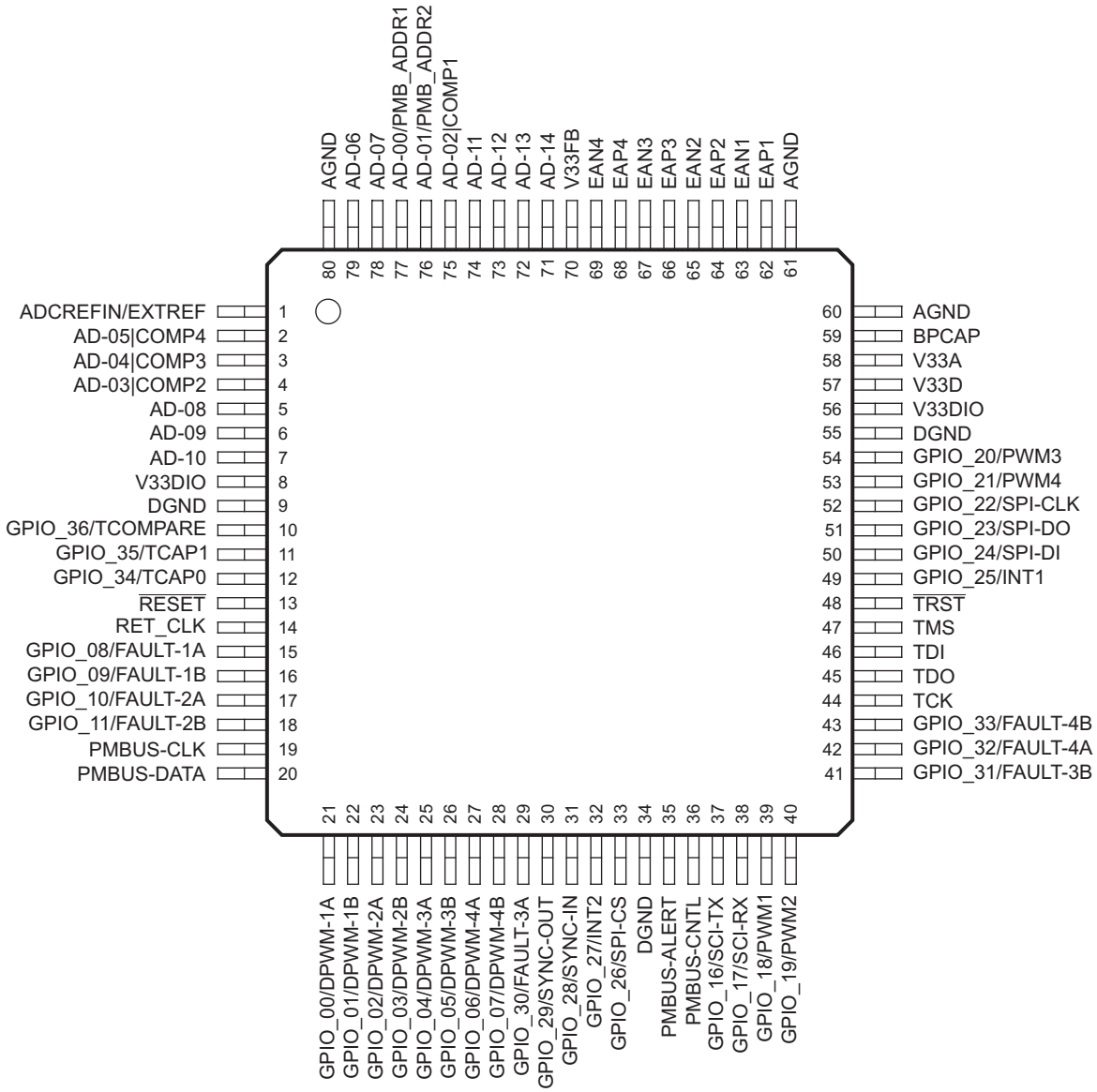



(1) Requires configuration of IO_FUNC_MODE bits in the I/O functional multiplexer control register (IOMUXCTRL)

## UCD3040 Pin Assignments

**PFC Package**
**(Top View)**





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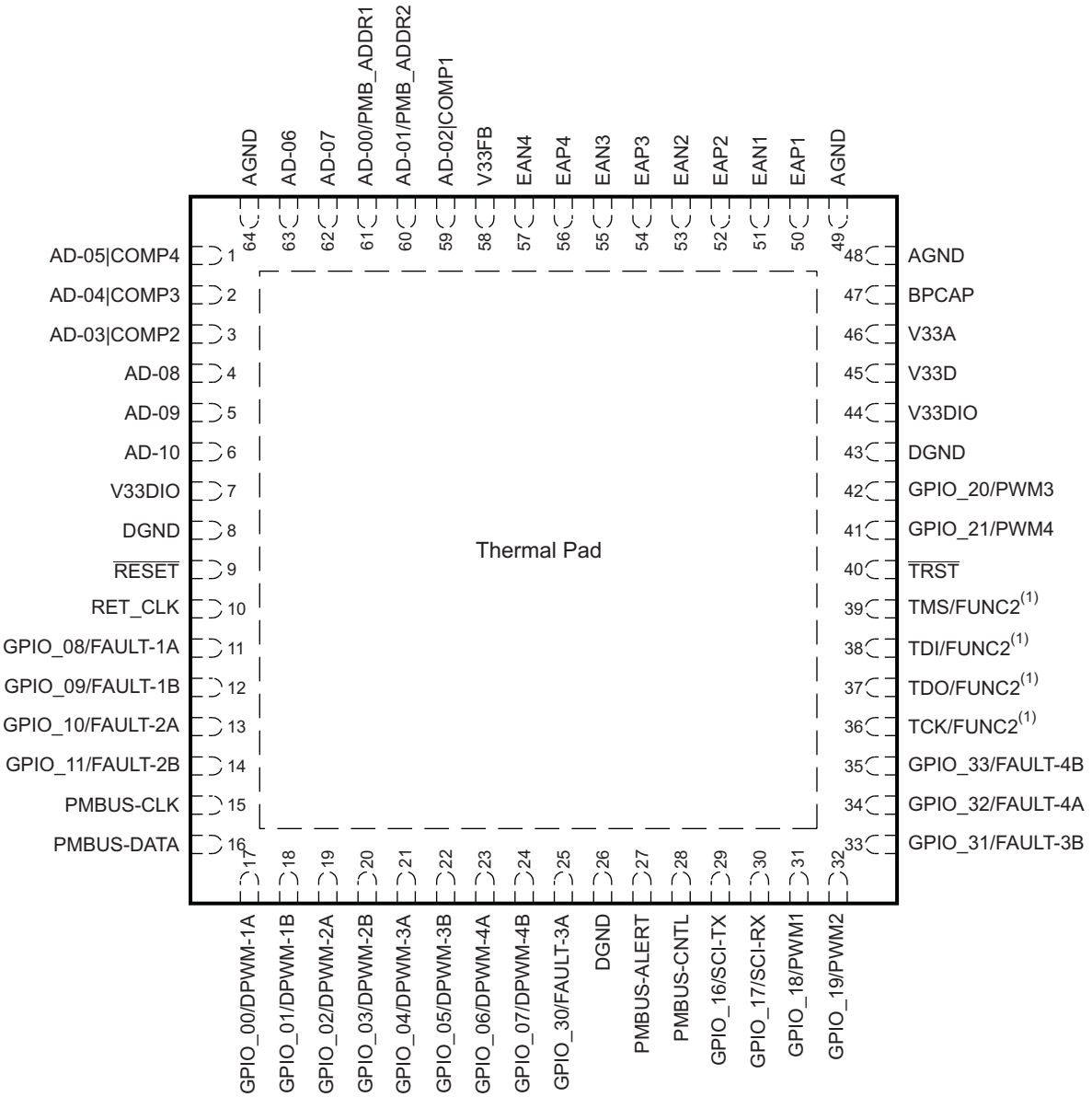
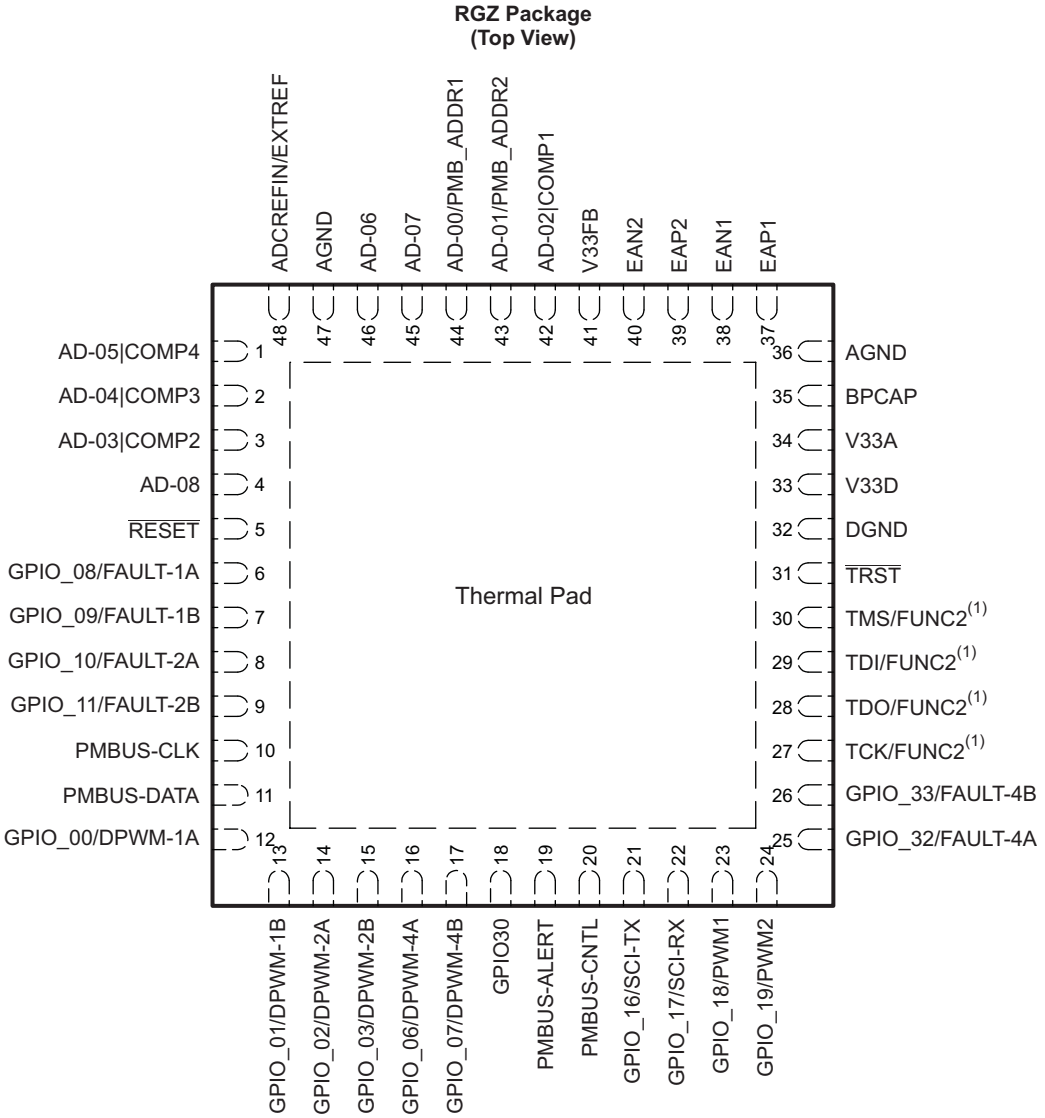
**RGC Package**
**(Top View)**




(1) FUNC2 for the four pins TMS, TDI, TDO, and TCK indicates secondary functions available on these pins. These are configurable by the IO_FUNC_MODE bits in the I/O Functional Multiplexer Control register (IOMUXCTRL).

The UCD3040 is available in a plastic 80-pin ***TQFP*** package and a 64-pin ***QFN*** package.

## UCD3020 Pin Assignments




(1) FUNC2 for the four pins TMS, TDI, TDO, and TCK indicates secondary functions available on these pins. These are configurable by the IO_FUNC_MODE bits in the I/O Functional Multiplexer Control register (IOMUXCTRL).

The UCD3020 is available in a plastic 48-pin *QFN* package.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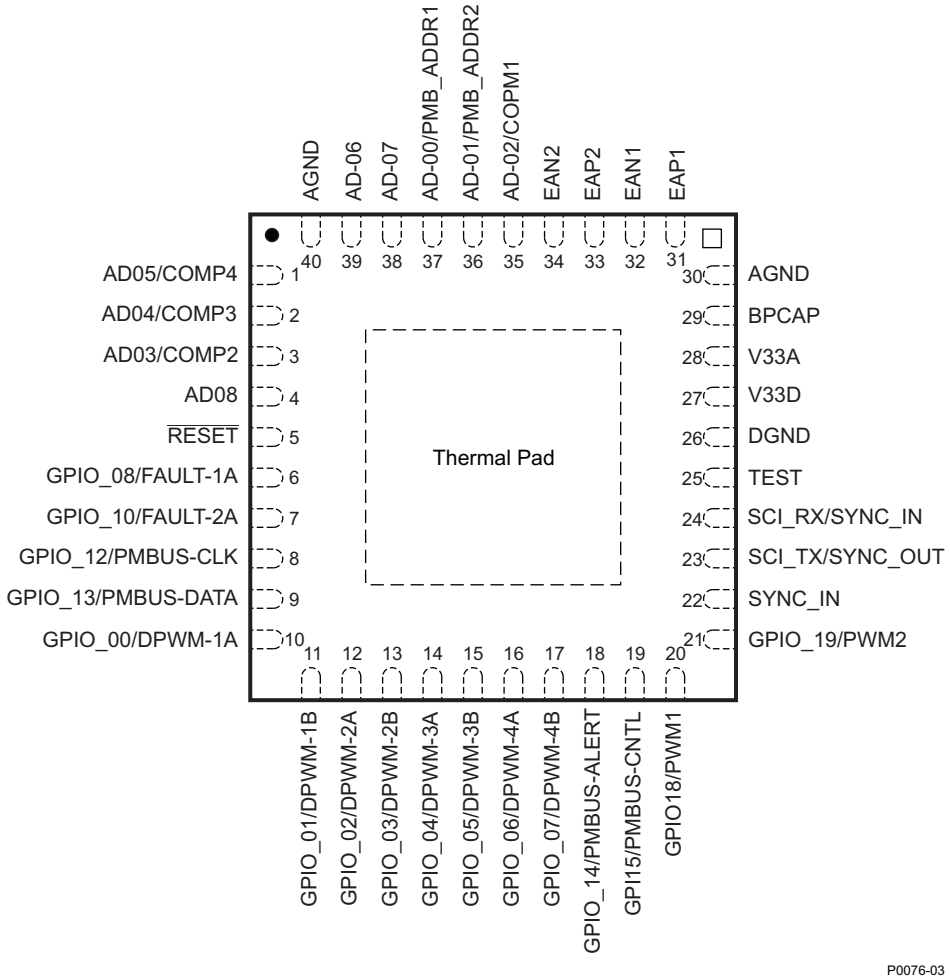
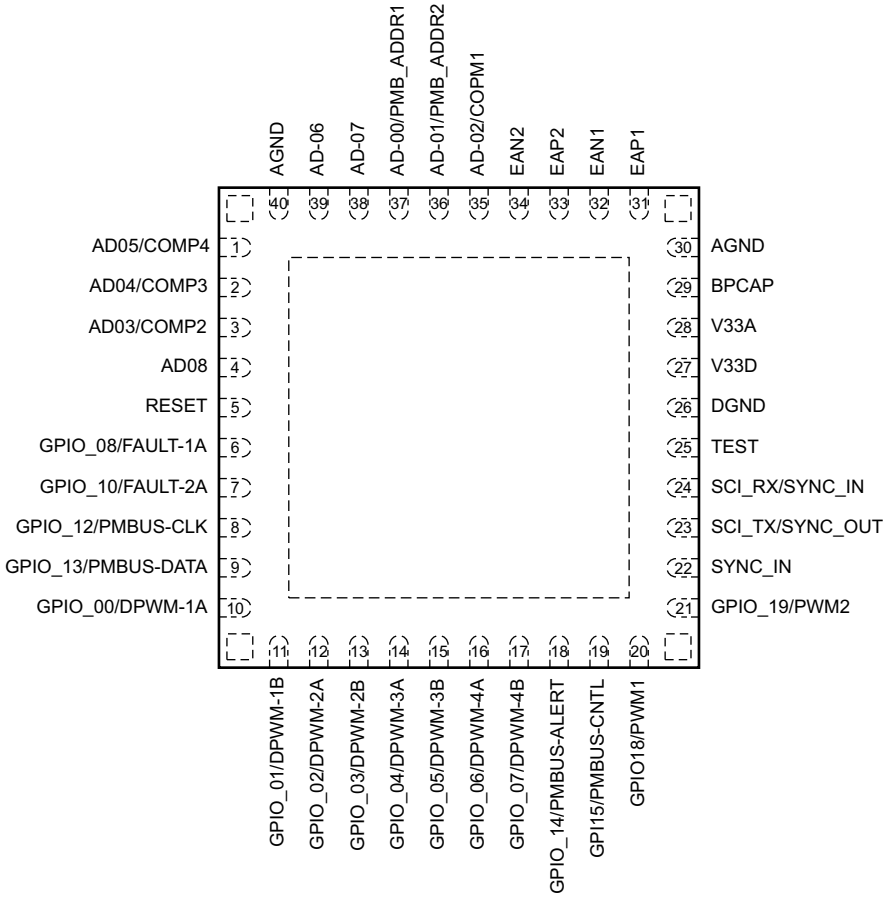
## UDC3028 Pin Assignments

**RHA Package**
**(Top View)**



**RMH Package**
**(Top View)**




**NOTE**

RMH package has thinner package height compared to RHA package.

RMH package also adds four corner pins. These features help to improve solder joint reliability

The corner anchor pins and thermal pad should be soldered for robust mechanical performance and should be tied to the appropriate ground signal.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## PIN DESCRIPTIONS

| UCD3040 PFC PACKAGE | | UCD3040 RGC PACKAGE | | I/O | DESCRIPTION |
|---|---|---|---|---|---|
| Signal | NO. | Signal | NO. | | |
| AD-00/PMB_ADDR1 | 77 | AD-00/PMB_ADDR1 | 61 | I | 12-bit ADC, Ch0/PMBus address sense |
| AD-01/PMB_ADDR2 | 76 | AD-01/PMB_ADDR2 | 60 | I | 12-bit ADC, Ch1/PMBus address sense |
| AD-02\|COMP1 | 75 | AD-02\|COMP1 | 59 | I | 12-bit ADC, Ch2 and analog comparator #1 |
| AD-03\|COMP2 | 4 | AD-03\|COMP2 | 3 | I | 12-bit ADC, Ch3 and analog comparator #2 |
| AD-04\|COMP3 | 3 | AD-04\|COMP3 | 2 | I | 12-bit ADC, Ch4 and analog comparator #3 |
| AD-05\|COMP4 | 2 | AD-05\|COMP4 | 1 | I | 12-bit ADC, Ch5 and analog comparator #4 |
| AD-06 | 79 | AD-06 | 63 | I | 12-bit ADC, Ch6 |
| AD-07 | 78 | AD-07 | 62 | I | 12-bit ADC, Ch7 |
| AD-08 | 5 | AD-08 | 4 | I | 12-bit ADC, Ch8 |
| AD-09 | 6 | AD-09 | 5 | I | 12-bit ADC, Ch9 |
| AD-10 | 7 | AD-10 | 6 | I | 12-bit ADC, Ch10 |
| AD-11 | 74 | — | — | I | 12-bit ADC, Ch11 |
| AD-12 | 73 | — | — | I | 12-bit ADC, Ch12 |
| AD-13 | 72 | — | — | I | 12-bit ADC, Ch13 |
| AD-14 | 71 | — | — | I | 12-bit ADC, Ch14 |
| ADCREFIN/EXTREF | 1 | — | — | I | 12-bit ADC, external reference |
| AGND | 60 | AGND | 48 | — | Analog ground |
| AGND | 61 | AGND | 49 | — | Analog ground |
| AGND | 80 | AGND | 64 | — | Analog ground |
| BPCAP | 59 | BPCAP | 47 | O | 1.8-V bypass capacitor connect pin |
| DGND | 9 | DGND | 8 | — | Digital ground |
| DGND | 34 | DGND | 26 | — | Digital ground |
| DGND | 55 | DGND | 43 | — | Digital ground |
| EAN1 | 63 | EAN1 | 51 | I | Channel #1, differential analog voltage, negative input |
| EAN2 | 65 | EAN2 | 53 | I | Channel #2, differential analog voltage, negative input |
| EAN3 | 67 | EAN3 | 55 | I | Channel #3, differential analog voltage, negative input |
| EAN4 | 69 | EAN4 | 57 | I | Channel #4, differential analog voltage, negative input |
| EAP1 | 62 | EAP1 | 50 | I | Channel #1, differential analog voltage, positive input |
| EAP2 | 64 | EAP2 | 52 | I | Channel #2, differential analog voltage, positive input |
| EAP3 | 66 | EAP3 | 54 | I | Channel #3, differential analog voltage, positive input |
| EAP4 | 68 | EAP4 | 56 | I | Channel #4, differential analog voltage, positive input |
| GPIO_00/DPWM-1A | 21 | GPIO_00/DPWM-1A | 17 | I/O | GPIO port 0/DPWM 1A output |
| GPIO_01/DPWM-1B | 22 | GPIO_01/DPWM-1B | 18 | I/O | GPIO port 1/DPWM 1B output |
| GPIO_02/DPWM-2A | 23 | GPIO_02/DPWM-2A | 19 | I/O | GPIO port 2/DPWM 2A output |
| GPIO_03/DPWM-2B | 24 | GPIO_03/DPWM-2B | 20 | I/O | GPIO port 3/DPWM 2B output |
| GPIO_04/DPWM-3A | 25 | GPIO_04/DPWM-3A | 21 | I/O | GPIO port 4/DPWM 3A output |
| GPIO_05/DPWM-3B | 26 | GPIO_05/DPWM-3B | 22 | I/O | GPIO port 5/DPWM 3B output |
| GPIO_06/DPWM-4A | 27 | GPIO_06/DPWM-4A | 23 | I/O | GPIO port 6/DPWM 4A output |
| GPIO_07/DPWM-4B | 28 | GPIO_07/DPWM-4B | 24 | I/O | GPIO port 7/DPWM 4B output |
| GPIO_08/FAULT-1A | 15 | GPIO_08/FAULT-1A | 11 | I/O | GPIO port 8/external fault input 1A |
| GPIO_09/FAULT-1B | 16 | GPIO_09/FAULT-1B | 12 | I/O | GPIO port 9/external fault input 1B |
| GPIO_10/FAULT-2A | 17 | GPIO_10/FAULT-2A | 13 | I/O | GPIO port 10/external fault input 2A |
| GPIO_11/FAULT-2B | 18 | GPIO_11/FAULT-2B | 14 | I/O | GPIO port 11/external fault input 2B |
| GPIO_16/SCI-TX | 37 | GPIO_16/SCI-TX | 29 | I/O | GPIO port 16/SCI transmit |
| GPIO_17/SCI-RX | 38 | GPIO_17/SCI-RX | 30 | I/O | GPIO port 17/SCI receive |

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| UCD3040 PFC PACKAGE | | UCD3040 RGC PACKAGE | | I/O | DESCRIPTION |
|---|---|---|---|---|---|
| Signal | NO. | Signal | NO. | | |
| GPIO_19/PWM2 | 40 | GPIO_19/PWM2 | 32 | I/O | GPIO port 19/PWM output 2 (16-bit timer) |
| GPIO_18/PWM1 | 39 | GPIO_18/PWM1 | 31 | I/O | GPIO port 18/PWM output 1 (16-bit timer) |
| GPIO_20/PWM3 | 54 | GPIO_20/PWM3 | 42 | I/O | GPIO port 20/PWM output 3 (16-bit timer) |
| GPIO_21/PWM4 | 53 | GPIO_21/PWM4 | 41 | I/O | GPIO port 21/PWM output 4 (16-bit timer) |
| GPIO_22/SPI-CLK | 52 | — | — | I/O | GPIO port 22/SPI clock |
| GPIO_23/SPI-DO | 51 | — | — | I/O | GPIO port 23/SPI data out |
| GPIO_24/SPI-DI | 50 | — | — | I/O | GPIO port 24/SPI data in |
| GPIO_25/INT1 | 49 | — | — | I/O | GPIO port 25/interrupt 1 |
| GPIO_26/SPI-CS | 33 | — | — | I/O | GPIO port 26/SPI chip select |
| GPIO_27/INT2 | 32 | — | — | I/O | GPIO port 27/interrupt 2 |
| GPIO-28/SYNC-IN | 31 | — | — | I/O | GPIO port 28/sync input to DPWM |
| GPIO-29/SYNC-OUT | 30 | — | — | I/O | GPIO port 29/sync output from DPWM |
| GPIO_30/FAULT-3A | 29 | GPIO_30/FAULT-3A | 25 | I/O | GPIO port 30/external fault input 3A |
| GPIO_31/FAULT-3B | 41 | GPIO_31/FAULT-3B | 33 | I/O | GPIO port 31/external fault input 3B |
| GPIO_32FAULT-4A | 42 | GPIO_32FAULT-4A | 34 | I/O | GPIO port 32/external fault input 4A |
| GPIO_33/FAULT-4B | 43 | GPIO_33/FAULT-4B | 35 | I/O | GPIO port 33/external fault input 4B |
| GPIO_34/TCAP0 | 12 | — | — | I/O | GPIO port 34/timer capture input 0 |
| GPIO_35/TCAP1 | 11 | — | — | I/O | GPIO port 35/timer capture input 1 |
| GPIO_36/TCOMPARE | 10 | — | — | I/O | GPIO port 36/timer compare output |
| PMBUS-ALERT | 35 | PMBUS-ALERT | 27 | O | PMBus alert (must have pullup to 3.3 V), general-purpose output, open-drain |
| PMBUS-CLK | 19 | PMBUS-CLK | 15 | I/O | PMBus clock (must have pullup to 3.3 V) |
| PMBUS-CNTL | 36 | PMBUS-CNTL | 28 | I | PMBus control, general-purpose input |
| PMBUS-DATA | 20 | PMBUS-DATA | 16 | I/O | PMBus data (must have pullup to 3.3 V) |
| $\overline{\text{RESET}}$ | 13 | $\overline{\text{RESET}}$ | 9 | I | Active-low device-reset input |
| RET_CLK | 14 | RET_CLK | 10 | O | Return clock |
| TCK | 44 | TCK/FUNC2 | 36 | I/O | For 64-pin JTAG TCK or other secondary functions selectable by IO_FUNC_MODE bits in I/O functional multiplexer control register. For 80-pin JTAG TCK |
| TDI | 46 | TDI/FUNC2 | 38 | I/O | For 64-pin JTAG TDI or other secondary functions selectable by IO_FUNC_MODE bits in I/O functional multiplexer control register. For 80-pin JTAG TDI |
| TDO | 45 | TDO/FUNC2 | 37 | I/O | For 64-pin JTAG TDO or other secondary functions selectable by IO_FUNC_MODE bits in I/O functional multiplexer control register. For 80-pin JTAG TDO |
| TMS | 47 | TMS/FUNC2 | 39 | I/O | For 64-pin JTAG TMS or other secondary functions selectable by IO_FUNC_MODE bits in I/O functional multiplexer control register. For 80-pin JTAG TMS |
| $\overline{\text{TRST}}$ | 48 | $\overline{\text{TRST}}$ | 40 | I/O | JTAG $\overline{\text{TRST}}$ for both 80-pin and 64-pin devices |
| V33A | 58 | V33A | 46 | — | Analog 3.3-V supply |
| V33D | 57 | V33D | 45 | — | Digital core 3.3-V supply |
| V33DIO | 8 | V33DIO | 7 | — | Digital I/O 3.3-V supply |
| V33DIO | 56 | V33DIO | 44 | — | Digital I/O 3.3-V supply |
| V33FB | 70 | V33FB | 58 | — | 3.3-V linear-regulator feedback input |


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| UCD3020 RGZ PACKAGE | | I/O | DESCRIPTION |
|---|---|---|---|
| Signal | NO. | | |
| AD-00/PMB_ADDR1 | 44 | I | 12-bit ADC, Ch0/PMBus address sense, least-significant address bits |
| AD-01/PMB_ADDR2 | 43 | I | 12-bit ADC, Ch1/PMBus address sense, most-significant address bits |
| AD-02\|COMP1 | 42 | I | 12-bit ADC, Ch2 and analog comparator #1 |
| AD-03\|COMP2 | 3 | I | 12-bit ADC, Ch3 and analog comparator #2 |
| AD-04\|COMP3 | 2 | I | 12-bit ADC, Ch4 and analog comparator #3 |
| AD-05\|COMP4 | 1 | I | 12-bit ADC, Ch5 and analog comparator #4 |
| AD-06 | 46 | I | 12-bit ADC, Ch6 |
| AD-07 | 45 | I | 12-bit ADC, Ch7 |
| AD-08 | 4 | I | 12-bit ADC, Ch8 |
| ADCREFIN/EXTREF | 48 | I | 12-bit ADC, external reference |
| AGND | 36 | — | Analog ground |
| AGND | 47 | — | Analog ground |
| BPCAP | 35 | O | 1.8-V bypass-capacitor connect pin |
| DGND | 32 | — | Digital ground |
| EAN1 | 38 | I | Channel #1, differential analog voltage, negative input |
| EAN2 | 40 | I | Channel #2, differential analog voltage, negative input |
| EAP1 | 37 | I | Channel #1, differential analog voltage, positive input |
| EAP2 | 39 | I | Channel #2, differential analog voltage, positive input |
| GPIO_00/DPWM-1A | 12 | I/O | GPIO port 0/DPWM 1A output |
| GPIO_01/DPWM-1B | 13 | I/O | GPIO port 1/DPWM 1B output |
| GPIO_02/DPWM-2A | 14 | I/O | GPIO port 2/DPWM 2A output |
| GPIO_03/DPWM-2B | 15 | I/O | GPIO port 3/DPWM 2B output |
| GPIO_06/DPWM-4A | 16 | I/O | GPIO port 6/DPWM 4A output |
| GPIO_07/DPWM-4B | 17 | I/O | GPIO port 7/DPWM 4B output |
| GPIO_08/FAULT-1A | 6 | I/O | GPIO port 8/external fault input 1A |
| GPIO_09/FAULT-1B | 7 | I/O | GPIO port 9/external fault input 1B |
| GPIO_10/FAULT-2A | 8 | I/O | GPIO port 10/external fault input 2A |
| GPIO_11/FAULT-2B | 9 | I/O | GPIO port 11/external fault input 2B |
| GPIO_16/SCI-TX | 21 | I/O | GPIO port 16/SCI transmit |
| GPIO_17/SCI-RX | 22 | I/O | GPIO port 17/SCI receive |
| GPIO_18/PWM1 | 23 | I/O | GPIO port 18/PWM output 1 (16-bit timer) |
| GPIO_19/PWM2 | 24 | I/O | GPIO port 19/PWM output 2 (16-bit timer) |
| GPIO_30 | 18 | I/O | GPIO port 30 |
| GPIO_32/FAULT-4A | 25 | I/O | GPIO port 32/external fault input 4A |
| GPIO_33/FAULT-4B | 26 | I/O | GPIO port 33/external fault input 4B |
| PMBUS-ALERT | 19 | O | PMBUS alert (must have pullup to 3.3 V), general-purpose output, open-drain |
| PMBUS-CLK | 10 | I/O | PMBus clock (must have pullup to 3.3 V) |
| PMBUS-CNTL | 20 | I | PMBUS control, general-purpose input |
| PMBUS-DATA | 11 | I/O | PMBus data (must have pullup to 3.3 V) |
| $\overline{\text{RESET}}$ | 5 | I | Active-low device-reset input |

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| UCD3020 RGZ PACKAGE | | I/O | DESCRIPTION |
|---|---|---|---|
| Signal | NO. | | |
| TCK/FUNC2 | 27 | I/O | JTAG TCK or secondary functions selectable by IO_FUNC_MODE bits in I/O functional multiplexer control register |
| TDI/FUNC2 | 29 | I/O | JTAG TDI or secondary functions selectable by IO_FUNC_MODE bits in I/O functional multiplexer control register |
| TDO/FUNC2 | 28 | I/O | JTAG TDO or secondary functions selectable by IO_FUNC_MODE bits in I/O functional multiplexer control register |
| TMS/FUNC2 | 30 | I/O | JTAG TMS or secondary functions selectable by IO_FUNC_MODE bits in I/O functional multiplexer control register |
| $\overline{\text{TRST}}$ | 31 | I | JTAG reset |
| V33A | 34 | — | Analog 3.3-V supply |
| V33D | 33 | — | Digital core 3.3-V supply |
| V33FB | 41 | — | 3.3-V linear-regulator feedback input |


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| UCD3028 RHA and RMH Package | | I/O | DESCRIPTION |
|---|---|---|---|
| Signal | NO. | | |
| AD-00/PMB_ADDR1 | 37 | I | ADC12, Ch0/PMBus address sense, most-significant address bits |
| AD-01/PMB_ADDR2 | 36 | I | ADC12, Ch1/PMBus address sense, least-significant address bits |
| AD-02/COMP1 | 35 | I | ADC12, Ch2/analog comparator #1 |
| AD-03/COMP2 | 3 | I | ADC12, Ch3/analog comparator #2 |
| AD-04/COMP3 | 2 | I | ADC12, Ch4/analog comparator #3 |
| AD-05/COMP4 | 1 | I | ADC12, Ch5/analog comparator #4 |
| AD-06 | 39 | I | ADC12, Ch6 |
| AD-07 | 38 | I | ADC12, Ch7 |
| AD-08 | 4 | I | ADC12, Ch8 |
| AGND | 30 | – | Analog ground |
| AGND | 40 | – | Analog ground |
| BPCAP | 29 | O | 1.8-V bypass capacitor connect pin |
| DGND | 26 | – | Digital ground |
| EAN1 | 32 | I | Channel #1, differential analog error voltage, negative input |
| EAN2 | 34 | I | Channel #2, differential analog error voltage, negative input |
| EAP1 | 31 | I | Channel #1, differential analog error voltage, positive input |
| EAP2 | 33 | I | Channel #2, differential analog error voltage, positive input |
| GPIO_00/DPWM-1A | 10 | I/O | GPIO port 0/DPWM 1A output |
| GPIO_01/DPWM-1B | 11 | I/O | GPIO port 1/DPWM 1B output |
| GPIO_02/DPWM-2A | 12 | I/O | GPIO port 2/DPWM 2A output |
| GPIO_03/DPWM-2B | 13 | I/O | GPIO port 3/DPWM 2B output |
| GPIO_04/DPWM-3A | 14 | I/O | GPIO port 4/DPWM 3A output |
| GPIO_05/DPWM-3B | 15 | I/O | GPIO port 5/DPWM 3B output |
| GPIO_06/DPWM-4A | 16 | I/O | GPIO port 6/DPWM 4A output |
| GPIO_07/DPWM-4B | 17 | I/O | GPIO port 7/DPWM 4B output |
| GPIO_08/FAULT-1A | 6 | I/O | GPIO port 8/external fault input 1A |
| GPIO_10/FAULT-2A | 7 | I | GPIO port 10/external fault input 2A |
| GPIO_12/PMBUS-CLK | 8 | I/O | GPIO port 12/PMBus clock (must have pullup to 3.3 V) |
| GPIO_13/PMBUS-DATA | 9 | I/O | GPIO port 13/PMBus data (Must have pullup to 3.3 V) |

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| UCD3028 RHA and RMH Package | | I/O | DESCRIPTION |
|---|---|---|---|
| Signal | NO. | | |
| GPIO_14/PMBUS-ALERT | 18 | O | GPO port 14/PMBUS alert |
| GPIO_15/PMBUS-CNTL | 19 | I | GPI port 15/PMBUS control |
| GPIO_18/PWM1 | 20 | I/O | GPIO port 18/ PWM output 1 (16-bit timer) |
| GPIO_19/PWM2 | 21 | I/O | GPIO port 19/ PWM output 2 (16-bit timer) |
| TEST | 25 | I | Manufacturer Test Pin - This pin must be tied to ground. Unexpected behavior will result if not grounded. |
| SCI_RX/SYNC_IN | 24 | I/O | GPIO port 39/SCI receive/sync input to DPWM |
| SCI_TX/SYNC_OUT | 23 | I/O | GPIO port 40/SCI transmit/sync output from DPWM |
| SYNC_IN | 22 | I/O | GPIO port 41/sync input to DPWM |
| $\overline{\text{RESET}}$ | 5 | I | Active-low device-reset input |
| V33A | 28 | I | Analog 3.3-V supply |
| V33D | 27 | I | Digital core 3.3-V supply |
| Thermal pad | – | – | It is recommended that this pad be connected to analog ground. |
| Corner anchor pins (RMH only) | Corner (n/a) | – | All four corner anchors should be spoldered and tied to GND. |


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## PIN MULTIPLEXING

The 64/48 pin devices incorporate an alternate function multiplexer that allows for all of the pins associated with the JTAG port to be used as an SPI port, UART port, or sync/IO port. Therefore, some of the function pins are lost when packaging the lower-pin-count devices. At power up, the default pins are set for JTAG TMS, TDI, TDO, and TCK functions. To switch to the alternate functions requires writing to the IO_FUNC_MODE bits in the *I/O Functional Multiplexer Control Register* (IOMUXCTRL). The following table lists six alternative functions for the JTAG pins, selectable by setting the IO_FUNC_MODE bits.

| PIN NAME | PIN # (64/48) | Alt. Func1 | Alt. Func2 | Alt. Func3 | Alt. Func4 | Alt. Func5 | Alt. Func6 |
|---|---|---|---|---|---|---|---|
| TMS | 39/30 | SPI-CS/GPIO-38 | SYNC-OUT | FAULT-2B | INT1 | INT1 | INT1 |
| TDI | 38/29 | SPI-DI/GPIO-39 | SCI-RX | FAULT-1B | SCI-RX | SYNC-IN | TCAP0 |
| TDO | 37/28 | SPI-DO/GPIO-40 | SCI-TX | SYNC-OUT | SCI-TX | SYNC-OUT | TCOMPARE |
| TCK | 36/27 | SPI-CLK/GPIO-41 | SYNC-IN | SYNC-IN | INT2 | INT2 | TCAP1 |

For the 40-pin device, the following table shows six alternative functions selectable by setting the IO_FUNC_MODE bits.

| PIN # (40) | Alt. Func1 | Alt. Func2 | Alt. Func3 | Alt. Func4 | Alt. Func5 | Alt. Func6 |
|---|---|---|---|---|---|---|
| 24 | SPI-DI/GPIO-39 | SCI-RX | FAULT-1B | SCI-RX | SYNC-IN | TCAP0 |
| 23 | SPI-DO/GPIO-40 | SCI-TX | SYNC-OUT | SCI-TX | SYNC-OUT | TCOMPARE |
| 22 | SPI-CLK/GPIO-41 | SYNC-IN | SYNC-IN | INT2 | INT2 | TCAP1 |

## ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

| | | VALUE | UNIT |
|---|---|---|---|
| | Voltage applied at V33D to DVss | –0.3 to 3.8 | V |
| | Voltage applied at V33A to AVss | –0.3 to 3.8 | V |
| | Voltage applied to any pin (except BPCAP)(2) | –0.3 to 3.8 | V |
| | Voltage applied to BPCAP | –0.3 to 2.5 | V |
| $T_{stg}$ | Storage temperature | –55 to 150 | °C |

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages referenced to VSS.

## RECOMMENDED OPERATING CONDITIONS

| | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| V33D, V33DIO, V33A | Supply voltage during operation | 3 | 3.3 | 3.6 | V |
| $V_{BPCAP}$ | Voltage applied at BPCAP | | 1.8 | 1.95 | V |
| $T_A$ | Operating free-air temperature range | –40 | | 125 | °C |

## THERMAL INFORMATION

| THERMAL METRIC[1] | | UCD3020 RGZ 48 PINS | UCD3028 RHA 40 PINS | UCD3028 RMH 40 PINS | UNITS |
|---|---|---|---|---|---|
| $\theta_{JA}$ | Junction-to-ambient thermal resistance[2] | 26.9 | 29.4 | 31.1 | °C/W |
| $\theta_{JCtop}$ | Junction-to-case (top) thermal resistance[3] | 14.0 | 16.9 | 16.9 | |
| $\theta_{JB}$ | Junction-to-board thermal resistance[4] | 4.5 | 5.2 | 6.4 | |
| $\psi_{JT}$ | Junction-to-top characterization parameter[5] | 0.2 | 0.2 | 0.2 | |
| $\psi_{JB}$ | Junction-to-board characterization parameter[6] | 4.5 | 5.2 | 6.3 | |
| $\theta_{JCbot}$ | Junction-to-case (bottom) thermal resistance[7] | 1.0 | 1.5 | 1.1 | |

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.
(2) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
(3) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
(4) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
(5) The junction-to-top characterization parameter, $\psi_{JT}$, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining $\theta_{JA}$, using a procedure described in JESD51-2a (sections 6 and 7).
(6) The junction-to-board characterization parameter, $\psi_{JB}$, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining $\theta_{JA}$ , using a procedure described in JESD51-2a (sections 6 and 7).
(7) The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

## THERMAL INFORMATION

| THERMAL METRIC[1] | | UCD3040 RGC 64 PINS | UCD3040 PFC 80 PINS | UNITS |
|---|---|---|---|---|
| $\theta_{JA}$ | Junction-to-ambient thermal resistance[2] | 29.9 | 32.2 | °C/W |
| $\theta_{JCtop}$ | Junction-to-case (top) thermal resistance[3] | 15.4 | 8.7 | |
| $\theta_{JB}$ | Junction-to-board thermal resistance[4] | 8.8 | 10.4 | |
| $\psi_{JT}$ | Junction-to-top characterization parameter[5] | 0.2 | 0.2 | |
| $\psi_{JB}$ | Junction-to-board characterization parameter[6] | 8.7 | 10.0 | |
| $\theta_{JCbot}$ | Junction-to-case (bottom) thermal resistance[7] | 1.5 | 0.9 | |

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.
(2) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
(3) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
(4) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
(5) The junction-to-top characterization parameter, $\psi_{JT}$, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining $\theta_{JA}$, using a procedure described in JESD51-2a (sections 6 and 7).
(6) The junction-to-board characterization parameter, $\psi_{JB}$, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining $\theta_{JA}$ , using a procedure described in JESD51-2a (sections 6 and 7).
(7) The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.


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## ELECTRICAL CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **SUPPLY CURRENT** | | | | | | |
| I33A[1] | Supply current | V33A = 3.3 V | | 8 | 15 | mA |
| I33DIO[1] | | V33DIO = 3.3 V | | 2 | 10 | |
| I33D[1] | | V33D = 3.3 V | | 40 | 45 | |
| | | V33D = 3.3 V, storing configuration parameters in flash memory | | 50 | 55 | |
| I33 | Total supply current | V33D = 3.3 V, storing configuration parameters in flash memory | | 60 | 80 | mA |
| **INTERNAL REGULATOR CONTROLLER INPUTS/OUTPUTS** | | | | | | |
| V33 | 3.3-V linear regulator | Emitter of NPN transistor | 3.25 | 3.3 | 3.35 | V |
| V33FB | 3.3-V linear regulator feedback | | | 4 | 4.6 | V |
| I33FB | Series-pass base drive | Vin = 12 V | | 10 | | mA |
| Beta | Series-NPN-pass device | | 40 | | | |
| BPCAP | 1.8-V Regulator Output | V33D = 3.3V, TA = 25C | 1.76 | | 1.8 | mA |
| **ERROR ADC INPUTS EAPn, EANn** | | | | | | |
| $V_{CM}$ | Common-mode voltage, each pin | | –0.15 | | 1.6 | V |
| $V_{ERROR}$ | Internal error voltage range | AFE_GAIN field of CLA_GAINS = 0 | –256 | | 256 | mV |
| EAP-EAN | Error voltage digital resolution | AFE_GAIN field of CLA_GAINS = 3 | | 1 | | mV |
| $R_{EA}$ | Input impedance | Ground reference | 0.5 | | | MΩ |
| $I_{OFFSET}$ | Input offset current | 1-kΩ source impedance | –5 | | 5 | µA |
| $V_{Res_DAC}$ | EADC reference DAC resolution | | | 1.56 | | mV |
| | EADC offset | Gain = 1, 8 mV/LSB | | 2 | | LSB |
| | | Gain = 2, 4 mV/LSB | | 2 | | |
| | | Gain = 4, 2 mV/LSB | | 1 | | |
| | | Gain = 8, 1 mV/LSB | | 2 | | |
| **ANALOG INPUTS** | | | | | | |
| $I_{BIAS}$ | Bias current for PMBus addr. pins | | 9 | | 11 | µA |
| $V_{ADC_RANGE}$ | Measurement range for voltage monitoring | | 0 | | 2.5 | V |
| $V_{ADC_REF_INT}$ | Internal ADC reference voltage | –40°C to 125°C | 2.462 | 2.498 | 2.523 | V |
| ΔADC_Ref | Internal ADC reference ΔV to 25°C reference voltage[2] | 25°C to –40°C | | | 5 | mV |
| | | 25°C to 85°C | –10 | | | |
| | | 25°C to 125°C | –20 | | | |
| ΔADC_Ref_CMP | Internal analog comparator reference accuracy | 0°C to 125°C | | 0.6% (± 6 mV) | | |
| | EADC DAC reference voltage accuracy | | | 0.5% (± 4mV) | | |
| $V_{CMP_THRS}$ | Analog comparator threshold voltage range | | 0.032 | | 2 | V |
| $V_{CMP_RES}$ | Analog comparator threshold resolution | | | 31.25 | | mV |
| ADCRef | External reference input[3] | PFC and RGZ package | 1.8 | | V33A | V |
| $Temp_{Internal}$ | Internal temperature-sense accuracy[2] | Over range from –40°C to 125°C | –10[4] | ±5 | 10[4] | °C |
| INL | ADC integral nonlinearity | | –4 | | 4 | LSB |
| DNL | ADC differential nonlinearity | | –2 | | 2 | LSB |
| $I_{Leakage}$ | Input leakage current | 3 V applied to pin | | | 400 | nA |
| $R_{IN}$ | Input impedance | Ground reference | 8 | | | MΩ |
| $C_{IN}$ | Input capacitance | | | | 10 | pF |
| $t_{ADC}$ | ADC single sample time | | | 4.625 | | µs |

(1) Supply pins should be ramped at a 10-V/s or greater rate for proper device startup.
(2) Characterized by design and not production tested. Ambient temperature offset value should be used from the Data Flash information block to meet accuracy.
(3) For the applied external reference input (ADCRef), the actual internal reference voltage (Vref_internal) seen by the 12-bit ADC module should be computed using the equation: ADCRef = Vref_internal × 1.05185
(4) The max/min high/low temperature values are not production tested.

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## ELECTRICAL CHARACTERISTICS (continued)

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **DIGITAL INPUTS/OUTPUTS (5)** | | | | | | |
| $V_{OL}$ | Low-level output voltage | $I_{OH}$ = 6 mA (6), V33DIO = 3 V | | | DGND+0.25 | V |
| $V_{OH}$ | High-level output voltage | $I_{OH}$ = –6 mA (7), V33DIO = 3 V | V33DIO–0.6 | | | V |
| $V_{IH}$ | High-level input voltage | V33DIO = 3 V | 2.1 | | | V |
| $V_{IL}$ | Low-level input voltage | V33DIO = 3.5 V | | | 1.1 | V |
| **FAULT DETECTION LATENCY** | | | | | | |
| $t_{(FAULT)}$ | Time to disable PWM output based on active FAULT pin signal | High level on FAULT pin | | 70 | | ns |
| $t_{(CLF)}$ | Time to disable the DPWM output based on internal analog comparator | Step change in analog comparator input voltage from 0 V to 2 V | 52 | | | ns |
| **SYSTEM PERFORMANCE** | | | | | | |
| $t_{Delay}$ | Digital compensator delay (8) | | 208 | | | ns |
| $V_{RESET_HI}$ | Voltage at $\overline{RESET}$ pin at which device comes out of reset | For device reset | | 1.95 | 2.4 | V |
| $V_{RESET_LO}$ | Voltage at $\overline{RESET}$ pin at which device goes into reset | For device reset | | 1.4 | | V |
| $t_{(reset)}$ | Pulse width needed at reset | | 2 | | | µs |
| $t_{retention}$ | Retention period of flash content (data and program) | $T_J$ = 25°C | 100 | | | years |
| Write_Cycles | Number of nonvolatile erase/write cycles (data flash) | $T_J$ = 25°C | 20 | | | k cycles |
| $f_{(PCLK)}$ | Internal oscillator frequency (9) | $T_A$ = 125°C, $T_A$ = 25°C | | 250 | | MHz |
| | Sync-in/sync-out pulse width | $T_A$ = 25°C | | 16 | | ns |

(5) DPWM outputs are low after reset. Other GPIO pins are configured as inputs after reset.
(6) The maximum total current, $I_{OH}$max and $I_{OL}$max for all outputs combined, should not exceed 12 mA to hold the maximum voltage drop specified. Maximum sink current per pin = –4 mA at $V_{OL}$; maximum source current per pin = 4 mA at $V_{OH}$.
(7) The maximum total current, $I_{OH}$max and $I_{OL}$max for all outputs combined, should not exceed 48 mA to hold the maximum voltage drop specified. Maximum sink current per pin = –4 mA at $V_{OL}$; maximum source current per pin = 4 mA at $V_{OH}$.
(8) Time from close of error ADC sample window to time when digitally calculated control effort (duty cycle) is available. This delay must be accounted for when calculating the system dynamic response.
(9) For improved accuracy on the internal oscillator frequency, Texas Instruments provides application notes with detailed temperature-compensation schemes. Contact TI or your local TI representative.


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## PMBUS TIMING

### PMBus/SMBus/I²C

The timing characteristics and timing diagram for the communications interface that supports I²C, SMBus, and PMBus are shown in Table 1, Figure 1, and Figure 2. The numbers in Table 1 are for 400-kHz operating frequency. However, the device supports all three speeds, standard (100 kHz), fast (400 kHz), and fast mode plus (1 MHz)..

**Table 1. I²C/SMBus/PMBus Timing Characteristics**

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **Typical values at $T_A$ = 25°C and $V_{CC}$ = 3.3 V (unless otherwise noted)** | | | | | | |
| fSMB | SMBus/PMBus operating frequency | Slave mode, SMBC 50% duty cycle | 10 | | 400 | kHz |
| fI2C | I²C operating frequency | Slave mode, SCL 50% duty cycle | 10 | | 400 | kHz |
| $t_{(BUF)}$ | Bus free time between start and stop | | 1.3 | | | µs |
| $t_{(HD:STA)}$ | Hold time after (repeated) start | | 0.6 | | | µs |
| $t_{(SU:STA)}$ | Repeated start setup time | | 0.6 | | | µs |
| $t_{(SU:STO)}$ | Stop setup time | | 0.6 | | | µs |
| $t_{(HD:DAT)}$ | Data hold time | Receive mode | 0 | | | ns |
| $t_{(SU:DAT)}$ | Data setup time | | 100 | | | ns |
| $t_{(TIMEOUT)}$ | Error signal/detect | See (1) | | | 35 | ms |
| $t_{(LOW)}$ | Clock low period | | 1.3 | | | µs |
| $t_{(HIGH)}$ | Clock high period | See (2) | 0.6 | | | µs |
| $t_{(LOW:SEXT)}$ | Cumulative clock low slave extend time | See (3) | | | 25 | ms |
| $t_f$ | Clock/data fall time | Rise time $t_r$ = ($V_{IL}$max – 0.15) to ($V_{IH}$min + 0.15) | 20 + 0.1 Cb(4) | | 300 | ns |
| $t_r$ | Clock/data rise time | Fall time $t_f$ = 0.9 VDD to ($V_{IL}$max – 0.15) | 20 + 0.1 Cb(4) | | 300 | ns |
| Cb | Total capacitance of one bus line | | | | 400 | pF |

(1) The device times out when any clock low exceeds $t_{(TIMEOUT)}$.
(2) $t_{(HIGH)}$, Max, is the minimum bus idle time. SMBC = SMBD = 1 for t > 50 ms causes reset of any transaction that is in progress. This specification is valid when the NC_SMB control bit remains in the default cleared state (CLK[0] = 0).
(3) $t_{(LOW:SEXT)}$ is the cumulative time a slave device is allowed to extend the clock cycles in one message from initial start to the stop.
(4) Cb in picofarads (pF)

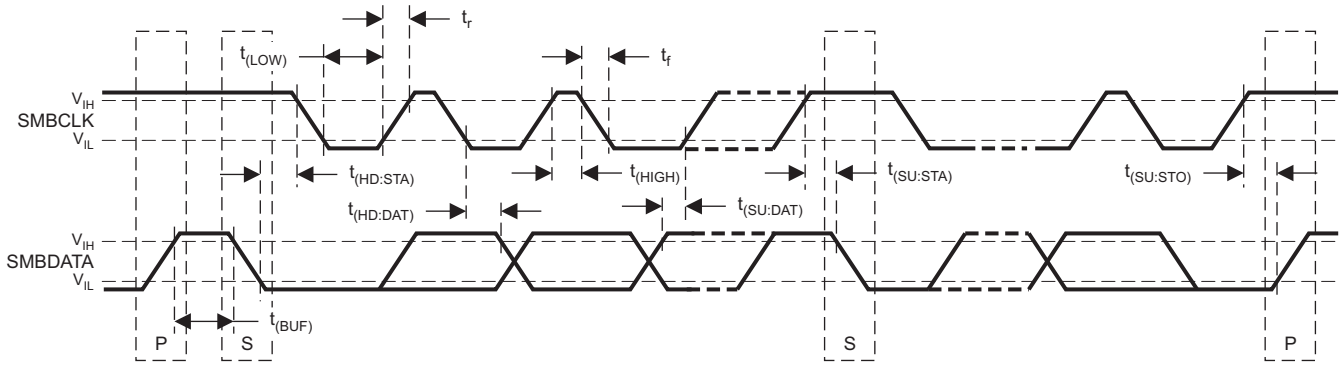


**Figure 1. I²C/SMBus/PMBus Timing Diagram**

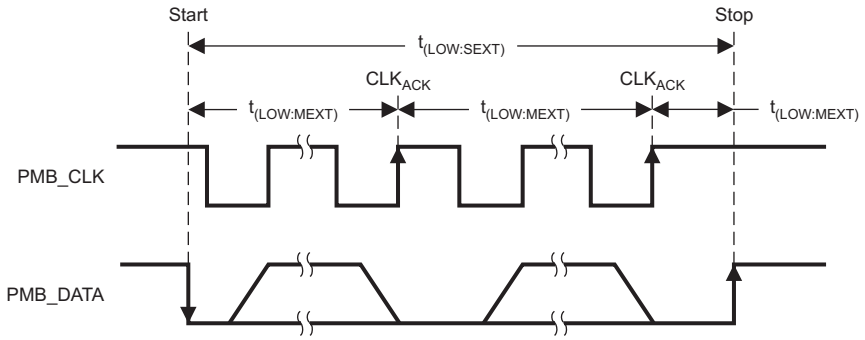


**Figure 2. Bus Timing in Extended Mode**

## FUNCTIONAL OVERVIEW

### ARM PROCESSOR

The ARM7TDMI-S processor is a member of the ARM family of general-purpose 32-bit microprocessors. The ARM architecture is based on reduced instruction set computer (RISC) principles where two instruction sets are available, the 32-bit ARM instruction set and the 16-bit thumb instruction set. The thumb instruction set allows for higher code density, equivalent to a 16-bit microprocessor, with the performance of the 32-bit microprocessor.

The three-stage pipelined ARM processor architectecture includes fetch, decode, and execute stages. Major blocks in the ARM processor include a 32-bit ALU, 32 × 8 multiplier, and barrel shifter. A JTAG port is also available for firmware debugging.

#### Memory

Within the UCD30xx architecture, there is a 1024 × 32-bit boot ROM that contains the initial firmware startup routines for PMBUS communication and nonvolatile (flash) memory download. This boot ROM is executed after power-up reset, and the code can determine if there is a valid flash program written. If a valid program is present, the ROM code branches to the main flash program execution.

Two separate flash memories are present inside the device. The 32-Kbyte program flash memory is organized as an 8-K × 32-bit memory block and is intended to be for firmware program space. The block is configured with page-erase capability for erasing blocks as small as 1 Kbyte per page, or with a mass erase for erasing the entire program flash array. This program flash endurance is specified at 1000 cycles and the data retention is good for 100 years. The 2-Kbyte data flash array is organized as a 512 × 32 memory. The data flash is intended for firmware data value storage and data logging. Thus, the data flash is specified as a high-endurance memory of 20 K cycles. The data retention for data flash is good for 100 years.

For run-time data storage and scratchpad memory, a 4-Kbyte RAM is available for firmware usage. The RAM is organized as a 1024 × 32-bit array.

The UCD30xx uses error-correcting code (ECC) for improving data integrity and providing high-reliability storage of data flash contents. ECC works by using dedicated hardware to generate extra check bits with the user data, as it is written into the flash memory. This adds to the 32-bit memory array an additional six bits, which are then stored into the flash array. These extra check bits, along with the hardware ECC algorithm, allow for any single-bit error to be detected and corrected on microprocessor reading from the data flash.

#### CPU Memory Map and Interrupts

When the device comes out of power-on reset and the boot ROM has executed, the large data memories are mapped to the processor in two different ways.

For code execution out of ROM, the boot ROM configures the memory as follows:


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- **Memory Map (ROM Mode)**

| ADDRESS | SIZE | MODULE | COMMENT |
|---|---|---|---|
| 0x0000 0000–0x0000 0FFF | 16 blocks, 4 KBytes (each) | Boot ROM (maps to all 16 blocks) | Memory select[0] |
| 0x0000 1000–0x0000 1FFF | | | |
| ... | | | |
| 0x0000 9000–0x0000 9FFF | | | |
| 0x0000 A000–0x0000 AFFF | | | |
| 0x0000 B000–0x0000 EFFF | | | |
| ... | | | |
| 0x0000 F000–0x0000 FFFF | | | |
| 0x0001 0000–0x0001 7FFF | 32 Kbytes | Program flash | Memory select[1] |
| 0x0001 8000–0x0001 87FF | 2 Kbytes | Not used | |
| 0x0001 8800–0x0001 8FFF | 2 Kbytes | Data flash | Memory select[2] |
| 0x0001 9000–0x0001 9FFF | 4 Kbytes | Data RAM | Memory select[3] |

For code execution out of flash, the boot ROM configures the memory as follows:

- **Memory Map (Flash Mode)**

| ADDRESS | SIZE | MODULE | COMMENT |
|---|---|---|---|
| 0x0000 0000–0x0000 7FFF | 32K bytes | Program flash | Memory select[1] |
| 0x0000 8000–0x0000 9FFF | 8K bytes | Not used | |
| 0x0000 A000–0x0000 AFFF | 4K bytes | Boot ROM | Memory select[0] |
| 0x0000 B000–0x0001 7FFF | 52K bytes | Not used | |
| 0x0001 8000–0x0001 87FF | 2K bytes | Not used | |
| 0x0001 8800–0x0001 8FFF | 2K bytes | Data flash | Memory select[2] |
| 0x0001 9000–0x0001 9FFF | 4K bytes | Data RAM | Memory select[3] |

- **Memory Map (System and Peripherals Blocks)**

| ADDRESS | SIZE | MODULE | COMMENT |
|---|---|---|---|
| 0xFFF7 D800–0xFFF7 D8FF | 256 bytes | UART | Peripheral select[9] |
| 0xFFF7 DC00–0xFFF7 DCFF | 256 bytes | 12-BIT ADC | Peripheral select[8] |
| 0xFFF7 E000–0xFFF7 E0FF | 256 bytes | Loop 4 CLA filter | Peripheral select[7] |
| 0xFFF7 E100–0xFFF7 E1FF | 256 bytes | Loop 4 DPWM | Peripheral select[7] |
| 0xFFF7 E400–0xFFF7 E4FF | 256 bytes | Loop 3 CLA filter | Peripheral select[6] |
| 0xFFF7 E500–0xFFF7 E5FF | 256 bytes | Loop 3 DPWM | Peripheral select[6] |
| 0xFFF7 E800–0xFFF7 E8FF | 256 bytes | Loop 2 CLA filter | Peripheral select[5] |
| 0xFFF7 E900–0xFFF7 E9FF | 256 bytes | Loop 2 DPWM | Peripheral select[5] |
| 0xFFF7 EC00–0xFFF7 ECFF | 256 bytes | Loop 1 CLA filter | Peripheral select[4] |
| 0xFFF7 ED00–0xFFF7 EDFF | 256 bytes | Loop 1 DPWM | Peripheral select[4] |
| 0xFFF7 F000–0xFFF7 F0FF | 256 bytes | Misc. analog control | Peripheral select[3] |
| 0xFFF7 F600–0xFFF7 F6FF | 256 bytes | PMBus interface | Peripheral select[2] |
| 0xFFF7 F800–0xFFF7 F8FF | 256 bytes | SPI | Peripheral select[1] |
| 0xFFF7 FA00–0xFFF7 FAFF | 256 bytes | GIO | Peripheral select[1] |
| 0xFFF7 FD00–0xFFF7 FDFF | 256 bytes | Timer | Peripheral select[0] |
| 0xFFFF FD00–0xFFFF FDFF | 256 bytes | MMC | SAR select[2] |
| 0xFFFF FE00–0xFFFF FEFF | 256 bytes | DEC | SAR select[1] |
| 0xFFFF FF20–0xFFFF FF37 | 23 bytes | CIM | SAR select[0] |
| 0xFFFF FF40–0xFFFF FF50 | 16 bytes | PSA | SAR select[0] |

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| ADDRESS | SIZE | MODULE | COMMENT |
|---|---|---|---|
| 0xFFFF FFD0–0xFFFF FFEC | 28 bytes | SYS | SAR select[0] |

The registers and bit definitions inside the system and peripheral blocks are detailed in the programmer's guide for each peripheral.

**Table 2. Interrupt Vector Table**

| NAME | MEMORY MODULE NAME | MODULE COMPONENT OR REGISTER | DESCRIPTION | PRIORITY |
|---|---|---|---|---|
| Unused | | | | (Lowest) 0 |
| BRN_OUT_INT | Misc. analog control | Brownout | Brownout interrupt | 1 |
| EXT_INT | GIO | External interrupts | Interrupt on one or all external input pins | 2 |
| WDRST_INT | Timer | Watchdog control | Interrupt from watchdog exceeded (reset) | 3 |
| WDWAKE_INT | Timer | Watchdog control | Wake-up interrupt when watchdog equals half of set watch time | 4 |
| SCI_ERR_INT | UART or SCI | UART or SCI control | UART or SCI error interrupt. Frame, parity, or overrun | 5 |
| SPI_INT | SPI | SPI control | SPI-related interrupt for overrun and/or end of SPI transmission | 6 |
| SCI_RX_INT | UART or SCI | UART or SCI control | UART RX buffer has a byte | 7 |
| SCI_TX_INT | UART or SCI | UART or SCI control | UART TX buffer empty | 8 |
| PMBUS_INT | PMBus | PMBus | PMBus-related interrupt | 9 |
| COMP_INT | Misc. analog control | Analog comparator control | Analog comparator interrupt | 10 |
| DIG_COMP_INT | ADC | 12-bit ADC control | Digital comparator interrupt | 11 |
| OVF16_4_INT | Timer | 16-bit timer PWM 4 | 16-bit timer PWM4 counter overflow interrupt | 12 |
| PWM4CMP_INT | Timer | 16-bit timer PWM 4 | 16-bit timer PWM4 counter compare interrupt | 13 |
| OVF16_3_INT | Timer | 16-bit timer PWM 3 | 16-bit timer PWM3 counter overflow interrupt | 14 |
| PWM3CMP_INT | Timer | 16-bit timer PWM 3 | 16-bit timer PWM3 counter compare interrupt | 15 |
| OVF16_2_INT | Timer | 16-bit timer PWM 2 | 16-bit timer PWM2 counter overflow interrupt | 16 |
| PWM2CMP_INT | Timer | 16-bit timer PWM 2 | 16-bit timer PWM2 counter compare interrupt | 17 |
| OVF16_1_INT | Timer | 16-bit timer PWM 1 | 16-bit timer PWM1 counter overflow interrupt | 18 |
| PWM1CMP_INT | Timer | 16-bit timer PWM 1 | 16-bit timer PWM1 counter compare interrupt | 19 |
| OVF24_INT | Timer | 24-bit timer control | 24-bit timer counter overflow interrupt | 20 |
| CAP1_INT | Timer | 24-bit timer control | 24-bit timer capture 1 interrupt | 21 |
| CMP1_INT | Timer | 24-bit timer control | 24-bit timer compare 1 interrupt | 22 |
| CMP0_INT | Timer | 24-bit timer control | 24-bit timer compare 0 interrupt | 23 |
| CAP0_INT | Timer | 24-bit timer control | 24-bit timer capture 0 interrupt | 24 |
| ADC_CONV_INT | ADC | 12-bit ADC control | ADC control end-of-conversion interrupt | 25 |
| HS Loop4 | DPWM | Loop 4 | 1) Every (1–16) DPWM switching cycles<br>2) CLF flag shutdown | 26 |
| HS Loop3 | DPWM | Loop 3 | 1) Every (1–16) DPWM switching cycles<br>2) CLF flag shutdown | 27 |
| HS Loop1 | DPWM | Loop 1 | 1) Every (1–16) DPWM switching cycles<br>2) CLF flag shutdown | 28 |
| HS Loop2 | DPWM | Loop 2 | 1) Every (1–16) DPWM switching cycles<br>2) CLF flag shutdown | 29 |
| FAULT_INT | GIO | External faults | Fault-pin interrupt | 30 |
| SYS_SSI_INT | SYS | System software | System-software interrupt | (Highest) 31 |


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## SYSTEM MODULE

The system module contains the interface logic and configuration registers to control/configure all the memory, peripherals, and interrupt mechanisms. The blocks inside the system module are the address decoder, memory management controller, system management, central interrupt, and clock control units.

### Address Decoder (DEC)

***Programmer's Reference Manual:*** *UCD30xx Memory Address Manager (DEC) Programmer's Manual*

The address decoder generates the memory selects for flash, ROM and RAM arrays. The memory map addresses are selectable through configurable register settings for low and high boundaries. These fine memory selects can be configured from 1-K to 16-M sizes. Power-on reset uses the default addresses in the memory map for ROM execution, which is then configured by the ROM code to the application setup. During access to the DEC registers, a wait state is asserted to the CPU. DEC registers are only writable in the privilege mode for user-mode protection.

### Memory Management Controller (MMC)

***Programmer's Reference Manual:*** *UCD30xx Memory Controller (MMC) Programmer's Manual*

The MMC manages the interface to the peripherals by controlling the interface bus for extending the read and write accesses to each peripheral. The unit generates eight peripheral select lines with 1 Kbyte of address space decoding. The interface can be configured with an interface clock from divide-by-2 through divide-by-16. For divide-by-2, each peripheral requires two clock accesses.

### System Management (SYS)

***Programmer's Reference Manual:*** *UCD30xx System Module (SYS) Programmer's Manual*

The SYS unit contains the software access protection by configuring user privilege levels to memory or peripheral modules. It contains the ability to generate fault or reset conditions on decoding of illegal address or access conditions. Also available is clock control setup for system operation.

### Central Interrupt Module (CIM)

***Programmer's Reference Manual:*** *UCD30xx Central Interrupt Module (CIM) Programmer's Manual*

The central interrupt module accepts 32 interrupt requests for meeting firmware timing requirements. The ARM itself only supports two levels of interrupts, FIQ and IRQ, with FIQ being the higher interrupt to IRQ. The CIM provides hardware expansion of interrupts by the use of FIQ/IRQ vector registers for providing the offset index in a vector table. This numerical index value indicates the highest-precedence channel with a pending interrupt and is used to locate the interrupt-vector address from the interrupt-vector table. Interrupt channel 0 has the lowest precedence (priority 0), and interrupt channel 31 has the highest precedence (priority 31). The CIM is level-sensitive to the interrupt requests, and each peripheral must keep the request high until the ARM responds to it. To remove the interrupt request, the firmware should clear the request as the first action in the interrupt service routine. The request channels are maskable. This allows individual channels to be selectively disabled.

### Clock Control Module (CCM)

***Programmer's Reference Manual:*** *UCD30xx Miscellaneous Analog Control (MAC) Programmer's Manual*

The clock-control module performs the peripheral clock divide-down and maintains the phase relationship needed for communication between the ARM processor and MMC-controlled peripheral bus. Figure 3 shows the UCD30xx clock domains. The interface clock (ICLK) is the peripheral clock nomenclature. This clock can run at a frequency between one-half to one-eighth of the ARM microcontroller clock (MCLK). The clock setting is configurable through firmware control. The default ICLK frequency is set to 15.6 MHz.

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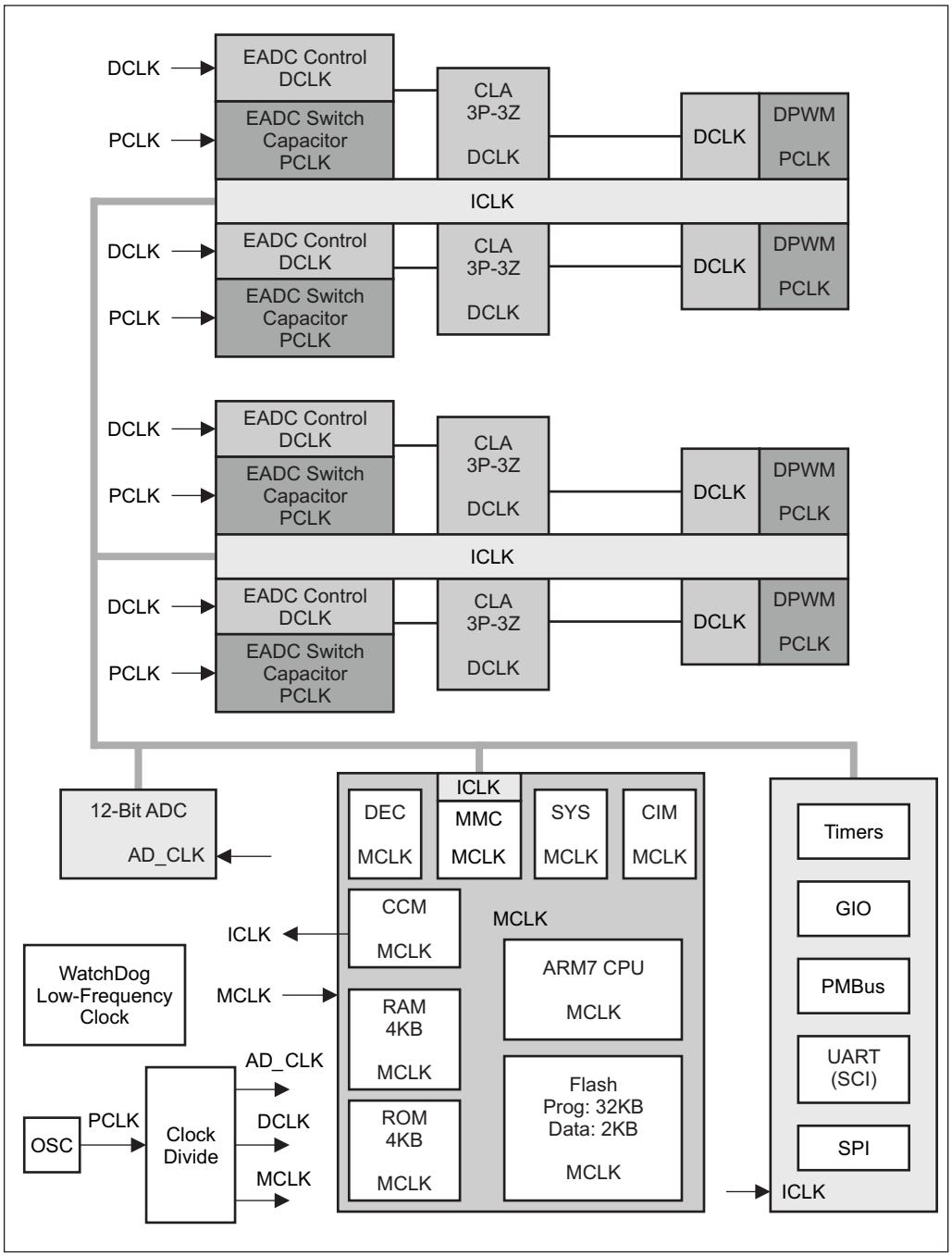
The clock source for the logic comes from a high-speed oscillator that can run at a maximum frequency of 250 MHz. This high-frequency clock domain is known at the DPWM clock (PCLK) domain. This is divided down by 8 to generate the data clock (DCLK, 31.25 MHz) domain and the microcontroller (MCLK, 31.25 MHz) domain. The default MCLK frequency is set to 31.25 MHz. However, just like ICLK, this MCLK frequency is also configurable through firmware control. DCLK supports the control-loop processing, whereas MCLK supports the ARM processor. Inside the clock-control module (CCM), MCLK has divide-down ratios for generating the interface clock (ICLK) in support of peripherals. For watchdog monitoring of the processor, a separate low-frequency oscillator is provided for generating independent watchdog events.




PCLK = 250 MHz DCLK = 31.25 MHz AD_CLK = 15.6 MHz
MCLK = 31.25 MHz (default) ICLK = 15.6 MHz (default)

**Figure 3. UCD30xx Clock Domains**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## PERIPHERALS

### Fusion Digital Power Peripherals

At the core of the UCD30xx controller are its four Fusion Digital Power peripherals (FDPP). Each FDPP can be configured to drive from one to eight DPWM outputs. Each FDPP consists of a differential input error ADC (EADC), a hardware-accelerated digital three-pole/three-zero (3p/3z) compensator, and a digital PWM module.

#### *Error ADC (EADC) Module*

***Programmer's Reference Manual:*** *UCD30xx Fusion Digital Power Peripherals Programmer's Manual*

**For initialization of the EADC module, see the UCD30xx *Fusion Digital Power Peripherals Programmer's Manual.***

The EADC module within the UCD30xx is shown in Figure 4. It contains a differential input, switch-capacitor filter circuit for receiving the differential voltage signal (signal being sensed) from external pins EAPx and EANx. It is compared with an internal 10-bit DAC output in order to measure the error voltage signal. Gain control (G) is provided in the amplifier for 1-, 2-, 4-, or 8-times amplification of the differential error signal. This error signal is then summed with an internal reference voltage (800 mV) and compared against this same reference voltage as input to the EADC module. Thus the error signal input to EADC is:

$$\text{Error} = G \times [(\text{Vrefp} - \text{Vrefm}) - (\text{EAPx} - \text{EANx})]$$

The full-scale of the EADC range is effectively 512 mV (8 mV times 64). Finally, the EADC value is converted from thermometer code to a 2s-complement value for digital processing.

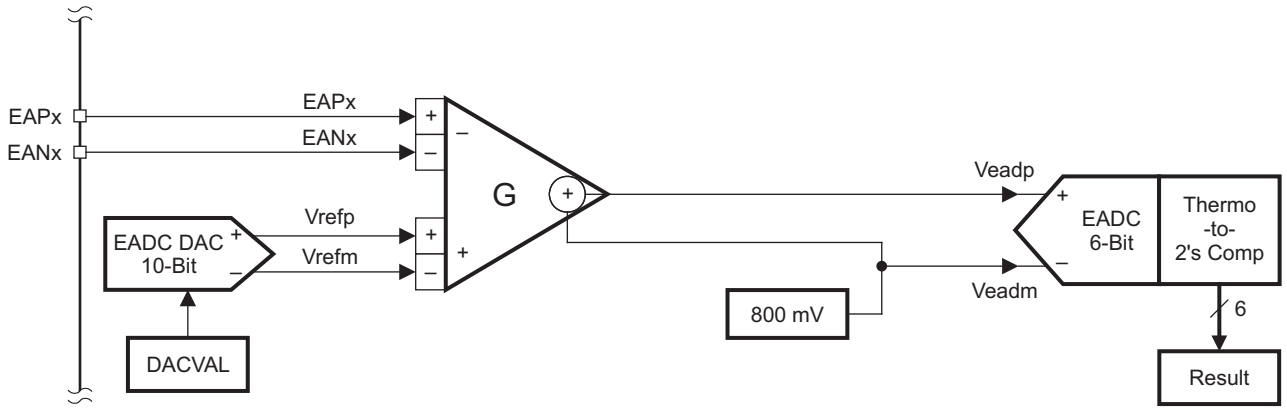


**Figure 4. Error ADC Module**

The EADC control logic receives the sample request from the DPWM module for initiating an EADC conversion. EADC control circuitry captures the EADC 6-bit code and strobes the 3p/3z digital compensator for processing of the representative error.

**Table 3. EADC and DAC Parameters**

| **EADC** | |
|---|---|
| Input differential range (EAPx – EANx) | 0 V–1.6 V |
| Common-mode range (EAPx, EANx) | 0 V–1.6 V |
| Input impedance | 1.5 MΩ (typical) |
| Sampling rate | > 10 Msps |
| Conversion time | < 100 nS |
| INL | ±2 LSB (max) |
| DNL | ±1 LSB (max) |
| Gain error | ±1 LSB (~1.5% max) |

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**Table 3. EADC and DAC Parameters (continued)**

| | |
|---|---|
| **DAC** | |
| DAC output range (Vrefp – Vrefm) | 0 V–1.6 V |
| DAC resolution | 10 bits (1024 steps) |
| DAC LSB | 1600/1024 = 1.56 mV |
| INL | ±1.5 LSB (max) |
| DNL | ±1 LSB (max) |
| Gain error | ±1% (max) |
| Settling time | < 1 µS |
| **GENERAL** | |
| Front-end gain (G) | 1, 2, 4, 8 |
| Effective resolution (EAPx – EANx) | 8 mV (G = 1), 4 mV (G = 2), 2 mV (G = 4), 1 mV (G = 8) |
| Temperature coefficient | < 50 PPM / °C |

### Digital Compensator

***Programmer's Reference Manual:*** *UCD30xx Fusion Digital Power Peripherals Programmer's Manual*

The architecture of the digital compensator in the UCD30xx system is shown in Figure 5. The compensator is a digital filter consisting of a second-order infinite-impulse-response (IIR) filter section cascaded with a first-order IIR filter section. The function of the CLA is to operate on the 6-bit output from the error ADC (EADC) and generate a command output for: (1) a fixed-frequency DPWM duty-ratio control (duty-ratio control mode), or (2) a fixed-duty-ratio DPWM frequency control (resonant mode), or (3) a fixed-frequency DPWM phase-shift control of a slave DPWM with respect to a master DPWM (phase-shift control mode).

The filter mathematics calculates a per-unit command (duty-ratio control or frequency control) output [$Y_{Q15}(n)$] between 0 and 1. In duty-ratio-control mode, this command output is then multiplied by the user-programmable DPWM switching period (PRD) to determine the duty ratio of the DPWM output. The 18-bit commanded duty ratio output [$Y_{Q0}(n)$] from the CLA is made up as a 14.4 word. The upper 14 bits specify the low-resolution DPWM clock (PCLK, 250 MHz or 4 ns) counts, and the lower 4 bits specify the high-resolution clock phase, allowing a best-case DPWM resolution of 250 ps. In resonant mode, the per-unit command output [$Y_{Q15}(n)$] is multiplied by the user-programmable maximum switching period (Max PRD) to determine the switching period of the DPWM output. This commanded switching period output [$Y_{PQ0}(n)$] is a 14-bit word. In this case, the CLA also generates a fixed-duty-ratio output [$Y_{Q0}(n)$] that is based on a user-programmable percentage of the maximum switching period. In Figure 5 this programmable percentage is indicated as % of PRD.

Two banks of filter coefficients can be saved in the device. The user firmware can switch them, depending on the operation of the power stage. The coefficients can be calculated using standard digital control techniques.


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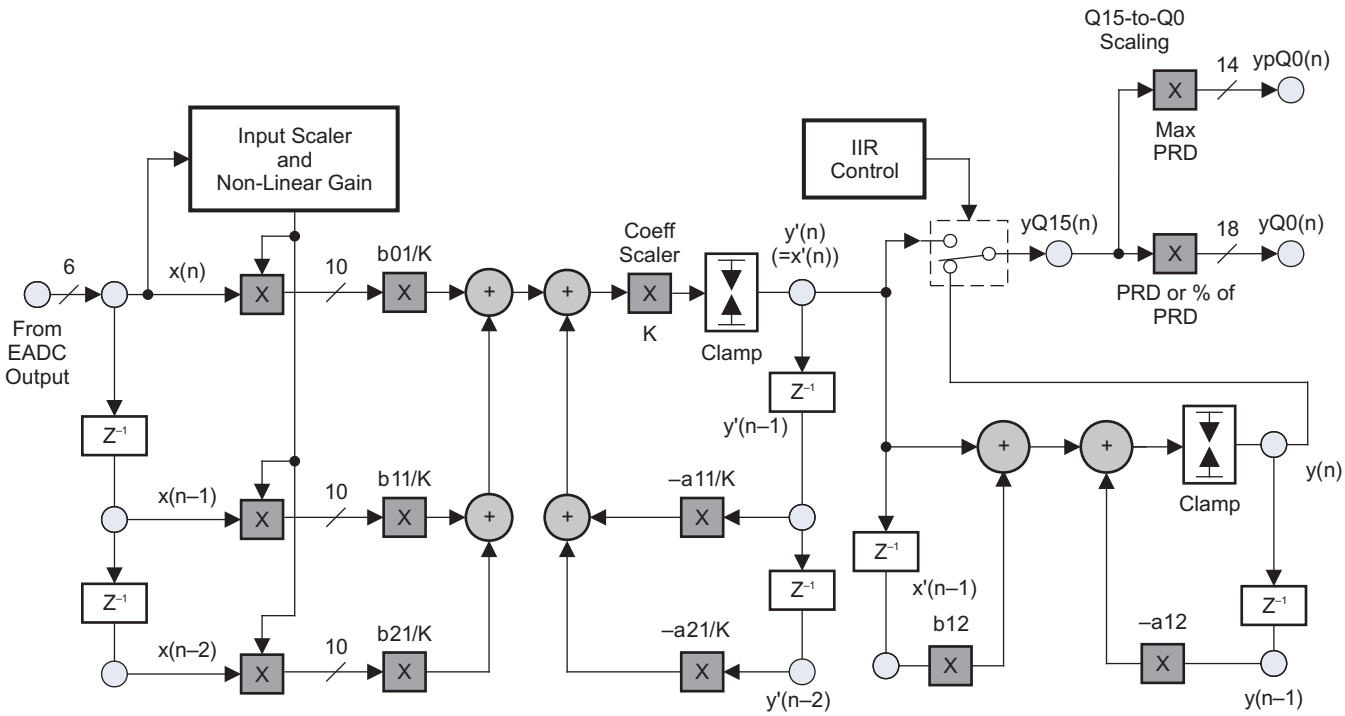


**Figure 5. Compensator Architecture**

The compensator also allows the minimum and maximum duty cycle to be programmed.

### *Compensator (CLA) Input*

The input to the filter is a 6-bit signed number generated by the EADC. This number represents a 2s-complement value of the power-supply output-voltage error signal (Vref – Vsense). This data value is registered on the system clock inside the EADC, and a converted data-ready signal is supplied to start the filter operation on this new data. The error inputs E(n – 1) and E(n – 2) are registered in the 6-bit format to save space. The current E(n) is not registered inside the filter. The E(n) inputs to the filter can also come from a register that is programmed by the user software. This happens only when the CPU sample-control bit is enabled. This allows the CLA to be a math coprocessor for the UCD30xx CPU. The E(n), E(n – 1), and E(n – 2) values can only be written by the user software by setting the filter-enable bit to 0.

### *Compensator Input Scaling*

The input of the CLA is scaled to retain the physical meaning of the converted data and to implement nonlinear control. The scaling function does two things. First, it divides the input by 1024, which approximately converts it back to the millivolts (1/1000 V) scale that was converted. Second, it multiplies the input by a user-programmable nonlinear gain, and the resulting 10-bit output of the scaler is applied to the filter input. During power-supply control-loop design, the nominal gain value in the nonlinear gain table and the EADC analog front end (AFE) gain must be taken into consideration. After the control design, if one of these values (nonlinear gain or AFE gain) is changed, then the other one must be adjusted accordingly in order to maintain the same product (nonlinear gain × AFE gain) and hence the same (designed) loop gain for the power supply. The following shows the AFE control-bit settings, the corresponding AFE gain applied to the input, and the resulting EADC resolution.

Control bits = 0x3 → 8× AFE gain → EADC resolution = 1mV/lsb
Control bits = 0x2 → 4× AFE gain → EADC resolution = 2mV/lsb
Control bits = 0x1 → 2× AFE gain → EADC resolution = 4mV/lsb
Control bits = 0x0 → 1× AFE gain → EADC resolution = 8mV/lsb

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### *Digital Compensator Coefficients*

Each compensator in the UCD30xx has a set of seven coefficients. These are stored in 12-bit Q11 format. There are two such banks or *pages* of these coefficient sets. This allows CLA-coefficient bank switching at any time during operation. Both pages of coefficients are based at the same CPU (ARM) offset address and are accessed through the page-active control bit and page-read control bit. To read a bank of coefficients, the page-read bit is set to point to the desired bank (1 for bank 1 or 0 for bank 0). To program/write a bank of coefficients, one must first make the opposite bank active by writing to the page-active control bit. The switching of coefficient banks occurs only after the filter has completed the control output calculations for the current sampling period. The coefficient bank-active status bit must be polled to determine which bank is active. Once the opposite bank is active, the user software can then write to the inactive page.

The compensator architecture in UCD30XX results in the following z-domain transfer function:

$$G_{CLA}(z) = \frac{b_{01} + b_{11}z^{-1} + b_{21}z^{-2}}{1 + a_{11}z^{-1} + a_{21}z^{-2}} \times \frac{1 + b_{12}z^{-1}}{1 + a_{12}z^{-1}} \tag{1}$$

The compensator calculates a duty-ratio command from 0 to 100 percent of the switching period. To do this, all the values inside the compensator are kept as fractions. The hardware expects the coefficients to be scaled down to fractions and be in 2s-complement form. This is done by dividing all of the coefficients of the second-order IIR filter by a $2^n$ integer that is larger than the largest coefficient.

Example:

$$G_{CLA}(z) = \frac{14.35 - 24.635z^{-1} + 10.418z^{-2}}{1 - 1.521z^{-1} + 0.521z^{-2}} \times \frac{1 - 0.612z^{-1}}{1 - 0.128z^{-1}} \tag{2}$$

B01 = 14.350 → In 12-bit Q11 format, B01 = $(14.350/2^5) \times (2^{11})$ = 0x0396
B11 = –24.635 → In 12-bit Q11 format, B11 = $(-24.635/2^5) \times (2^{11})$ = 0xF9D7
B21 = 10.418 → In 12-bit Q11 format, B21 = $(10.418/2^5) \times (2^{11})$ = 0x029B
A11 = –1.521 → In 12-bit Q11 format, A11 = $-(-1.521/2^5) \times (2^{11})$ = 0x0061
A21 = 0.521 → In 12-bit Q11 format, A21 = $-(0.521/2^5) \times (2^{11})$ = 0xFFDF
B12 = –0.612 → In 12-bit Q11 format, B12 = $(-0.612) \times (2^{11})$ = 0xFB1B
A12 = –0.128 → In 12-bit Q11 format, A12 = $-(-0.128) \times (2^{11})$ = 0x0106

Notice that the scaling factor in the previous example was $2^5 = 32$, the smallest $2^n$ that is larger than the largest coefficient (24.635 in this example). The scaling factor exponent is programmed into the device for use in the hardware. This scaling factor is also stored as banks so that each independent coefficient set is scaled separately. The same procedure to write new coefficients is used to program the scaling factor.

### *Duty-Cycle Clamps*

The digital filter is equipped with upper and lower duty-ratio clamp values. These clamp values are programmed as percentages that are multiplied by the maximum switching period. These clamp values are fed back into the filter output storage [y'(n – 1) and y'(n – 2)]. The clamp values are also stored in pages with their own page control. The user must poll the clamp active-status bit to determine the active page.

### *Compensator Stored Calculations Y(n)*

The calculated outputs of the filter are stored in 16-bit registers. Thus y'(n – 1), y'(n – 2), and y(n – 1) are stored in 16-bit registers. The filter outputs y'(n – 1) and y'(n – 2) represent the old sampled values of the 2p/2z section of the filter. The old sample output of the complete 3p/3z filter is represented by y(n – 1). These values are truncated down and stored in 16-bit Q15 formats. The user software can read these values at any time during operation by accessing the appropriate registers. The user software can also write to these registers, but this is allowed only when the filter is disabled.

### *Output Scaling*

The output of the CLA represents a control command output in per unit, i.e., in fraction (0 to 1). This output is then multiplied by the switching period of the DPWM to compute the DPWM duty ratio. This duty ratio is an 18-bit value. The 4 least-significant bits determine the high-resolution duty adjustment (250 ps) of the DPWM output. The 14 most-significant bits are used for coarse duty adjustment (4 ns) of the DPWM output.


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In resonant mode, the output is multiplied by the maximum-allowed switching period to modulate the DPWM switching frequency. The filter output is also multiplied by a programmed percentage of the maximum-allowed switching period to generate the required fixed DPWM duty ratio.

### *Nonlinear Control Capability*

The nonlinear control capability of the UCD30xx is implemented by applying a user-programmable gain to the incoming error signal. This gain is applied by use of the filter input scaler. The user has a paged table of five 6-bit values that represent a 4.2 binary number. This allows a gain range of 0.25 to 15.75 in 0.25 increments. The gain values are selected based on the range of the incoming error voltage from the EADC. The error voltage range is determined by comparing it to a set of four 6-bit limits.

| Error Range | Gain Applied | Register Bits Used (FLTRNLR1) |
|---|---|---|
| E(n) < Limit_0 | ≥ Gain0 | [5–0] |
| Limit_0 < E(n) < Limit_1 | ≥ Gain1 | [11–6] |
| Limit_1 < E(n) < Limit_2 | ≥ Gain2 | [29–24] |
| Limit_2 < E(n) < Limit_3 | ≥ Gain3 | [23–18] |
| E(n) > Limit_3 | ≥ Gain4 | [17–2] |

Five gain values and the four limit selections are set up in a paged structure (Figure 6). This allows the user to configure the off page. The active page is controlled by a bit in the control register. The switching of the pages occurs when the filter is inactive. The status bit must be polled to determine the active page before writing to a bank.

### *Status Signals*

There are five status signals available to the user.

- Two EADC rail signals indicate that the EADC value coming into the filter has reached the maximum or minimum limits.
- A nonlinear page-active status shows the nonlinear table that is currently in use.
- A clamp page-active status shows the clamp page that is currently in use.
- A page-active status shows the coefficient page that is currently in use.

### *Control Signals*

There are seven control signals available to the user.

- The *filter enable control* that turns on and off filter processing. When this bit is disabled the user's software can write to the input error terms and the stored output results.
- The *page active control* sets which bank of coefficients is in use by the filter. The ability to write to the coefficient banks depends on the setting of this control.
- The *read page control* selects which coefficient bank is being read by the user's software.
- The *3 pole 3 zero enable control* turns on the filter processing through the optional 1 pole 1 zero stage.
- The *CPU sample enable control* forces the filter to use the E(n) terms written by the user's software.
- The *clamp page active control* sets which page of clamps are in use by the filter. The ability to write to the clamp pages depends on the setting of this control.
- The *non-linear page active control* sets which page of non-linear gain table and limits are in use by the filter. The ability to write to the non-linear gain table and limits depend on the setting of this control.

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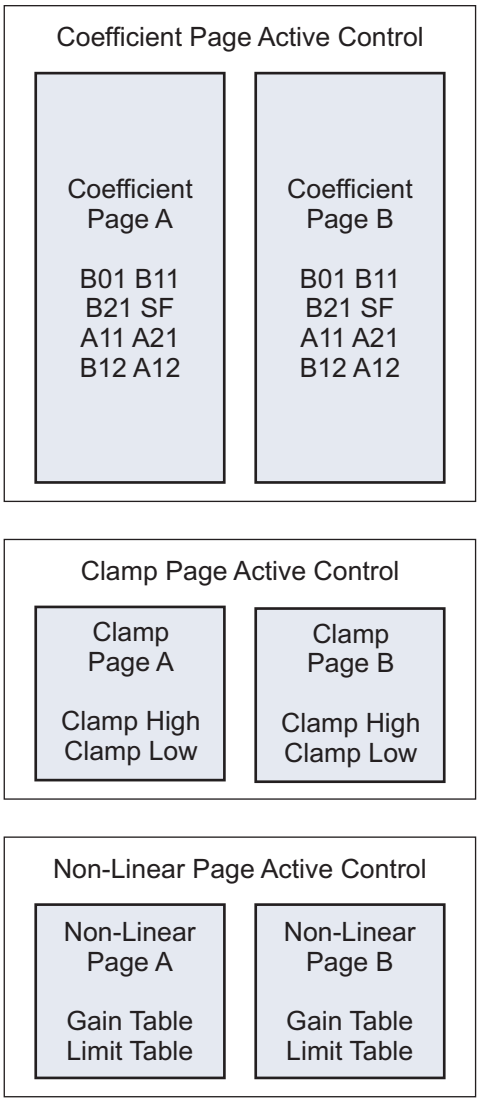


**Figure 6. Page Setup for Nonlinear Gain and Limits**

### DPWM Module

***Programmers' Reference Manual:*** *UCD30xx Fusion Digital Power Peripherals Programmer's Manual*

The DPWM module represents one complete DPWM channel with two independent outputs, A and B. Multiple DPWM modules within the UCD30xx system can be configured to support all key power topologies. DPWM modules can be used as independent DPWM outputs, each controlling one power-supply output-voltage rail. A DPWM module can also be used as a synchronized DPWM, with user-selectable phase shift between the DPWM channels, in order to control power-supply outputs with multiphase or interleaved DPWM configurations.

The output of the compensator feeds the high-resolution DPWM module. The DPWM module produces the pulse-width-modulated outputs for the power-stage switches. The compensator calculates the necessary duty ratio as a 16-bit number in Q15 fixed-point format. This represents a value within the range 0.0 to 1.0. This duty-ratio value is multiplied by the period of the DPWM output to generate the ON time of the corresponding DPWM output. The resolution of the DPWM ON time is 250 ps.


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When the UCD30xx is configured to control multiple power stages from one compensator, each DPWM output-pulse width is adjusted to correct for current imbalance between the power stages. This is done by monitoring the current using the 12-bit ADC and increasing the pulse width of the DPWM signal driving the power stage with the lower current and decreasing the pulse width of the DPWM signal driving the power stage with the higher-measured current.

Each DPWM module can be synchronized to another module or to an external sync signal. An input sync signal causes a DPWM ramp timer to reset. Sync-signal outputs from each of the four DPWM modules occur when the ramp timer crosses a programmed threshold. In this way, the phase of the DPWM outputs for multiple power stages can be tightly controlled.

Each DPWM module supports the following basic features:

- Dedicated 14-bit time base with period/frequency control
- Shadow-period register for end-of-period updates
- Quadruple event-control registers (A and B, rising and falling) (events 1–4), used for on/off DPWM duty-ratio updates
- Phase control relative to other DPWM modules – phase trigger
- Sample trigger placement for output voltage sensing at any point during the DPWM cycle
- Supports two independent edge-placement DPWM outputs (same frequency or period setting)
- Dead time between DPWM A and B outputs
- High-resolution capabilities – 16× clock frequency
- Pulse cycle adjustment: ±11.4 = ±2048 DPWM clocks (PCLK) and 16 high-resolution (HR) phases
- Current-limit flag (CLF) counter/flag capability
- Active-high/active-low output-polarity selection
- Provides events to trigger both CPU interrupts and start of ADC conversions

### *DPWM Events*

Each DPWM can control the following timing events:

1. *Sample trigger count* – This register defines where the error voltage is sampled by the error ADC (EADC) in relationship to the DPWM period. The programmed value set in the register should be one-fourth of the value calculated based on the DPWM clock, as the DCLK (DCLK = 31.25 MHz max) controlling the circuitry runs at one-fourth of the DPWM clock (PCLK = 250 MHz max). When this sample trigger count is equal to the DPWM counter, it initiates a front-end calculation by triggering the error ADC, resulting in CLA calculation and DPWM update. Oversampling can be set for 2, 4, or 8 times the sampling rate.
2. *Phase trigger count* – Count offset for slaving another DPWM (multiphase/interleaved operation)
3. *Period* – Low-resolution switching-period count (count of PCLK cycles)
4. *Event 1* – Count offset for rising DPWM A event (count of PCLK cycles)
5. *Event 2* – DPWM count for falling DPWM A event that sets the duty ratio. Last 4 bits of register are for high-resolution control. Upper 14 bits are the number of PCLK cycle counts.
6. *Event 3* – DPWM count for rising DPWM B event. The last 4 bits of register are for high-resolution control. The upper 14 bits are the number of PCLK cycle counts.
7. *Event 4* – DPWM count for falling DPWM B event. The last 4 bits of register are for high-resolution control. The upper 14 bits are the number of PCLK cycle counts.
8. *Cycle adjust* – Constant offset for event-2 and event-4 adjustments

Basic comparisons between the programmed registers and the DPWM counter can create the desired edge placements in the DPWM. High-resolution edge capability is available on events 2, 3, and 4.

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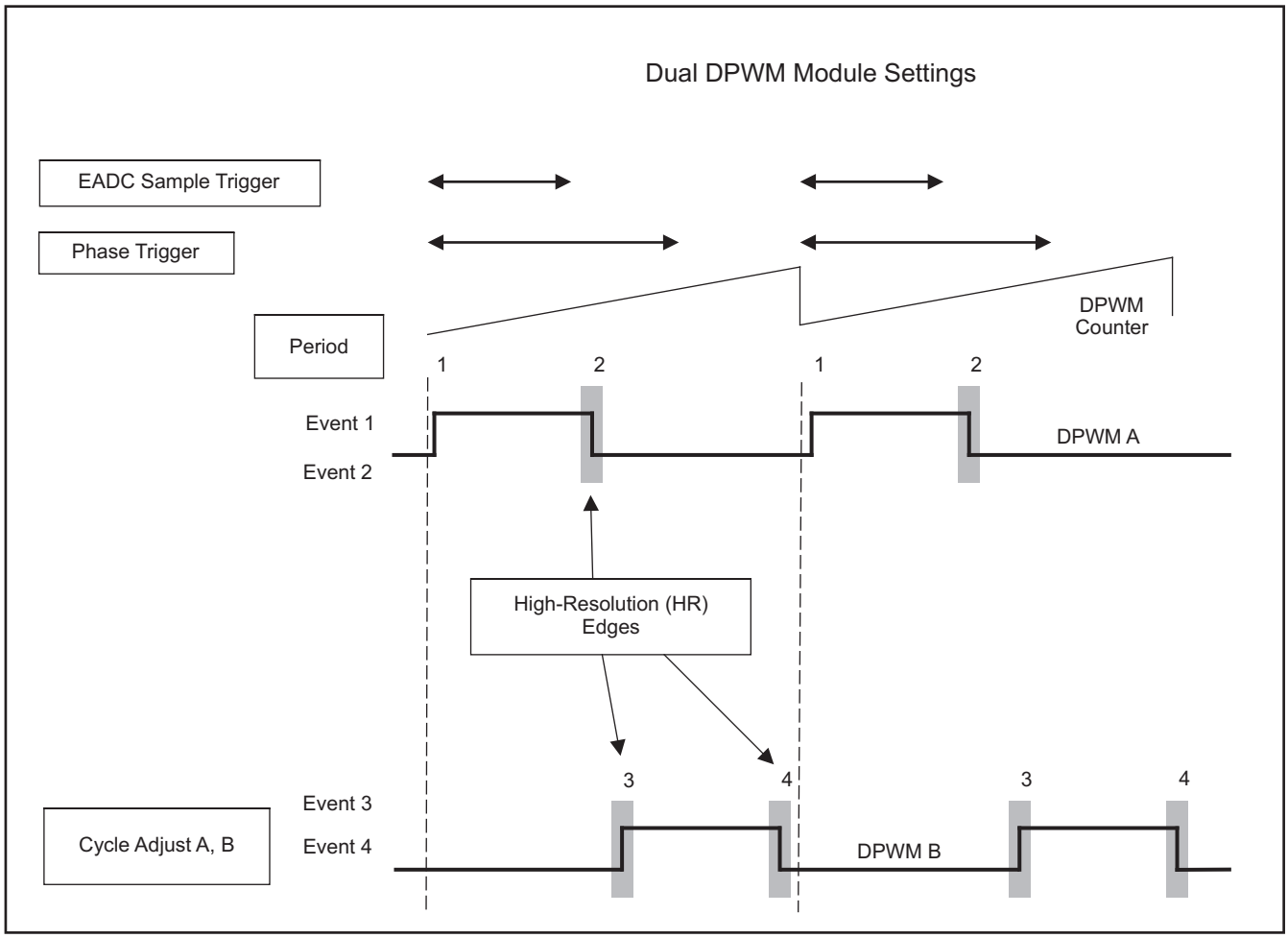


**Figure 7. DPWM Events**


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### *DPWM Frequency*

The following table shows a few examples of different DPWM frequencies based on a maximum PCLK frequency value of 250 MHz.

**Table 4. DPWM Frequency Range**

| DPWM FREQUENCY (kHz) | PERIOD REGISTER VALUE (Hex) | NUMBER OF BITS (in 14-Bit Period Register) |
|---|---|---|
| 1953.125 | 007F | 7 |
| 976.563 | 00FF | 8 |
| 488.28 | 01FF | 9 |
| 244.14 | 03FF | 10 |
| 122.07 | 07FF | 11 |
| 61.035 | 0FFF | 12 |
| 30.517 | 1FFF | 13 |
| 15.26 | 3FFF | 14 |
| Period register = $(f_{PCLK}/f_{DPWM}) - 1$ | | |

### *DPWM Modes of Operation*

DPWM has four modes of operation. These are (1) duty-ratio control (normal), (2) phase control, (3) frequency control (resonance), and (4) multi-output mode.

**Normal Mode (Duty-Ratio Control)**

- DPWM B output is slaved and relative to DPWM A.
- When the CLA is enabled for closed-loop control, the event-2 comparison for DPWM A is controlled by the CLA value.
  - The CLA value then sets the pulse width of DPWM A.
- For calculating the dead time between the falling edge of DPWM A and the rising edge of DPWM B, the initial settings of the event-2 and event-3 registers (delta) are used.
  - So for CLA-enabled closed-loop control, the calculated delta (event 3 – event 2) is used to place event 3.
- The event-4 to event-1 registers are used for the front-end dead time by controlling the falling edge of DPWM B to the rising edge of DPWM A.
- Events 2, 3, and 4 can be high-resolution (HR) edges.
- Cycle-adjust A is used for DPWM A pulse-duration adjustment.

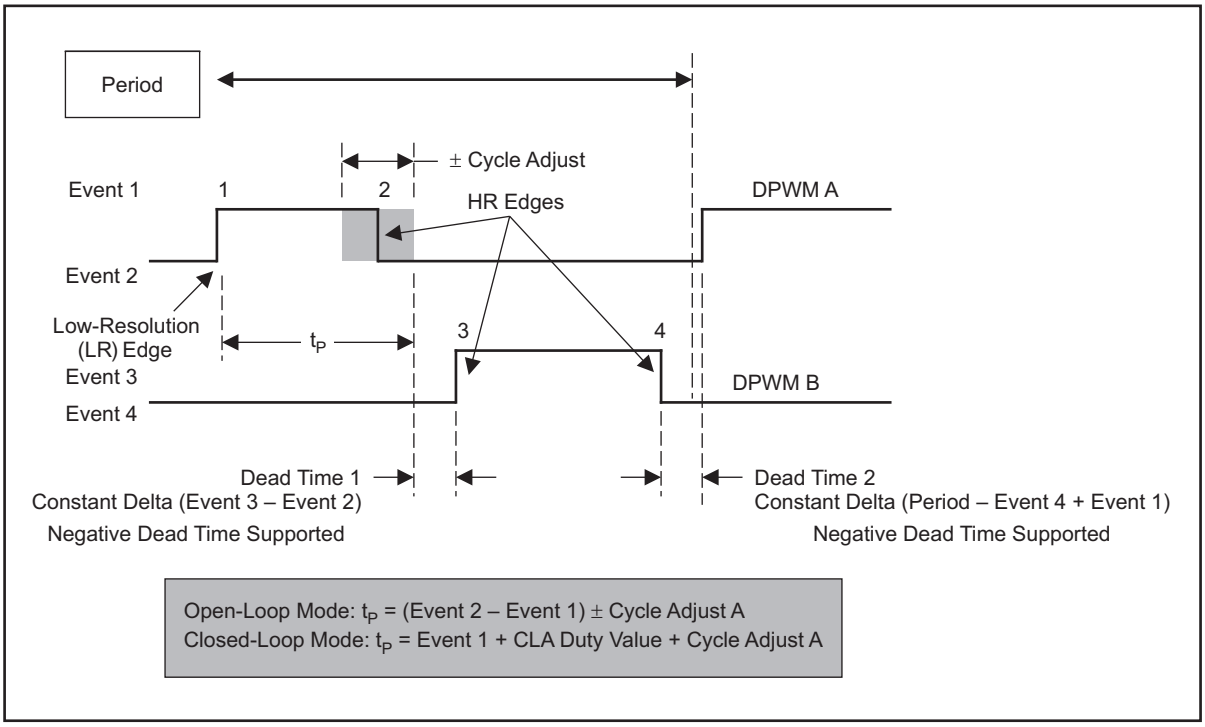


**Figure 8. Normal Mode (Duty-Ratio Control) – DPWM Timing Diagram**

***Compensator Phase Mode (Phase-Shift Control)***

- Only used for a slave-mode setup, where the CLA duty-value output is used to calculate the phase offset from a master DPWM.
  - The CLA output is used as the phase adjustment and is supported by low resolution.
- Setting of event 1 and event 2 sets the pulse width of DPWM A.
- Setting of event 3 and event 4 sets the pulse width of DPWM B.
- Events 2, 3, and 4 can be high-resolution edges.
- Cycle-adjust A is used for DPWM A pulse-width adjustment.


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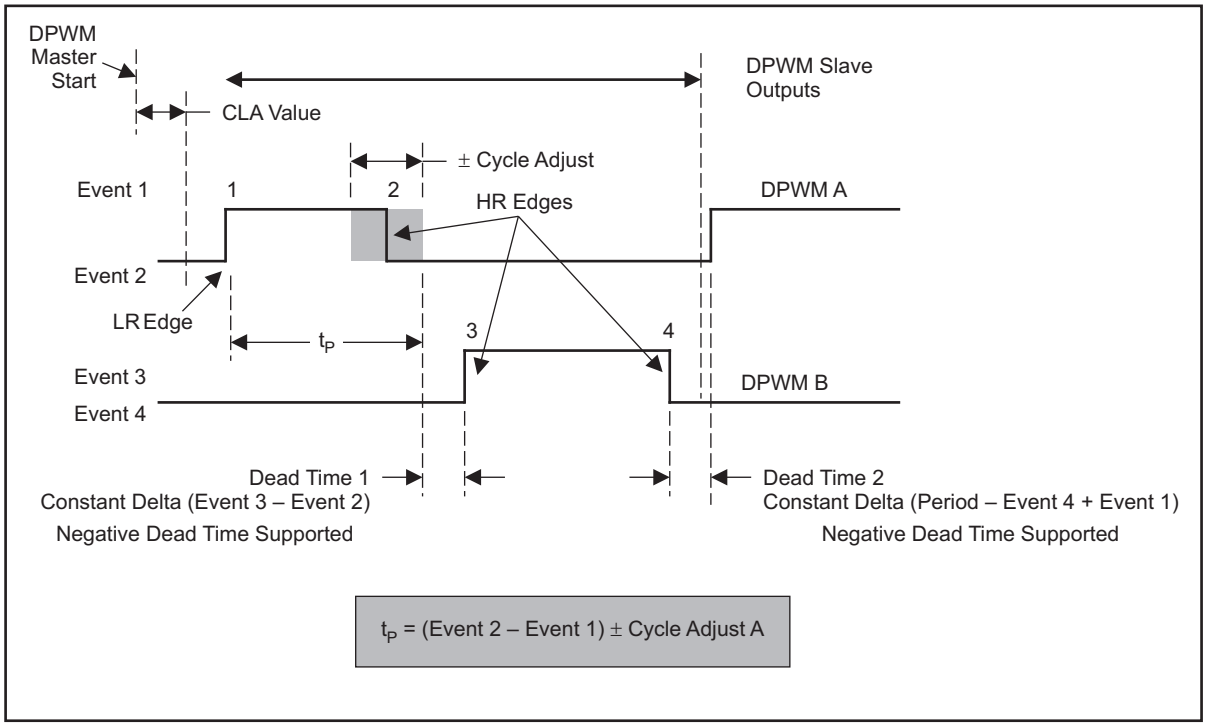


**Figure 9. Compensator Phase Mode (Phase-Shift Control) – DPWM Timing Diagram**

***Resonance Mode (Constant-On Duty Ratio With Variable Period)***

- DPWM B output is slaved and relative to DPWM A.
- When the CLA is enabled for closed-loop operation, the event-2 comparison is controlled by the CLA duty-output value.
  - The CLA value sets the pulse width of DPWM A.
- When the CLA is enabled for closed-loop operation, the period is controlled by the CLA period-output value.
- The initial settings of event 2 and event 3 (delta) are used for the calculation of the dead time between the falling edge of DPWM A and the rising edge of DPWM B.
  - So, when the CLA is enabled for closed-loop operation, the calculated delta is used with the CLA duty-output value to place event 3.
- The initial settings of period and event 4 (delta) are used for the calculation of the dead time between the falling edge of DPWM B and rising edge of DPWM A.
  - So, when the CLA is enabled for closed-loop operation, the calculated delta is used with the CLA duty-output value to place event 4.
- Events 2, 3, and 4 can be high-resolution edges.
- Cycle-adjust A is used for period adjustment by the CPU.

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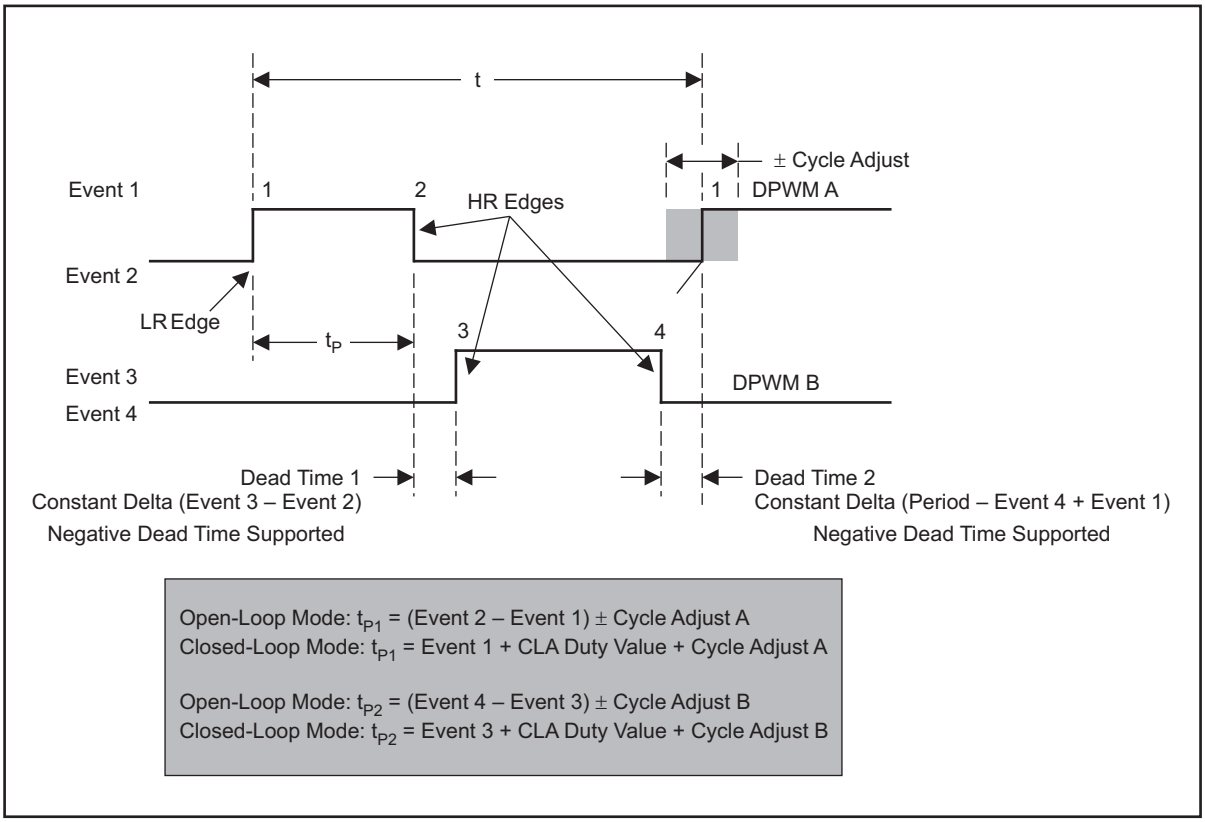


**Figure 10. Resonance Mode (Constant-On Duty Ratio With Variable Period) – DPWM Timing Diagram**

***Multi-Output Mode***

- Each DPWM module can be set up with two DPWM outputs of thesame frequency and same duty ratio.
- For multiphase operation, both master- and slave-mode setup.
- CLA duty-ratio output value sets the pulse width of both DPWM A and DPWM B.
- DPWM A always starts at the event-1 setting
- DPWM B always starts at the event-3 setting.
- Can be set up as a slave DPWM, with the phase offset from another DPWM.
- DPWM B can cross over the period count for full on-time duty-cycle operation.
- Events 2 and 4 can be high-resolution edges.
- Cycle-adjust registers for DPWM A and DPWM B are available for small pulse-width adjustments, making independent DPWM duty-ratio adjustments between phases for current-balancing applications.
- While applying a –ve cycle adjust to DPWM B, the minimum on-pulse width (calculated value of tp2 in Figure 11) should be limited to 0. A –ve value for the DPWM B on-pulse width is not valid.


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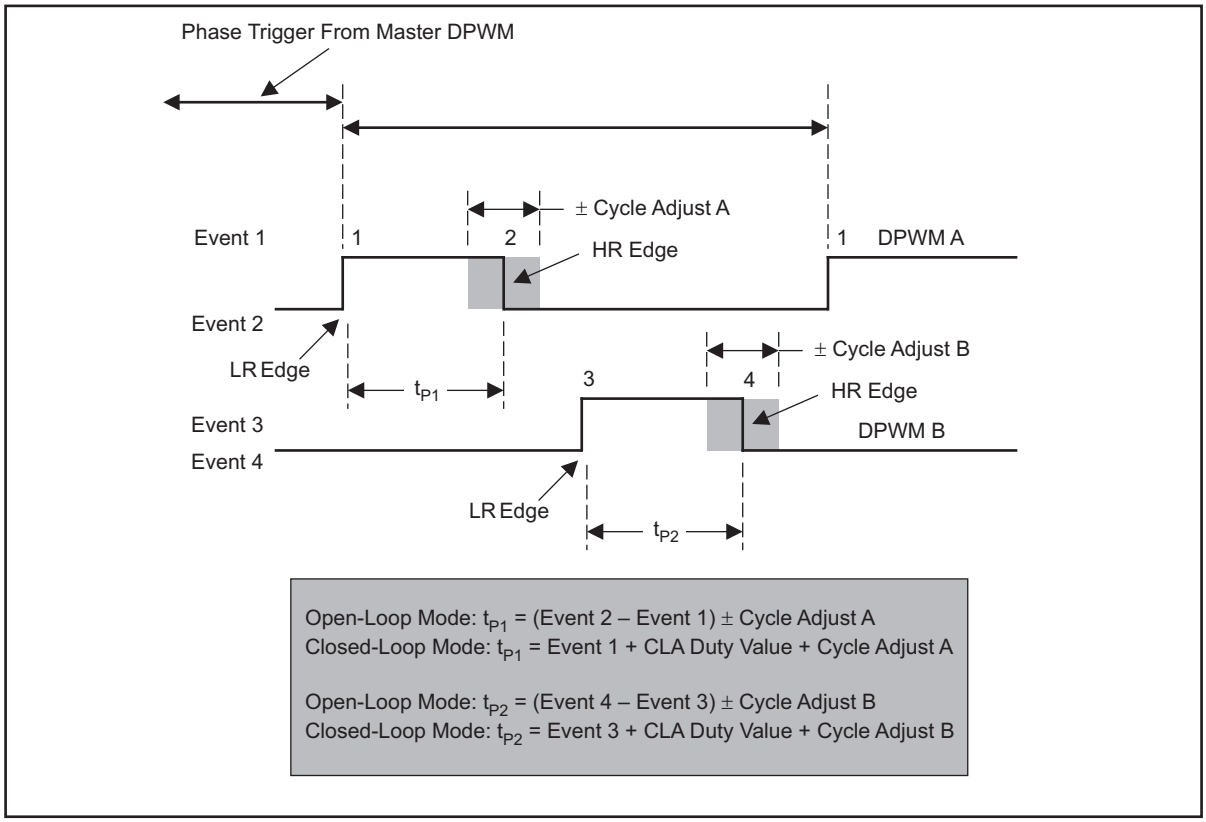


**Figure 11. Multi-Output Mode – DPWM Timing Diagram**

### *High-Resolution DPWM*

The DPWM high-resolution section has DPWM edge placement capability for up to 16 phases of subclock resolution. For the maximum 250-MHz PCLK (DPWM clock), each phase then represents 1/16 of the 4-ns DPWM clock time, or 250 ps. The DPWM section has a disable bit and resolution-setting bits. The default resolution setting (00) has 16 phases, and the 01 setting has eight phases (even number of phases from 0 to 15). The 10 setting uses four phases set to 0, 4, 8, and 12, whereas the 11 setting uses just the 0 and 8 phases. So, for the maximum 250-MHz DPWM clock, the 00 setting has 250 ps resolution, the 01 setting has 500 ps resolution, the 10 setting has 1 ns resolution, and the 11 setting has 2 ns resolution.

### *Oversampling*

The DPWM module has the capability to trigger an oversampling event by initiating the EADC to sample the error voltage. The default 00 configuration has the DPWM trigger the EADC once based on the sample trigger register value. The oversampling register has the ability to trigger the sampling 2, 4, or 8 times per DPWM period.

### *DPWM Interrupt Generation*

The DPWM has the capability to generate a CPU interrupt based on the DPWM frequency programmed in the period register. The interrupt can be scaled by a divided ratio of up to 255 for developing a slower interrupt service execution loop. Table 5 outlines the divide ratios that can be programmed.

**Table 5. DPWM Interrupt Divide Ratio**

| DPWM INTERRUPT SCALING/RANGE | | | | | | |
|---|---|---|---|---|---|---|
| INTERRUPT DIVIDE SETTING | INTERRUPT DIVIDE COUNT | INTERRUPT DIVIDE COUNT (hex) | SWITCHING PERIOD FRAMES (assume 1-MHz loop) | NUMBER OF 32-MHz PROCESSOR CYCLES | NUMBER OF 16-MHz PROCESSOR CYCLES | NUMBER OF 8-MHz PROCESSOR CYCLES |
| 1 | 0 | 00 | 1 | 32 | 16 | 8 |
| 2 | 1 | 01 | 2 | 64 | 32 | 16 |
| 3 | 3 | 03 | 4 | 128 | 64 | 32 |
| 4 | 7 | 07 | 8 | 256 | 128 | 64 |
| 5 | 15 | 0F | 16 | 512 | 256 | 128 |
| 6 | 31 | 1F | 32 | 1024 | 512 | 256 |
| 7 | 47 | 2F | 48 | 1536 | 768 | 384 |
| 8 | 63 | 3F | 64 | 2048 | 1024 | 512 |
| 9 | 79 | 4F | 80 | 2560 | 1280 | 640 |
| 10 | 95 | 5F | 96 | 3072 | 1536 | 768 |
| 11 | 127 | 7F | 128 | 4096 | 2048 | 1024 |
| 12 | 159 | 9F | 160 | 5120 | 2560 | 1280 |
| 13 | 191 | BF | 192 | 6144 | 3072 | 1536 |
| 14 | 223 | DF | 224 | 7168 | 3584 | 1792 |
| 15 | 255 | FF | 256 | 8192 | 4096 | 2048 |

### *Compensator Updates of DPWM*

Once the sampling trigger register comparison to DPWM counter count is complete, a sampling event is initiated by the DPWM to the EADC. After some logic latency, the updated CLA value is used in event calculations. Usually, the sampling trigger is placed away from the DPWM switching transitions. However, the DPWM has register controls for forcing the CLA event to happen at the end of the DPWM cycle by using the update end of period-enable bit. This control prevents updates from occurring between dead-time events. For testing, a single-frame enable bit can be used for single-step frame operation.

### *Compensator Output Scaling*

The DPWM has the capability to scale the incoming CLA value. The value can be multiplied by 2, 4, or 8 or divided by 2, 4, or 8 for providing different switch capacitor gain/CLA gain options.

### *DPWM Current-Limit Fault (CLF) Trip Logic*

The CLF logic can be enabled for counting the number of current-limit indications per DPWM switching period. The current-limit indication is sampled at the CLA event-2 time. The number of current-limit faults allowed prior to setting the current-limit fault flag is programmed by use of the 8-bit CLF maximum-count register. The logic can be configured with the CLF count-continuous bit set to zero, for counting CLF indications on continuous DPWM switching cycles. This allows the circuit to reset back to 0 if one switching cycle does not have a current-limit fault input. Alternatively, the logic can be configured with the CLF count-continuous bit set to 1, for posting a flag if the CLF maximum-count register value is reached over an indefinite period of time. Generation of the CLF flag is routed to the processor and can be used as a CPU interrupt. The CLF flag is also directly connected to the DPWM logic and is used to make the DPWM outputs go inactive.

For the UCD30xx, the source of the CLF input comes from the output of the analog comparators. Any one of the four analog comparators (A–D) can be selected in the misc. control register as the source of the DPWM CLF input.


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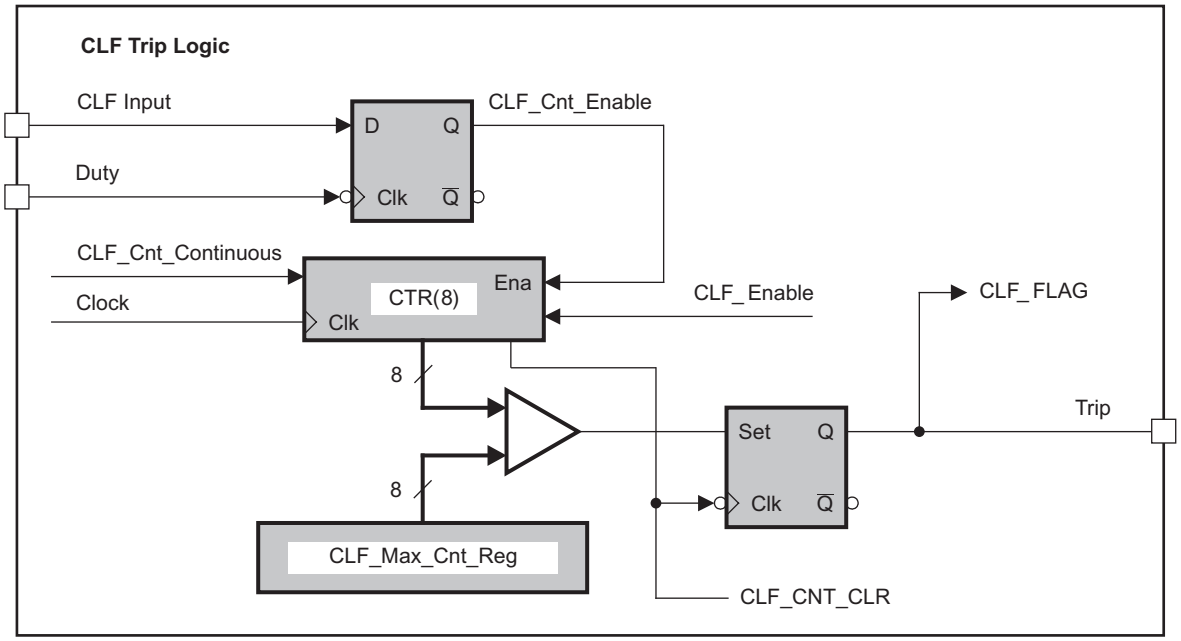


**Figure 12. Current-Limit-Flag (CLF) Trip Logic**

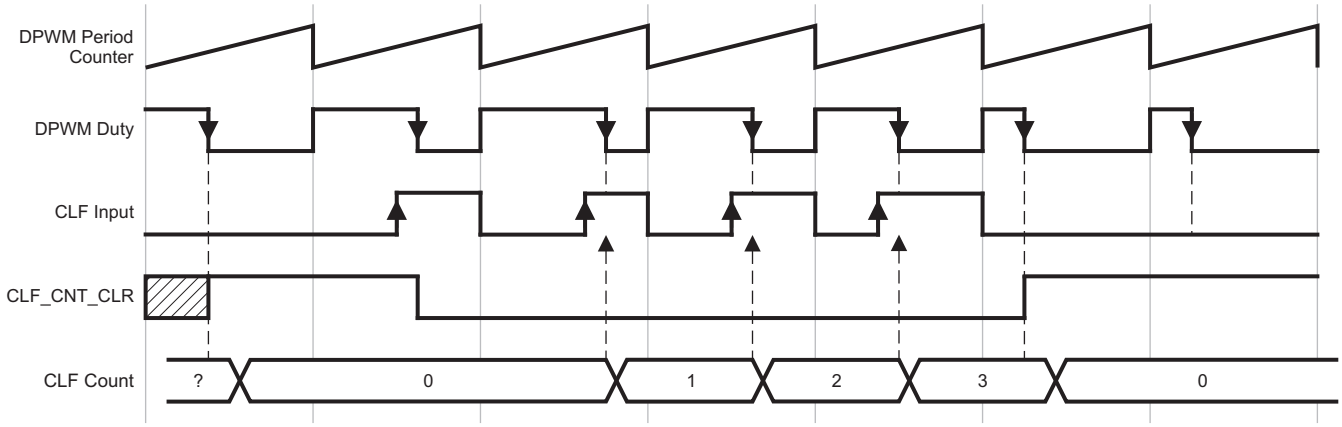


**Figure 13. Current-Limit-Flag Trip-Logic Waveform**

### *DPWM GPIO Capability*

The DPWM module can be configured to have each A and B output set up independently for GPIO capability. For setting the output, the corresponding GPIO enable bit must be set, and the GPIO value bit must be set to the desired level (1 or 0). Separate enable and value bits exist for each A and B output. Input to the DPWM pins is read from the DPWM overflow register.

### *DPWM Fault-Protection Logic*

A DPWM fault-enable bit is available for causing the DPWM to turn off and go inactive on a fault input from an external pin. Two fault pins are routed to the general-purpose I/O module first, where a latched version of the fault is sent to the CPU as an interrupt, and to the DPWM as a fault input (Fault[1:0]). In normal mode (no DPWM mode bits set), the connected fault signals control both the A and B outputs of the DPWM, causing both DPWM outputs to go inactive with either fault present. In all other modes (MULTI_OUT, RESONANCE, or PHASE), Fault[0] controls DPWM output A and Fault[1] controls DPWM B output, allowing individual fault control of each phase. Once the latched fault value from the general-purpose I/O is cleared through the pending-GPIO fault register, the DPWM resumes at the beginning of a switching period.

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### *Multiple DPWMs*

Compensator Selection

Each DPWM has a 2-bit field for selecting the compensator. Because each EADC is tied to one compensator, this capability allows for multiphase operation from any EADC source. However, this is not true for resonance-mode operation, when CLA1 only controls DPWM1, CLA2 controls DPWM2, and so on.

Internal Device Multisync Capability

The DPWM can be enabled as a slave using the *Multisync Slave-Enable Bit*, for accepting a trigger source set by the master's phase trigger. This trigger is used to reset the slave DPWM to zero count for phase-offset synchronization. The DPWM *Multisync Channel-Select* bits are used for master trigger selection.

Figure 14 and Figure 15 portray the compensator and sync multiplexing options:


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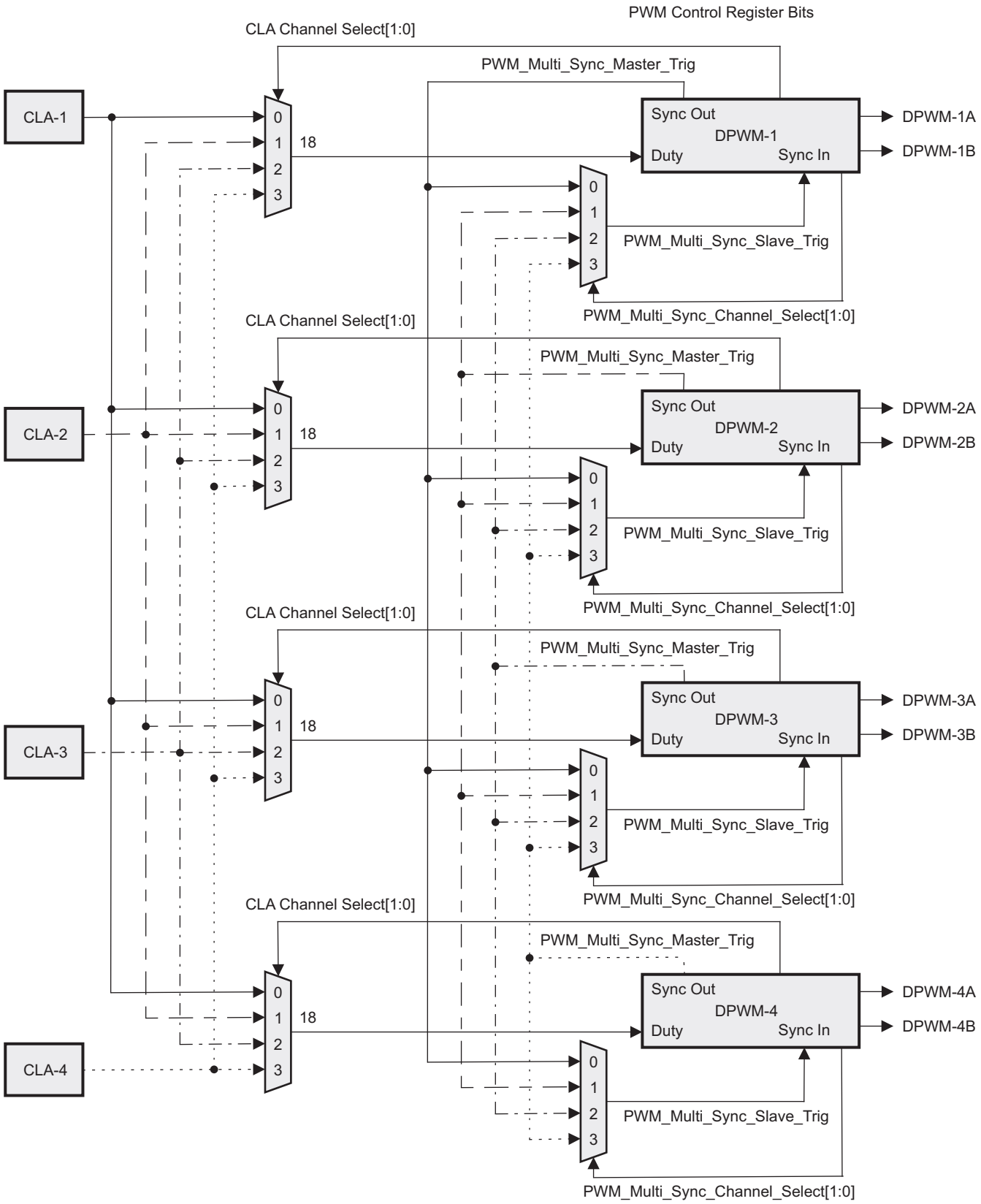


**Figure 14. Multiple DPWMs in the UCD3040**

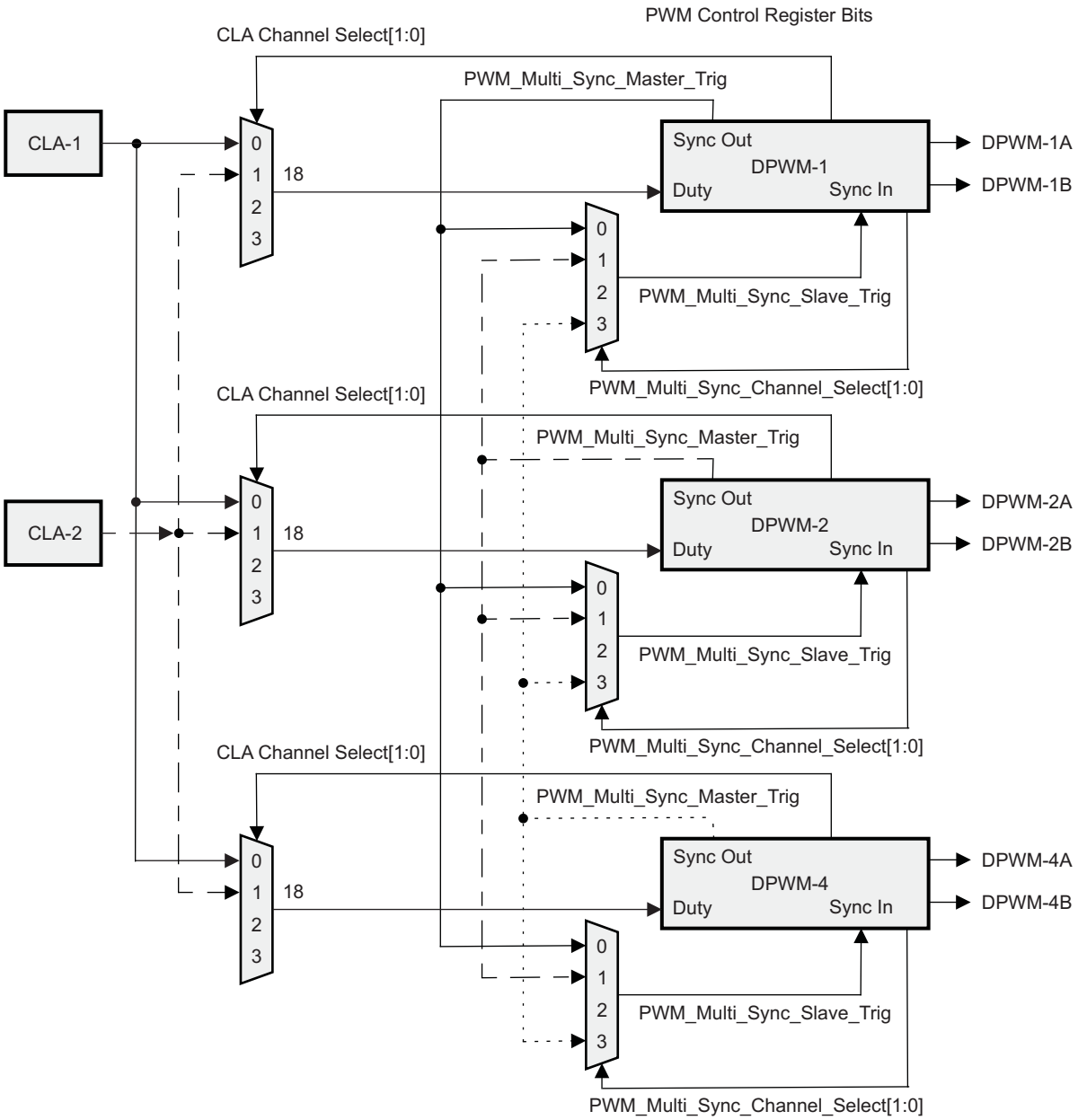


**Figure 15. Multiple DPWMs in the UCD3020**


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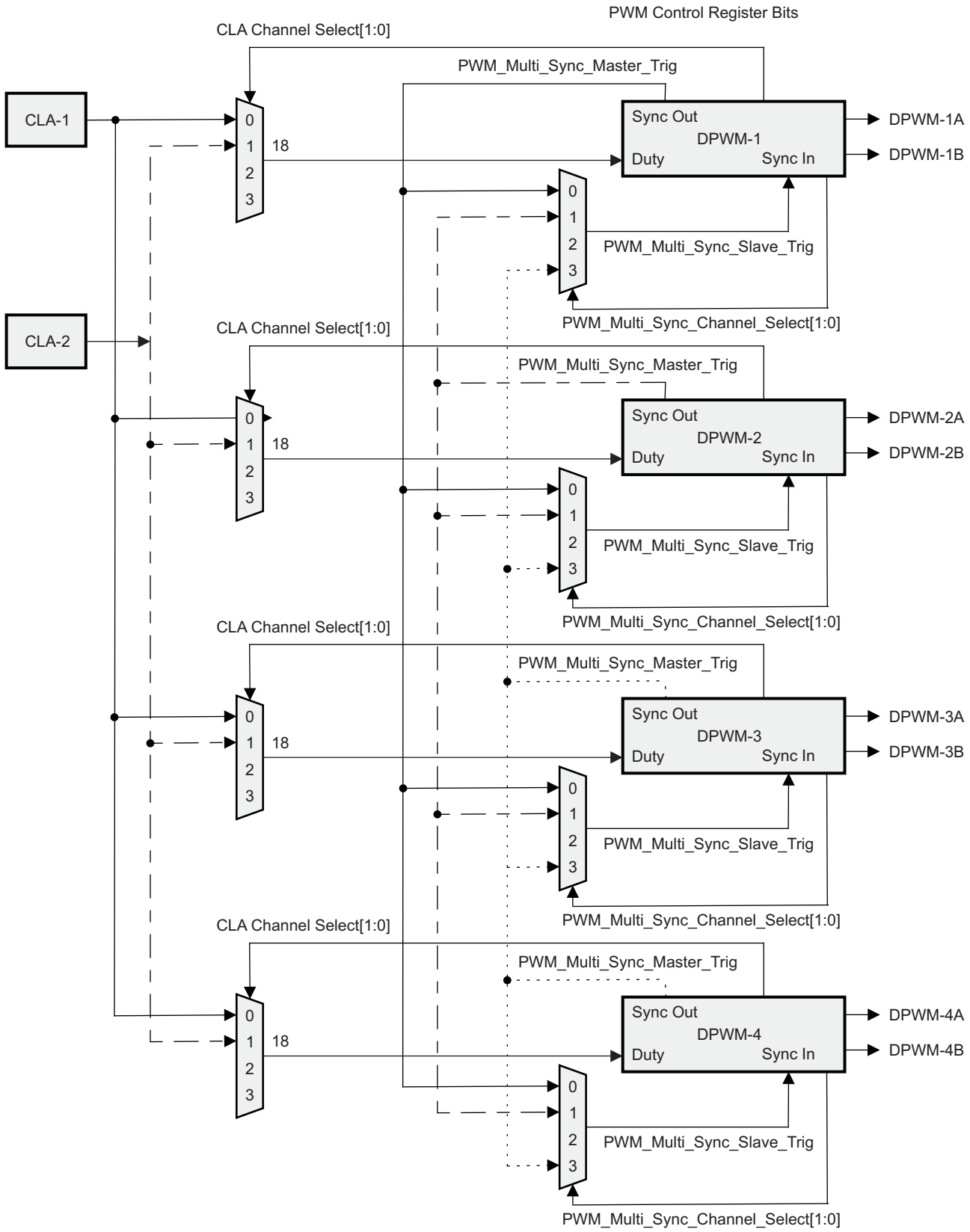


**Figure 16. Multiple DPWMs in the UCD3028**

External Sync Capability

The DPWM can output a sync signal for synchronizing multiple devices, or can sync to an input pin from an external device. The remote-sync slave-enable bit is used for synchronizing the DPWM from an external pin. For generating an output sync signal, the sync-output divide-ratio bits provide a divide-down ratio pulse of the DPWM switching period. In addition, the output sync must be configured in the device as an output source.

## COMMUNICATION PORTS

### SPI

***Programmer's Reference Manual:*** *UCD30xx SPI Module Programmer's Manual*

The four-pin serial-peripheral interface (SPI) port controls the SCLK, SIMO (slave-in, master-out), SOMI (slave-out, master-in) and SPICS (SPI chip-select) external pins. The SPI port can be configured as a master or slave. Capability to control the serial clock phase and polarity can be configured. An 8-bit baud-clock generator is included for selecting slower interface frequencies, as the maximum shift clock is divide-by-2 of the interface clock (ICLK). The transmit and receive buffers have programmable data-word length from 3 to 16 bits. Interrupts can be enabled for transmission-complete or receive-buffer reception. For noninterrupt configurations, transmit and receive flags can be used for control status. When no SPI port is needed, the pins can be configured as GPIO through control bits.

### UART Serial Communication Interface

***Programmer's Reference Manual:*** *UCD30xx UART Module Programmer's Manual*

The universal asynchronous receiver/transmitter (UART) or serial communication interface (SCI) is included within the device for asynchronous start-stop serial data communication. The interface has a 24-bit prescaler for supporting programmable baud rates and has programmable data-word and stop-bit options. Half- or full-duplex operation is configurable through register bits. A loopback feature can also be set up for firmware verification. The SCI-TX and SCI-RX pins can be used as GPIO pins when the peripheral is not being used.

### PMBus

***Programmer's Reference Manual:*** *UCD30xx PMBus Interface Programmer's Manual*

The PMBus interface supports independent master and slave modes controlled directly by firmware through a processor bus interface. Individual control and status registers enable firmware to send or receive $I^2C$, SMBus, or PMBus messages in any of the accepted protocols, in accordance with the $I^2C$ Specification, SMBus Specification (Version 2.0), or PMBus Power System Management Protocol Specification, respectively.

The PMBus I/F is controlled through a processor bus interface, using a 32-bit data bus and 6-bit address bus. The PMBus I/F is connected to the expansion bus, which features four byte-write enables, a peripheral select dedicated for the PMBus I/F, separated 32-bit data buses for reading and writing of data, and active-low write and output-enable control signals. In addition, the PMBus interface connects directly to the $I^2C$/SMBus/PMBus clock, data, alert, and control signals.

### Example: PMBus Address Decode via ADC12 Reading

The user can allocate two pins of 12-bit ADC input channels, AD-00 and AD-01, for PMBus address decoding. At power up, the device applies $I_{BIAS}$ to each address-detect pin, and the voltage on that pin is captured by the internal 12-bit ADC. The PMBus address is calculated as follows:

$$\text{PMBus Address} = 12 \times \text{bin}(V_{AD01}) + \text{bin}(V_{AD00})$$

where $\text{bin}(V_{AD0x})$ is the address bin for one of 12 addresses as shown in Table 6.


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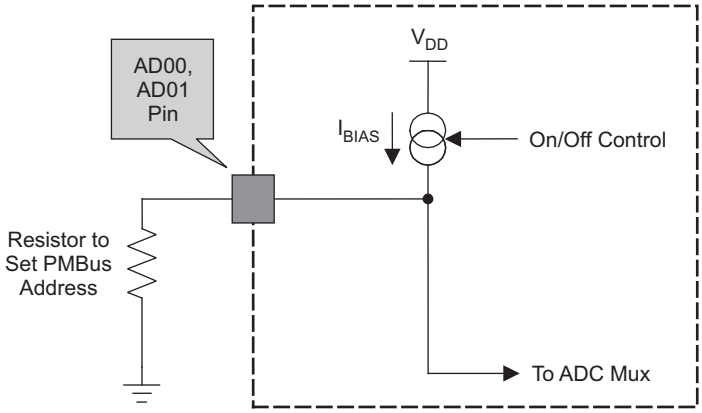


**Figure 17. PMBus Address-Detection Method**

**Table 6. PMBus Address Bins**

| ADDRESS | VOLTAGE, V | RESISTOR, kΩ |
|---|---|---|
| 12 | 2.299 | 209 |
| 11 | 1.815 | 165 |
| 10 | 1.463 | 133 |
| 9 | 1.177 | 107 |
| 8 | 0.953 | 86.6 |
| 7 | 0.749 | 68.1 |
| 6 | 0.604 | 54.9 |
| 5 | 0.486 | 44.2 |
| 4 | 0.383 | 34.8 |
| 3 | 0.308 | 28.0 |
| 2 | 0.249 | 22.6 |
| 1 | 0.196 | 17.8 |
| 0 | 0.157 | 14.3 |

A low impedance (short) on the address pin may produce a voltage below the minimum voltage. Also, a high impedance (open) on the address pin may produce a voltage above the maximum voltage. In these cases, the user may design the system to use a default PMBus address.

## FAULT PORTS/GIO

***Programmer's Reference Manual:*** *UCD30xx Faults and External Interrupts (GIO) Programmer's Manual*

The general-purpose input/output (GIO) ports are for pins that are not associated with any hardware communication port. These bidirectional pins can be configured by firmware to set the pin to a 1 or 0 value as an output signal. Or the bidirectional pins can be read as inputs through memory-map reads for determining the digital value of the pin. Two of the pins, INT1 and INT2, have additional external interrupt capability. These interrupts can be configured for either falling- or rising-edge detection. Interrupts can be enabled or disabled and flags can be monitored for level status.

For naming purposes, all fault input pins are GIO and are typically used in most power-controller applications as fault-input connections.

## TIMERS

***Programmer's Reference Manual:*** *UCD30xx Timer Modules Programmer's Manual*

External to the Fusion Digital Power peripherals, there are three different types of timers in UCD30xx. They are the 24-bit timer, the 16-bit timer, and the watchdog timer.

### PWM 24-Bit Timer

For all UCD30xx devices, there is one 24-bit counter PWM timer which runs off the interface clock and can further be divided down by an 8-bit prescaler to generate a slower PWM time period. The timer has two compare registers (data registers) for generating the PWM set/unset events. This PWM compare output (TCOMPARE) is, however, available only in 80-pin UCD3040. The timer has a shadow register (data-buffer register) which can be used to store CPU updates of the compare events while still using the timer. The selected shadow-register update mode happens after the compare event matches.

The two capture pins TCAP0 and TCAP1 (available only in the 80-pin UCD3040) are inputs for recording a capture event. A capture event can be set either to rising, falling, or both edges of the capture pin. On this event, the counter value is stored in the corresponding capture-data register.

The counter reset can be configured to happen on a counter rollover. Five Interrupts from the PWM timer can be set, which are the counter rollover event (overflow), either capture event 0 or 1, or the two comparison-match events. Each interrupt can be disabled or enabled.

On an event comparison on only the second event, the TCMP pin can be configured to set, clear, toggle, or have no action at the output. The value of the PWM pin output can be read for status or simply configured as general-purpose I/O for reading the value of the input at the pin. The first compare event can only be used as an interrupt.

### PWM 16-Bit Timers

For all UCD30xx devices, there are four 16-bit counter PWM timers which run off the interface clock and can further be divided down by an 8-bit prescaler to generate slower PWM time periods. Each timer has two compare registers (data registers) for generating the PWM set/unset events. The number of such PWM outputs varies between different UCD30xx devices. For details, check the related pin description table. Each 16-bit timer has a shadow register (data-buffer register) which can be used to store CPU updates of compare events while still using the timer. The selected shadow-register update mode happens after the compare event matches.

The counter reset can be configured to happen on a counter rollover, on a compare-equal event, or by a software-controlled register. Interrupts from the PWM timer can be set due to the counter rollover event, called an overflow, or by the two comparison-match events. Each comparison match and the overflow interrupts can be disabled or enabled.

On an event comparison, the PWM pin can be configured to set, clear, toggle, or have no action at the output. The value of the PWM pin output can be read for status or simply configured as general-purpose I/O for reading the value of the input at the pin.

### Watchdog Timer

A watchdog timer is provided on the device for ensuring proper firmware loop execution. The timer is clocked from a separate low-speed oscillator source for providing a timeout range between 10 ms and 1.3 seconds. If the timer is allowed to expire, a reset command is issued to the ARM processor. The watchdog is reset by a simple CPU write bit to the watchdog key register by the firmware routine. On device power up, the watchdog is disabled. Yet after it is enabled, the watchdog cannot be disabled by firmware. Only a device reset can put this bit back to the default disabled state. A half-timer flag is also provided for status monitoring of the watchdog.

## ADC12 MODULE

***Programmer's Reference Manual:*** *UCD30xx General Purpose 12-bit ADC (ADC12) Programmer's Manual*

The 12-bit ADC in the UCD30xx is controlled by a state machine that generates the necessary control signals for the successive-approximation register (SAR) ADC operation. The binary search algorithm, sampling time, and bit timing are controlled by the logic for converging on the input analog signal and generating the 12-bit result. The ADC module contains the wrapper and conversion logic for autosequencing a series of ADC conversions. Each sequence has the choice of selecting any one of the 32 input channels, external and internal, available through an analog multiplexer to the ADC. Once converted, the selected channel value is stored in the appropriate result register. Input channels can be sampled in any desired order or programmed to repeat the same channel multiple times during a conversion sequence. Selected channel conversions are also stored in the result registers in time order, where result 0 is the first conversion of a session and result 15 is the last. The maximum number of conversions that can be programmed in an autosequenced session is 16.


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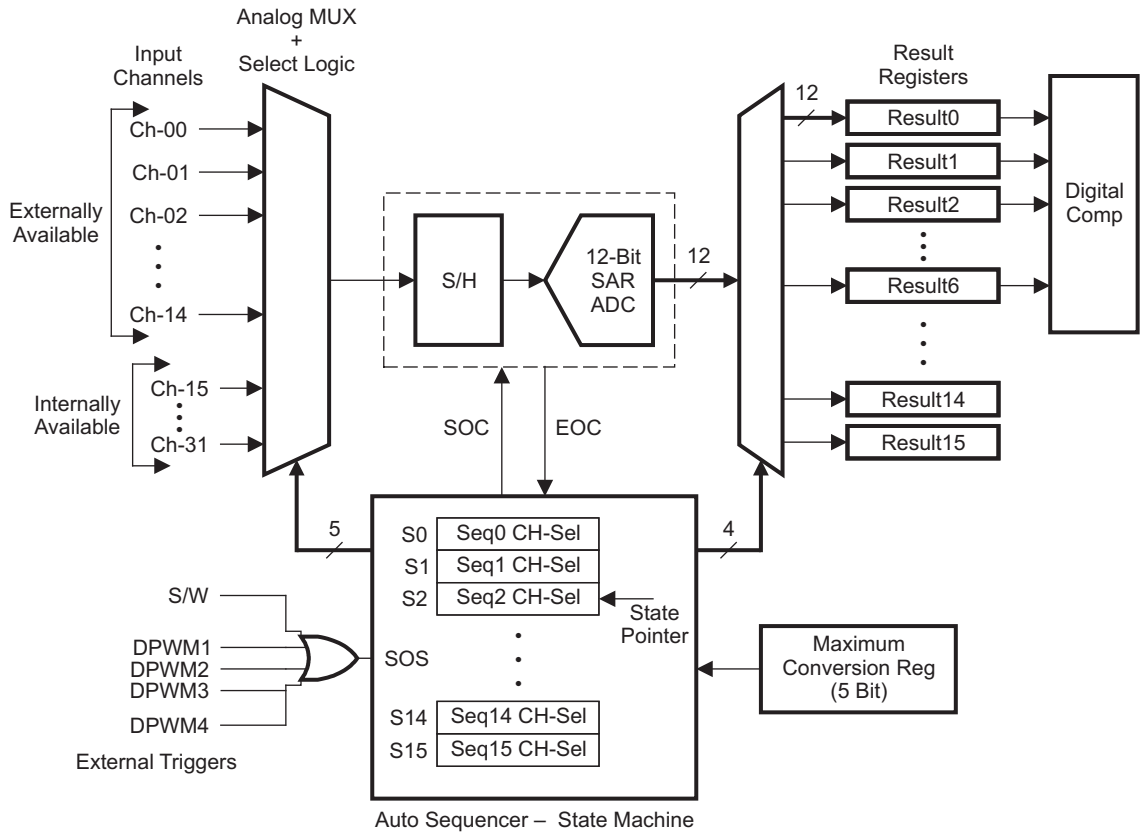


**Figure 18. 12-Bit ADC Module**

### Sequencer

The state sequencer can *autosequence* up to 16 conversions of any channel in a single sequencing session. The result of each conversion is stored in a 16-word result buffer. The desired input channel for each sequenced conversion is programmed in the channel-select sequence registers. So, each channel-select sequence register can be programmed with any of the 32 analog channel inputs to the ADC. The sequence always starts with the programmed channel input in the first channel-select sequence register and progresses to the next channel-select sequence register until the maximum-count register value is reached. The maximum-count register defines the number of conversions in the sequence. Each of the five-bit channel-selection fields can be programmed with any channel. Also, the same channel may be selected multiple times.

The sequencer can be triggered by the CPU or by external trigger sources. The external trigger sources are the DPWM module A and B outputs. Additionally, the sequence can be set up to perform one single-sweep sequence or continually start the sequence on the external trigger source. The sequencer can be enabled to generate a CPU interrupt at the end of the sequence. The end-of-sequence can also be determined by polling the latched-sequence-complete indication bit. This indication bit is cleared on read to ensure a valid complete status.

### Channel Mapping

The ADC12 is used to measure both internal and external voltage signals. Table 7 shows the mapping between external/internal analog inputs and the ADC12 converter. The 32 inputs to the ADC12 are referred to by channel numbers. Fifteen of the channels are connected to external pins. The remaining channels are internal and not available to the user. These are used to convert the internal temperature reference and various test signals.

### PMBus Address Detection

The PMBus needs six address bits to uniquely identify devices on the bus, where two physical ADC pins have been assigned to decode the address. Thus, each pin is capable of resolving one of eight possible states for decoding three bits. For address detection, the 10-µA current sources must be enabled in the PMBUS trim register for driving current out of channels 0 and 1. Where resistors are connected to ground for producing a voltage in the range from 0.25 V to 2 V, resulting in 0.25 V-per-address-bit steps. Grounded inputs or open pins then result in nonvalid states. Then an ADC conversion can be performed on those channels for detecting the address. The resistor values shown in the table are 1% EIA standard values.

| RESISTOR VALUE | PIN VOLTAGE | Addr. VALUE |
|---|---|---|
| Open | Vdd | Invalid |
| 200 kΩ | 2 V | 111 |
| 174 kΩ | 1.74 V | 110 |
| 150 kΩ | 1.5 V | 101 |
| 124 kΩ | 1.24V | 100 |
| 100 kΩ | 1 V | 011 |
| 75 kΩ | 0.75 V | 010 |
| 49.9 kΩ | 0.5 V | 001 |
| 24.9 kΩ | 0.25 V | 000 |
| Ground | 0 V | Invalid |

**Table 7. Analog Input Mapping to ADC12**

| CHANNEL NO. | INTERNAL/EXTERNAL SIGNALS | DESCRIPTION |
|---|---|---|
| Ch-31 | AD-15 | Loop 4 test signals |
| Ch-30 | AD-15 | |
| Ch-29 | AD-15 | |
| Ch-28 | AD-15 | |
| Ch-27 | AD-15 | Loop 3 test signals |
| Ch-26 | AD-15 | |
| Ch-25 | AD-15 | |
| Ch-24 | AD-15 | |
| Ch-23 | AD-15 | Loop 2 test signals |
| Ch-22 | AD-15 | |
| Ch-21 | AD-15 | |
| Ch-20 | AD-15 | |
| Ch-19 | AD-15 | Loop 1 test signals |
| Ch-18 | AD-15 | |
| Ch-17 | AD-15 | |
| Ch-16 | AD-15 | |
| Ch-15 | Temp sensor | Internal temperature sensor |
| Ch-14 | AD-14 | GP analog input to ADC12 |
| Ch-13 | AD-13 | GP analog input to ADC12 |
| Ch-12 | AD-12 | GP analog input to ADC12 |
| Ch-11 | AD-11 | GP analog input to ADC12 |
| Ch-10 | AD-10 | GP analog input to ADC12 |
| Ch-9 | AD-09 | GP analog input to ADC12 |
| Ch-8 | AD-08 | GP analog input to ADC12 |
| Ch-7 | AD-07 | GP analog input to ADC12 |
| Ch-6 | AD-06 | GP analog input to ADC12 |
| Ch-5 | AD-05 | GP analog input to ADC12 |


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**Table 7. Analog Input Mapping to ADC12 (continued)**

| CHANNEL NO. | INTERNAL/EXTERNAL SIGNALS | DESCRIPTION |
|---|---|---|
| Ch-4 | AD-04 | GP analog input to ADC12 |
| Ch-3 | AD-03 | GP analog input to ADC12 |
| Ch-2 | AD-02 | GP analog input to ADC12 |
| Ch-1 | AD-01 | PMBus addr ID #2 or GP analog input |
| Ch-0 | AD-00 | PMBus addr ID #1 or GP analog input |

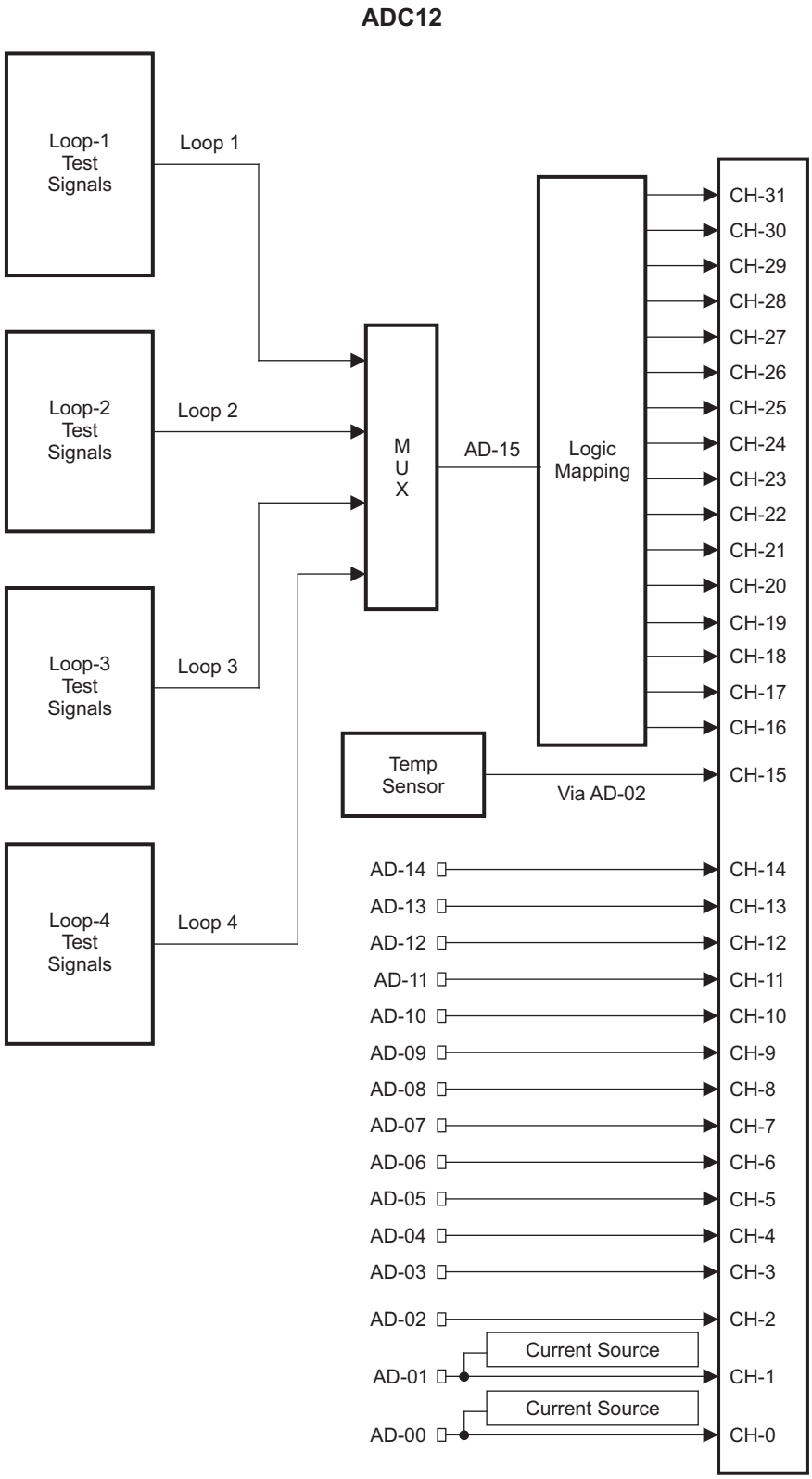


**Figure 19. External Analog Input Pin and Internal Connections to ADC12**


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### Digital Comparators

The ADC wrapper logic has digital comparators that can be used to compare the result registers against programmed high and low limits. The first six conversion result registers (Result 0–Result 5) of the ADC sequence are the ADC results having digital comparator functionality. Therefore, for any signals requiring auto limit monitoring, the user must use these six ADC conversion slots for monitoring of those signals. All 12 bits of conversion result are used for comparison. The digital-comparator logic provides 12 status bits for monitoring, two from each ADC result comparison. These status bits indicate whether the ADC result is higher than or equal to the limit-high register setting, or is lower than or equal to the limit-low register setting.

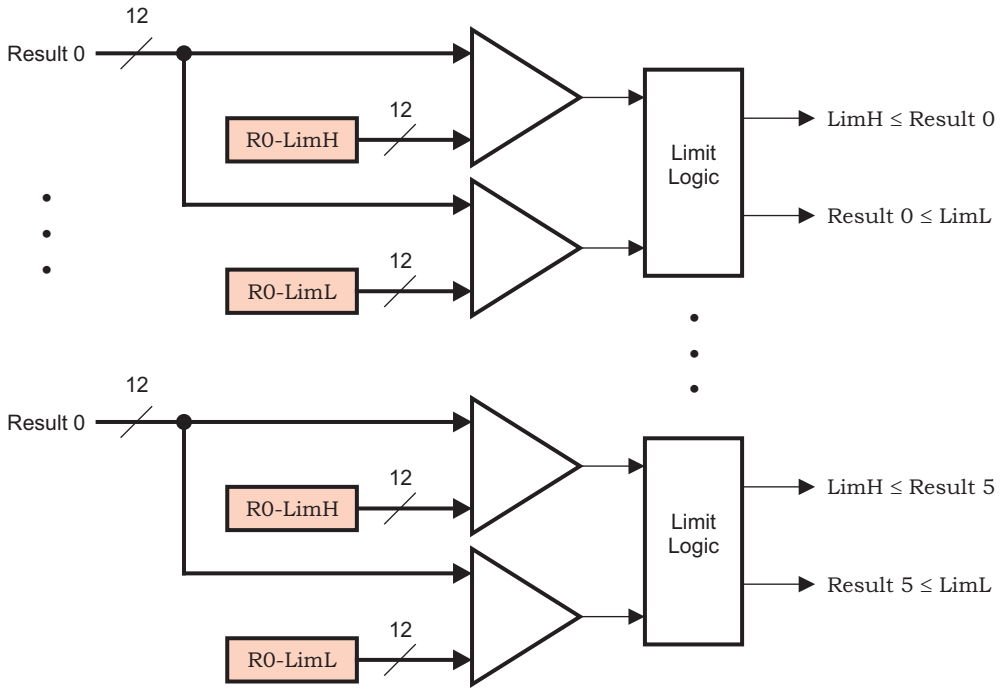


**Figure 20. Digital Comparators**

## MISCELLANEOUS ANALOG

***Programmer's Reference Manual:*** *UCD30xx Miscellaneous Analog Control (MAC) Programmer's Manual*

### Power-On Reset (POR)/Brownout Detect (BOD)

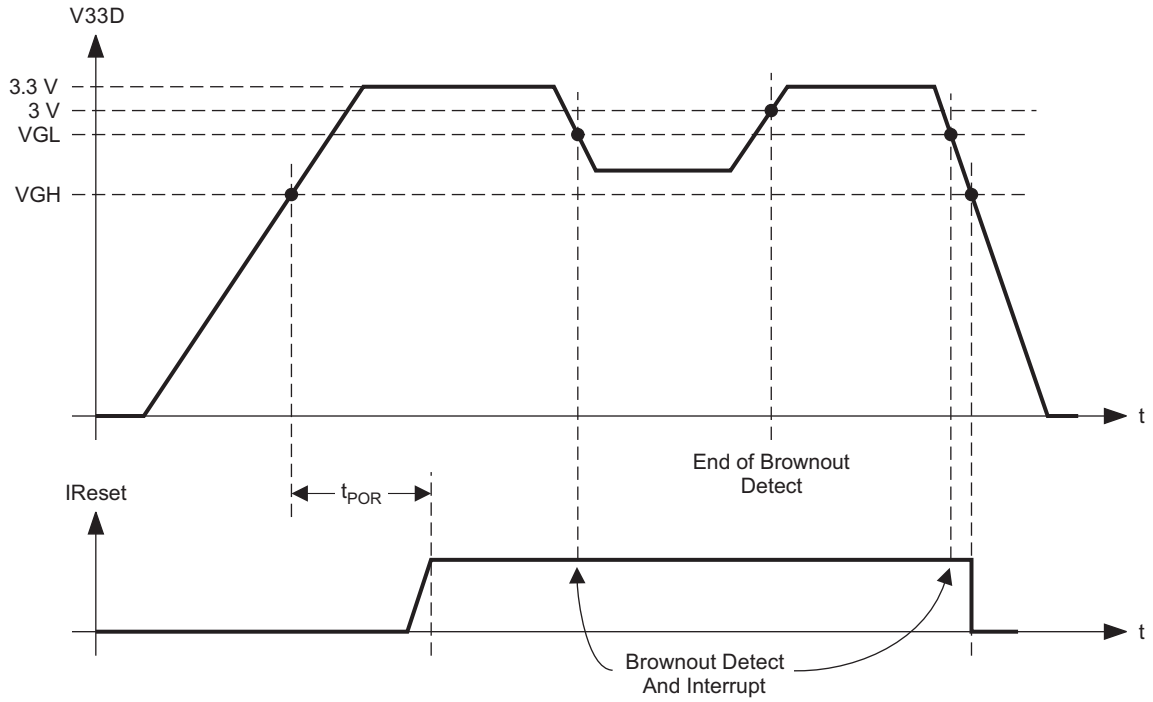


**Figure 21. Power-On Reset (POR)/Brownout Detect (BOD) Timing Diagram**

**Table 8. POR/BOD Limits**

| PARAMETER | | VALUE |
|---|---|---|
| **VGH** | Voltage-good High | 2.4 V |
| **VGL** | Voltage-good Low | 2.9 V |
| **$t_{POR}$** | Time delay after power is good or $\overline{\text{RESET}}$ relinquished | 1 ms |
| **IReset** | Internal reset signal used by CPU core and all logic | |


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The device is held in reset until the 3.3-V supply (V33D) is in the range of 2.1 V to 2.4 V. At 2.4 V, a POR is triggered. The brownout detection is set for 2.9 V, at which level an interrupt is sent to the microprocessor for doing any power-down housekeeping.

## Analog Comparators

### *Analog Comparator Connections*

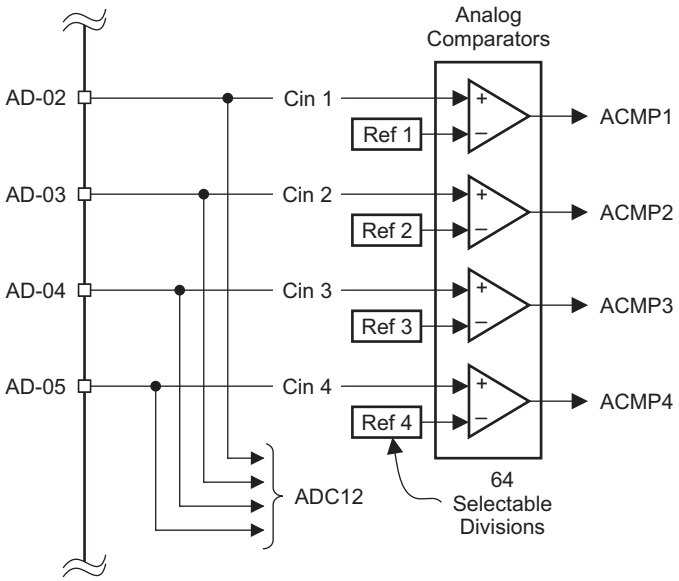


**Figure 22. Analog Comparator Connections**

There are four analog comparators that can compare an internal voltage reference to an external output pin voltage. The external pins are common with the general purpose ADC12 pins AD-02 through AD-05. The analog comparator reference voltages are programmable independently between 0 V and 2 V. Each programmable reference is controlled by the microprocessor for setting up each 6-bit digital register value. This allows for $2^6$ steps or 3.125-mV (2 V/64) step sizes during programming of the comparator reference voltage.

### *Analog Comparator Actions/Usage*

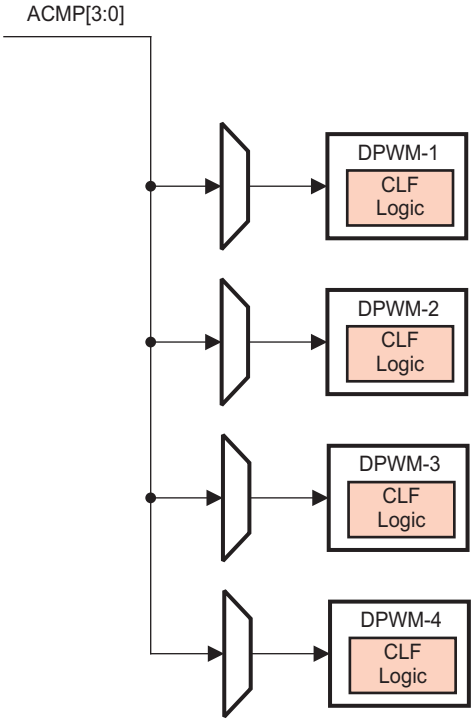


**Figure 23. Analog Comparator Usage**

The four analog comparator outputs are routed through a multiplexer for routing one of the comparator outputs to the current-limit flag (CLF) input of a DPWM. Each DPWM CLF input source from the multiplexer can be programmed by the CPU.


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### Internal Temperature Sensor

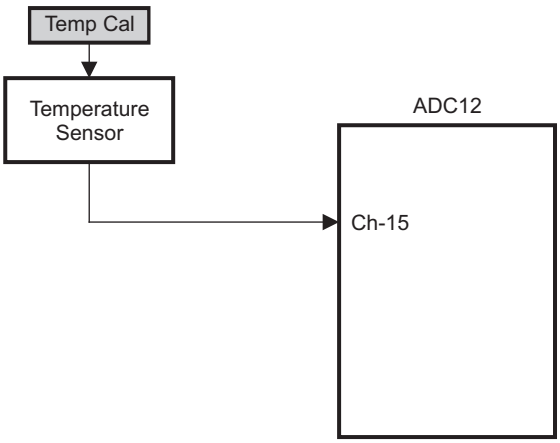


**Figure 24. Internal Temperature Sensor**

The temperature sensor is calibrated at room temperature (25°C) via a calibration register value.

The temperature sensor output is measured using an internal channel (Ch15) of the 12-bit ADC (ADC12). This temperature sensing is internal for all UCD30xx devices. The sensed temperature is then calculated using a mathematical formula involving the calibration register (this effectively adds an offset to the ADC measurement). Thus, the temperature sensor output voltage, at any temperature T, is calculated from:

$V(T) = 1.717 + [T – 25] \times 5.93 \times 10^{-3} + V_{offset}$, where T is in °C.

The temperature sensor can be enabled or disabled.

**Table 9. Temperature Sensor Limits**

| | | |
|---|---|---|
| **$V_{TEMP}$** | Voltage range of sensor | 1.347 V to 2.326 V |
| **Voltage resolution** | Volts/°C. | 5.93 mV/°C |
| **Temperature resolution** | Degree C per bit | 0.7°C / bit |
| **Temperature range** | –40°C to 125°C | –40°C to 125°C |
| **$I_{TEMP}$** | Current draw of sensor when active | 30 µA |
| **$t_{ON}$** | Turn-on time/settling time of sensor | 100 µs |
| **Vroom temperature** | Trimmed 25°C reading | 1.717 V |

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### Internal Voltage Regulators

The internal 1.8-V regulator requires an external capacitor on the BPCAP pin of the device. The value of this capacitor ranges from 1 µF to 4.7 µF.

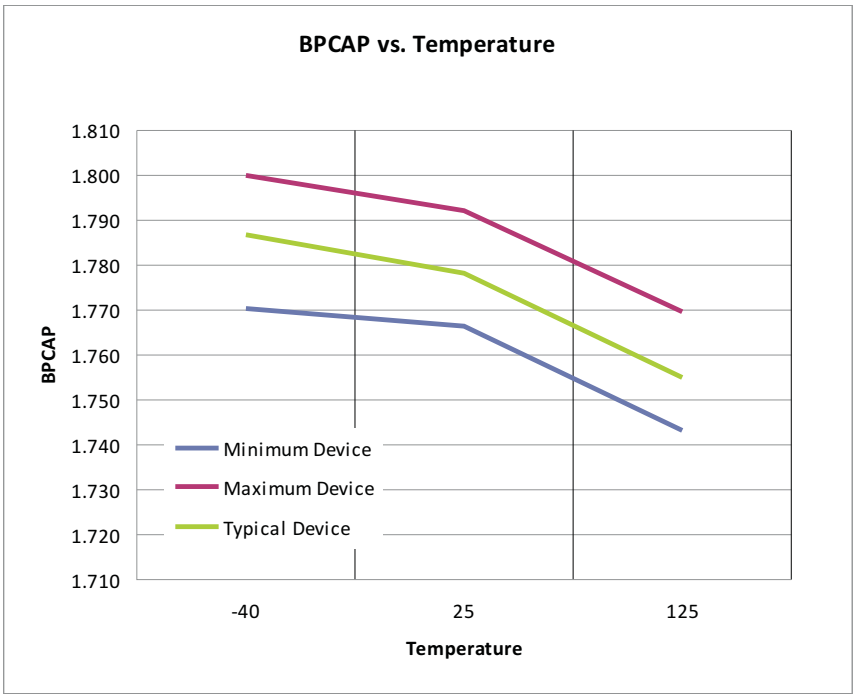


**Figure 25. BPCAP vs. Temperature**


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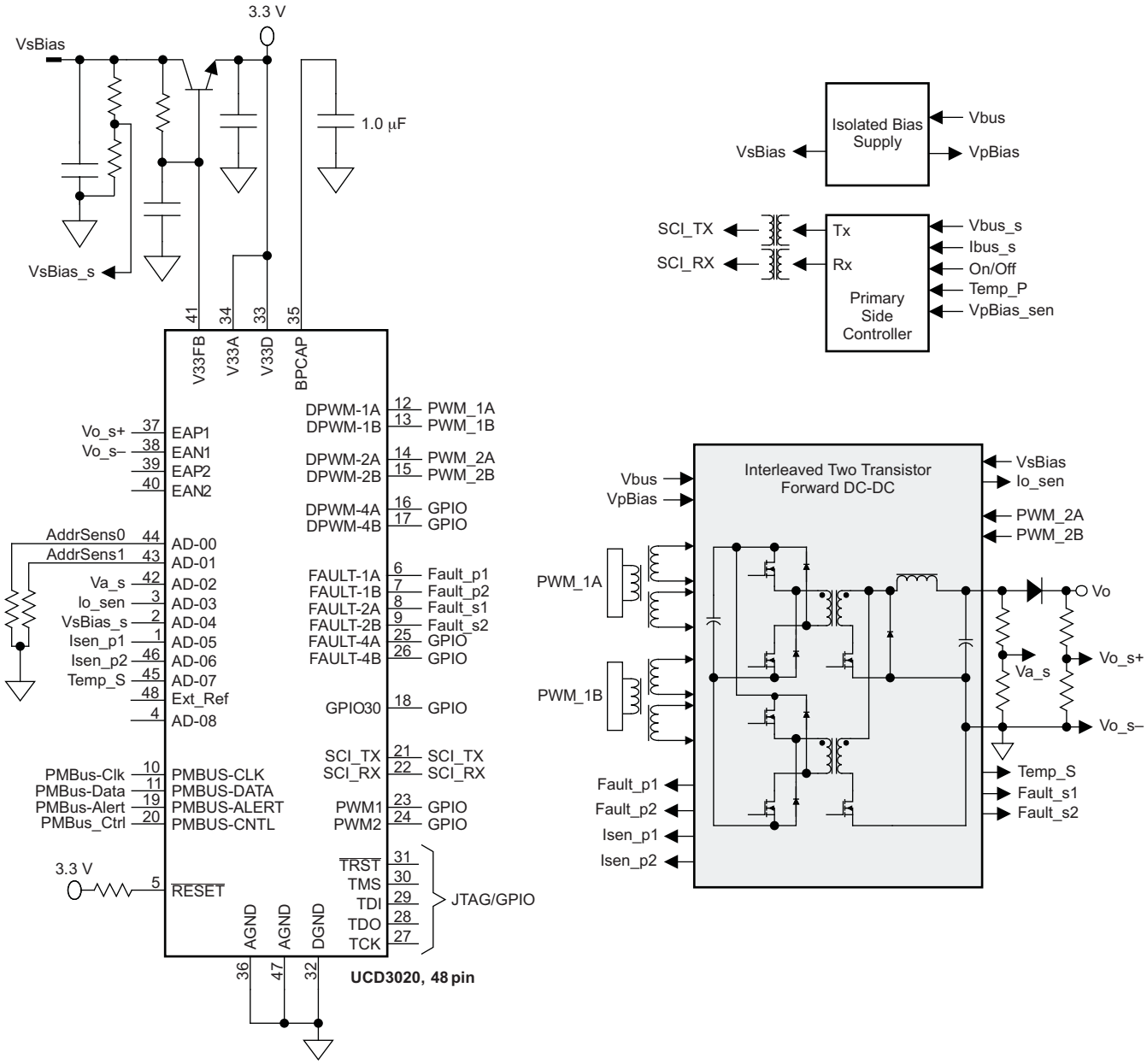
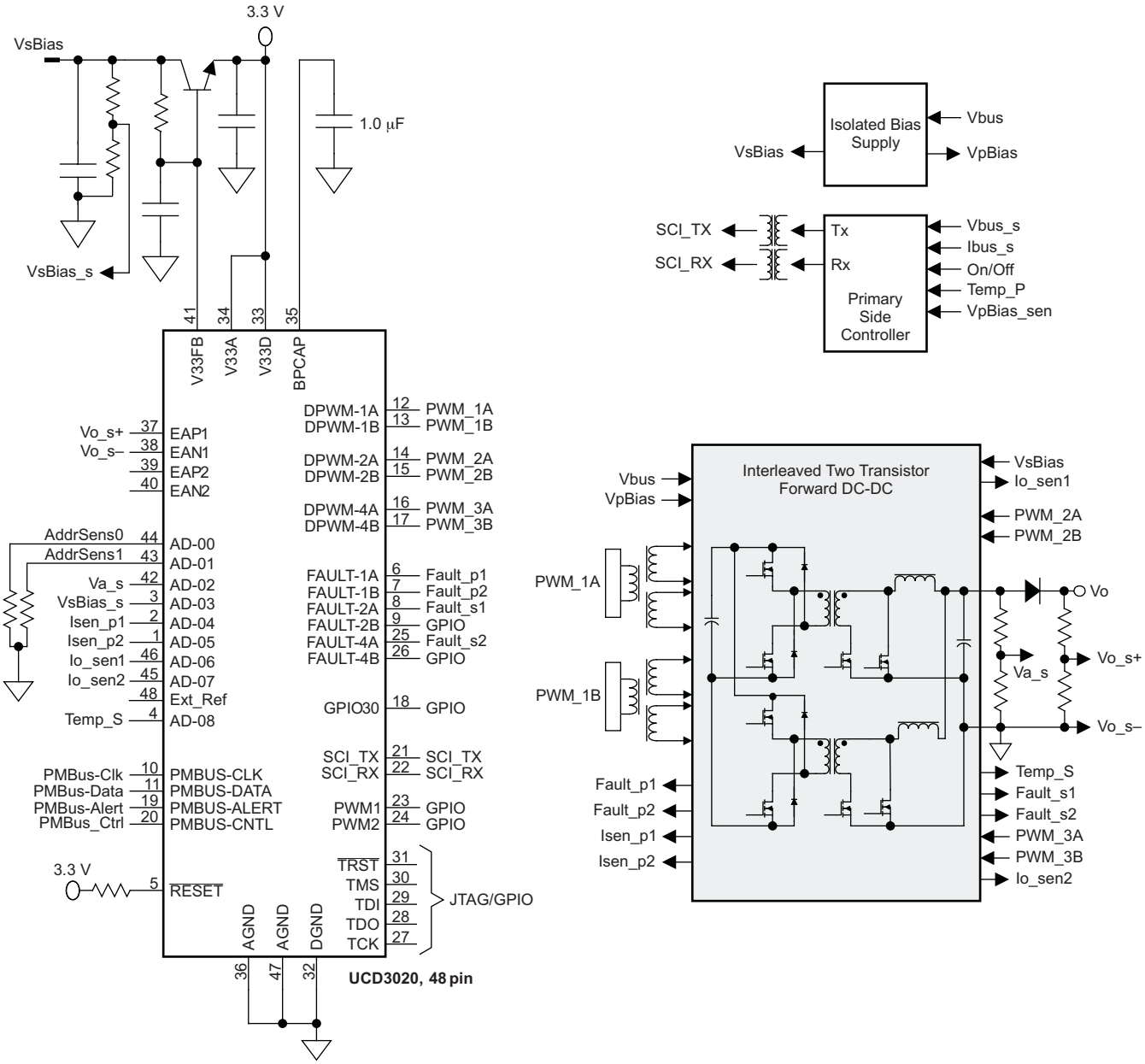
# APPLICATION INFORMATION

## TYPICAL APPLICATION SCHEMATICS

### Example 1: Secondary-Referenced Interleaved Two-Transistor Forward



### Example 2: Secondary-Referenced Interleaved Two-Transistor Forward With Synchronous Rectification





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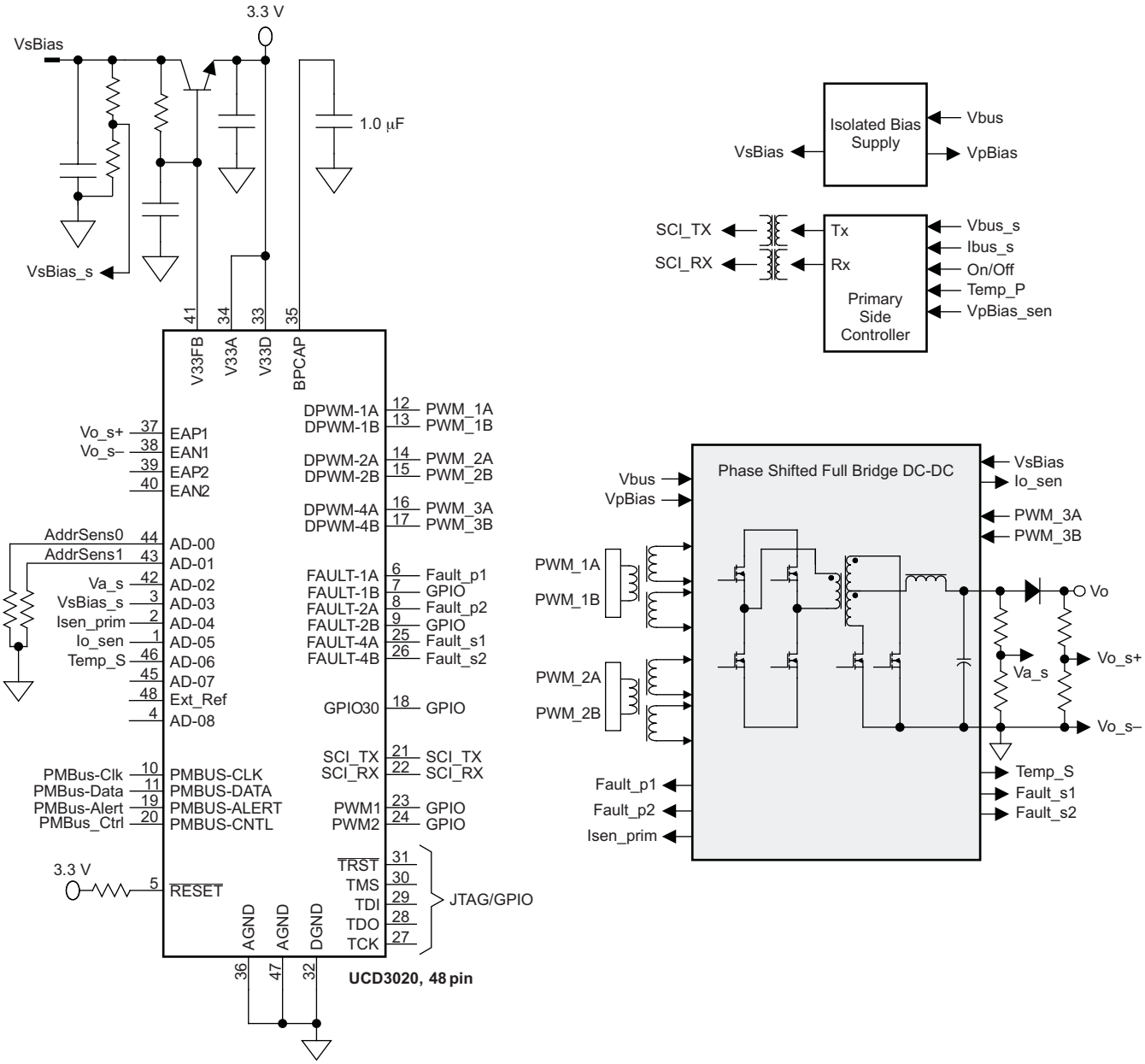
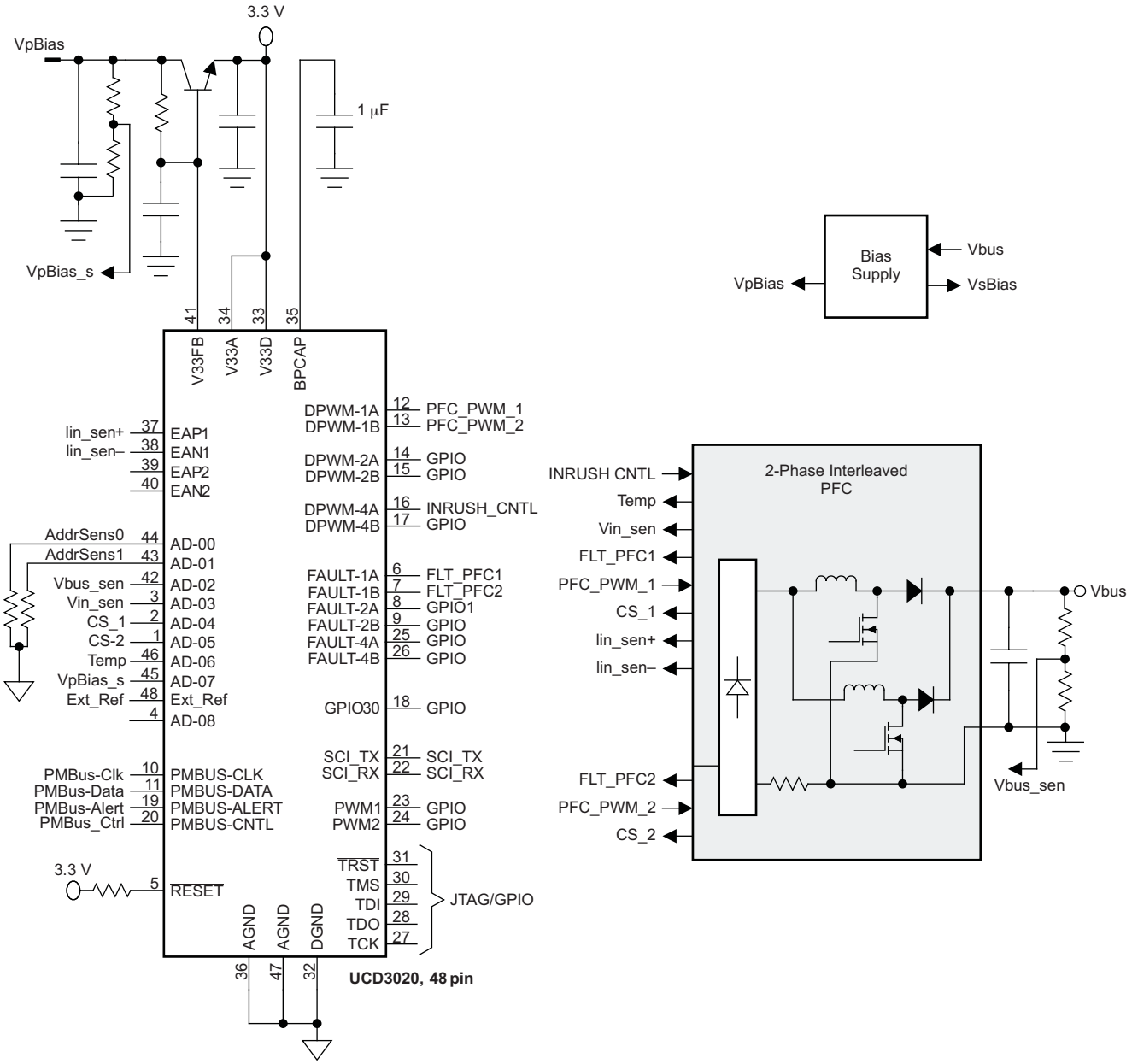
### Example 3: Secondary-Referenced Phase-Shifted Full Bridge With Synchronous Rectification



### Example 4: Primary-Side Two-Phase Interleaved Power-Factor Correction Control





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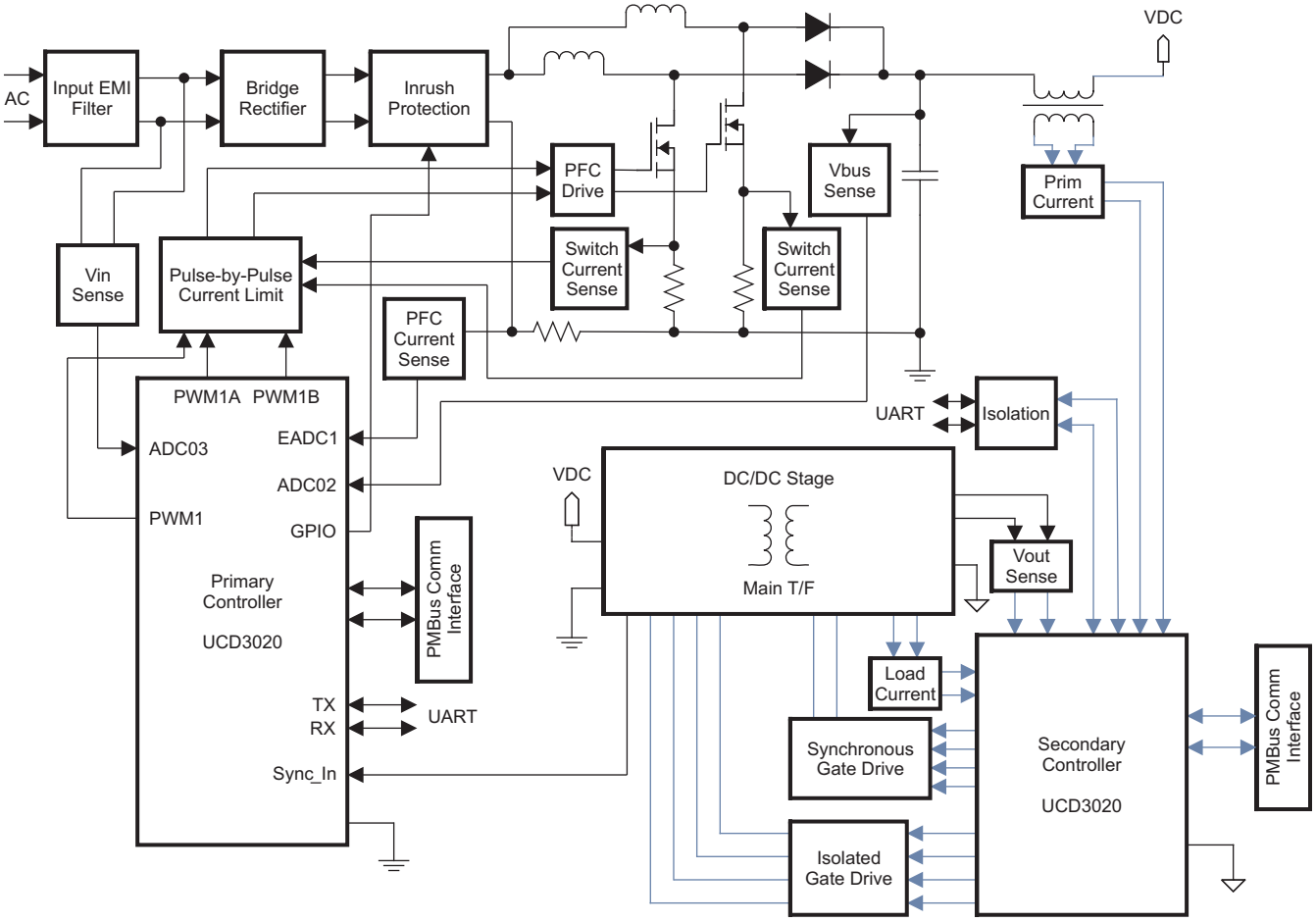
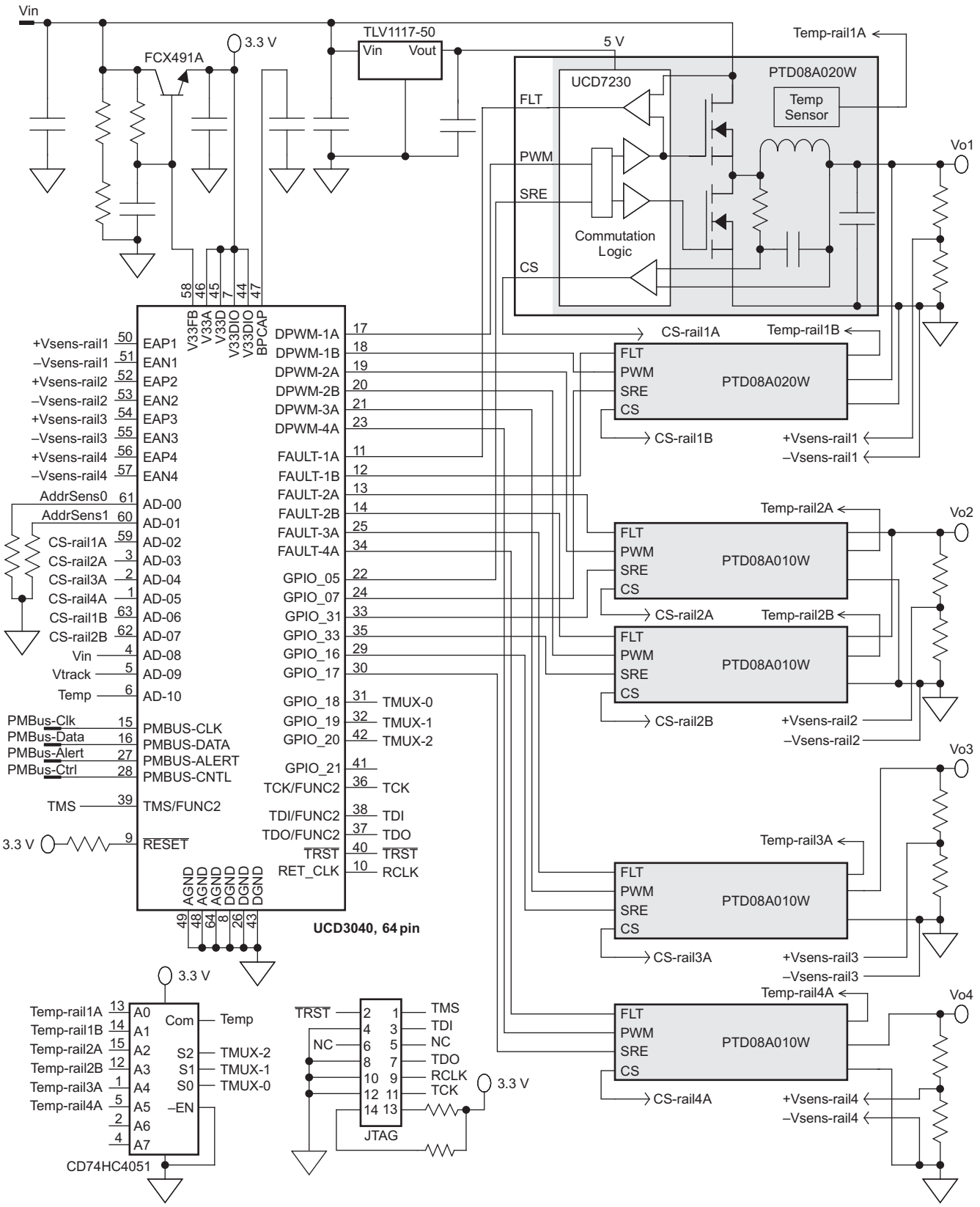
### Example 5: AC/DC Power System Block Diagram




### Example 6: Nonisolated Multiphase DC/DC Converter Control (UCD3040, 64-Pin)

The application diagram for Example 6 shows the UCD3040 power-supply controller working in a system which requires the regulation of four independent power supplies. The first and second outputs have a 2-phase configuration while the third and fourth have single-phase configuration. The loop for each power supply is created by the voltage outputs feeding into the error ADC differential inputs, and completed by DPWM outputs feeding into separate power modules.





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## REFERENCE MANUALS

In this section a list of other supporting manuals for the UCD30xx controllers is provided. Contact your local TI representative for a copy of these manuals.

UCD30xx Programmer's Manuals

1. UCD30xx Memory Controller (MMC) Programmer's Manual
2. UCD30xx Central Interrupt Module (CIM) Programmer's Manual
3. UCD30xx System Module (SYS) Programmer's Manual
4. UCD30xx Memory Address Manager (DEC) Programmer's Manual
5. UCD30xx Fusion Digital Power Peripherals Programmer's Manual
6. UCD30xx General-Purpose 12-Bit ADC (ADC12) Programmer's Manual
7. UCD30xx PMBus Interface Programmer's Manual
8. UCD30xx UART Module Programmer's Manual
9. UCD30xx SPI Module Programmer's Manual
10. UCD30xx Miscellaneous Analog Control (MAC) Programmer's Manual
11. UCD30xx Timer Modules Programmer's Manual
12. UCD30xx Faults and External Interrupts (GIO) Programmer's Manual
13. UCD30xx General Purpose I/O (GPIO) Programmer's Manual
14. UCD30xx Boot ROM Reference Manual

## REVISION HISTORY

| Changes from Revision D (February 2012) to Revision E | Page |
|---|---|
| • Changed Voltage applied at V33D to DVss max value from 3.6 to 3.8. | 19 |
| • Added BPCAP data to the EC table. | 21 |
| • Added BPCAP vs. Temperature graph to the Internal Voltage Regulators section. | 60 |

| Changes from Revision E (February 2013) to Revision F | Page |
|---|---|
| • Changed Error signal/detect values. | 23 |
| • Changed Cumulative clock low slave extend time values. | 23 |

| Changes from Revision F (March 2013) to Revision G | Page |
|---|---|
| • Changed BPCAP I?O assignment. | 13 |
| • Changed BPCAP I/O assignment. | 15 |
| • Changed TEST, pin descriptin. | 18 |
| • Added ABSOLUTE MAXIMUM RATINGS for BPCAP. | 19 |
| • Added RECOMMENDED OPERATING CONDITIONS for BPCAP. | 19 |
| • Changed TYPICAL APPLICATION SCHEMATICS. | 61 |

| Changes from Revision G (April 2013) to Revision H | Page |
|---|---|
| • Added 40-Pin QFN (RHA and RMH) Package Offerings. | 1 |
| • Added UCD3028RMHR and UCD3028RMHT packaging information. | 2 |
| • Changed top side markings from UCD3020 to 3020RMH in two places. | 2 |
| • Added corner anchor pin information. | 18 |
| • Added External reference input package availability. | 21 |

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## PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| UCD3020RGZR | Active | Production | VQFN (RGZ) \| 48 | 2500 \| LARGE T&R | Yes | FULL NIPDAU \| NIPDAU | Level-3-260C-168 HR | -40 to 125 | UCD3020 |
| UCD3020RGZR.A | Active | Production | VQFN (RGZ) \| 48 | 2500 \| LARGE T&R | Yes | FULL NIPDAU | Level-3-260C-168 HR | -40 to 125 | UCD3020 |
| UCD3020RGZT | Active | Production | VQFN (RGZ) \| 48 | 250 \| SMALL T&R | Yes | FULL NIPDAU \| NIPDAU | Level-3-260C-168 HR | -40 to 125 | UCD3020 |
| UCD3020RGZT.A | Active | Production | VQFN (RGZ) \| 48 | 250 \| SMALL T&R | Yes | FULL NIPDAU | Level-3-260C-168 HR | -40 to 125 | UCD3020 |
| UCD3028RHAR | Active | Production | VQFN (RHA) \| 40 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | UCD3028 |
| UCD3028RHAR.A | Active | Production | VQFN (RHA) \| 40 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | UCD3028 |
| UCD3028RHAT | Active | Production | VQFN (RHA) \| 40 | 250 \| SMALL T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | UCD3028 |
| UCD3028RHAT.A | Active | Production | VQFN (RHA) \| 40 | 250 \| SMALL T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | UCD3028 |
| UCD3040PFC | Active | Production | TQFP (PFC) \| 80 | 96 \| JEDEC TRAY (10+1) | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | UCD 3040 |
| UCD3040PFC.A | Active | Production | TQFP (PFC) \| 80 | 96 \| JEDEC TRAY (10+1) | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | UCD 3040 |
| UCD3040PFCR | Active | Production | TQFP (PFC) \| 80 | 1000 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | UCD 3040 |
| UCD3040PFCR.A | Active | Production | TQFP (PFC) \| 80 | 1000 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | UCD 3040 |
| UCD3040RGCR | Active | Production | VQFN (RGC) \| 64 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-3-260C-168 HR | -40 to 125 | UCD3040 |
| UCD3040RGCR.A | Active | Production | VQFN (RGC) \| 64 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-3-260C-168 HR | -40 to 125 | UCD3040 |
| UCD3040RGCT | Active | Production | VQFN (RGC) \| 64 | 250 \| SMALL T&R | Yes | NIPDAU | Level-3-260C-168 HR | -40 to 125 | UCD3040 |
| UCD3040RGCT.A | Active | Production | VQFN (RGC) \| 64 | 250 \| SMALL T&R | Yes | NIPDAU | Level-3-260C-168 HR | -40 to 125 | UCD3040 |

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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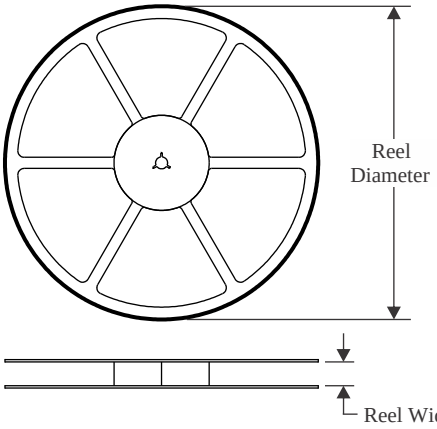
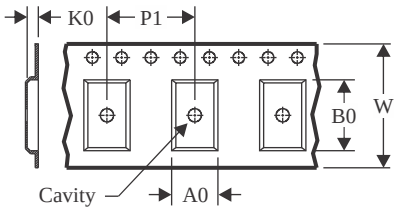
## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

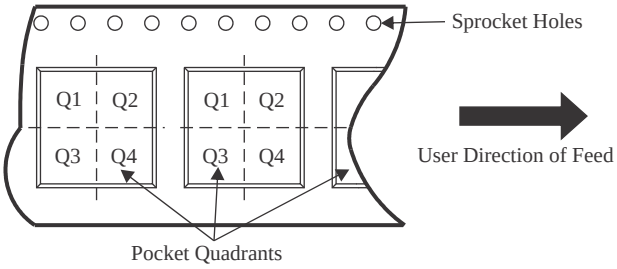



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

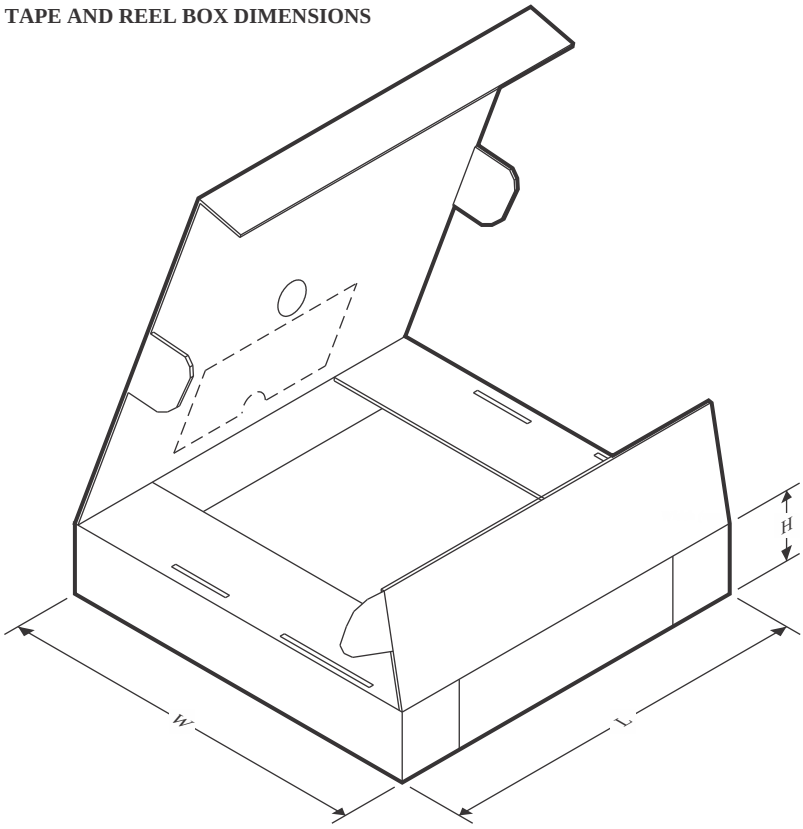
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| UCD3020RGZR | VQFN | RGZ | 48 | 2500 | 330.0 | 16.4 | 7.3 | 7.3 | 1.1 | 12.0 | 16.0 | Q2 |
| UCD3020RGZT | VQFN | RGZ | 48 | 250 | 180.0 | 16.4 | 7.3 | 7.3 | 1.1 | 12.0 | 16.0 | Q2 |
| UCD3028RHAR | VQFN | RHA | 40 | 2500 | 330.0 | 16.4 | 6.3 | 6.3 | 1.1 | 12.0 | 16.0 | Q2 |
| UCD3028RHAR | VQFN | RHA | 40 | 2500 | 330.0 | 16.4 | 6.3 | 6.3 | 1.1 | 12.0 | 16.0 | Q2 |
| UCD3028RHAT | VQFN | RHA | 40 | 250 | 180.0 | 16.4 | 6.3 | 6.3 | 1.1 | 12.0 | 16.0 | Q2 |
| UCD3040PFCR | TQFP | PFC | 80 | 1000 | 330.0 | 24.4 | 15.0 | 15.0 | 1.5 | 20.0 | 24.0 | Q2 |
| UCD3040RGCR | VQFN | RGC | 64 | 2000 | 330.0 | 16.4 | 9.3 | 9.3 | 1.5 | 12.0 | 16.0 | Q2 |
| UCD3040RGCT | VQFN | RGC | 64 | 250 | 180.0 | 16.4 | 9.3 | 9.3 | 1.5 | 12.0 | 16.0 | Q2 |

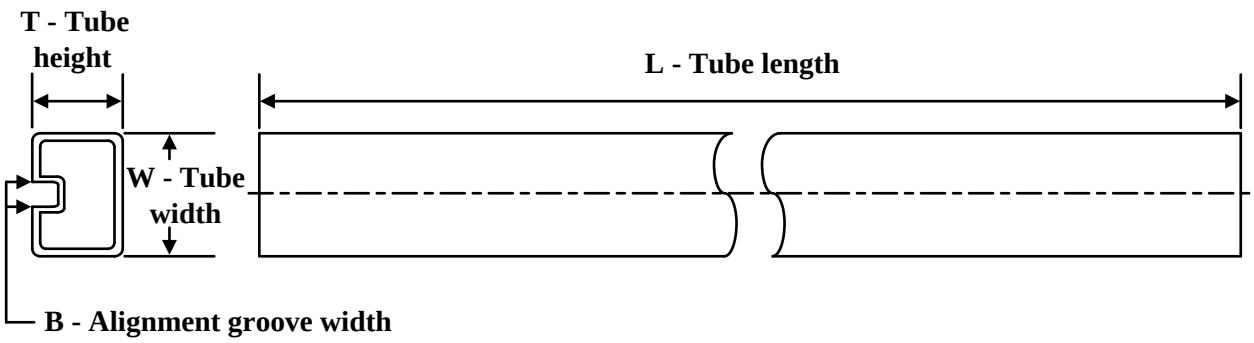
TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| UCD3020RGZR | VQFN | RGZ | 48 | 2500 | 367.0 | 367.0 | 38.0 |
| UCD3020RGZT | VQFN | RGZ | 48 | 250 | 210.0 | 185.0 | 35.0 |
| UCD3028RHAR | VQFN | RHA | 40 | 2500 | 552.0 | 367.0 | 38.0 |
| UCD3028RHAR | VQFN | RHA | 40 | 2500 | 353.0 | 353.0 | 32.0 |
| UCD3028RHAT | VQFN | RHA | 40 | 250 | 210.0 | 185.0 | 35.0 |
| UCD3040PFCR | TQFP | PFC | 80 | 1000 | 350.0 | 350.0 | 43.0 |
| UCD3040RGCR | VQFN | RGC | 64 | 2000 | 353.0 | 353.0 | 32.0 |
| UCD3040RGCT | VQFN | RGC | 64 | 250 | 213.0 | 191.0 | 35.0 |

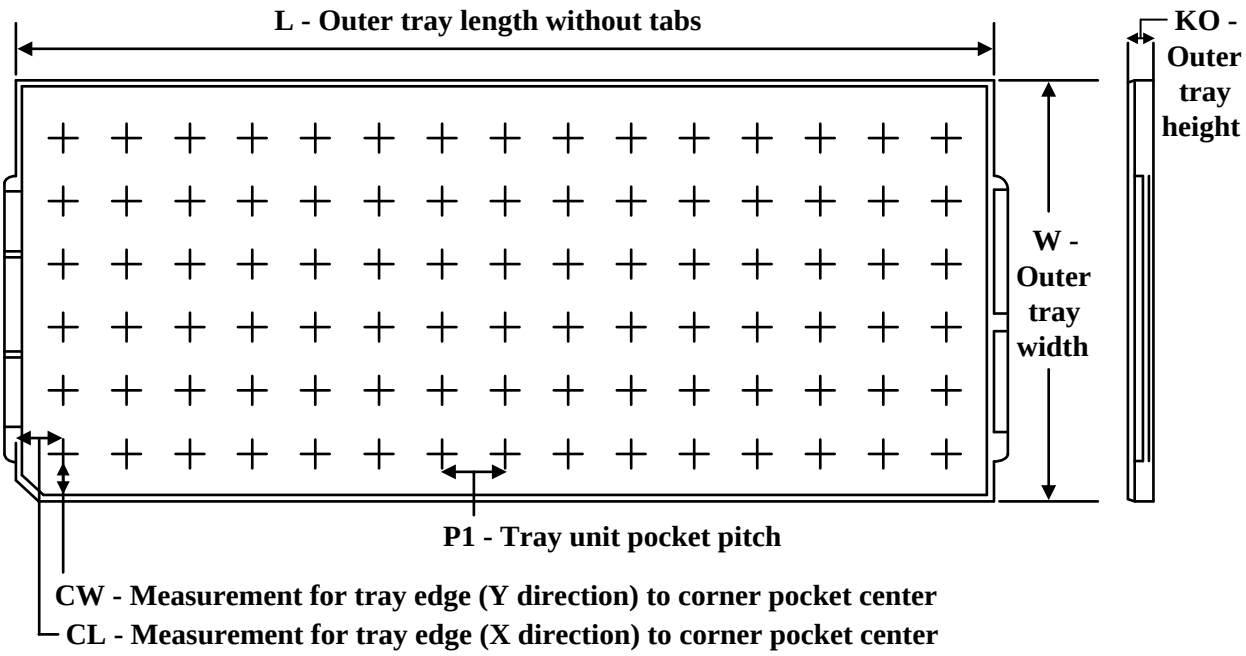
## TUBE




*All dimensions are nominal

| Device | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (µm) | B (mm) |
|---|---|---|---|---|---|---|---|---|
| UCD3028RHAR | RHA | VQFN | 40 | 2500 | 381.5 | 7.92 | 2286 | 0 |
| UCD3028RHAR.A | RHA | VQFN | 40 | 2500 | 381.5 | 7.92 | 2286 | 0 |

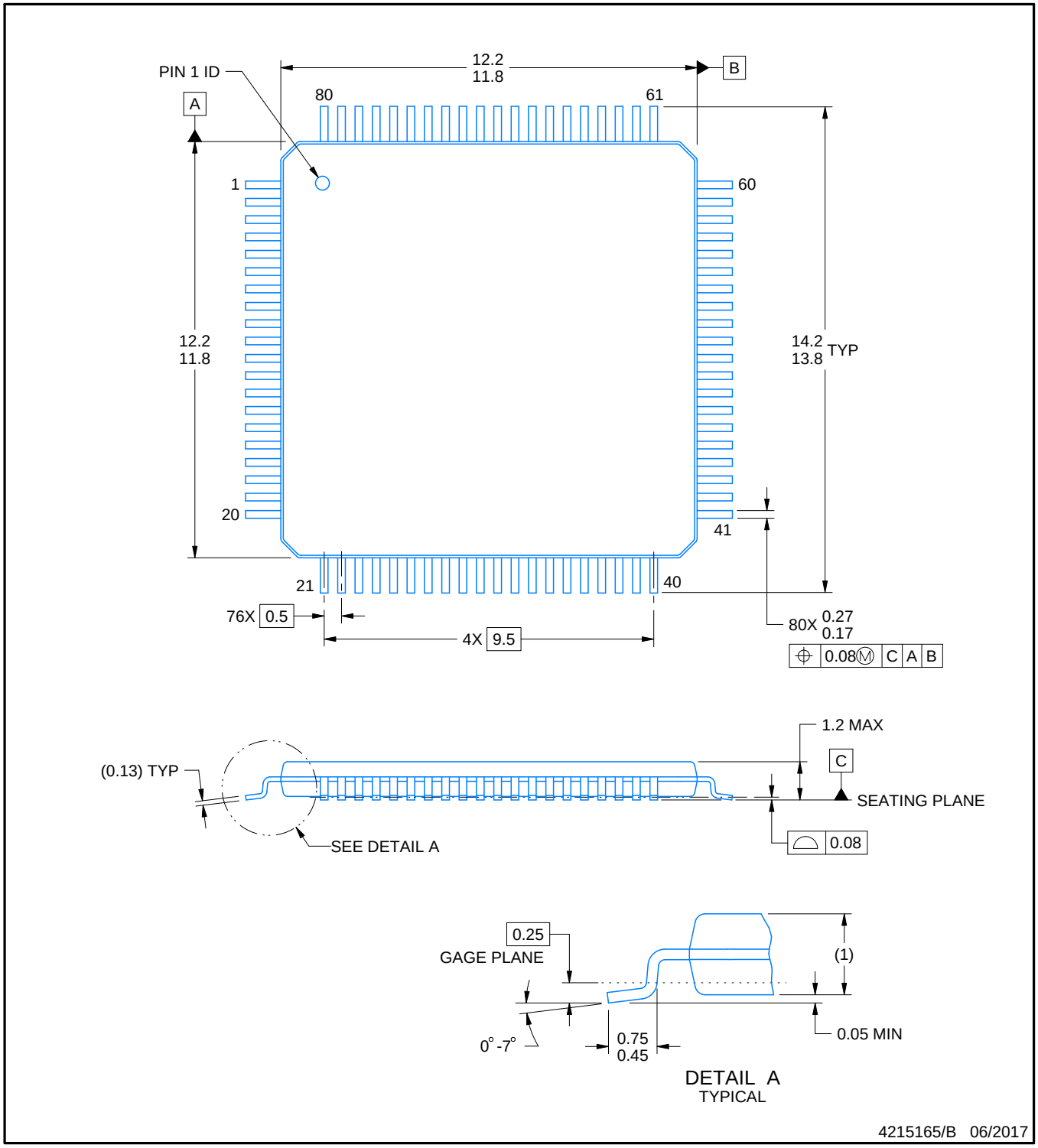
## TRAY




Chamfer on Tray corner indicates Pin 1 orientation of packed units.

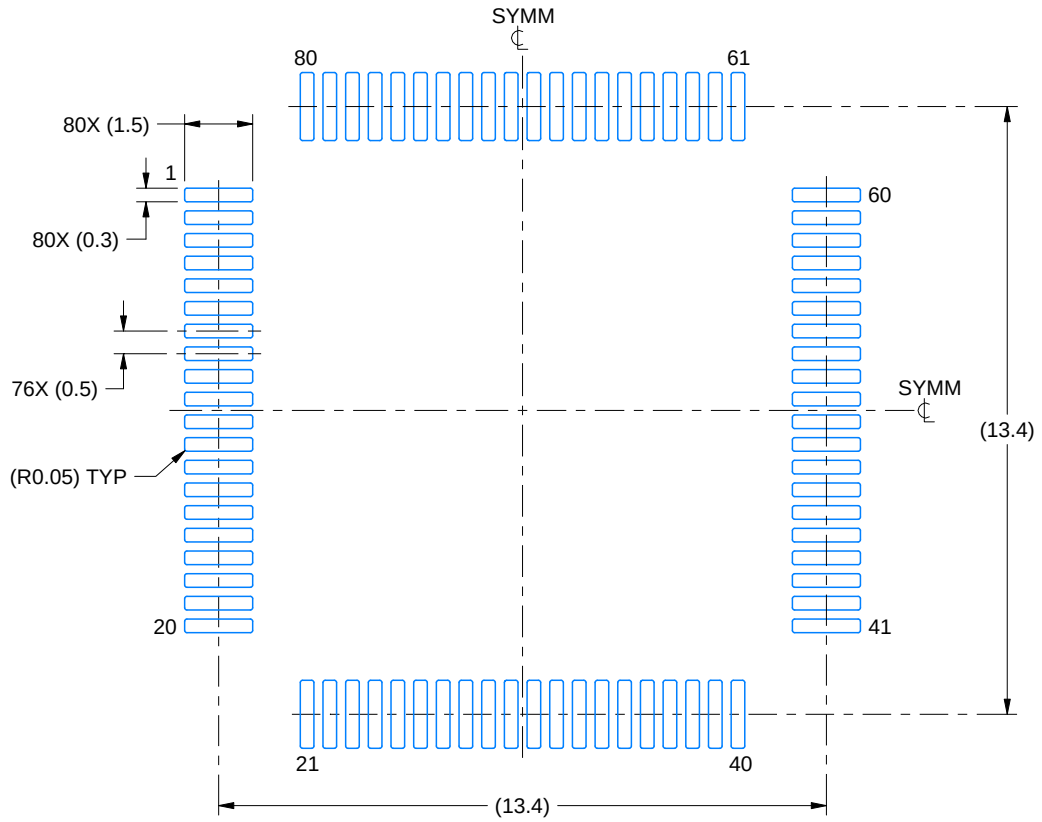
*All dimensions are nominal

| Device | Package Name | Package Type | Pins | SPQ | Unit array matrix | Max temperature (°C) | L (mm) | W (mm) | K0 (µm) | P1 (mm) | CL (mm) | CW (mm) |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| UCD3040PFC | PFC | TQFP | 80 | 96 | 6 x 16 | 150 | 315 | 135.9 | 7620 | 18.7 | 17.25 | 18.3 |
| UCD3040PFC.A | PFC | TQFP | 80 | 96 | 6 x 16 | 150 | 315 | 135.9 | 7620 | 18.7 | 17.25 | 18.3 |

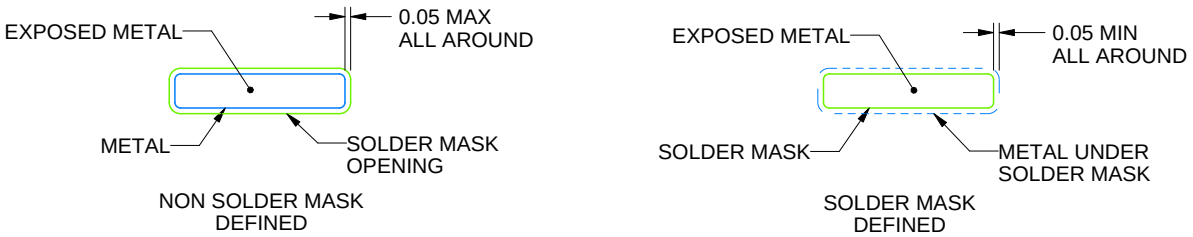



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC registration MS-026.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:6X

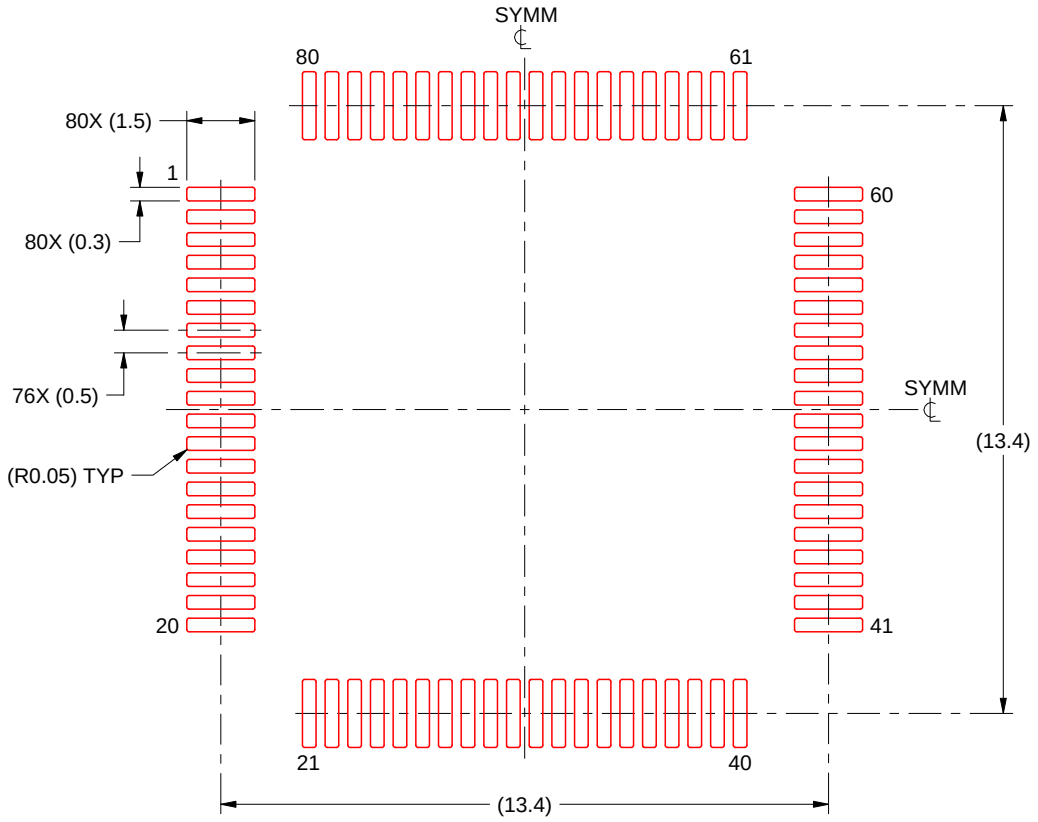



SOLDER MASK DETAILS

4215165/B 06/2017

NOTES: (continued)

4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
6. For more information, see Texas Instruments literature number SLMA004 (www.ti.com/lit/slma004).




SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:6X

4215165/B 06/2017

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

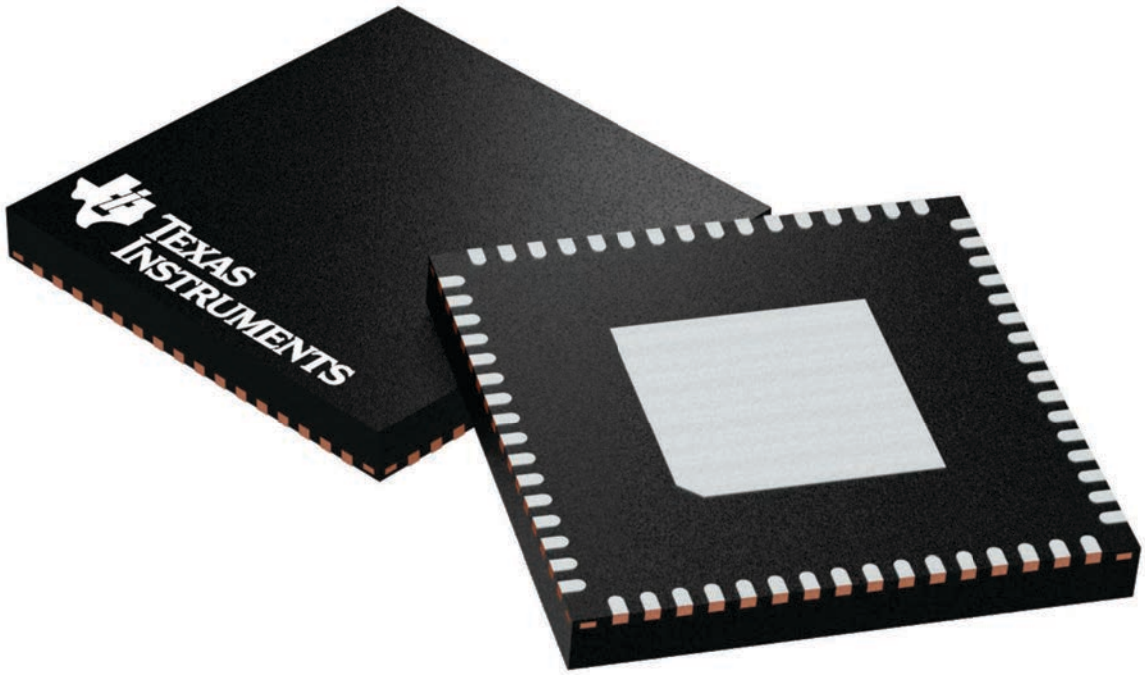
# GENERIC PACKAGE VIEW

## RGC 64

## VQFN - 1 mm max height

**9 x 9, 0.5 mm pitch**

PLASTIC QUAD FLATPACK - NO LEAD




Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

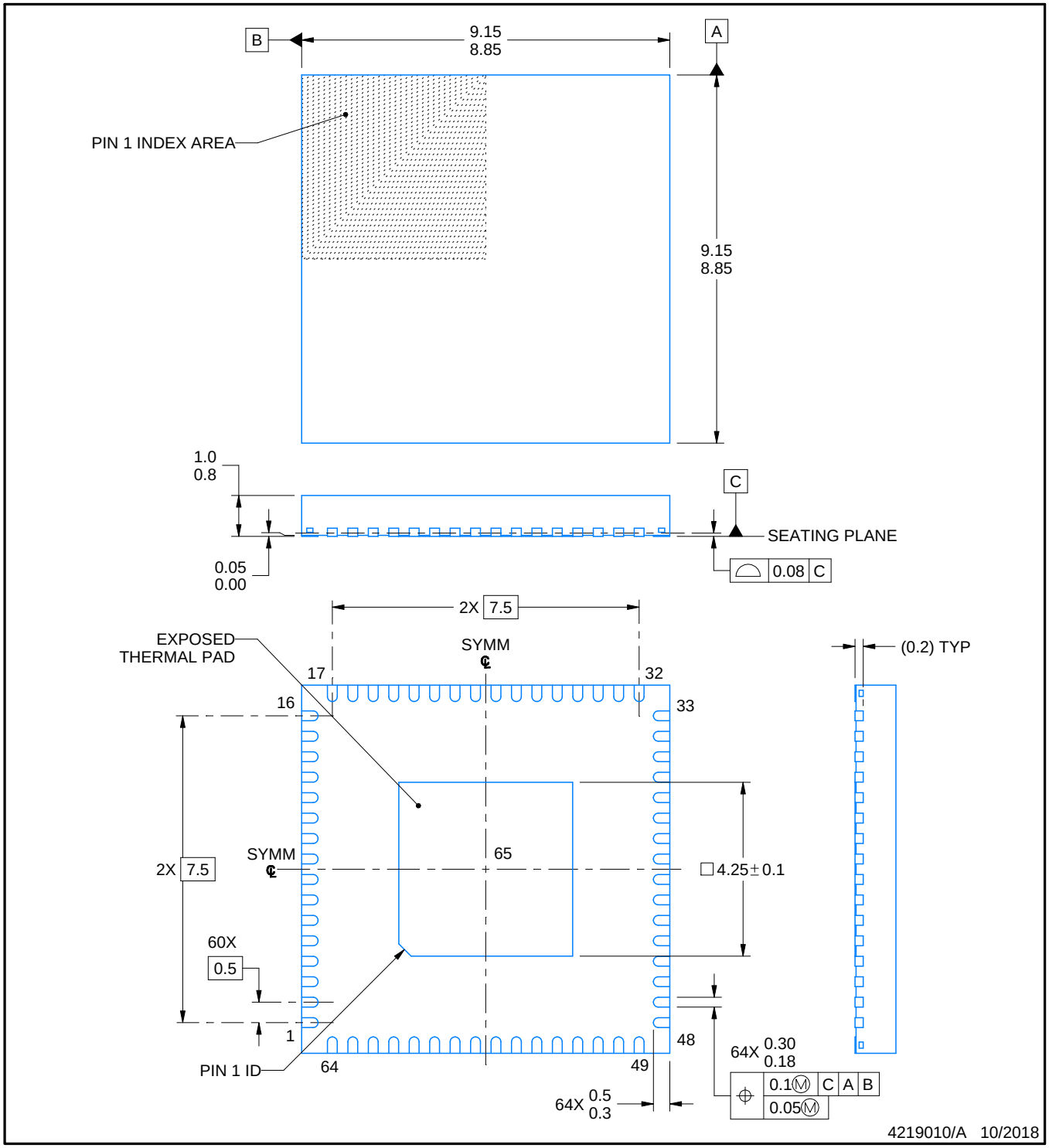
4224597/A

# PACKAGE OUTLINE

## RGC0064B

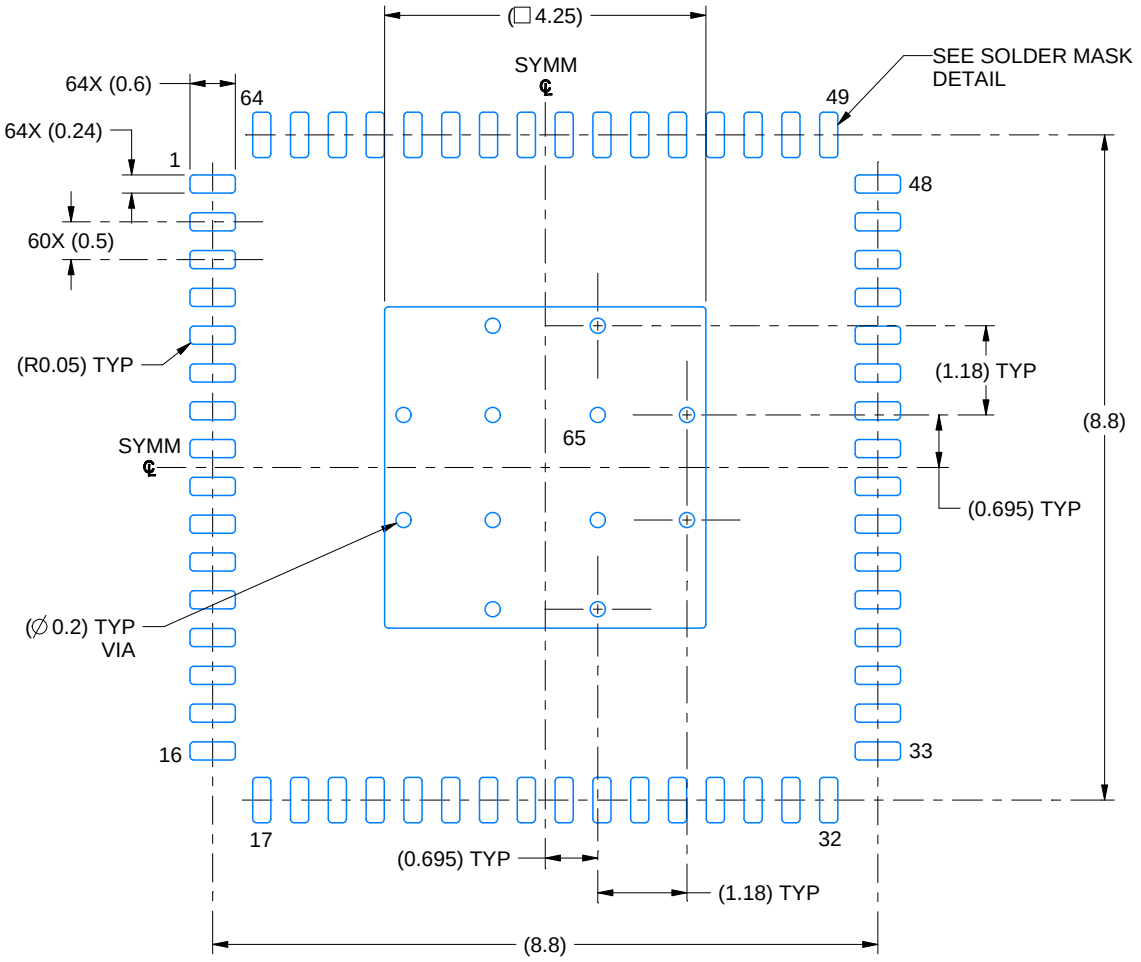
## VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

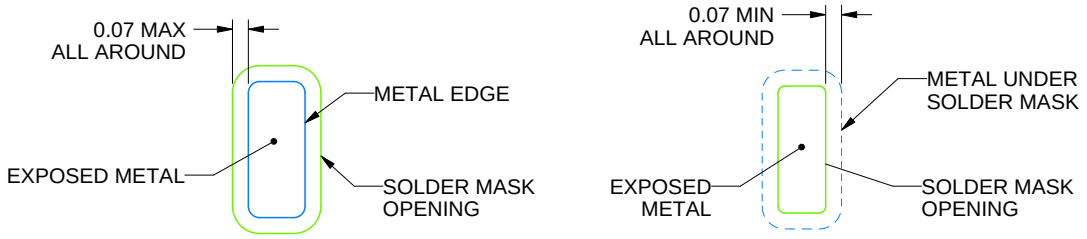



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X




NON SOLDER MASK DEFINED (PREFERRED)

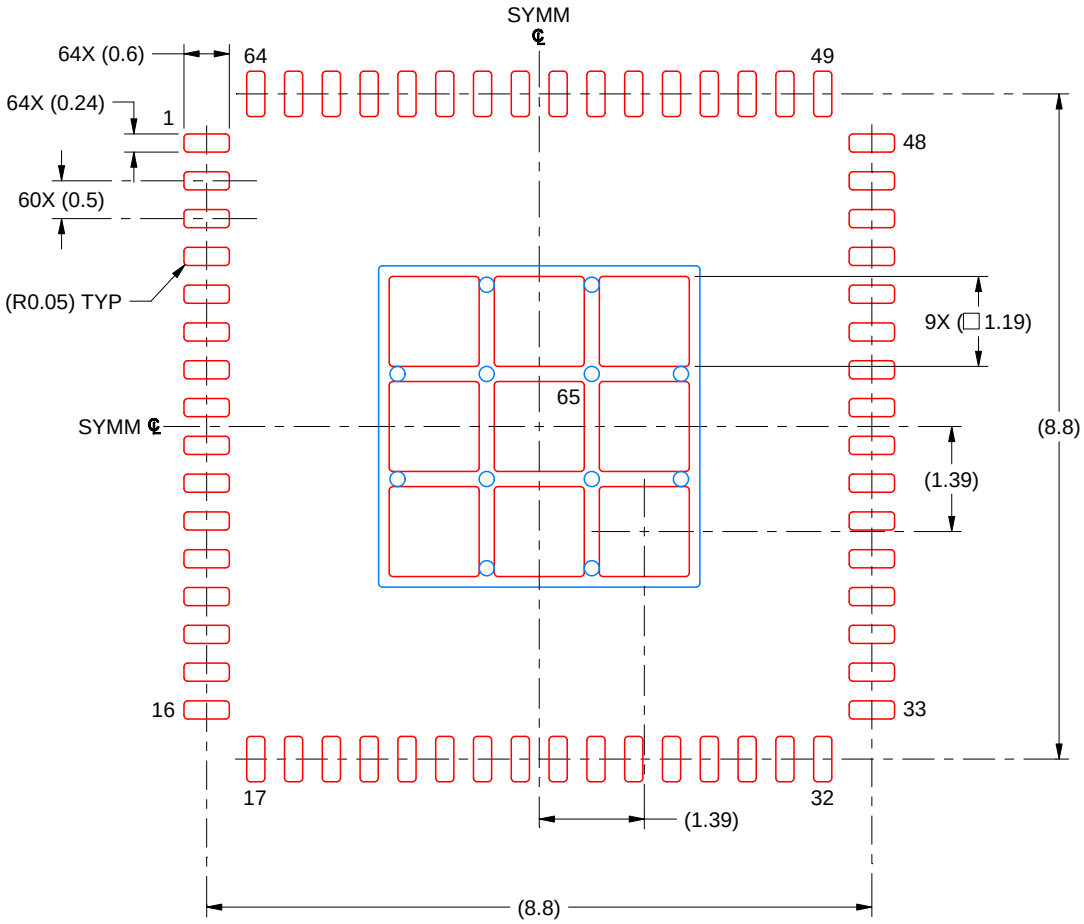
SOLDER MASK DEFINED

SOLDER MASK DETAILS

4219010/A 10/2018

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.




SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 10X

EXPOSED PAD 65
71% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

4219010/A 10/2018

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

# GENERIC PACKAGE VIEW

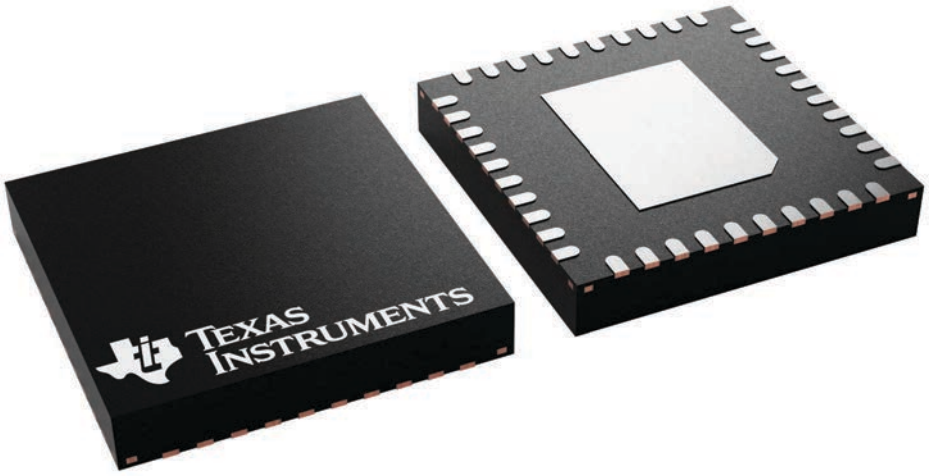
## RHA 40

## VQFN - 1 mm max height

**6 x 6, 0.5 mm pitch**

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



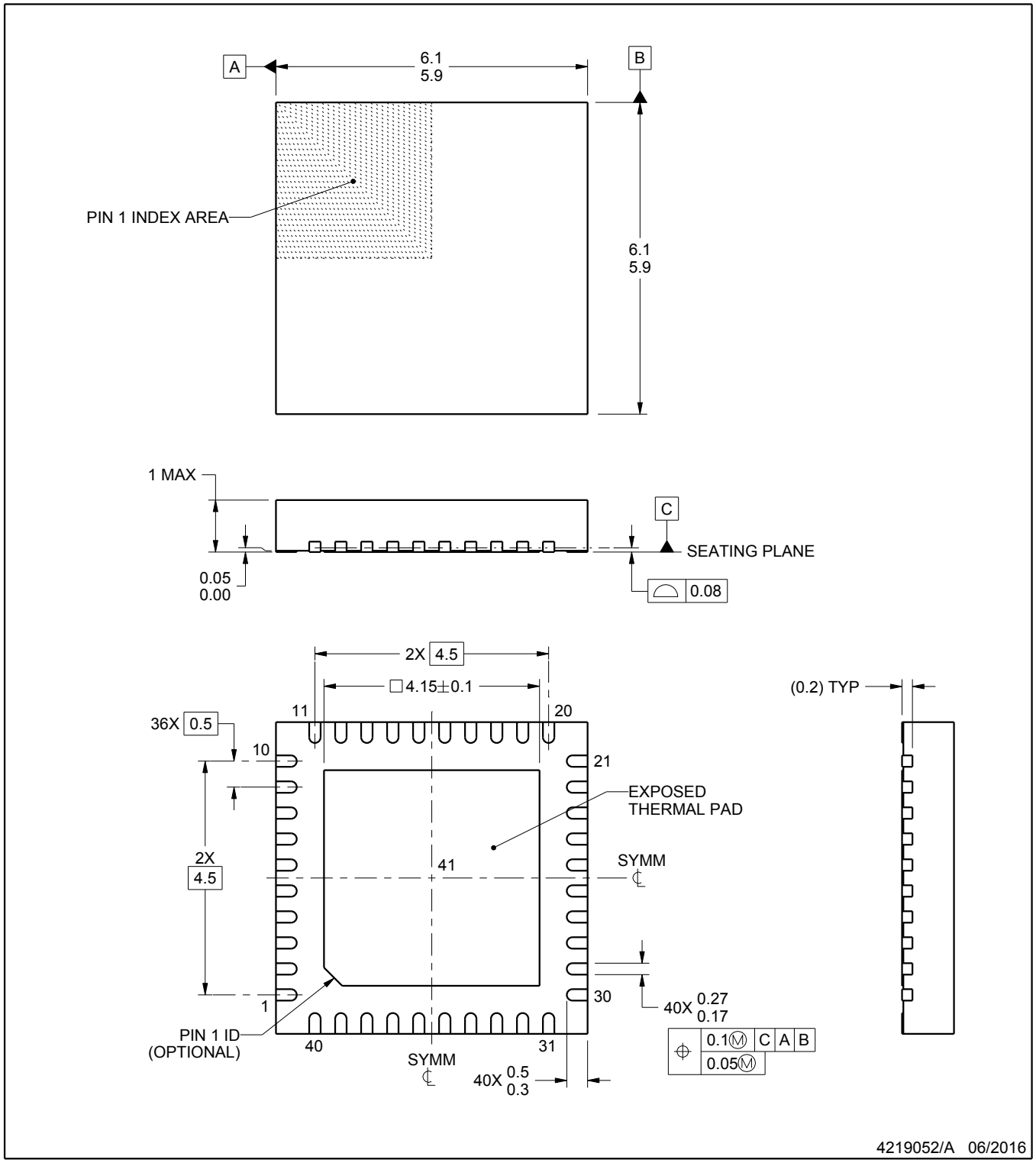

4225870/A

# PACKAGE OUTLINE

## RHA0040B

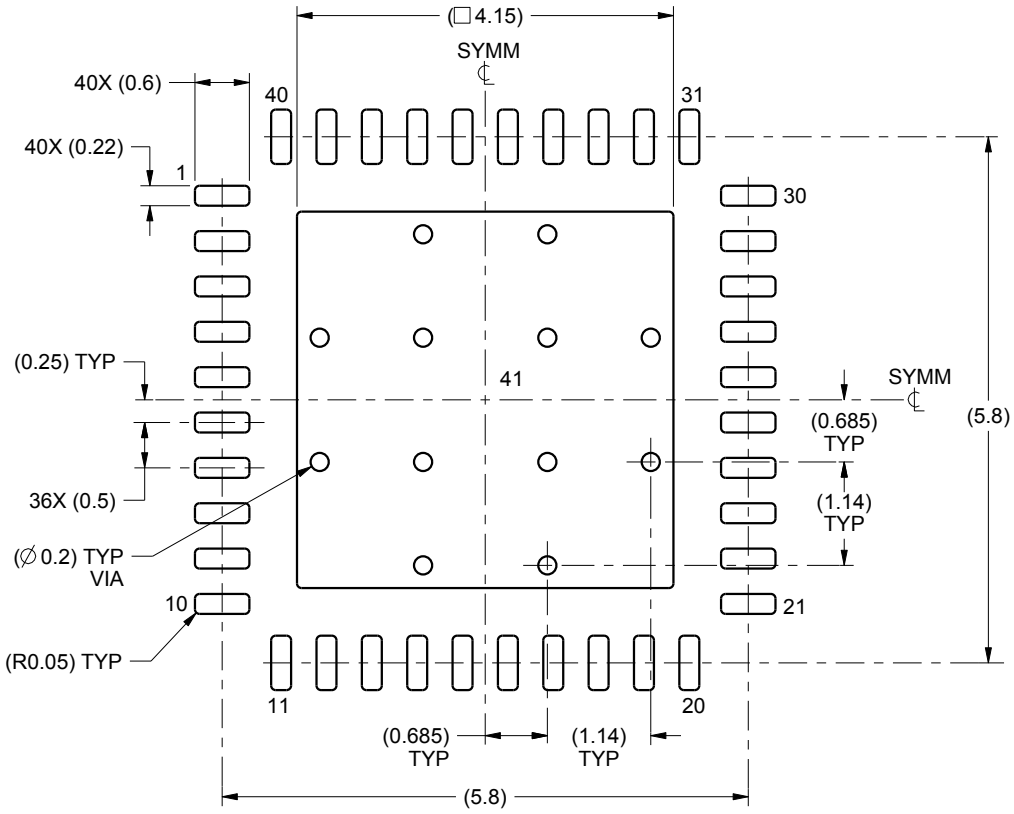
## VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

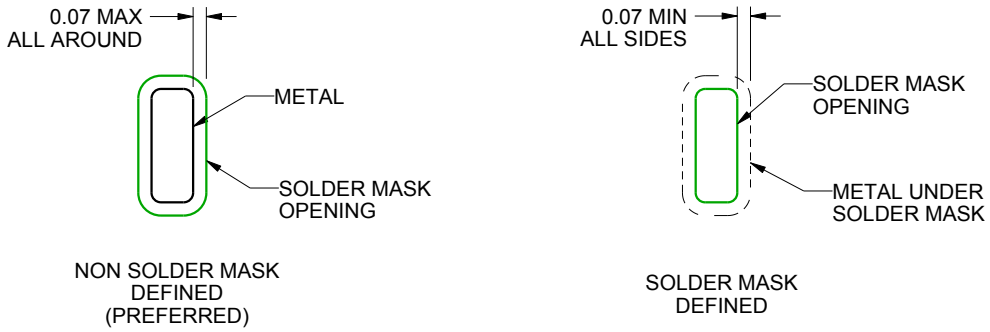



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.




LAND PATTERN EXAMPLE
SCALE:12X

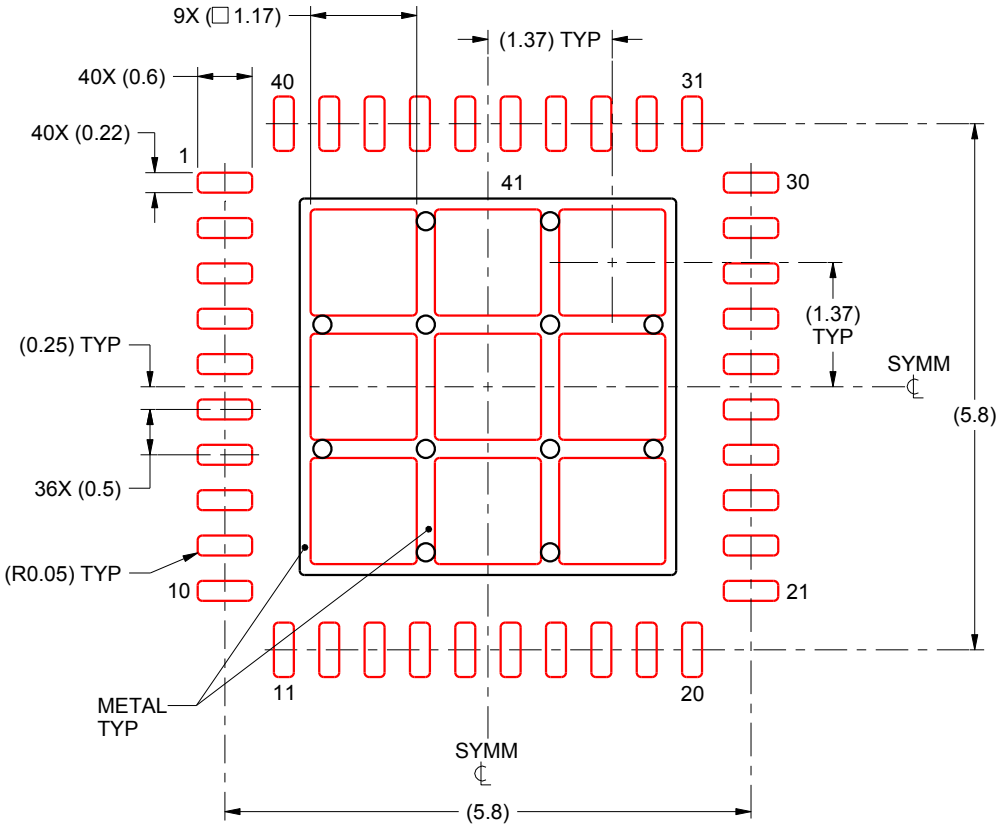



SOLDER MASK DETAILS

4219052/A 06/2016

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 41:
72% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:12X

4219052/A 06/2016

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

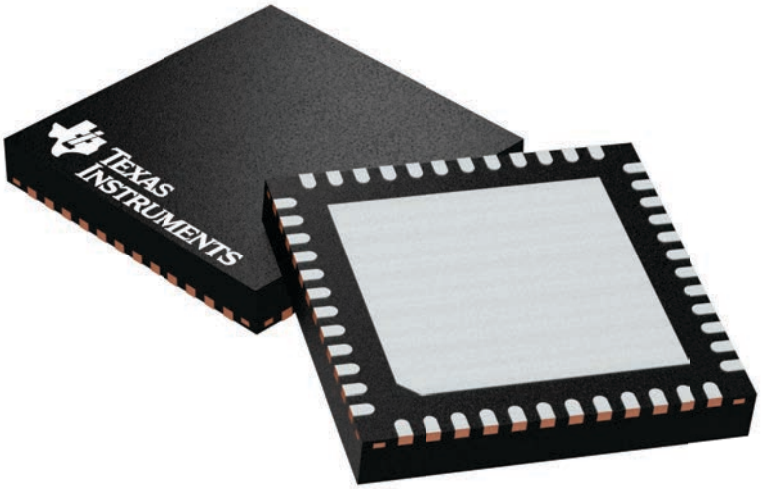
# GENERIC PACKAGE VIEW

## RGZ 48

## VQFN - 1 mm max height

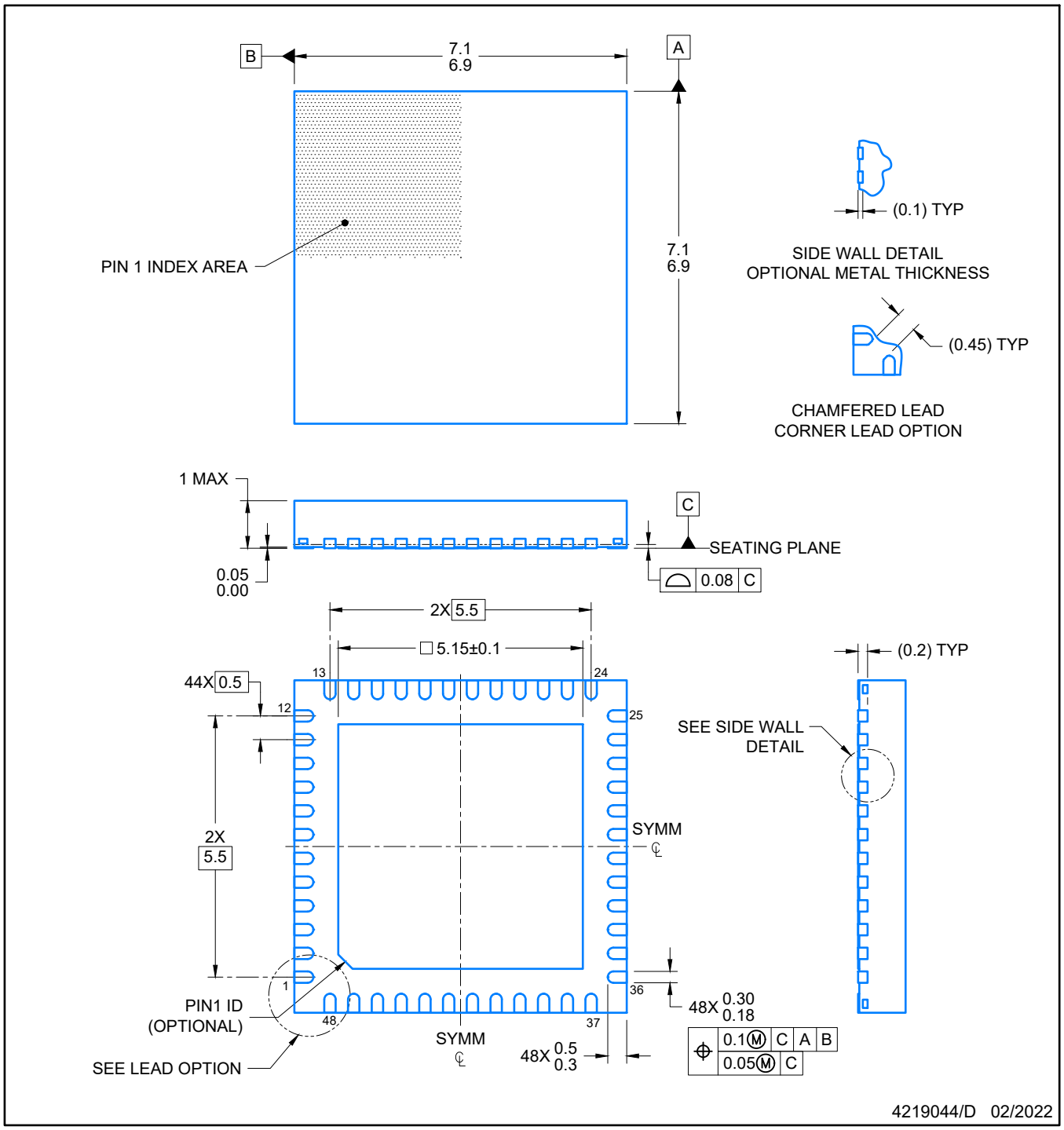
**7 x 7, 0.5 mm pitch**

PLASTIC QUADFLAT PACK- NO LEAD



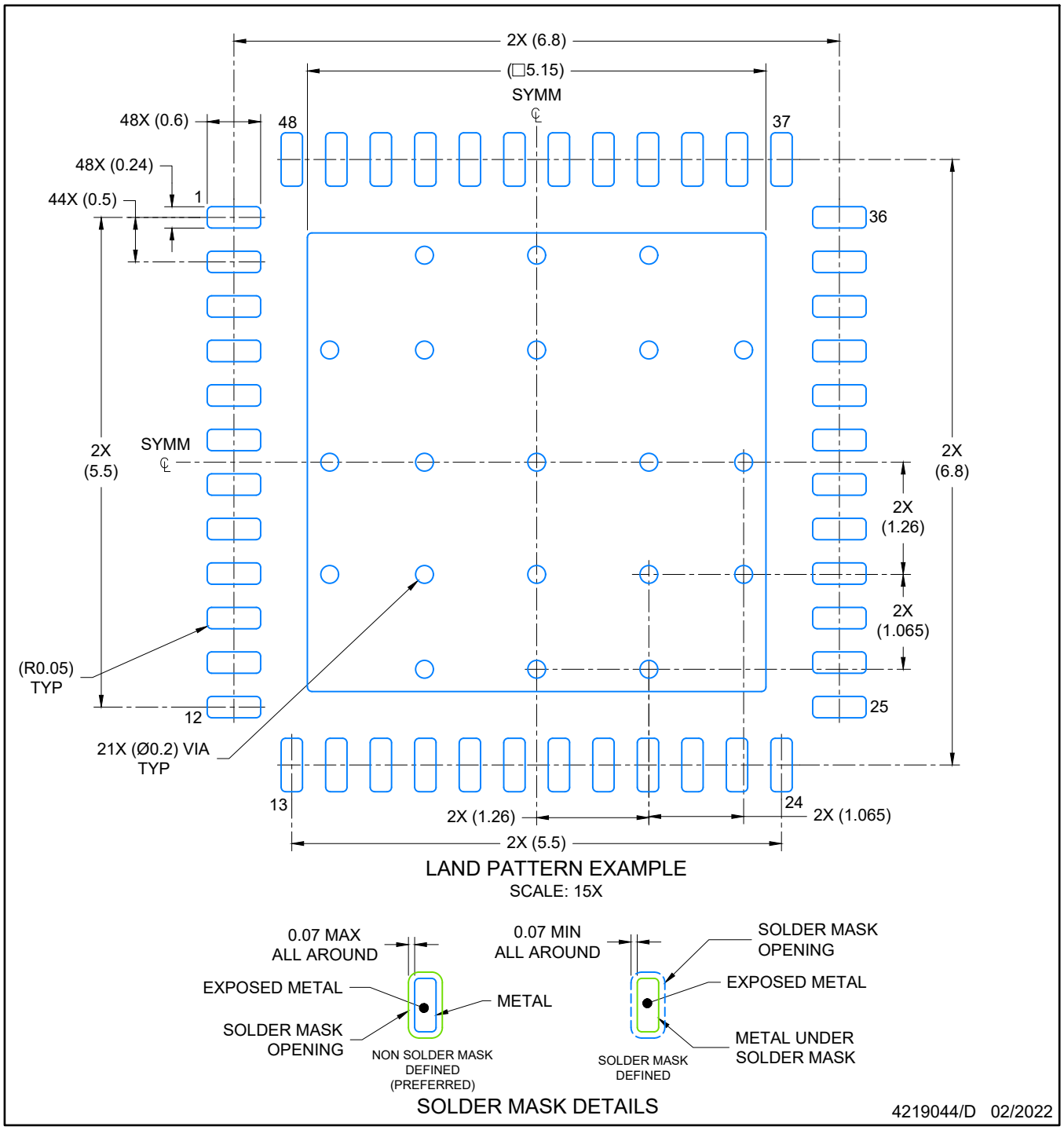

Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4224671/A



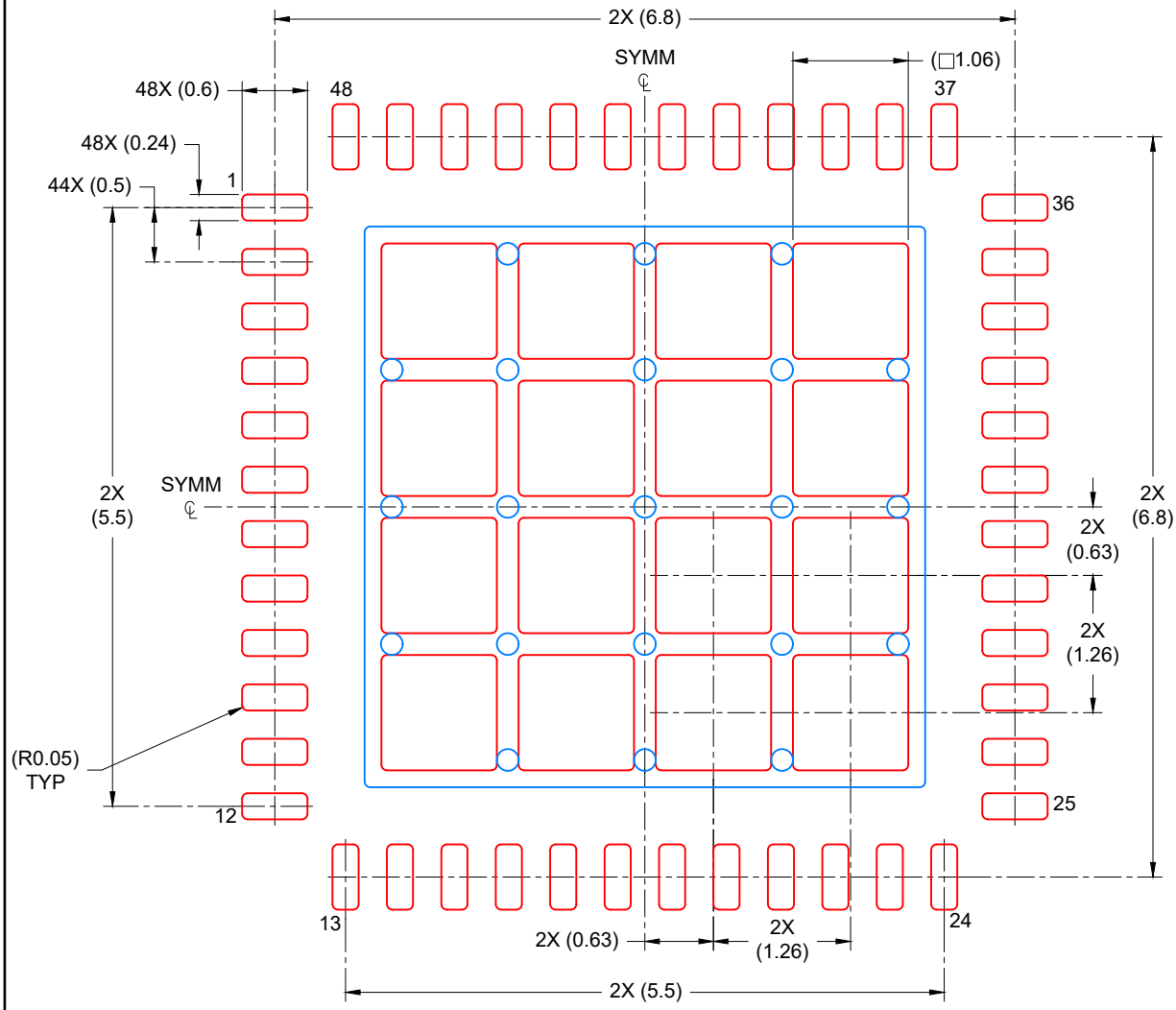

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.




NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
67% PRINTED COVERAGE BY AREA
SCALE: 15X

4219044/D 02/2022

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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