UCC5881-Q1 Isolated 20A Adjustable Gate Drive IGBT/SiC MOSFET Gate Driver With Advanced Protection Features For Automotive Applications

1 Features

- Dual-output driver with real time variable drive strength
  - ±15A and ±5A drive current outputs
  - Digital input pins (GD*) for drive strength adjustment without SPI
  - 3 resistor settings R1, R2, or R1||R2
  - Integrated 4A active Miller clamp or optional external drive for Miller clamp transistor
- Primary-side and secondary-side active short circuit (ASC) support
- Under-voltage and over-voltage protection on internal and external supplies
- Driver die temperature sensing and over temperature protection
- Short-circuit protection:
  - 110ns response time to DESAT event
  - DESAT protection – selections up to 14V
  - Shunt resistor based short-circuit (SC) and over-current (OC) protection
  - Configurable protection threshold values and blanking times
  - Programmable soft turn-off (STO) and two-level soft turn-off (2STO) current
- Integrated 10-bit ADC
  - Able to measure power switch temperature, DC Link voltage, driver die temperature, DESAT pin voltage, VCC2 voltage
  - Programmable digital comparators
- Advanced VCE/VDS clamping circuit
- Functional Safety-Compliant
  - Developed for functional safety applications
  - Documentation available to aid ISO 26262 system design up to ASIL D
- Integrated diagnostics:
  - Built in self-test (BIST) for protection comparators
  - Gate threshold voltage measurement for power device health monitoring
  - INP to transistor gate path integrity
  - Internal clock monitoring
  - Fault alarm and warning outputs (nFLT*)
  - ISO communication data integrity check
- SPI based device reconfiguration, verification, supervision, and diagnosis
- 150V/ns CMTI
- AEC-Q100 qualified with the following results:
  - Device temperature grade 1: -40°C to +125°C ambient operating temperature
  - Device HBM ESD classification level 2
  - Device CDM ESD classification level C2b

2 Applications

- EV and HEV traction inverter
- EV and HEV power modules

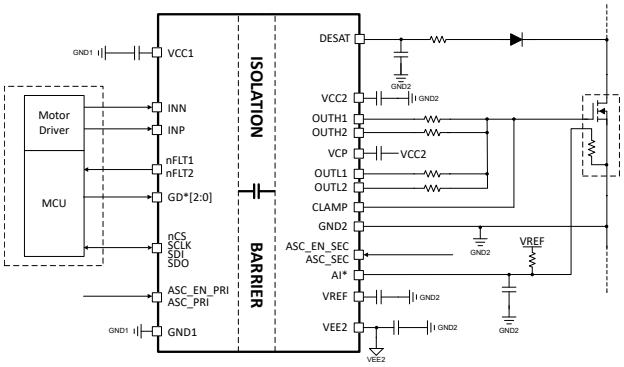
3 Description

The UCC5881-Q1 device is an isolated, highly configurable adjustable drive strength gate driver targeted to drive high power SiC MOSFETs and IGBTs in EV/HEV applications. Power transistor protections are included, such as shunt resistor based over-current, over-temperature (PTC, NTC, or diode), and DESAT detection, with selectable soft turn-off or two-level soft turn-off during these faults. An integrated 10-bit ADC enables monitoring of up to 2 analog inputs, VCC2, DESAT, and the gate driver temperature for enhanced system management. Diagnostics and detection functions are integrated to simplify the design of ASIL compliant systems. The parameters and thresholds for these features are configurable using the SPI, which allows the device to be used with nearly any SiC MOSFET or IGBT.

Device Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)	BODY SIZE (NOM)
UCC5881-Q1	DFC (SSOP, 32)	10.3mm × 10.3mm	10.5mm x 7.5mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Simplified Schematic

4 Device and Documentation Support

4.1 Device Support

4.1.1 Third-Party Products Disclaimer

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4.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

4.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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4.4 Trademarks

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4.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

4.6 Glossary

TI Glossary — This glossary lists and explains terms, acronyms, and definitions.

5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
December 2024	*	Initial Release

6 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
UCC5881QDFCRQ1	Active	Production	SSOP (DFC) | 32	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	UCC5881Q
UCC5881QDFCRQ1.A	Active	Production	SSOP (DFC) | 32	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	UCC5881Q

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

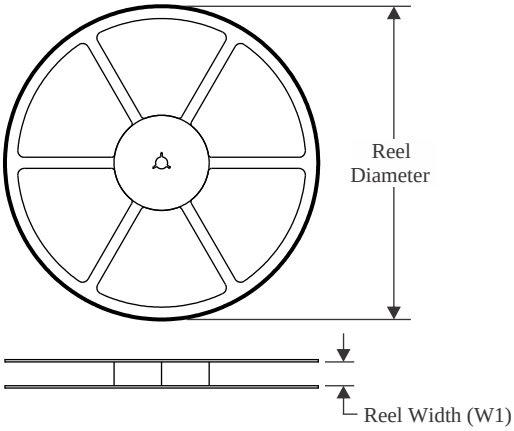
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

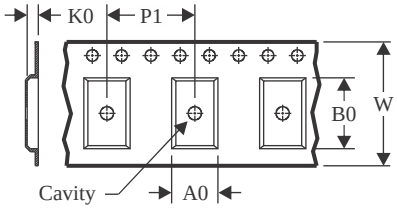
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

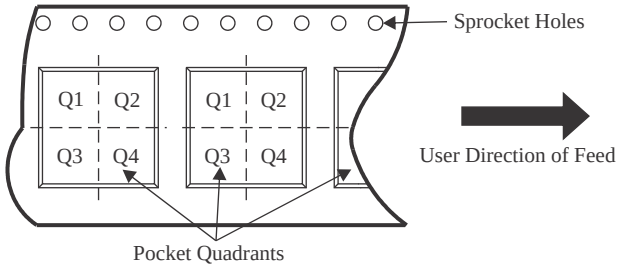


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

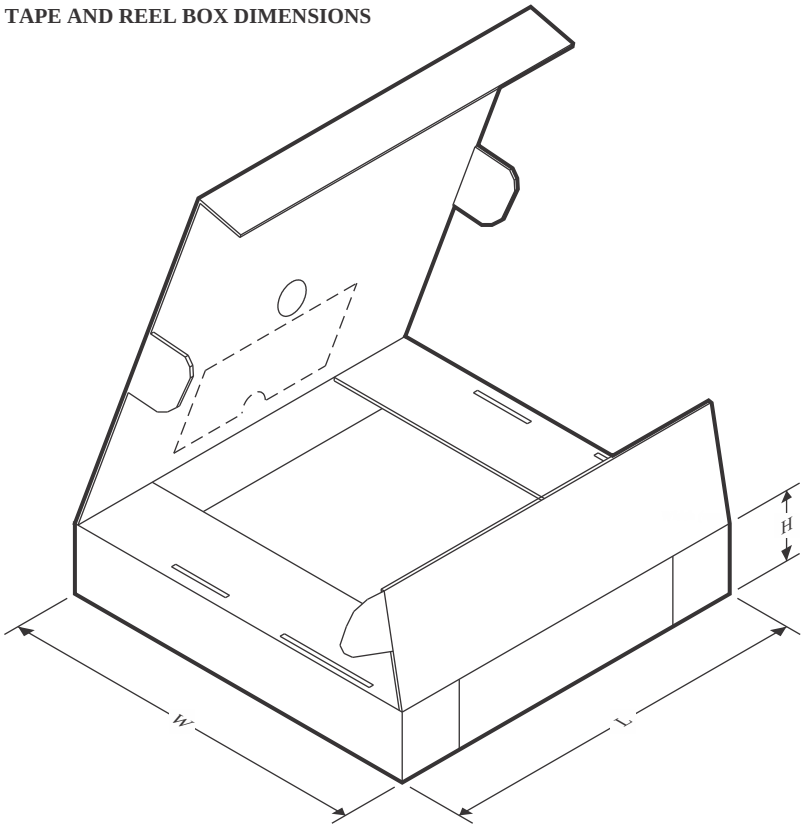
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UCC5881QDFCRQ1	SSOP	DFC	32	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

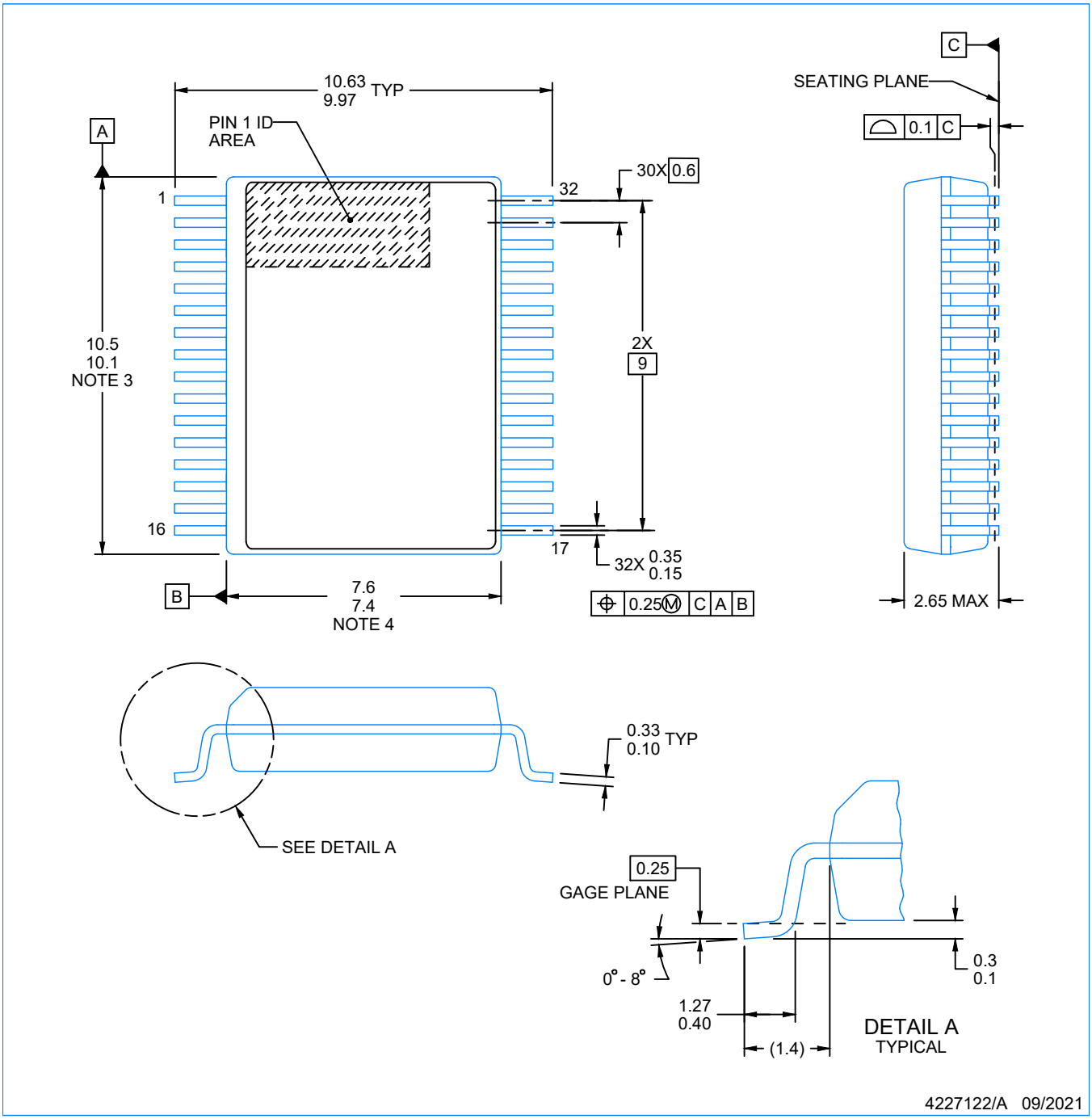
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UCC5881QDFCRQ1	SSOP	DFC	32	2000	350.0	350.0	43.0

PACKAGE OUTLINE

DFC0032A

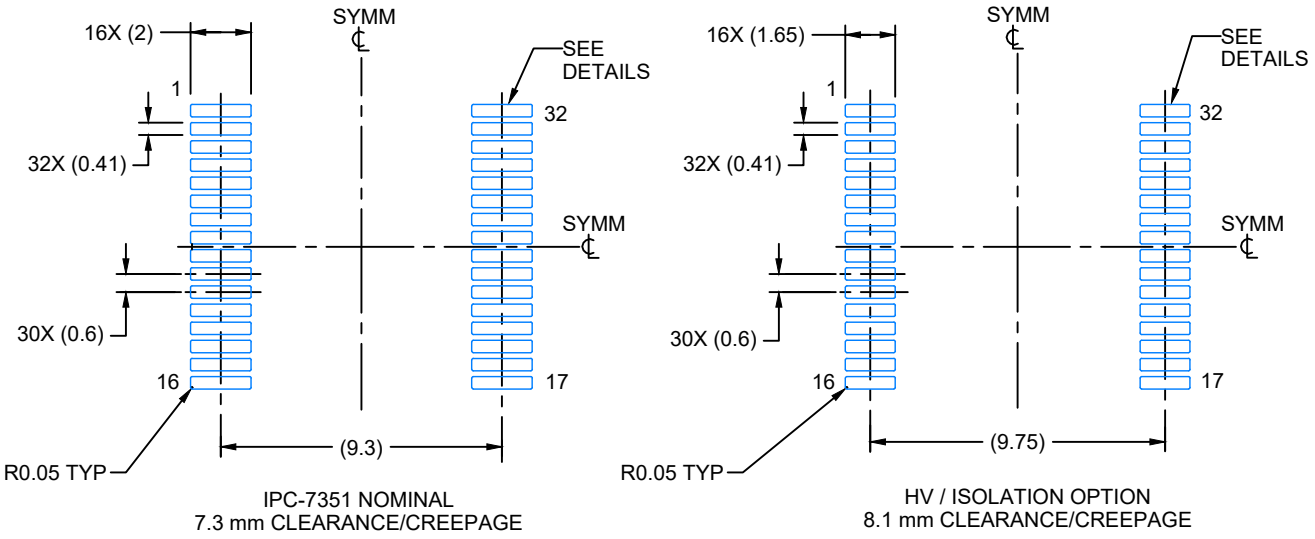
SSOP - 2.65 mm max height

SMALL OUTLINE PACKAGE

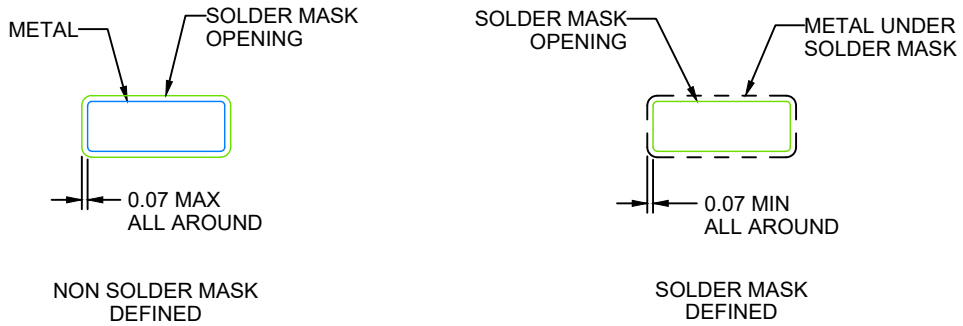


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.
5. Reference JEDEC registration MS-013.



LAND PATTERN EXAMPLE
SCALE:4X



SOLDER MASK DETAILS

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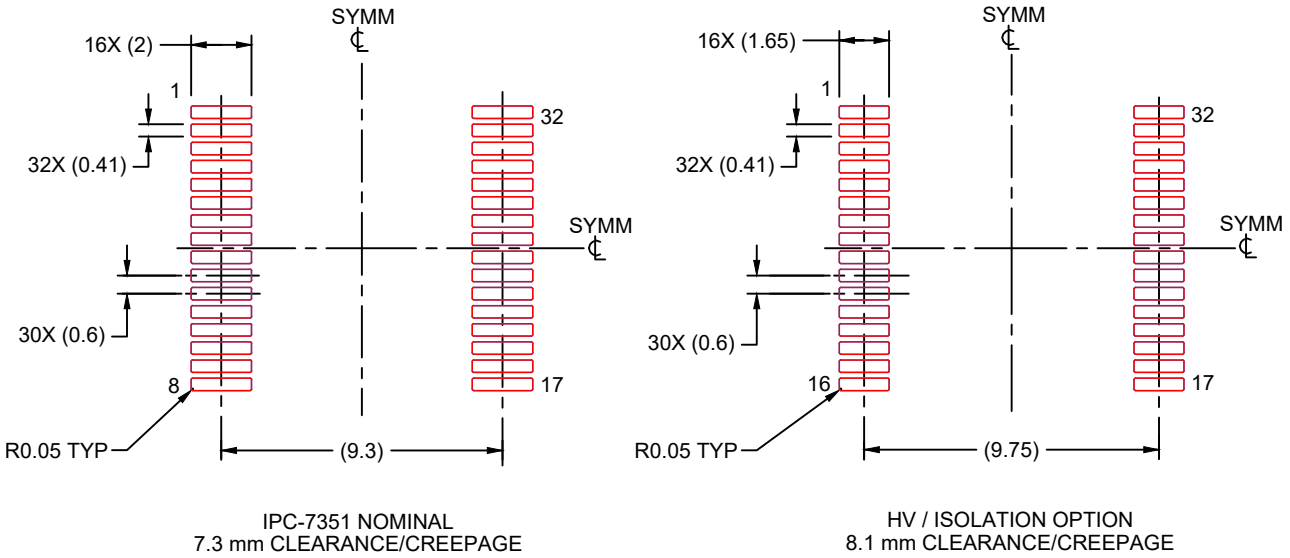
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



IPC-7351 NOMINAL
7.3 mm CLEARANCE/CREEPAGE

HV / ISOLATION OPTION
8.1 mm CLEARANCE/CREEPAGE

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:4X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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