

# UCC34141-Q1 Automotive 1.5W, 12V $V_{IN}$ , High-Density, > 5kV<sub>RMS</sub>, Isolated DC/DC Module

## 1 Features

- Fully integrated high-density isolated DC/DC module with isolation planar transformer
- Wide input range: 5.5V to 28V (with 22V OVLO)
  - $\geq 0.6W$  typical output for  $6V \leq V_{VIN} \leq 7V$ , and  $\geq 0.3W$  for  $V_{VIN} = 5.5V$ , at  $T_A \leq 105^\circ C$
  - $\geq 1.5W$  typical output for  $8V \leq V_{VIN} \leq 18V$ ,  $18V \leq V_{VDD-COM} \leq 20V$ , at  $T_A \leq 85^\circ C$
  - $\geq 2W$  typical output for  $10.8V \leq V_{VIN} \leq 13.2V$ ,  $18V \leq V_{VDD-COM} \leq 20V$ , at  $T_A \leq 85^\circ C$
  - $\geq 1W$  typical output for  $8V \leq V_{VIN} \leq 18V$ ,  $15V \leq V_{VDD-COM} < 18V$ , at  $T_A \leq 85^\circ C$
- Programmable (VDD – COM) output voltage
  - 15V to 20V,  $\leq \pm 1.5\%$  total regulation accuracy
- Programmable (VEE – COM) output voltage
  - 2V to -8V,  $\leq \pm 5\%$  total regulation accuracy
- Adaptive spread spectrum modulation (SSM)
- Strong magnetic and radiated field immunities
- Reduced inrush current soft-start
- ENA pin for logic enable and programming input UVLO
- Open-drain  $\overline{PG}$  for fault indicator, power good
- Integrated protections: UVLO, OVLO, short-circuit, OVP, UVP, and thermal shutdown.
- < 3pF isolation capacitance
- Static and dynamic CMTI >  $\pm 250kV/\mu s$
- AEC-Q100 qualified for automotive applications
  - Temperature grade 1:  $-40^\circ C \leq T_A \leq 125^\circ C$
- Safety-related certifications (Planned):
  - Reinforced isolation per DIN EN IEC 60747-17 (VDE 0884-17)
  - UL 1577 / CSA component recognition program
- 16-pin, wide body SOIC package

## 2 Applications

- Hybrid, electric and power train system (EV/HEV)
  - Inverter and motor control
  - On-board (OBC) and wireless charger
  - DC/DC converter
- Grid infrastructure
  - EV charging station power module
  - DC charging (pile) station
  - String inverter
- Industrial transport
  - Off-highway vehicle electric drive
- Power Delivery
  - Rack and Server Power

## 3 Description

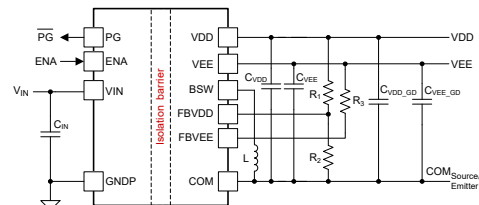
The UCC34141-Q1 is an automotive qualified high isolation voltage DC/DC power module designed to provide power to SiC and IGBT isolated gate drivers. Its proprietary integrated transformer, flip-chip package, and advanced control architectures achieve high power density, low noise, and lowest system BOM. This device is capable of delivering 1.5W typical output power at  $85^\circ C$  ambient temperature. The highly accurate dual-output voltages, easily set by resistor dividers, enable low on-resistance, fast and reliable switching for SiC/IGBT. The low-latency feedback control reduces the output capacitance for fast load transient and supports dynamic voltage programming. The wide input voltage and adjustable  $V_{IN}$  UVLO supports both wide battery voltage of electric vehicles and regulated input rails. It is operational from 5.5V to 20V  $V_{IN}$ , and can withstand  $V_{IN}$  overvoltage transient up to 28V.

The integrated protection features, fault-report  $\overline{PG}$  pin, and enable function increase system robustness and save external components. The SOIC package with 8.2mm creepage and clearance distance ensures high isolation capability.

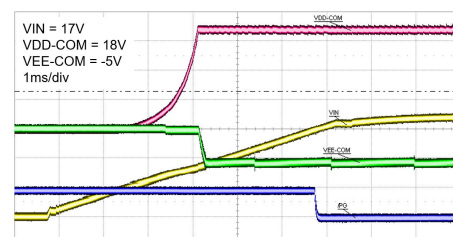
### Device Information

ORDERABLE PART NUMBER	PACKAGE <sup>(1)</sup>	BODY SIZE (NOM)
PUCC34141 QDHARQ1	DHA (SSOP, 16)	5.85mm × 7.50mm

(1) For all available packages, see [Section 11](#).



### Simplified Application



### Typical Power-up Sequence



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## 4 Device Comparison

**Table 4-1. Device Comparison Table**

DEVICE NAME	V <sub>VIN</sub> RANGE	OUTPUT (VDD-COM) ADJUSTABLE RANGE	OUTPUT (VEE-COM) ADJUSTABLE RANGE	TYPICAL POWER	POWER GOOD (PG) ACTIVE POLARITY
UCC34141-Q1	8V to 20V	15V to 20V	-2V to -8V	1.5W	LOW
	5.5V to 8V	15V to 20V	-2V to -8V	≥0.3W	

## 5 Pin Configuration and Functions

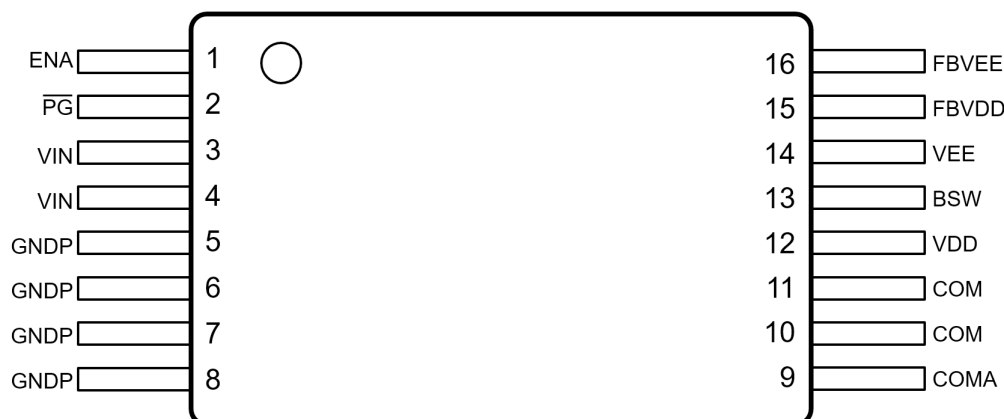


Figure 5-1. DHA Package, 16-Pin SSOP (Top View)

Table 5-1. Pin Functions

PIN		TYPE <sup>(1)</sup>	DESCRIPTION
NAME	NO.		
ENA	1	I	Enable pin. Forcing ENA LOW disables the device. Pull HIGH to enable normal device functionality. 5.5V recommended maximum. Can be used to program input UVLO with a resistor divider from VIN.
PG	2	O	Active low power-good open-drain output pin. $\overline{PG}$ remains low when $V_{VIN\_UVLOP} \leq V_{VIN} \leq V_{VIN\_OVLOP}$ ; $V_{VDD\_UVP} \leq V_{FBVDD} \leq V_{VDD\_OVP}$ ; $V_{VEE\_UVP} \leq V_{FBVEE} \leq V_{VEE\_OVP}$ ; $T_{J\_Primary} \leq T_{SHUT\_P\_R}$ ; and $T_{J\_secondary} \leq T_{SHUT\_S\_R}$ .
VIN	3, 4	P	Primary input voltage. Connect a 10 $\mu$ F and a parallel 0.1 $\mu$ F ceramic capacitor from VIN to GNDP. The 0.1 $\mu$ F ceramic capacitor in 0402 body size is for by-passing the high frequency noise and must be next to the VIN and GNDP pins on the same side of the PCB as the IC.
GNDP	5, 6, 7, 8	G	Primary-side ground connection for VIN. Place several vias to copper pours for thermal relief. See the "Layout" section for more details.
COMA	9	G	Secondary-side analog sense reference connection for the noise sensitive analog feedback input FBVDD, and FBVEE. Connect the low-side FBVDD feedback resistor and high frequency decoupling filter capacitors close to the COMA pin and respective feedback pin FBVDD. Connect to secondary-side gate drive voltage reference, COM. Use a single point connection and place the high frequency decoupling ceramic capacitor close to the COMA pin.
COM	10, 11	G	Secondary ground. Connect to Source of power switch.
VDD	12	P	Secondary-side isolated output voltage from transformer. Connect a 10 $\mu$ F and a parallel 0.1 $\mu$ F ceramic capacitor from VDD to COM. The 0.1 $\mu$ F ceramic capacitor in 0402 body size is for bypassing high frequency noise and must be next to the VDD and COM pins.
VEE	14	P	Secondary-side isolated output voltage for negative rail. Connect a 2.2 $\mu$ F ceramic capacitor from VEE to COM for bypassing high frequency noise.
FBVDD	15	I	Feedback (VDD – COM) output voltage sense pin and to adjust the output (VDD – COM) voltage. Connect a resistor divider from VDD to COMA so that the midpoint is connected to FBVDD. The equivalent FBVDD voltage is regulated at 2.5V with the internal hysteresis control across isolation. Adding a 220pF ceramic capacitor for high frequency decoupling in parallel with the low-side feedback resistor is needed. The 220pF ceramic capacitor for high frequency bypass must be next to the FBVDD and COMA pins on top layer or back layer connected with vias.

**Table 5-1. Pin Functions (continued)**

PIN		TYPE <sup>(1)</sup>	DESCRIPTION
NAME	NO.		
FBVEE	16	I	Feedback (COM – VEE) output voltage sense pin used to adjust the output (COM – VEE) voltage. Connect one feedback resistor, 40kΩ to 160kΩ, to VEE to program the (COM – VEE) voltage from 2V to 8V. The equivalent FBVEE voltage is regulated close to 0V with the internal hysteresis control. Connect a 10pF ceramic capacitor from FBVEE to COMA for bypassing high frequency noise. The 10pF ceramic capacitor must be next to the FBVEE pin on top layer or back layer connected with vias.

(1) P = power, G = ground, I = input, O = output

## 6 Specifications

### 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

		MIN	TYP	MAX	UNIT
V <sub>VIN</sub>	VIN to GNDP	−0.3		30	V
V <sub>ENA</sub> , V <sub>PG</sub>	ENA, PG to GNDP	−0.3		7	V
V <sub>BSW-COM</sub> , V <sub>FBVEE-COM</sub>	BSW, FBVEE to COM	−10		25.5	V
V <sub>BSW-VEE</sub>	BSW to VEE	−0.7		32	V
V <sub>BSW-VEE_tran</sub>	BSW to VEE (0.24ns transient)	−2.1		33.4	V
V <sub>COM-VEE</sub>	COM to VEE	−0.3		10	V
V <sub>VDD-COM</sub> , V <sub>FBVDD-COM</sub>	VDD, FBVDD to COM	−0.3		25.5	V
V <sub>VDD-VEE</sub>	VDD to VEE	−0.3		32	V
P <sub>OUT_VDD_MAX</sub>	Total output power at T <sub>A</sub> =25°C			3	W
T <sub>J</sub>	Operating junction temperature range	−40		150	°C
T <sub>stg</sub>	Storage temperature	−65		150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

### 6.2 ESD Ratings

			VALUE	UNIT
V <sub>(ESD)</sub>	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002 <sup>(1)</sup>	±2000	V
		Charged-device model (CDM), per AEC Q100-011 Section 7.2	±750	V

- (1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

### 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	TYP	MAX	UNIT
V <sub>VIN</sub>	Primary-side input voltage to GNDP during continuous operation	5.5 <sup>(1)</sup>	12	20	V
V <sub>VIN</sub>	Primary-side input voltage to GNDP during overvoltage transient			28	V
V <sub>ENA</sub>	Enable to GNDP	0		5.5	V
V <sub>PG</sub>	Powergood to GNDP	0		5.5	V
V <sub>VDD-COM</sub>	VDD to COM	15	18	20	V
V <sub>VDD-VEE</sub>	VDD to VEE	15	22	25	V
V <sub>COM-VEE</sub>	COM to VEE	2	4	8	V
T <sub>A</sub>	Ambient temperature	−40		125	°C
T <sub>J</sub> <sup>(2)</sup>	Junction temperature	−40		150	°C

- (1) See the V<sub>VIN\_UVLO\_R</sub> and V<sub>VIN\_UVLO\_F</sub> electrical characteristics for the minimum operational V<sub>VIN</sub>.  
(2) See the (VDD-COM) and (COM-VEE) Load Recommended Operating Area section for maximum rated values across temperature and V<sub>VIN</sub> conditions for different (VDD-COM) and (COM-VEE) output voltage settings.

## 6.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		DHA (SOIC)	UNIT
		16 PINS	
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	63.2	°C/W
R <sub>θJC(top)</sub>	Junction-to-case (top) thermal resistance	32.3	°C/W
R <sub>θJB</sub>	Junction-to-board thermal resistance	20.1	°C/W
Ψ <sub>JA</sub>	Junction-to-ambient characterization parameter	47.8	°C/W
Ψ <sub>JB</sub>	Junction-to-board characterization parameter	20.5	°C/W
Ψ <sub>JT</sub>	Junction-to-top characterization parameter	3	°C/W

(1) The thermal resistances (R) are based on JEDEC board, and the characterization parameters (Ψ) are based on the EVM described in the Layout section. For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

## 6.5 Insulation Specifications

PARAMETER		TEST CONDITIONS	VALUE	UNIT
General				
CLR	External clearance <sup>(1)</sup>	Shortest terminal-to-terminal distance through air	> 8.2	mm
CPG	External creepage <sup>(1)</sup>	Shortest terminal-to-terminal distance across the package surface	> 8.2	mm
DTI	Distance through the insulation	Minimum internal gap (internal clearance – transformer power isolation)	> 70	μm
CTI	Comparative tracking index	DIN EN 60112 (VDE 0303-11); IEC 60112	> 600	V
	Material group	According to IEC 60664-1	I	
	Overvoltage category	Rated mains voltage ≤ 300V <sub>RMS</sub>	I-IV	
		Rated mains voltage ≤ 600V <sub>RMS</sub>	I-IV	
		Rated mains voltage ≤ 1000V <sub>RMS</sub>	I-III	
DIN EN IEC 60747-17 (VDE 0884-17) (Planned Certification Targets) <sup>(2)</sup>				
V <sub>IORM</sub>	Maximum repetitive peak isolation voltage	AC voltage (bipolar)	1700	V <sub>PK</sub>
V <sub>IOWM</sub>	Maximum working isolation voltage	AC voltage (sine wave) Time dependent dielectric breakdown (TDDb) test	1202	V <sub>RMS</sub>
		DC voltage	1700	V <sub>DC</sub>
V <sub>IOTM</sub>	Maximum transient isolation voltage	V <sub>TEST</sub> = V <sub>IOTM</sub> , t = 60s (qualification); V <sub>TEST</sub> = 1.2 × V <sub>IOTM</sub> , t = 1s (100% production)	7071	V <sub>PK</sub>
V <sub>IMP</sub>	Maximum impulse voltage <sup>(3)</sup>	Tested in air, 1.2/50μs waveform per IEC 62368-1	8000	V <sub>PK</sub>
V <sub>IOSM</sub>	Maximum surge isolation voltage <sup>(3)</sup>	V <sub>IOSM</sub> ≥ 1.3 × V <sub>IMP</sub> ; Tested in oil (qualification test), 1.2/50μs waveform per IEC 62368-1	10400	V <sub>PK</sub>
q <sub>pd</sub>	Apparent charge <sup>(4)</sup>	Method a: After I/O safety test subgroup 2/3, V <sub>ini</sub> = V <sub>IOTM</sub> , t <sub>ini</sub> = 60s; V <sub>pd(m)</sub> = 1.2 × V <sub>IORM</sub> , t <sub>m</sub> = 10s	≤ 5	pC
		Method a: After environmental tests subgroup 1, V <sub>ini</sub> = V <sub>IOTM</sub> , t <sub>ini</sub> = 60s; V <sub>pd(m)</sub> = 1.6 × V <sub>IORM</sub> , t <sub>m</sub> = 10s	≤ 5	pC
		Method b1: At routine test (100% production), V <sub>ini</sub> = 1.2 × V <sub>IOTM</sub> , t <sub>ini</sub> = 1s; V <sub>pd(m)</sub> = 1.875 × V <sub>IORM</sub> , t <sub>m</sub> = 1s	≤ 5	pC
C <sub>IO</sub>	Barrier capacitance, input to output <sup>(5)</sup>	V <sub>IO</sub> = 0.4 sin (2πft), f = 1MHz	< 3	pF
R <sub>IO</sub>	Isolation resistance, input to output <sup>(5)</sup>	V <sub>IO</sub> = 500V, T <sub>A</sub> = 25°C	> 10 <sup>12</sup>	Ω
		V <sub>IO</sub> = 500V, 100°C ≤ T <sub>A</sub> ≤ 125°C	> 10 <sup>11</sup>	Ω
		V <sub>IO</sub> = 500V at T <sub>S</sub> = 150°C	> 10 <sup>9</sup>	Ω
	Pollution degree		2	

## 6.5 Insulation Specifications (continued)

PARAMETER		TEST CONDITIONS	VALUE	UNIT
	Climatic category		40/125/21	
<b>UL 1577 (Planned Certification Target)</b>				
$V_{ISO}$	Withstand isolation voltage	$V_{TEST} = V_{ISO} = 5000V_{RMS}$ , $t = 60s$ (qualification); $V_{TEST} = 1.2 \times V_{ISO} = 6000V_{RMS}$ , $t = 1s$ (100% production)	5000	$V_{RMS}$

- (1) Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed-circuit board do not reduce this distance. Creepage and clearance on a printed-circuit board become equal in certain cases. Techniques such as inserting grooves and/or ribs on a printed-circuit board are used to help increase these specifications.
- (2) This coupler is suitable for *safe electrical insulation* only within the maximum operating ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.
- (3) Testing is carried out in air to determine the surge immunity of the package. Testing is carried out in oil to determine the intrinsic surge immunity of the isolation barrier.
- (4) Apparent charge is electrical discharge caused by a partial discharge (pd).
- (5) All pins on each side of the barrier tied together creating a two-terminal device.

## 6.6 Electrical Characteristics

Over operating temperature range ( $T_J = -40^{\circ}C$  to  $150^{\circ}C$ ), unless otherwise noted. All typical values at  $T_A = 25^{\circ}C$  and  $V_{VIN} = 12V$ . External BOM components are listed in the pin description table.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>INPUT SUPPLY (Primary-side. All voltages with respect to GNDP)</b>						
$V_{VIN}$	Input voltage range	Primary-side input voltage to GNDP. (VDD-COM)=18V; (COM-VEE)=4V; $P_{VDD-COM} = 0.3W$ ; $P_{COM-VEE} = 0$ ; $T_A = 85^{\circ}C$ .	5.5 <sup>(1)</sup>	12	20	V
$V_{VIN}$	Input voltage range	Primary-side input voltage to GNDP. (VDD-COM)=18V; (COM-VEE)=4V; $P_{VDD-COM} = 1.3W$ ; $P_{COM-VEE} = 0$ ; $T_A = 85^{\circ}C$ .	8 <sup>(1)</sup>	12	18	V
$I_{VINQ}$	VIN quiescent current, disabled	$V_{ENA} = 0V$ ; $V_{VIN} = 5.5V-18V$ ;			600	$\mu A$
$I_{VINP\_NL}$	VIN operating current, enabled, No Load	$V_{ENA} = 5V$ ; $V_{VIN} = 5.5V-18V$ ; (VDD-COM) = 18V, (COM-VEE)=4V, regulating; $I_{VDD-COM} = I_{COM-VEE} = 0$ mA.			10	mA
$I_{VINP\_FL}$	VIN operating current, enabled, Full Load	$V_{ENA} = 5V$ ; $V_{VIN} = 12V$ ; (VDD-COM) = 18V, (COM-VEE)=4V, regulating; $I_{VDD-COM} = 83mA$ ; $I_{COM-VEE} = 0$		250		mA
<b>UVLOP COMPARATOR (Primary-side. All voltages with respect to GNDP)</b>						
$V_{VIN\_UVLO\_R}$	VIN analog undervoltage lockout rising threshold	Analog Comparator Always Active First	4	4.25	4.5	V
$V_{VIN\_UVLO\_F}$	VIN analog undervoltage lockout falling threshold	Analog Comparator Always Active First	3.8	4.04	4.28	V
<b>OVLOP COMPARATOR (Primary-side. All voltages with respect to GNDP)</b>						
$V_{VIN\_OVLO\_R}$	VIN overvoltage lockout rising threshold		21.5	22	22.5	V
$V_{VIN\_OVLO\_F}$	VIN overvoltage lockout falling threshold		20	20.3	20.6	V
<b>TSHUTP THERMAL SHUTDOWN COMPARATOR (Primary-side. All voltages with respect to GNDP)</b>						
$T_{SHUT\_P\_R}$	Primary-side over-temperature shutdown rising threshold		150	165		$^{\circ}C$
$T_{SHUT\_P\_HYST}$	Primary-side over-temperature shutdown hysteresis		15	20		$^{\circ}C$



## 6.6 Electrical Characteristics (continued)

Over operating temperature range ( $T_J = -40^{\circ}\text{C}$  to  $150^{\circ}\text{C}$ ), unless otherwise noted. All typical values at  $T_A = 25^{\circ}\text{C}$  and  $V_{VIN} = 12\text{V}$ . External BOM components are listed in the pin description table.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>ENA INPUT PIN (Primary-side. All voltages with respect to GNDP)</b>						
$V_{ENA\_R}$	Enable pin rising threshold	Rising edge	1.425	1.5	1.575	V
$V_{ENA\_F}$	Enable pin falling threshold	Falling edge	1.282	1.35	1.418	V
$I_{ENA}$	Enable Pin Input Current	$V_{ENA} = 5.0\text{V}$		5	10	$\mu\text{A}$
$t_{ENA\_LO\_RST}$	Minimum period for EN = Low to reset latch off		400			$\mu\text{s}$
$t_{ENA\_LO\_DLY}$	Minimum period required before EN = Low to reset latch off		200			$\mu\text{s}$
<b>PG OPEN-DRAIN OUTPUT PIN (Primary-side. All voltages with respect to GNDP)</b>						
$V_{PG\_L}$	PG output-low saturation voltage	Sink Current = 5mA			0.5	V
$I_{PG\_H}$	PG Leakage current	$V_{PG} = 5.5\text{V}$			5	$\mu\text{A}$
<b>PRIMARY-SIDE SOFT START</b>						
$t_{PG\_Delay}$	Deglintch time during soft start between VDD reaches regulation and power good signal (PG) is issued.		2.7	3	3.3	ms
<b>Primary-side Control (All voltages with respect to GNDP)</b>						
$f_{SW}$	Switching frequency	$V_{VIN} = 12\text{V}$ ; $V_{ENA} = 5\text{V}$ ; ( $V_{DD-COM}$ )= $18\text{V}$ , ( $COM-VEE$ )= $4\text{V}$		16.5		MHz
$t_{SSTO}$	Primary-side soft-start time-out	Timer begins when $V_{IN} > UVLOP$ and ENA = High and reset when Powergood pin indicates Good		32		ms
<b>(VDD-COM) OUTPUT VOLTAGE (Secondary-side)</b>						
$V_{VDD}$	(VDD – COM) output voltage range		15	18	20	V
$V_{VDD\_REG}$	(VDD – COM) output voltage DC regulation accuracy	Secondary-side (VDD – COM) output voltage accuracy at FBVDD, over load, line and temperature range, externally adjust with external resistor divider, within SOA range.	-1.45		1.45	%
<b>(VDD-COM) REGULATION HYSTERETIC COMPARATOR (Secondary-side)</b>						
$V_{FBVDD\_REF}$	Feedback regulation reference voltage for (VDD – COM)		2.467	2.505	2.533	V
$V_{FBVDD\_HYST}$	(VDD-COM) hysteresis comparator hysteresis settings. Hysteresis at the FBVDD pin. The value represents peak-to-peak magnitude.	Hysteresis Setting	18	20	22	mV
<b>(COM-VEE) REGULATION HYSTERETIC COMPARATOR (Secondary-side)</b>						
$V_{FBVEE\_HYST}$	(COM-VEE) hysteresis comparator settings. Hysteresis at the FBVEE pin. The value represents peak-to-peak magnitude.	Hysteresis Setting	50	60	70	mV
<b>(VDD-COM) UVLOs COMPARATOR (Secondary-side)</b>						
$V_{VDD\_UVLOS\_R}$	(VDD – COM) undervoltage lockout rising threshold	Voltage from VDD to COM, rising	3.2	3.45	3.7	V
$V_{VDD\_UVLOS\_F}$	(VDD – COM) undervoltage lockout falling threshold	Voltage from VDD to COM, falling	3	3.25	3.5	V
<b>(VDD-COM) OVLOs COMPARATOR (Secondary-side)</b>						
$V_{VDD\_OVLOS\_R}$	(VDD – COM) over-voltage lockout rising threshold	Voltage from VDD to COM, rising	22.5	23	23.5	V

## 6.6 Electrical Characteristics (continued)

Over operating temperature range ( $T_J = -40^{\circ}\text{C}$  to  $150^{\circ}\text{C}$ ), unless otherwise noted. All typical values at  $T_A = 25^{\circ}\text{C}$  and  $V_{VIN} = 12\text{V}$ . External BOM components are listed in the pin description table.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{VDD\_OVLOS\_F}$	(VDD – COM) over-voltage lockout falling threshold	Voltage from VDD to COM, falling	21.7	22.2	22.7	V
<b>(VDD-COM) UVP, UNDER -VOLTAGE PROTECTION COMPARATOR (Secondary-side)</b>						
$V_{VDD\_UVP\_R}$	(VDD – COM) under-voltage protection rising threshold, $V_{UVP} = V_{REF} \times 90\%$	At FBVDD	2.175	2.25	2.35	V
$V_{VDD\_UVP\_HYST}$	(VDD – COM) under-voltage protection hysteresis	At FBVDD		22		mV
<b>(VDD-COM) OVP, OVER-VOLTAGE PROTECTION COMPARATOR (Secondary-side)</b>						
$V_{VDD\_OVP\_R}$	(VDD – COM) over-voltage protection rising threshold, $V_{OVP} = V_{REF} \times 110\%$	At FBVDD	2.7	2.75	2.825	V
$V_{VDD\_OVP\_HYST}$	(VDD – COM) over-voltage protection hysteresis	At FBVDD		23		mV
<b>(COM-VEE) Buck-Boost Converter (Secondary Side)</b>						
$V_{VEE\_REG}$	(COM-VEE) regulation accuracy	COM-VEE=2V, with 1% feedback resistance accuracy			7.5	%
		COM-VEE=3V, 4V, 5V, with 1% feedback resistance accuracy			4.5	%
		COM-VEE=6V, 7V, 8V, with 1% feedback resistance accuracy			6.5	%
$V_{VEE\_OVLOS\_R}$	(COM-VEE) over-voltage lockout rising threshold	Voltage from COM to VEE, rising	8.8	9	9.2	V
$V_{VEE\_OVLOS\_F}$	(COM-VEE) over-voltage lockout falling threshold	Voltage from COM to VEE, falling	8.4	8.6	8.8	V
$f_{SW\_VEE}$	Switching frequency of VEE converter	VDD-COM=18V, COM-VEE=4V, 3.3uH external inductor		3.2		MHz
$I_{LIM}$	Buck boost inductor current limit, out of BSW pin	Max current limit without Vin feedforward	0.235	0.261	0.287	A
$t_{VEE\_SSTO}$	Timeout threshold to determine if the VEE soft start is succesful		1.3	1.6	2	ms
<b>(COM-VEE) UVP, UNDER -VOLTAGE PROTECTION COMPARATOR (Secondary-side)</b>						
$V_{VEE\_UVP\_F}$	(COM – VEE) under-voltage protection falling threshold	COM-VEE=2V		83		%
		COM-VEE=5V		90		%
		COM-VEE=8V		92		%
$V_{VEE\_UVP\_HYST}$	(COM – VEE) under-voltage protection hysteresis	COM-VEE=5V		85		mV
<b>(COM-VEE) OVP, OVER-VOLTAGE PROTECTION COMPARATOR (Secondary-side)</b>						
$V_{VEE\_OVP\_R}$	(COM – VEE) over-voltage protection rising threshold	COM-VEE=2V		117		%
		COM-VEE=5V		110		%
		COM-VEE=8V		108		%
$V_{VEE\_OVP\_HYST}$	(COM – VEE) over-voltage protection hysteresis	COM-VEE=5V		84		mV
<b>TSHUTS THERMAL SHUTDOWN COMPARATOR (Secondary-side)</b>						
$T_{SHUT\_S\_R}$	Secondary -side over-temperature shutdown rising threshold		150	165		$^{\circ}\text{C}$
$T_{SHUT\_S\_HYST}$	Secondary-side over-temperature shutdown hysteresis		15	20		$^{\circ}\text{C}$
<b>CMTI (Common Mode Transient Immunity)</b>						

## 6.6 Electrical Characteristics (continued)

Over operating temperature range ( $T_J = -40^{\circ}\text{C}$  to  $150^{\circ}\text{C}$ ), unless otherwise noted. All typical values at  $T_A = 25^{\circ}\text{C}$  and  $V_{VIN} = 12\text{V}$ . External BOM components are listed in the pin description table.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
CMTI	Common Mode Transient Immunity	Positive COM with respect to GNDP	250			V/ns
		Negative COM with respect to GNDP			-250	V/ns
INTEGRATED TRANSFORMER						
N	Transformer effective turns ratio	Secondary side to primary side		2.43		

(1) See the  $V_{VIN\_UVLO\_R}$  and  $V_{VIN\_UVLO\_F}$  electrical characteristics for the minimum operational  $V_{VIN}$ .

## 6.7 Safety-Related Certifications

VDE	UL
Plan to certify according to DIN EN IEC 60747-17 (VDE 0884-17)	Plan to certify under UL 1577 / CSA Component Recognition Program
Certificate planned	Certificate planned

## 7 Detailed Description

### 7.1 Overview

UCC34141-Q1 device is suitable for applications that have limited board space and require more integration. It is also suitable for very-high voltage applications, where power transformers meeting the required isolation specifications are bulky and expensive. The low-profile, low-center of gravity, and low weight provides a higher vibration tolerance than systems using large bulky transformers. The device is easy-to-use and provides flexibility to adjust both positive and negative output voltages as needed when optimizing the gate voltage for maximum efficiency while protecting gate oxide from over-stress with its tight voltage regulation accuracy.

The device integrates a high-efficiency, low-emissions isolated DC/DC converter for powering the gate drive of GaN, SiC or IGBT power devices in traction inverter motor drives, on-board-charger (OBC), server telecom rectifiers, industrial motor drives, or other high voltage DC/DC converters. This DC/DC converter can provide greater than 1.5W of power.

The integrated DC/DC converter uses switched mode operation and proprietary circuit techniques to reduce power losses and boost efficiency. Specialized control mechanisms, clocking schemes, and the use of an on-chip transformer provide high efficiency and low radiated emissions.

The integrated transformer provides power delivery throughout a wide temperature range while maintaining a 5000V<sub>RMS</sub> isolation, and an 1202V<sub>RMS</sub> continuous working voltage. The low isolation capacitance of the transformer provides high CMTI allowing fast dv/dt switching and higher switching frequencies, while emitting less noise.

The VIN supply is provided to the primary-side power controller that switches the input stage connected to the integrated transformer. Power is transferred to the secondary-side output stage, and regulated to a level set by the resistor divider connected between the VDD pin and the FBVDD pin with respect to the COMA pin. The output voltage is adjustable with external resistor divider allowing a wide (VDD – COM) range.

For optimal performance ensure to maintain the V<sub>VIN</sub> input voltage within the recommended operating voltage range. Do not exceed the absolute maximum voltage rating to avoid over-stressing the input pins.

A fast hysteretic feedback burst control loop monitors (VDD – COM) and ensures the output voltage is kept within the hysteresis with low overshoots and undershoots during load and line transients. The burst control loop enables efficient operation across full load and allows a wide output voltage adjustability throughout the whole V<sub>VIN</sub> range. The undervoltage lockout (UVLO) protection monitors the input voltage pin, VIN, with hysteresis and input filter ensuring robust system performance under noisy conditions. The overvoltage lockout (OVLO) protection monitors the input voltage pin, VIN, protects against over-voltage stress by disabling switching and reducing the internal peak voltage. Controlled soft-start timing, provided throughout the full power-up time, limits the peak input inrush current while charging the output capacitor and load.

The UCC34141-Q1 can also provide a second output rail, (COM – VEE), that is used as a negative bias for the gate drivers, allowing quicker turn-off switching for the IGBTs, and also to protect from unwanted turn-on during fast switching of SiC devices. (COM – VEE) has a simple, yet fast and efficient bias controller to ensure the positive and negative rails are regulated during the PWM switching. In this case, COM pin is used as the common reference point. The COM pin connects to the source of SiC device or emitter of an IGBT device.

A fault protection and powergood status pin provides a mechanism for the host controller to monitor the status of the DC/DC converter and provide proper sequencing of power and PWM control signals to the gate driver. Fault protection includes undervoltage, overvoltage, over-temperature shutdown, and isolated channel communication interface watchdog timer.

A typical soft-start ramp-up time is lower than t<sub>SSTO</sub>, and varies based on input voltage, output voltage, output capacitance, and load. If either output is shorted or over-loaded, the device is not able to power-up within the t<sub>SSTO</sub> soft-start time, and the device shuts down and latches off for protection. The latch can be reset by toggling the ENA pin or resetting V<sub>VIN</sub>.

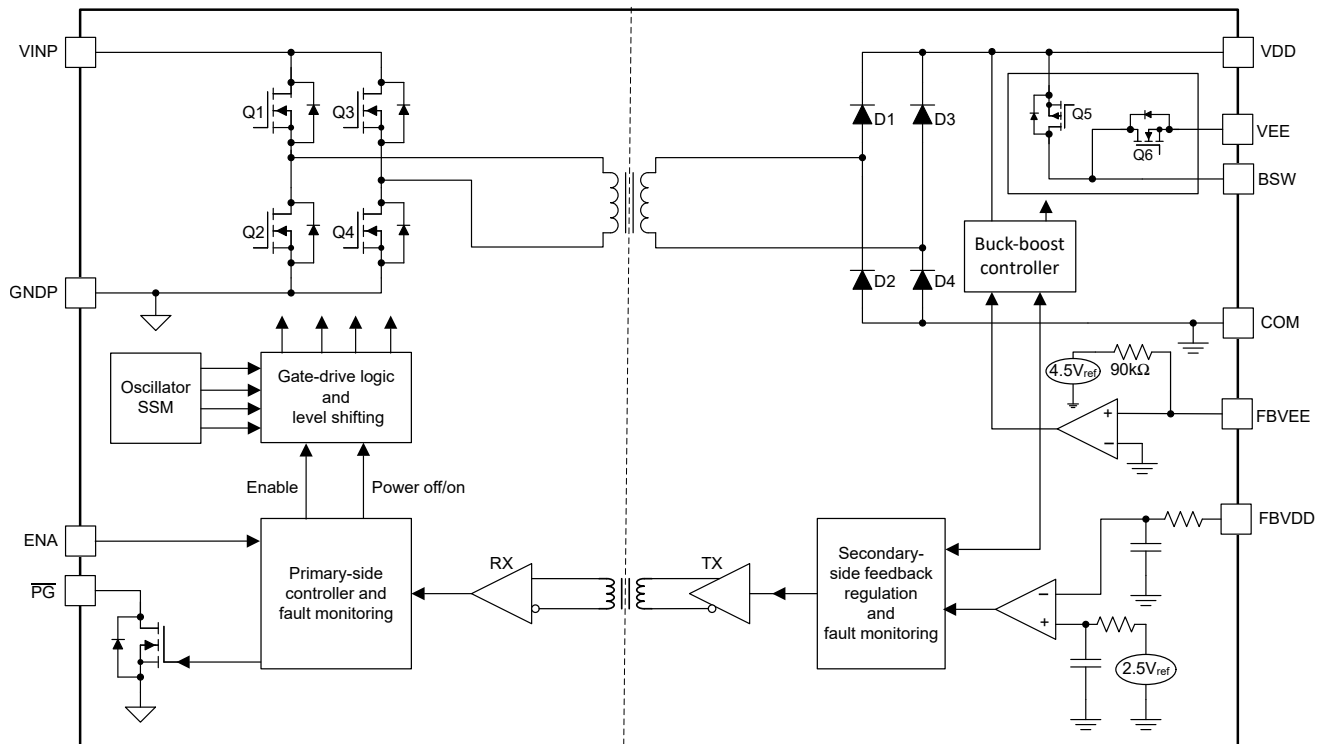
The output load must be kept low until start-up is complete and  $\overline{\text{PG}}$  pin becomes low. For successful soft-start, do not apply a heavy load to (VDD – COM) or (COM – VEE) outputs until the  $\overline{\text{PG}}$  pin has indicated power is good.

TI recommends to use the  $\overline{PG}$  status indicator as a trigger point to start the PWM signal into the gate driver.  $\overline{PG}$  output removes any ambiguity as to when the outputs are ready by providing a robust closed loop indication of when both (VDD – COM) and (COM – VEE) outputs have reached their regulation threshold within  $\pm 10\%$ .

Do not allow the host to begin PWM to gate driver until  $\overline{PG}$  goes low. This action typically occurs less than  $t_{SSTO}$  after  $V_{VIN} > V_{VIN\_UVLOP}$  and ENA goes high. The  $\overline{PG}$  status output indicates the power is good after soft-start of (VDD – COM) and (COM – VEE) and are within  $\pm 10\%$  of regulation.

If the host is not monitoring  $\overline{PG}$ , it is recommended that the host disables PWM to gate driver until 50 ms after  $V_{VIN} > V_{VIN\_UVLOP}$  and ENA goes high in order to allow enough time for power to be good after soft-start of VDD and VEE.

## 7.2 Functional Block Diagram



ADVANCE INFORMATION

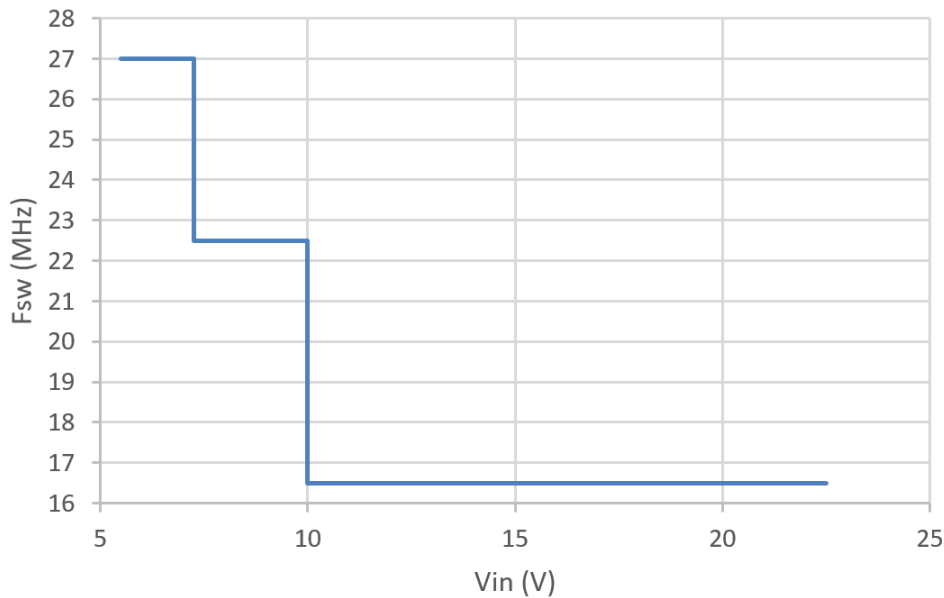
## 7.3 Feature Description

### 7.3.1 Power Stage Operation

The UCC34141-Q1 module uses a soft-switching full-bridge converter on the primary-side and a passive full-bridge rectifier on the secondary-side. The small integrated transformer operates with a high switching frequency to reduce the size for integrating into the 16-pin SSOP package. The power stage switching frequency is within 16.5MHz to 27MHz. The power stage switching frequency is determined by input voltage with a feed-forward control as illustrated by the figure below. Adaptive spread spectrum modulation, ASSM, is used to reduce emissions. ZVS operation is maintained to reduce switching power losses.

The UCC34141-Q1 module creates two regulated outputs. It can be configured as a single output converter, VDD to COM only, or a dual-output converter, VDD to COM and COM to VEE.

These two outputs are controlled independently through hysteresis control. Furthermore, the VDD to COM is the main output, and COM to VEE uses the main output as its input to create a second regulated output voltage.

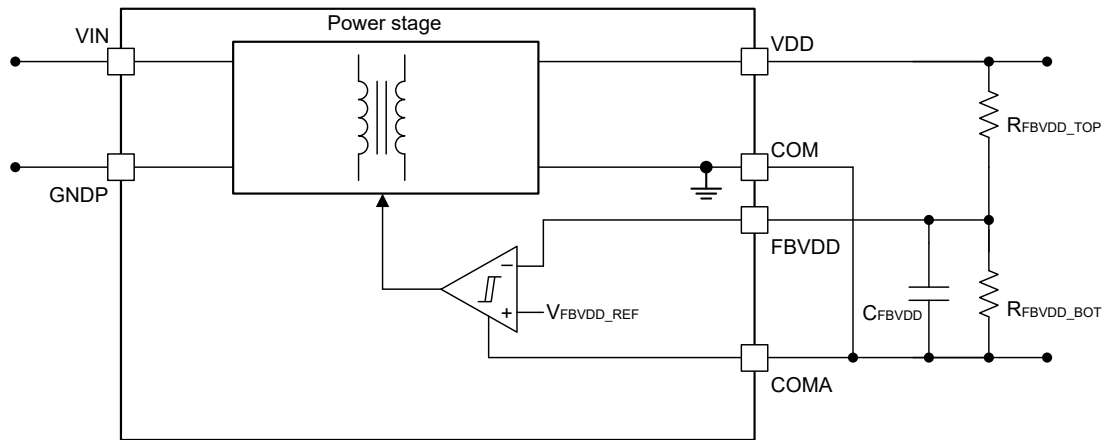


**Figure 7-1. VDD-COM Switching Frequency with Respect to Input Voltage**

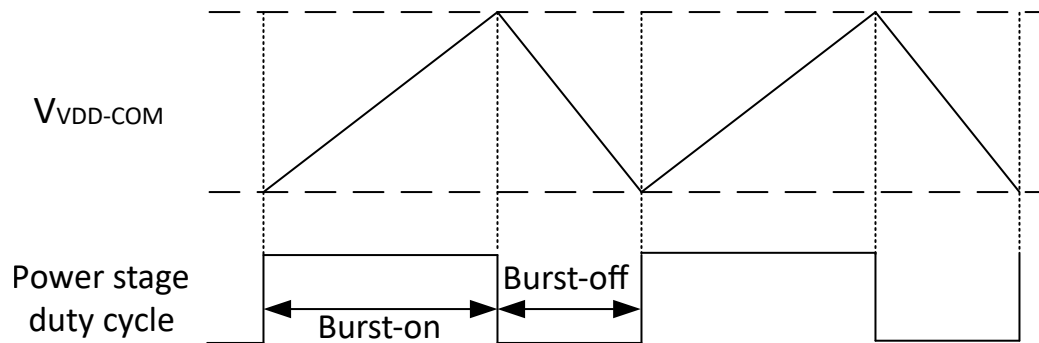
#### 7.3.1.1 VDD-COM Voltage Regulation

The VDD output is the main output of the module. The power stage operation is determined by the sensed VDD voltage on FBVDD pin using hysteresis control. The internal reference voltage  $V_{FBVDD\_REF} = 2.5V$ . The VDD voltage is sensed through a voltage divider  $R_{FBVDD\_TOP}$  and  $R_{FBVDD\_BOT}$ . When FBVDD voltage stays below the turn-off threshold, the power stage operates in burst on state, delivers power to the secondary side and makes the VDD output voltage rise. After FBVDD reaches the turn-off threshold, the power stage turns off. VDD Output voltage drops because of the load current. After FBVDD voltage drops below the turn-on threshold, the power stage is turned on again. With the accurate voltage reference and hysteresis control, the VDD output voltage can be regulated with  $\leq 1.5\%$  accuracy.

To improve the noise immunity, a small capacitor  $C_{FBVDD}$  of 220pF should be added between FBVDD and COMA pins.



**Figure 7-2. VDD-COM Voltage Regulation Functional Block Diagram**



**Figure 7-3. Concept of VDD-COM Regulation Scheme**

### 7.3.1.2 COM-VEE Voltage Regulation

An internal buck-boost converter generates the regulated negative VEE voltage. The buck-boost converter operation is determined by the sensed VEE voltage on FBVEE pin. With an internal 90k resistor and a 4.5V reference voltage, VEE voltage can be programmed and regulated between -2V to -8V.

The buck-boost converter is controlled by an integrated hysteresis voltage feedback loop for COM-to-VEE voltage regulation and an integrated current control loop for cycle-to-cycle current limit. When FBVEE voltage stays below the turn-off threshold, the buck-boost converter operates with peak current mode control. The inductor current increases at the beginning of a switching cycle until it reaches the peak current limit, then returns to zero. In normal operation, the converter operates in boundary conduction mode, but can enter continuous conduction mode during start-up. As the peak current of the buck-boost is limited to less than 300mA, the chosen inductor must have a saturation current above 300mA. As shown in the [Electrical Characteristics](#) table, the peak current limit,  $I_{LIM}$ , is implemented with a feedforward control based on VDD voltage, so that the maximum inductor current will not exceed 300mA, considering the overshoot due to the control loop delay at different VDD voltages. A higher VDD voltage leads to a bigger overshoot, and thus results in a lower  $I_{LIM}$  value for compensation. The recommended inductor selection is between 3.3uH and 10uH. The typical switching frequency is  $f_{sw\_VEE}$  as shown in the [Electrical Characteristics](#) table, with VDD-COM=18V, COM-VEE=4V, and a 3.3uH inductor.

After the FBVEE voltage reaches the turn-off threshold, the buck-boost converter turns off. After the FBVEE voltage drops below the turn-on threshold due to the load current, the buck-boost converter is turned on again. With the accurate voltage reference and hysteresis control, the VEE output voltage can be regulated with  $\leq 5\%$  accuracy.

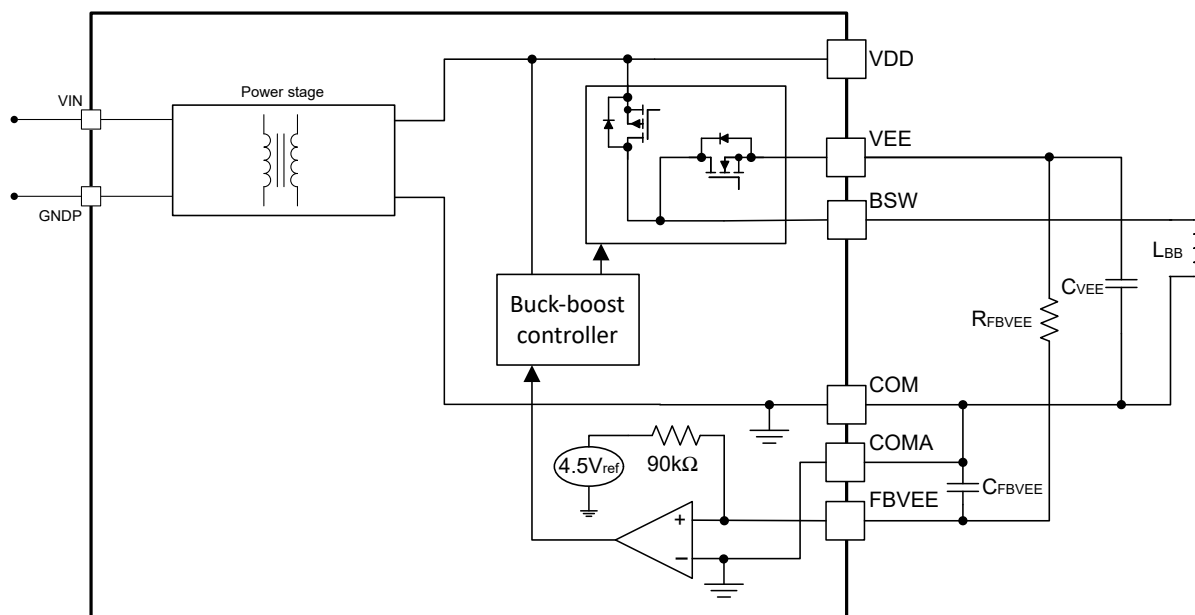
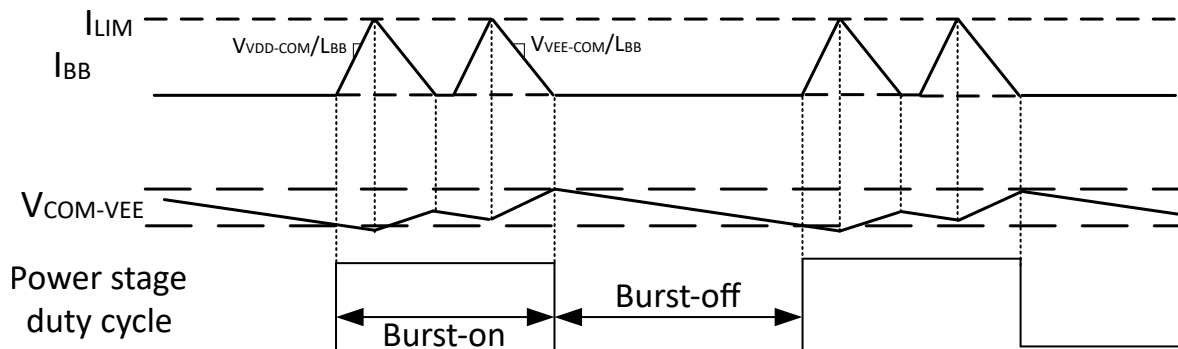


Figure 7-4. COM-VEE Voltage Regulation Functional Block Diagram





**Figure 7-5. Concept of COM-VEE Regulation Scheme**

### 7.3.2 Output Voltage Soft Start

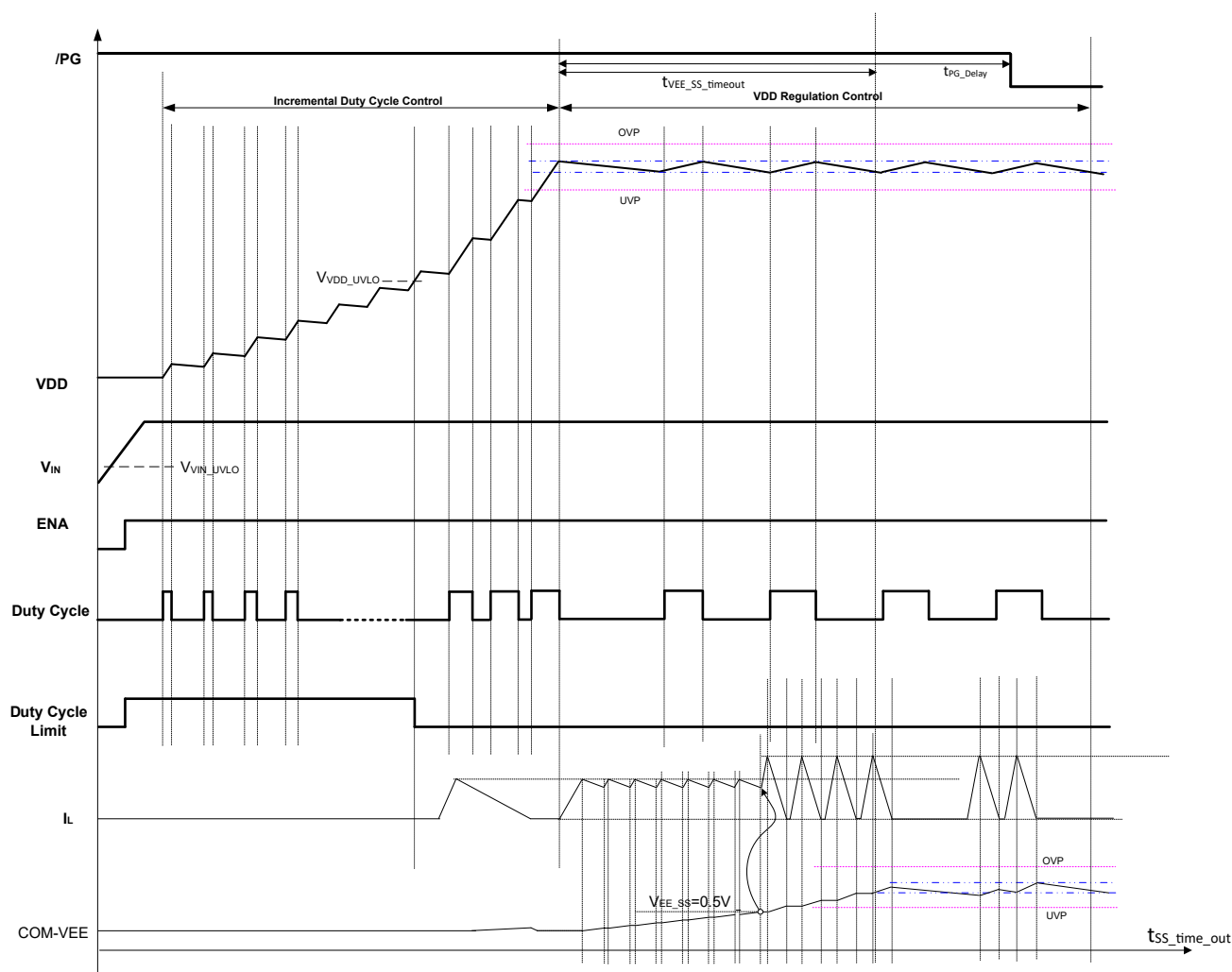
UCC34141-Q1 has soft-start mechanism that ensures a smooth and fast soft-start operation with minimum input inrush current. The output voltage soft-start diagram is shown in the figure below. After input voltage is higher than the VIN\_UVLO threshold, and the ENA signal is pulled high, the soft-start sequence starts with a primary duty cycle open loop control. The power stage operates with a fixed burst frequency with an incremental increasing duty cycle starting at 6.5%. The rate of change of the duty cycle is pre-programmed in the part to reduce the input inrush current while building the output voltage VDD. The primary side limits the maximum duty cycle to 62.5% during this phase till the secondary side VDD voltage passes VDD\_UVLO before releasing this duty cycle limit. This limit will ensure minimum input current in case the device starts on a short circuit and the VDD is not building up. Once the VDD reaches the regulation range, the duty cycle is no longer determined from the primary side controller but instead VDD hysteretic control is active to tightly regulate the output voltage within the defined hysteresis band.

When VDD passes V<sub>VDD\_UVLO</sub>, a FBVEE status check will be performed, and then a single inductor current pulse is generated for BSW pin fault detection. When VDD reaches regulation, the VEE soft start occurs with low peak current. In this way, the charge current of isolated converter can dedicatedly supply VDD cap first before the VEE soft start. The soft start process of VEE voltage has two phases. In phase 1, limited VEE soft start peak current at the beginning reduces the power loss before the soft-start timeout expires, especially when VEE pin is shorted to COM. When V<sub>COM-VEE</sub> is higher than V<sub>VEE\_SS</sub> (0.5V Typ.), the VEE soft start enters phase 2, and the inductor peak current is increased to a higher value so that the startup time of charging VEE capacitor will show faster ramp rate.

For the power good signal generation, when VDD reaches regulation, two timers of t<sub>VEE\_SSTO</sub> and t<sub>PG\_Delay</sub> are started. If VEE does not pass VEE\_UVP threshold within t<sub>VEE\_SSTO</sub> period, a fault will be triggered to flagged a failed soft start. If no fault is detected up within t<sub>PG\_Delay</sub> period, PG signal will be pulled low to indicate a power good state.

To ensure VEE reaches VEE\_UVP threshold within t<sub>VEE\_SSTO</sub> period, the sum of the COM-to-VEE output capacitance at gate driver side (C<sub>VEE\_GD</sub>) and at isolated-converter bias side (C<sub>VEE\_BIAS</sub>) should not exceed a maximum allowed value. The maximum allowed value at gate driver side (C<sub>VEE\_GD</sub>) is available in a calculation tool, as another design supporting document besides this datasheet. The equation to determine the maximum allowed capacitor value is shown as below, and is implemented in the calculation tool. In the equation, I<sub>LOAD\_SS\_VEE</sub> represents the quiescent current of output load during VEE soft start.

$$C_{VEE\_GD} \leq \frac{t_{VEE\_SSOT\_min}}{\frac{V_{VEE\_SS}}{I_{VEE\_Phase1} - I_{LOAD\_SS\_VEE}} + \frac{V_{VEE} - V_{VEE\_SS}}{I_{VEE\_Phase2} - I_{LOAD\_SS\_VEE}}} - C_{VEE\_BIAS} \quad (1)$$



**Figure 7-6. Output Voltage Soft-Start Diagram**

**Pre-production sample limitation on soft start (production devices will have the limitation removed):**

For pre-production samples, as shown in the figure below, a rising slope change during soft start may be observed on the VDD-COM waveform, when the part is enabled by toggling the ENA signal from low to high. This limitation shows no impact to the successful completion of start-up and reaching desired regulation setpoint, as long as the soft-start duration is below the soft-start timeout ( $t_{SSTO}$ ) and the VDD-COM load could be applied after  $\overline{PG}$  signal goes low. Production devices will have the limitation removed.

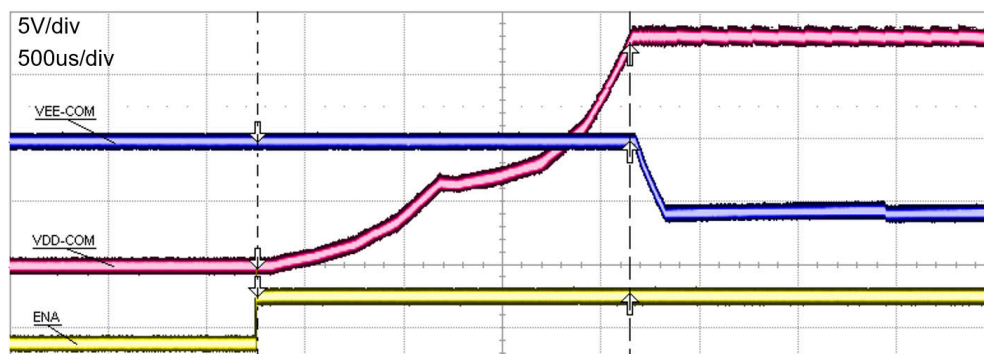


Figure 7-7. VDD-COM Rising Slope Change During Soft Start of the Pre-production Sample

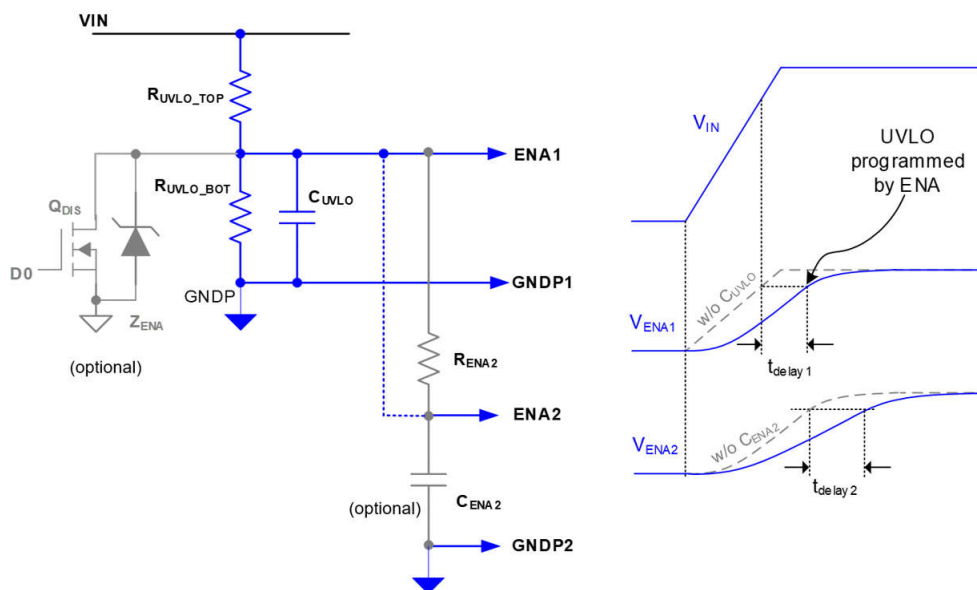
### 7.3.3 ENA and $\overline{PG}$

The ENA input pin and  $\overline{PG}$  output pin on the primary-side support both TTL and CMOS logic levels in 5V or 3.3V domain. The active-high enable input (ENA) pin is used to turn-on the isolated DC/DC converter. Either 3.3V or 5V logic rail can be used. The recommended maximum ENA-pin voltage is 5.5V. After ENA pin voltage becomes above the enable threshold  $V_{ENA\_R}$ , the power module enables, starts switching, goes through the soft-start process and delivers power to the secondary side. After ENA pin voltage falls below the disable threshold  $V_{ENA\_F}$ , UCC34141-Q1 is disabled, and the internal power stage stops switching.

The ENA pin can also be used to reset the device after it enters the protection safe-state mode. After a detected fault, the protection logic will latch off and place the device into a safe state. To reset the part, the user is required to wait for  $t_{EN\_LO\_DLY}$  after fault, and then toggle the ENA-pin voltage below  $V_{ENA\_F}$  for longer than  $t_{EN\_LO\_RST}$ , and then toggle back up to 3.3V or 5V. The device will then exit the latch-off mode and a soft-start sequence will be reinitiated.

The ENA pin can also be used to implement a programmable input UVLO by using an external resistor divider between  $V_{IN}$  and ENA pins. For the device and application with relatively low input UVLO and relatively high  $V_{IN}$ , when there is a slow  $V_{IN}$  ramp during start-up, the relatively low transformer turns-ratio will not be about to generate enough power to charge up the output capacitor and thus fail the start-up. This issue can be solved by adding a resistor divider between  $V_{IN}$ , ENA, and GNDP pins to program the ENA signal time and override the internal input UVLO. The  $V_{ENA\_R}$  rising threshold is set at 1.5V and the  $V_{ENA\_F}$  falling threshold is set at 1.35V. The programmable input UVLO feature can also be used to sequentially start-up multiple integrated DC/DC modules, by adding delay capacitors between ENA and GNDP pins to program the delay time between each power module. Specifically, the ENA1 signal can enable one module or one grouped modules, while the delayed ENA2 signal from ENA1 can sequentially enable another module or another grouped modules. For the application where ENA1 and ENA2 are too far away for the  $R_{ENA2}$  routing, the RC circuitry for ENA1 can be duplicated at the ENA pin of each module to enable sequential startup. If the sequential power up is not needed, multiple modules can share the same resistor divider to program input UVLO threshold. To facilitate the implementation, the recommended resistor and capacitor values are available in a calculation tool, as another design supporting document besides this datasheet.

If a single fault event on the resistor divider needs to be considered, e.g. the single bottom resistor is failed open, the risk of exceeding the 7V absolute maximum of ENA pin needs to be mitigated in application level. Two approaches can be applied: one option is adding an external Zener diode on ENA pin; another option is to split the bottom resistance into two resistor components.



**Figure 7-8. Input UVLO Programming Circuit and Operation Principle**

The active-low power-good ( $\overline{\text{PG}}$ ) pin is an open-drain output that indicates (short) when the module has no fault and the output voltages are within  $\pm 10\%$  of the output voltage regulation setpoints. To account for the maximum current sinking capability of the internal pull-down MOSFET  $< 5\text{mA}$ , a pull-up resistor ( $> 1\text{k}\Omega$ ) from  $\overline{\text{PG}}$  pin to either a 5V or 3.3V logic rail is recommended. Higher resistance will reduce the quiescent current in normal logic state of  $\overline{\text{PG}}$  pin. It is essential to maintain the  $\overline{\text{PG}}$  pin voltage below 5.5V without exceeding its recommended operating voltage. A  $10\text{k}\Omega$  pull-up resistor, and a  $1\mu\text{F}$  decoupling capacitor connecting  $\overline{\text{PG}}$  pin and ground are recommended to diminish the voltage drop during output voltage start up.

### 7.3.4 Protection Functions

UCC34141-Q1 is equipped with a full feature of protection functions, including input undervoltage lockout, overvoltage lockout, output undervoltage, overvoltage, and over-temperature. The input undervoltage and overvoltage lockout protections have an auto recovery response. All other protections have a latch-off response. After the latch-off-response protections are triggered, the converter enters a latch-off state, and stops switching. The latch is reset by either toggling the ENA pin Off then On, or by lowering the  $V_{\text{VIN}}$  voltage below the  $V_{\text{VIN\_UVLO\_F}}$  threshold, and then above the  $V_{\text{VIN\_UVLO\_R}}$  threshold.

#### 7.3.4.1 Input Undervoltage Lockout

The UCC34141-Q1 enters input undervoltage lockout when  $V_{\text{VIN}}$  voltage becomes lower than the UVLO threshold  $V_{\text{VIN\_UVLO\_F}}$ . In UVLO mode, the converter stops switching. After  $V_{\text{VIN}}$  pin voltage falls lower than the  $V_{\text{VIN\_UVLO\_F}}$ , UCC34141-Q1 resets all the protections. And then, after the  $V_{\text{VIN}}$  voltage rises above the UVLO threshold  $V_{\text{VIN\_UVLO\_R}}$ , the converter is enabled. Depending on the ENA pin voltage, the converter can start switching, go through the soft-start process, or in the disable mode, waiting for ENA pin voltage becomes high.

#### 7.3.4.2 Input Overvoltage Lockout

The input overvoltage lockout protection is used to protect the UCC34141-Q1 from overvoltage damage. The UCC34141-Q1 also has an auto-recovery response. When the  $V_{\text{VIN}}$  pin voltage becomes higher than the input overvoltage lockout threshold  $V_{\text{VIN\_OVLO\_R}}$ , switching stops, converter stops sending energy to the secondary side. Once  $V_{\text{VIN}}$  pin voltage drops below the recovery threshold  $V_{\text{VIN\_OVLO\_F}}$  following an overvoltage lockout, depending on the ENA pin voltage status, the converter can either resuming operation, go through the full soft-start process, or in the disabled mode, wait for ENA pin becomes high. The input overvoltage lockout does not reset other latch-off protections.

#### 7.3.4.3 Output Undervoltage Protection

The output voltage under voltage protection is based on the FBVDD and FBVEE pin voltages. When the FBVDD pin voltage falls below the UVP threshold  $V_{\text{VDD\_UVP\_F}}$ , or the FBVEE pin voltage falls below the UVP threshold  $V_{\text{VEE\_UVP\_F}}$ , the undervoltage protection is activated. The UCC34141-Q1 stops switching, and the  $\overline{\text{PG}}$  pin becomes high.

During soft start, the output voltages rise from zero volts, thus, both FBVDD and FBVEE pin voltages are below the UVP thresholds. The UVP is disabled during the soft start. If the pin voltage cannot reach the UVP recovery thresholds ( $V_{\text{VDD\_UVP\_R}}$ ,  $V_{\text{VEE\_UVP\_R}}$ ) after the soft start completes, undervoltage protection is activated, the UCC34141-Q1 stops switching, and the  $\overline{\text{PG}}$  pin becomes high.

The undervoltage protection has a latched-off response. After activation, the latch-off state can be cleared by recycling  $V_{\text{VIN}}$ . Toggling ENA pin can also reset the latch-off state. Refer to ENA and  $\overline{\text{PG}}$  section for more details.

#### 7.3.4.4 Output Overvoltage Protection

The UCC34141-Q1 senses the output voltage through FBVDD and FBVEE pins to control the output voltage. To prevent the output voltage becomes too high, damages the load or UCC34141-Q1 device, the UCC34141-Q1 is equipped with the output overvoltage protection. There are two levels of overvoltage protection, based on the feedback pin voltage, and the output voltage.

During the normal operation, because of load transient, the output voltages can exceed the regulation level. Based on the pin voltages on FBVDD and FBVEE, after the voltage exceeds the threshold,  $V_{\text{VDD\_OVP\_R}}$ , or  $V_{\text{VEE\_OVP\_R}}$ , the converter stops switching immediately.

In rare cases, the voltage divider can malfunction resulting in the wrong output voltage information. In turn, the control loop will regulate the output voltages at a wrong voltage level. For instances like this, the UCC34141-Q1 is also equipped with a fail-safe overvoltage protection. After the VDD-COM or COM-VEE voltage exceeds the overvoltage protection threshold  $V_{VDD\_OVLOS\_R}$  or  $V_{VEE\_OVLOS\_R}$ , the converter shuts down immediately. This fail-safe protection level is meant to protect UCC34141-Q1 rather than the load. The design must specify the voltage feedback divider normal operation at all conditions.

The output overvoltage protections have the latch-off response.

#### 7.3.4.5 Over-Temperature Protection

UCC34141-Q1 integrates the primary-side, secondary-side power stages, as well as the isolation transformer. The power loss caused by the power conversion causes the module temperature higher than the ambient temperature. For the safe operation of the power module, the UCC34141-Q1 is equipped with over-temperature protection. Both the primary-side power stage, and the secondary-side power stage temperatures are sensed and compared with the over-temperature protection threshold. If the primary-side power stage temperature becomes higher than  $T_{SHUT\_P\_R}$ , or the secondary-side power stage temperature becomes higher than  $T_{SHUT\_S\_R}$ , the module enters over-temperature protection mode. The module stops switching; PG pin becomes high and the module enters latch-off mode. When the power stage temperature drops below the over-temperature recovery threshold, recycling  $V_{VIN}$ , or toggling ENA pin voltage brings the module out of latch-off mode. Depending on ENA pin voltage, the module either resumes switching, delivering power to the secondary side, or in the standby mode waiting for ENA pin voltage becomes high.

#### 7.3.4.6 BSW Pin Faults Protection

UCC34141-Q1 has protection mechanism against BSW Pin faults during the soft-start period for the COM-VEE buck-boost converter.

In the case of BSW pin-open, when VDD voltage passes  $V_{VDD\_UVLOS\_R}$  threshold, the part detects the first inductor current pulse width, which is the current ramping up time until it hits the peak current limit. If the first inductor current pulse width is higher than the normal pulse width using largest inductance ( $>2.9\mu s$ ), the BSW fault protection will be triggered to disable the buck-boost switching. Then, the device will stop switching and enter into latch-off protection mode, after VDD soft start completion.

In the case of BSW pin-short to COM or VEE Pin, the part detects the inductor current at the end of leading-edge-blank period. If the current is higher than the inductor peak current limit during soft-start, the BSW fault protection will be triggered to disable the buck-boost switching. Then, the device will stop switching and enter into latch-off protection mode, after VDD soft start completion.

## 7.4 Device Functional Modes

Depending on the input and output conditions, ENA pin voltage, as well as the device temperature, the UCC34141-Q1 operates in one of the below operation modes.

1. Disable mode. In this mode, the module is off, but waiting for ENA pin becoming high to start operate.
2. Soft-start mode. In this mode, the module starts to deliver power to the secondary side. The primary-side operation duty cycle is raised gradually to reduce the stress to the module.
3. Normal operation mode. In this mode, the module operates normally, delivers power to the secondary side.
4. Protection mode, auto-recovery. In this mode, the module is off, due to the input UVLO or OVLO protection. After the input voltage fault is cleared, depending on the ENA pin voltage condition, it either becomes disabled mode if the ENA pin voltage is low, or it goes through soft-start mode to the normal operation mode.
5. Protection mode, latched-off. In this mode, the module is off, due to other protections. The module remains off even the fault causing the protection is cleared. Recycling  $V_{VIN}$  operation must ensure the input voltage goes below the analog UVLO falling threshold ( $V_{VIN\_UVLO\_F}$ ) first to reset the latch-off state, or the ENA pin is toggled Low (OFF) then High (ON).

Table 7-1 lists the supply functional modes for this device. The ENA pin has an internal weak pull-down resistance to ground, but TI does not recommend leaving this pin open.

**Table 7-1. Device Functional Modes**

INPUT			OUTPUTS			OPERATION MODE
$V_{VIN}$	ENA	FAULT	$V_{(VDD - COM)}$ Isolated Output1	$V_{(COM - VEE)}$ Isolated Output2	$\overline{PG}$ Open Drain	
$V_{VIN} < V_{VIN\_UVLO\_R}$	X	X	OFF	OFF	HIGH	Protection mode, auto-recovery
$V_{VIN\_UVLO\_R} < V_{VIN} < V_{VIN\_OVLO\_R}$	LOW	X	OFF	OFF	HIGH	Disable mode
$V_{VIN\_UVLO\_R} < V_{VIN} < V_{VIN\_OVLO\_R}$	HIGH	NO FAULT	Regulating at Setpoint	Regulating at Setpoint	LOW	Normal operation
$V_{VIN\_UVLO\_R} < V_{VIN} < V_{VIN\_OVLO\_R}$	HIGH	YES FAULT	OFF	OFF	HIGH	Protection mode, latched-off
$V_{VIN} > V_{VIN\_OVLO\_R}$	X	X	OFF	OFF	HIGH	Protection mode, auto-recovery



## 8 Application and Implementation

### Note

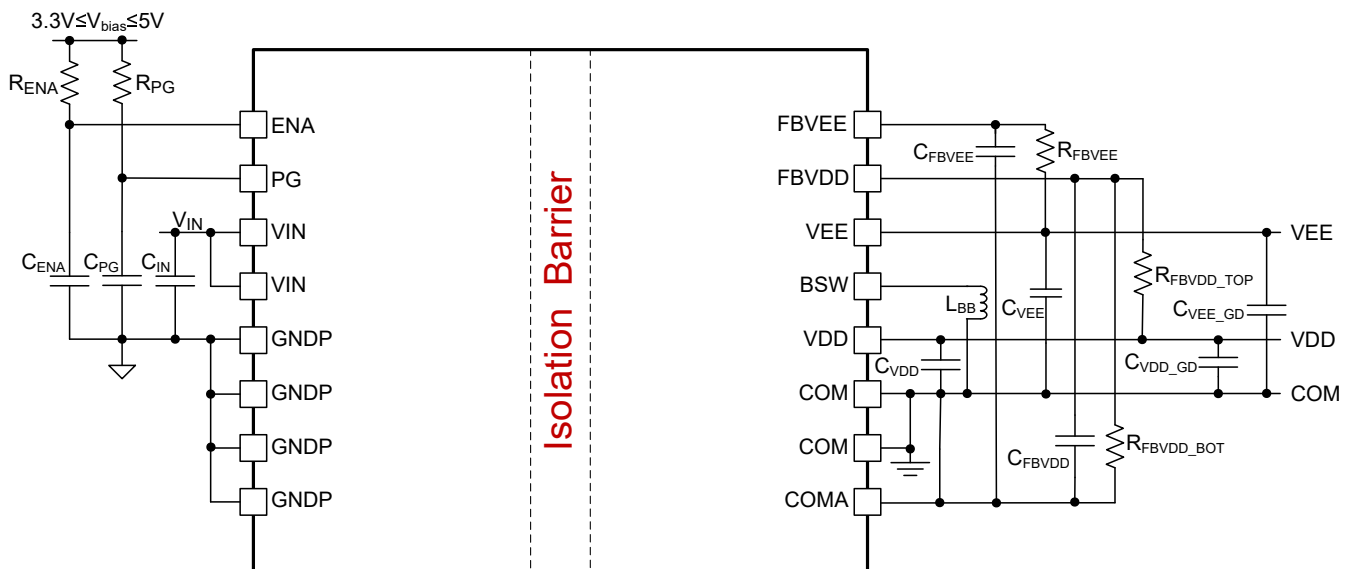
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

### 8.1 Application Information

The UCC34141-Q1 is suitable for applications that have limited board space and desire more integration. This device is also suitable for very high voltage applications, where power transformers meeting the required isolation specifications are bulky and expensive.

### 8.2 Typical Application

The following figures show the typical application schematics for the UCC34141-Q1 device configurations supplying an isolated load.



**Figure 8-1. Dual Adjustable Output Configuration**

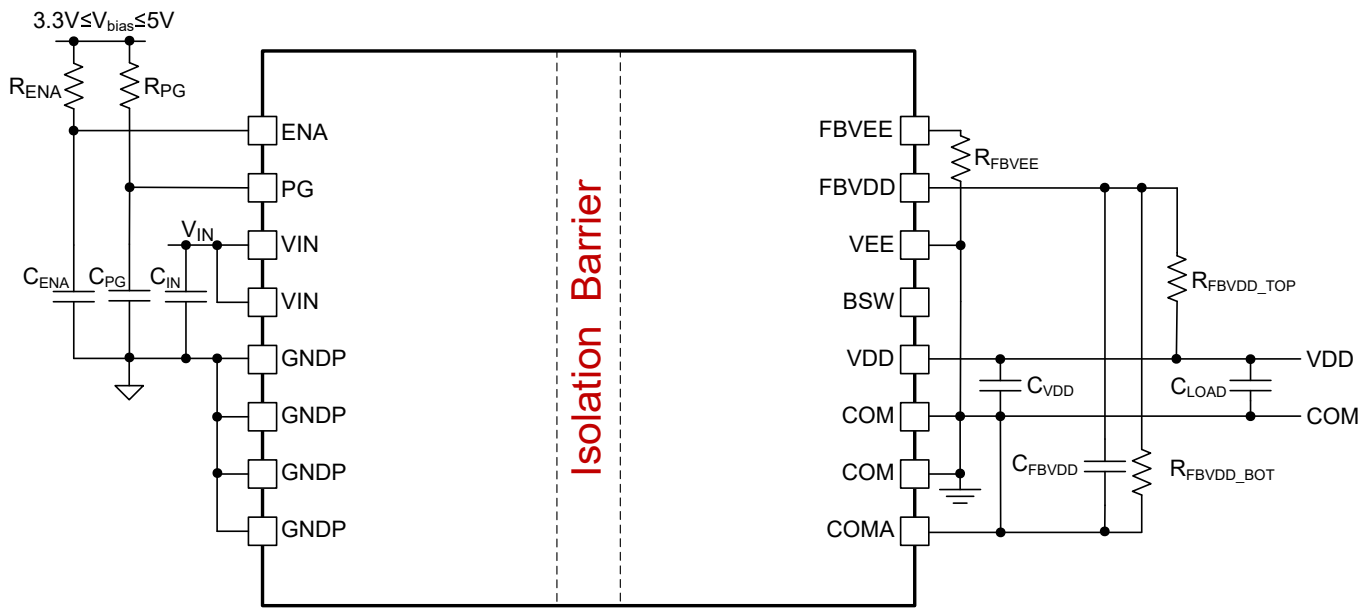


Figure 8-2. Single Adjustable Output Configuration

### 8.2.1 Design Requirements

Designing with the UCC34141-Q1 is simple. First, choose single output or dual output. Determine the voltage for each output and then set the regulation through feedback resistors. The gate charge of the power device determines the amount of output decoupling capacitance needed at the gate driver input.

For dual adjustable output configuration an internal inverting buck-boost converter generates a regulated negative rail for the turn-off supply (VEE). The buck-boost converter is controlled by a peak current mode, hysteretic controller. In normal operation, the converter remains in discontinuous-conduction mode, but can enter continuous-conduction mode during start-up. The converter is controlled internally and requires only a single surface-mount inductor ( $L_{BB}$ ) and output bypass capacitor ( $C_{VDD}$ ). Typically, the converter is designed to use a 3.3 $\mu$ H inductor and a 2.2 $\mu$ F output capacitor.

A summary table for the recommended values of BOM components is available in a calculation tool, as another design supporting document besides this datasheet.

### 8.2.2 Detailed Design Procedure

Place ceramic decoupling capacitors as close as possible to the device pins. For the input supply, place the capacitors between pin 4 (VIN) and pin 5 (GNDP). For the isolated output supply, (VDD – COM), place the  $C_{VDD}$  capacitor between pin 12 (VDD) and pin 11 (COM). For the negative voltage supply, (COM – VEE), place the  $C_{VEE}$  capacitor between pin 14 (VEE) and pin 11 (COM). These locations are of particular importance to all the decoupling capacitors because the capacitors supply the transient current associated with the fast switching waveforms of the power drive circuits. Ensure the capacitor dielectric material is compatible with the target application temperature.

### 8.2.2.1 VDD-COM Voltage Regulation

The UCC34141-Q1 creates an isolated output VDD-COM as its main output. The power stage operation is determined by sensing the VDD voltage on FBVDD pin using hysteresis control. The internal reference voltage  $V_{FBVDD\_REF} = 2.5V$ . To determine the values for  $R_{FBVDD\_TOP}$  with a chosen  $R_{FBVDD\_BOT}$ , please use the equation

$$R_{FBVDD\_TOP} = \frac{V_{VDD} * R_{FBVDD\_BOT}}{2.5V} - R_{FBVDD\_BOT} \quad (2)$$

As an example, to set a VDD value of 20V, a 10kΩ resistor can be chosen as  $R_{FBVDD\_BOT}$ , and the  $R_{FBVDD\_TOP}$  can be calculated as

$$R_{FBVDD\_TOP} = \frac{20V * 10k\Omega}{2.5V} - 10k\Omega = 70k\Omega \quad (3)$$

To improve the noise immunity, a small capacitor  $C_{FBVDD}$  of 220pF should be added between FBVDD and COMA pins.

### 8.2.2.2 COM-VEE Voltage Regulation and Single Output Configuration

UCC34141-Q1 can be configured either as a dual output or a single output converter, using the VEE feedback resistor  $R_{FBVEE}$ . The table below summarizes the programmable range with different  $R_{FBVEE}$  value. The VDD single output mode can be programmed by a  $R_{FBVEE}$  value between 300kΩ and 600kΩ. A  $R_{FBVEE}$  lower than 300kΩ could trigger VDD & VEE dual output mode, and a  $R_{FBVEE}$  higher than 600kΩ could trigger FBVEE pin-open fault. The typical application schematic of single output configuration is shown in [Figure 8-2](#)

**Table 8-1.  $R_{FBVEE}$  Programming**

$R_{FBVEE}$	0 - 7kΩ	40kΩ - 160kΩ	300kΩ - 600kΩ	>1000kΩ
Operation Mode	Trigger FBVEE pin-short fault SMD resistor with ±5% tolerance is enough	VEE in regulation, VDD & VEE dual output Recommend SMD resistor with ≤ ±1% tolerance for best regulation accuracy.	VDD single output Recommend 330 kΩ SMD resistor with ≤±5% tolerance.	Trigger FBVEE pin-open fault

An internal buck-boost converter generates the regulated negative VEE voltage. The buck-boost converter operation is determined by sensing the VEE voltage on FBVEE pin. With an internal 90k resistor and a 4.5V reference voltage, VEE voltage can be programed and regulated between -2V to -8V. The transfer function between COM-VEE and  $R_{FBVEE}$  in dual output mode is

$$R_{FBVEE} = \frac{-V_{VEE} * 90k\Omega}{4.5V} \quad (4)$$

An example equation to set a VEE regulation value at -5V

$$R_{FBVEE} = \frac{-(-5V) * 90k\Omega}{4.5V} = 100k\Omega \quad (5)$$

**Pre-production sample limitation on  $R_{FBVEE}$  (production devices will have the limitation removed):**

**An 110% correction factor needs to be applied to compensate the VEE regulation offset in the pre-production sample, using the relationship of  $R_{FBVEE\_Pre-Production} = R_{FBVEE\_Production} / 1.1$ .**

**Taking the above example , to set a VEE regulation value at -5V, the VEE feedback resistor value for the pre-production sample should be  $100k\Omega / 1.1 = 90.9k\Omega$ .**

## ADVANCE INFORMATION

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## 8.4 Power Supply Recommendations

The recommended input supply voltage ( $V_{VIN}$ ) for UCC34141-Q1 is between 5.5V and 20V. To help ensure reliable operation, adequate decoupling capacitors must be located as close to supply pins as possible. Local bypass capacitors must be placed between the VIN and GNDP pins at the input; between VDD and COM, and between COM and VEE at the output. TI recommends low ESR, ceramic surface mount capacitors to provide the recommended capacitance for high frequency decoupling. The input supply must have an appropriate current rating to support output load required by the end application.

## 8.5 Layout

### 8.5.1 Layout Guidelines

The UCC34141-Q1 integrated isolated power solution simplifies system design and reduces board area usage. Follow these guidelines for proper PCB layout to achieve optimum performance. A minimum of 4-layer PCB layer stack using 2 ounce copper on external layers is recommended to accomplish a good thermal PCB design.

1. Input capacitors between VIN pin and GNDP pin:
  - a. Place the 0.1 $\mu$ F high frequency bypass capacitor (C3) as close as possible to pins 3, 4 (VIN) and pins 5–8 (GNDP) and on the same side of the PCB as the IC. 0402 ceramic SMD or smaller is a desired size for optimal placement. The self-resonant frequency in a range between 10MHz to 30MHz is most ideal to offer low impedance decoupling for the switching frequency noise of the internal isolated converter. Do not place any vias between the bypass capacitor and the IC pins so as to force the high frequency current through the capacitor.
  - b. Place the bulk VIN capacitor(s) (C2) as close as possible and parallel to the 0.1 $\mu$ F high frequency bypass capacitor (C3) and on the same side of the PCB as the IC.
2. Output capacitors between VDD pin and COM pin:
  - a. Place the 0.1 $\mu$ F high frequency bypass capacitor (C5) as close as possible to pin 12 (VDD) and pins 10, 11 (COM) and on the same side of the PCB as the IC. 0402 ceramic SMD or smaller is a desired size for optimal placement. The self-resonant frequency in a range between 10MHz to 30MHz is most ideal to offer low impedance decoupling for the switching frequency noise of the internal isolated converter. Do not place any vias between the bypass capacitor and the IC pins so as to force the high frequency current through the capacitor.
  - b. Place the bulk VDD-COM capacitor (C8) as close as possible and parallel to the 0.1 $\mu$ F high frequency bypass capacitor (C5) and on the same side of the PCB as the IC.
3. Output capacitors between VEE pin and COM pin:
  - a. Place the 2.2 $\mu$ F high frequency bypass capacitor as close as possible to VEE and COM pins. The self-resonant frequency in 3MHz to 4MHz is most ideal to offer low impedance decoupling for the switching frequency noise of the buck-boost converter with the 3.3 $\mu$ H inductor selection. It is possible to put the capacitor on the different side of PCB and use via to connect, in order to reduce the switching loop between the internal low-side MOSFET and the capacitor. In addition, putting the capacitor on different side will also simplify the decoupling capacitor placement of VDD pin and COM pin.
4. Gate driver output capacitors:  $C_{VDD\_GD}$  and  $C_{VEE\_GD}$  are reference designators referred to in the Excel calculator tool.  $C_{VDD\_GD}$  is the capacitor(s) between VDD-COM and  $C_{VEE\_GD}$  is the capacitor(s) between COM-VEE.  $C_{VDD\_GD}$  and  $C_{VEE\_GD}$  are capacitors required by the gate driver IC.
  - a.  $C_{VDD\_GD}$  and  $C_{VEE\_GD}$  should be placed next to the gate driver IC for best decoupling and gate driver switching performance.
5. Feedback:
  - a. COMA should be isolated through all PCB layers, from the COM plane. Use one via to make a direct connection to the low-side resistor and filter capacitor from FBVDD pin, same as the low-side filter capacitor from FBVEE pin.
  - b. Place the  $R_{FBVDD}$  feedback resistors (R6 and R7) and the decoupling ceramic capacitor (C6) close to the IC.

- c. The top-side feedback resistor should be placed next to the low-side resistor with a short, direct connection between both resistors and single connection to FBVDD pin. The top connection to sense the regulated rail (VDD-COM) should be routed and connected at the VDD bias capacitor remote location near the gate driver pins for best accuracy and best transient response.
  - d. The VEE feedback resistor (R5) should be placed with the decoupling ceramic capacitor (C4) next to FBVEE (pin 15); while the connection to sense the regulated rail (COM-VEE) should be routed and connected at the COM bias capacitor remote location near the gate driver pins for best accuracy and best transient response.
  - e. When using the dual output mode, the buck-boost inductor and a 2.2uF decoupling ceramic capacitor must be populated. They can be place on the opposite side of the IC or on the same layer as IC.
  - f. A layout example is shown in [Figure 8-5](#). Please refer to the user's guide for more details.
6. Thermal Vias: The UCC34141-Q1 internal transformer makes a direct connection to the lead frame. It is therefore critical to provide adequate space and proper heatsinking designed into the PCB as outlined in the steps below.
- a. TI recommends to connect the VIN, GNDP, VDD, and COM pins to internal ground or power planes through multiple vias. Alternatively, make the polygons connected to these pins as wide as possible.
  - b. Use multiple thermal vias connecting PCB top side GNDP copper to bottom side GNDP copper. If possible, it is recommended to use 2 ounce copper on external top and bottom PCB layers.
  - c. Use multiple thermal vias connecting PCB top side VEE copper to bottom side VEE copper. If possible, it is recommended to use 2 ounce copper on external top and bottom PCB layers.
  - d. Thermal vias connecting top and bottom copper can also connect to internal copper layers for further improved heat extraction.
  - e. Thermal vias should be similar to pattern shown below but apply as many as the copper area will allow. TI recommends to use thermal via with 30mil diameter, 12mil hole size.
  - f. A layout example is shown in [Figure 8-6](#).
7. Creepage clearance: Avoid routing copper under the UCC34141-Q1 , to maintain the full creepage, clearance and voltage isolation ratings specified in the data sheet. Maintain the clearance width highlighted in red, throughout the entire defined isolation barrier. Keep-out clearance for basic isolation can be 50% less than the reinforced isolation requirement (8.2mm). Using 8.2mm provides additional margin. A layout example is shown in [Figure 8-7](#).
8. Gate driver capacitors and feedback routing:
- a. VDD-COM and VEE-COM gate driver capacitors need to be placed as close to the associated gate driver pins as possible.
  - b. For optimal voltage regulation, the feedback trace from VEE (VEE FB) and VDD (VDD FB) should be as direct as possible so that the voltage feedback is being sensed directly at the VDD and VEE capacitors near the gate driver IC.

### 8.5.2 Layout Example

The layout example shown in the following figures is based on the [Figure 8-1](#) design.

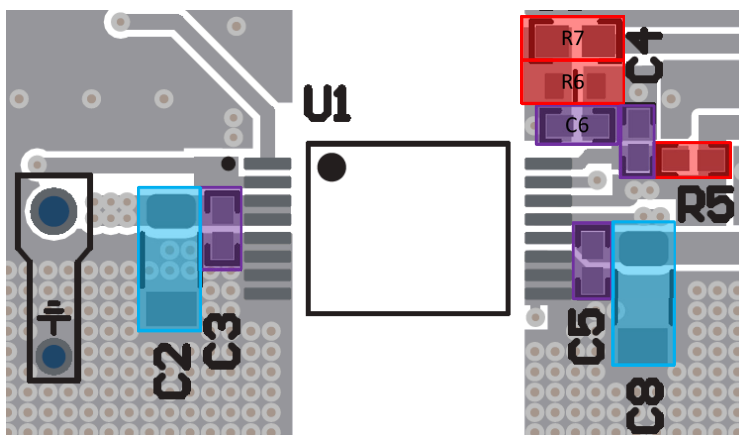


Figure 8-5. Layout Example of Components Locations

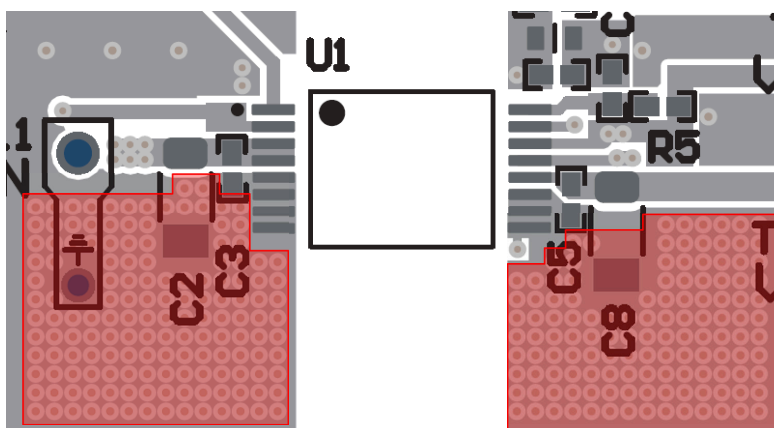


Figure 8-6. Layout Example of Thermal Vias

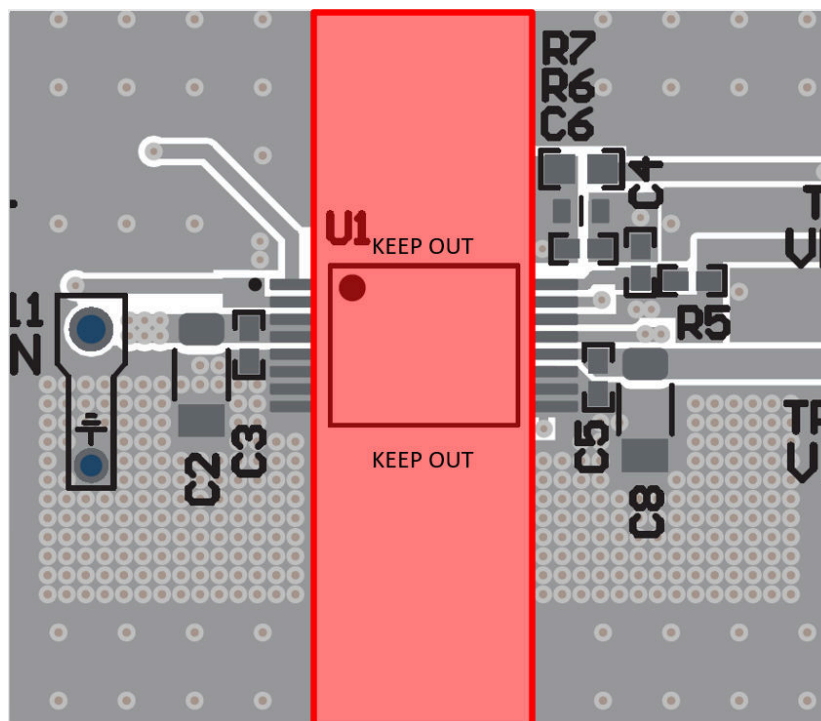


Figure 8-7. Layout Example of Keep Out Clearance



## 9 Device and Documentation Support

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### 9.2 Documentation Support

#### 9.2.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, [Isolation Glossary](#)

### 9.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](#). Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

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ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### 9.7 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

## 10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
April 2024	*	Advance Information release

## 11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

TI recommends to install the device with JEDEC standard J-STD-020 reflow process. The peak solder temperature should not exceed 260°C. If manual installation is needed during testing process, TI recommends to limit the peak temperature not exceeding 260°C.

## 11.1 Packaging Information

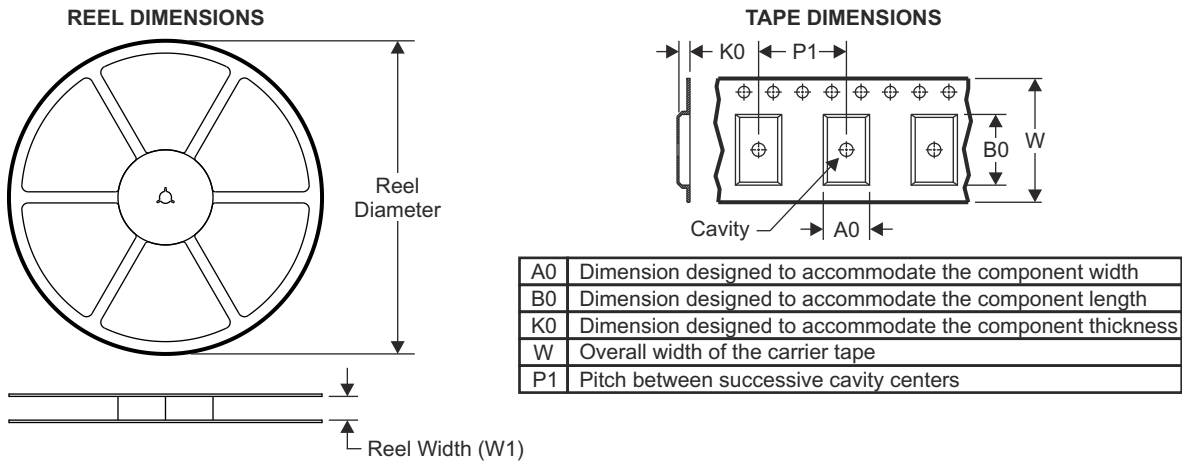
Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead finish/ Ball material <sup>(6)</sup>	MSL Peak Temp <sup>(3)</sup>	Op Temp (°C)	Device Marking <sup>(4) (5)</sup>
PUCC34141QD HARQ1	PREVIEW	SSOP	DHA	16					-40 to 125	

- (1) The marketing status values are defined as follows:  
**ACTIVE:** Product device recommended for new designs.  
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.  
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design. **PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.  
**OBSOLETE:** TI has discontinued the production of the device.
- (2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".  
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.  
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.
- (3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.
- (4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.
- (5) Multiple Device markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.
- (6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

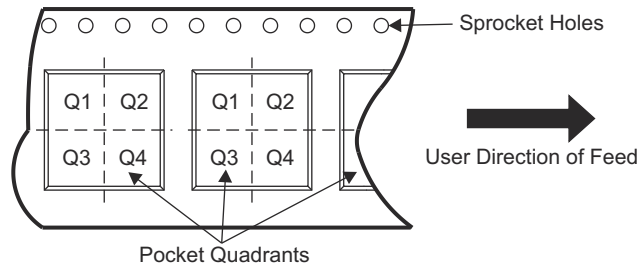
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## 11.2 Tape and Reel Information

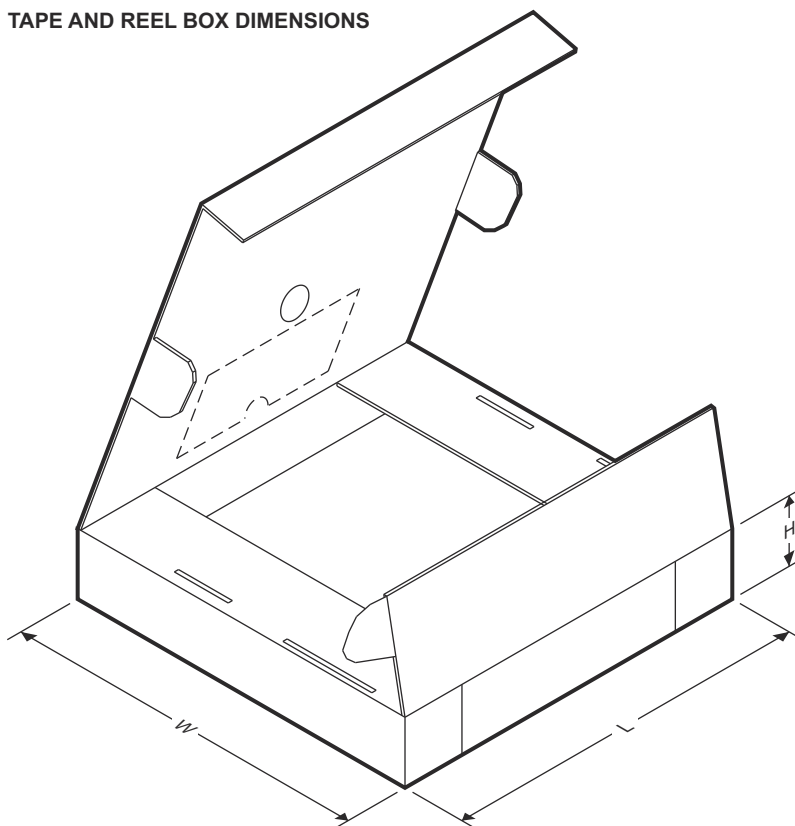


### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
PUCC34141QDHARQ1	SSOP	DHA	16									

TAPE AND REEL BOX DIMENSIONS



Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
PUCC34141QDHARQ1	SSOP	DHA	16				

ADVANCE INFORMATION

## 11.3 Mechanical Data

ADVANCE INFORMATION

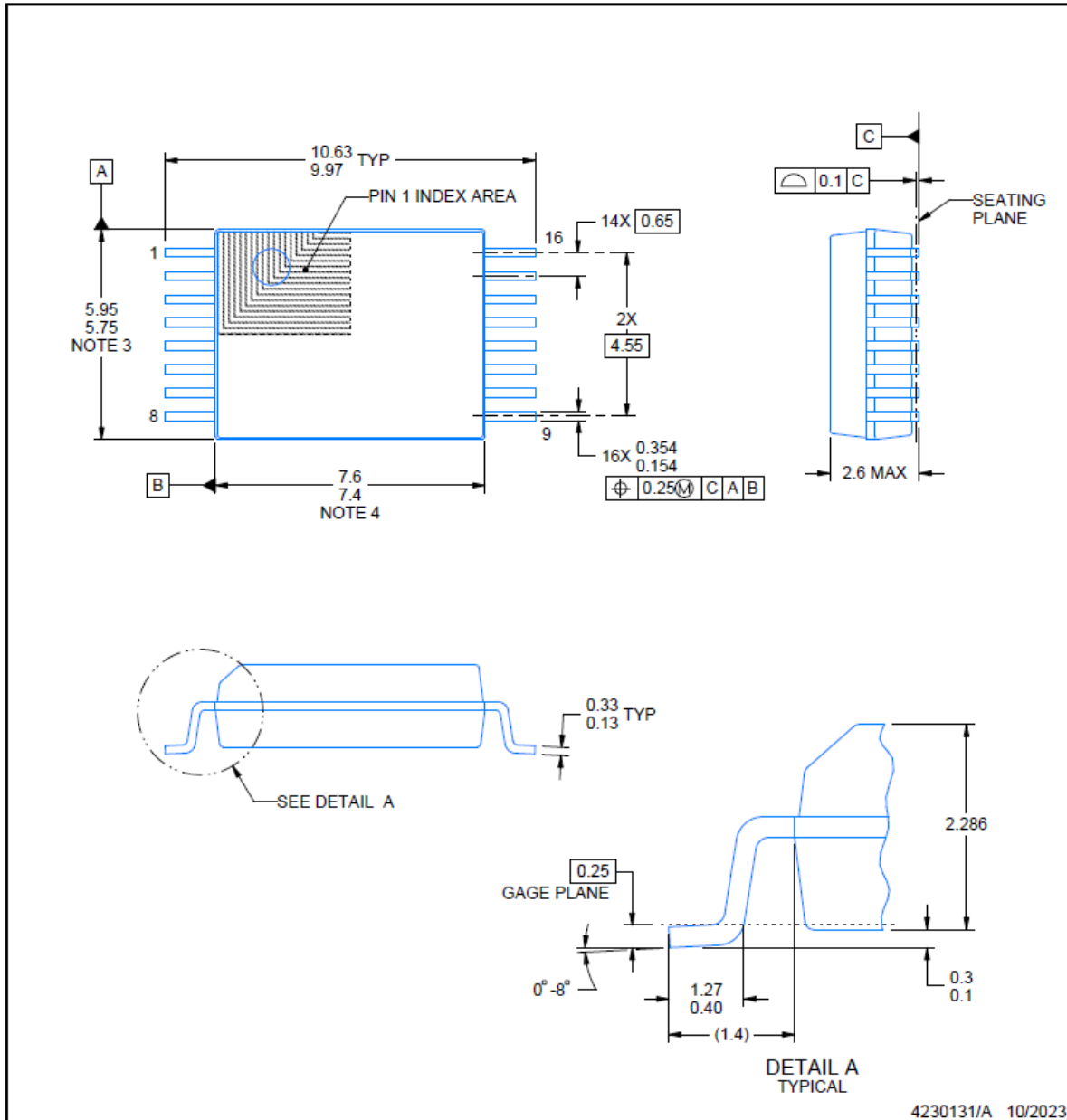
DHA0016A



### PACKAGE OUTLINE

SSOP - 2.6 mm max height

SMALL OUTLINE PACKAGE



#### NOTES:

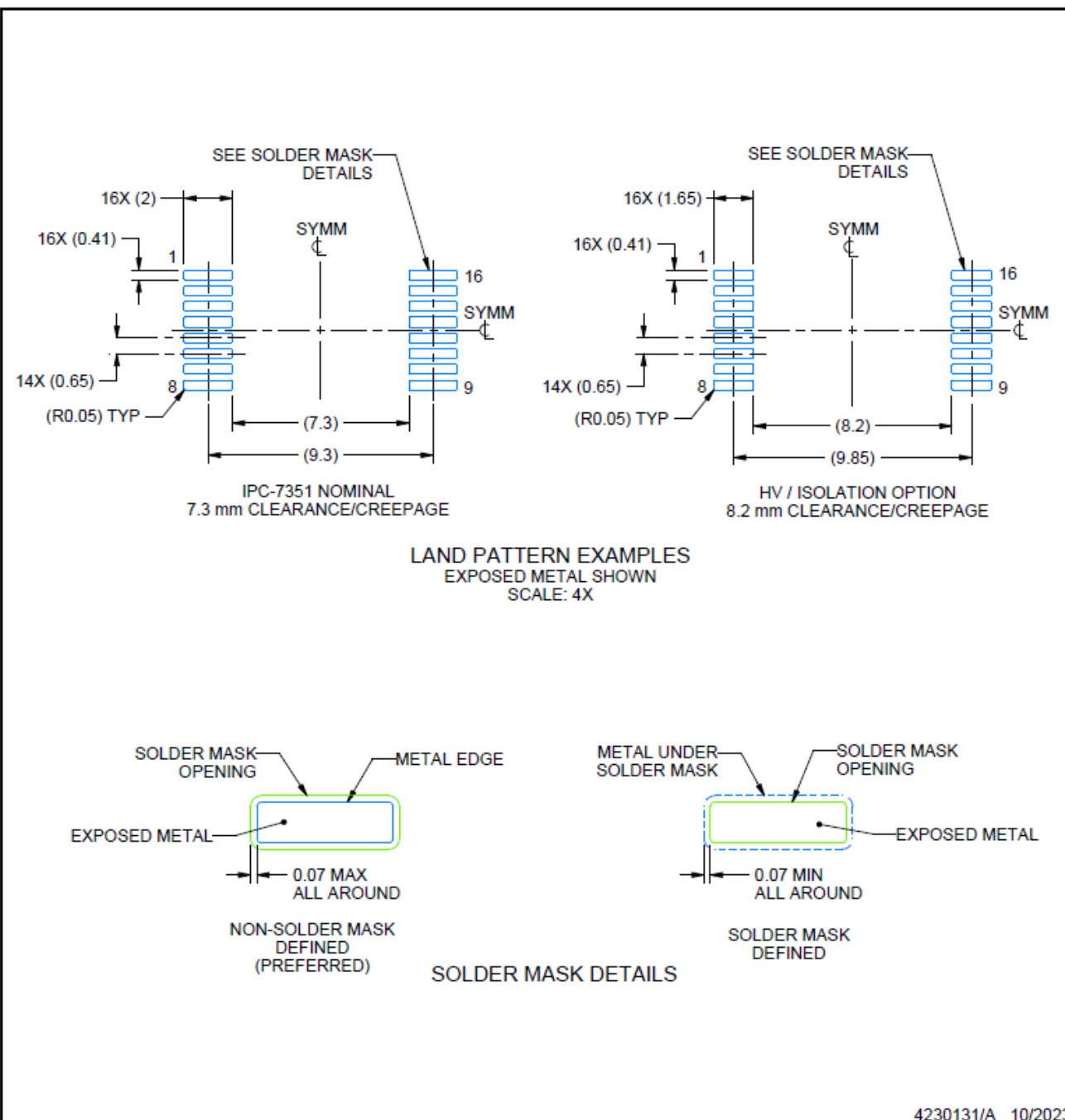
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.

## EXAMPLE BOARD LAYOUT

**DHA0016A**

**SSOP - 2.6 mm max height**

SMALL OUTLINE PACKAGE



ADVANCE INFORMATION

NOTES: (continued)

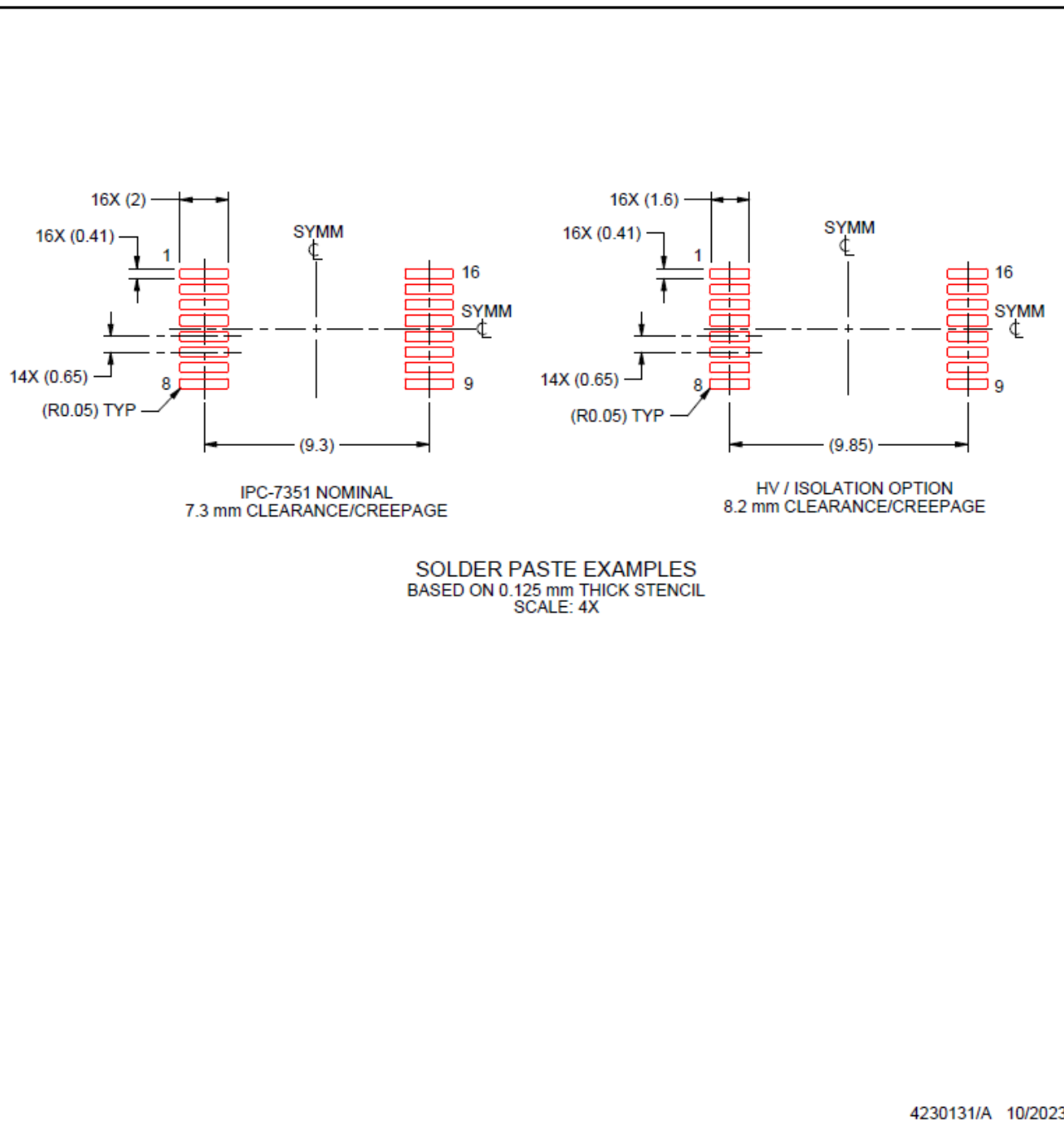
- Publication IPC-7351 may have alternate designs.
- Solder mask tolerances between and around signal pads can vary based on board fabrication site.

## EXAMPLE STENCIL DESIGN

**DHA0016A**

**SSOP - 2.6 mm max height**

SMALL OUTLINE PACKAGE



NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.



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