TEXAS INSTRUMENTS
UCC28781-Q1
SLUSEI6 – NOVEMBER 2021

UCC28781-Q1 Zero-Voltage-Switching Flyback Controller with Dedicated Synchronous Rectifier Gate-Drive

1 Features

- AEC-Q100 qualified for automotive applications:
  - Temperature grade 1, T_A: –40°C to 125°C
  - Device HBM ESD classification level 2
  - Device CDM ESD classification level C2A
- Functional Safety Capable
  - Documentation available to aid functional safety system design
- Switching frequency: > 500 kHz
- Enables peak efficiency > 93 %
- Enables < 50 mW stand-by power (basic systems)
- Adaptive control for zero voltage switching (ZVS) and dead time optimization
- EMI frequency dithering without trade-offs on transient response or audible noise
- Programmable adaptive burst mode (ABM) with internal compensation
- Over-temperature, overvoltage, output short-circuit, overcurrent, over-power, and pin-fault protections
- Auto-recovery fault-response
- 4 mm × 4 mm, 24-pin, QFN package

2 Applications

- Traction Inverters
- Auxiliary Bias Supply
- DC Portable Charger
- DC or AC Charging (pile) Station
- DC/DC Converter

3 Description

The UCC28781-Q1 is a zero-voltage-switching (ZVS) controller which can be used at very high switching frequencies to minimize the size of the transformer and enable high power density.

With direct synchronous rectifier (SR) control, the controller does not need a separate SR controller, as it can drive the SR FET directly to maximize efficiency and simplify design. (For isolated applications, an isolated gate-driver IC is required.)

Using adaptive dead-time control for ZVS, switching losses and EMI are minimized. This design results in a controller with extremely high conversion efficiency across the entire operating range.

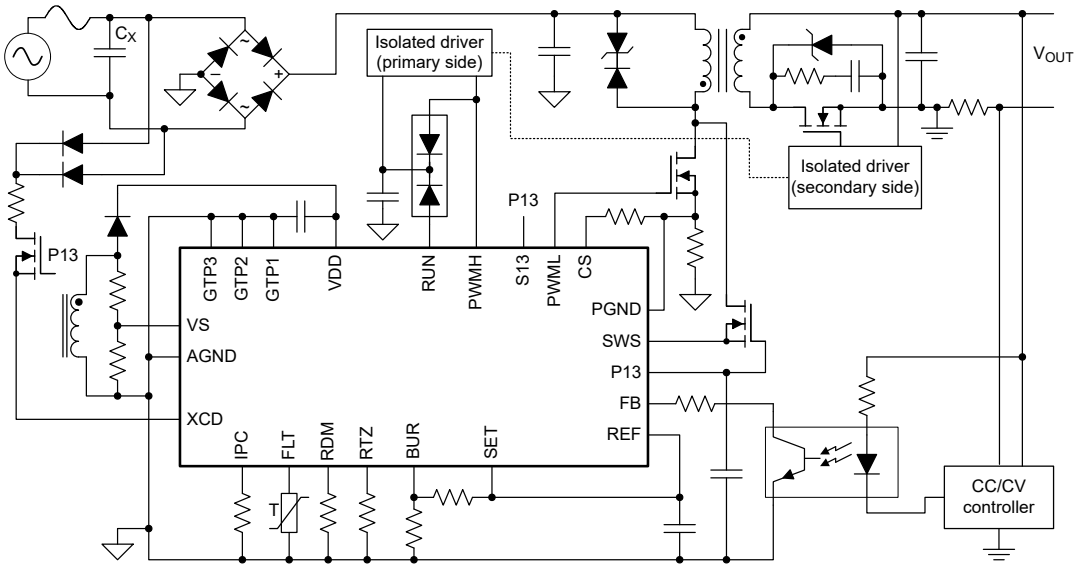
The programmable adaptive burst mode (ABM) gives flexibility to control when the controller enters and exits standby mode to optimize standby power in light and no-load conditions. ABM also helps to reduce ripple and minimize audible noise.

The controller offers multiple protection modes with automatic restart (retry) responses.

Device Information

PART NUMBER	PACKAGE(1)	BODY SIZE
UCC28781-Q1	WQFN (24)	4.00 mm × 4.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



Simplified Application

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
November 2021	*	Initial release.

5 Pin Configuration and Functions

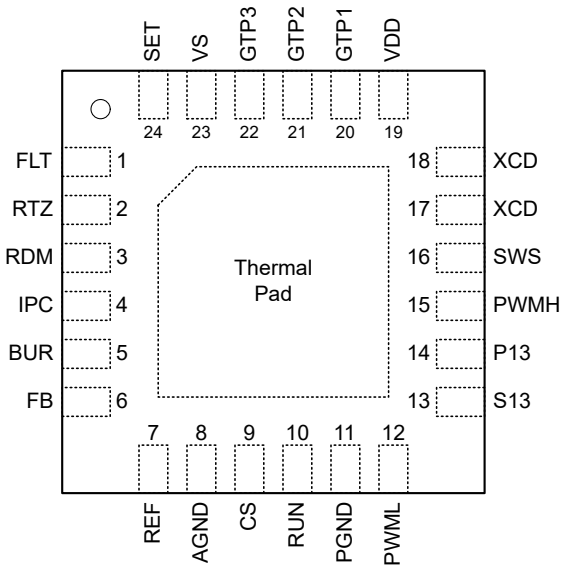


Figure 5-1. RTW Package, 24-Pin WQFN (Top View)

Table 5-1. Pin Functions

PIN		TYPE[1]	DESCRIPTION
NAME	NO.		
FLT	1	I	The controller enters into the fault state if the FLT-pin voltage is pulled above 4.5 V or below 0.5 V. A 50-µA current source interfaces directly with an external NTC (negative temperature coefficient) thermistor to AGND pin for remote temperature sensing. The current source is active during the run state and inactive during the wait state. A 50-µs fault delay allows a filter capacitor to be placed on the FLT pin without false triggering the 0.5-V OTP fault when the controller enters into a run state from a wait state. Alternatively, a high-resistance voltage divider can be used to sense the bulk input capacitor voltage for line-OVP detection, and a 750-µs fault delay helps to prevent false triggering the 4.5-V input line-OVP from a short-duration bulk capacitor voltage overshoot during line surge and ESD strike events. When FLT-pin voltage is used for line-OVP detection, the external OTP can be implemented on CS pin.
RTZ	2	I	A resistor between this pin and AGND pin programs an adaptive delay for transition to zero voltage from the turn-off edge of the PWMH signal to the turn-on edge of the PWML signal. Parasitic capacitance between this pin and any other net, including AGND, must be minimized to avoid noise coupling and its effect on the dead-time calculation.
RDM	3	I	A resistor between this pin and AGND pin programs a synthesized demagnetization time used to control the on-time of the PWMH signal to achieve zero voltage switching on the primary switch. The controller applies a voltage on this pin that varies with the output voltage derived from the VS pin signal. Parasitic capacitance between this pin and any other net, including AGND, must be minimized to avoid noise coupling and its effect on the internal PWMH on-time calculation.
IPC	4	I	This pin is an intelligent power control (IPC) pin to optimize the converter efficiency. A 50-µA current source directly interfaces with a resistor (R_{IPC}) to AGND pin to program an increase in the peak current level at very light load; the burst frequency can be further reduced, helping to achieve low standby power and tiny-load power. If the IPC pin is connected to AGND without R_{IPC}, the peak current level in very light load is set to a minimum level for the output ripple or audible noise sensitive designs. R_{IPC} can also be connected between this pin and the CS pin or IPC pin can be directly connected to CS pin, so the 50-µA IPC current can create an output voltage dependent offset voltage on the CS pin for reducing output ripple in adaptive burst mode and improving light-load efficiency at lower output voltage level of a wide output voltage range design.
BUR	5	I	This pin is used to program the burst threshold of the converter at light load. A resistor divider between REF and AGND is used to set a voltage at BUR to determine the peak current level when the converter enters adaptive burst mode (ABM). In addition, the Thevenin resistance on BUR is used to activate offset voltages for smooth mode transitions. A 2.7-µA pull up current increases the peak current threshold when the converter enters low-power mode (LPM) from ABM. A 5-µA pull down current reduces the peak current threshold when the converter enters into high-power mode (adaptive amplitude modulation, AAM) from ABM.

Table 5-1. Pin Functions (continued)

PIN		TYPE[1]	DESCRIPTION
NAME	NO.		
FB	6	I	A current signal is coupled to this pin to close the converter regulation feedback loop. This pin presents a 4.25-V output that is designed to have 0-µA to 75-µA current pulled out of the pin corresponding to the converter operating from full-power to zero-power conditions. A 220-pF filter capacitor between FB pin and REF pin is recommended to desensitize the feedback signal from noise interference.
REF	7	O	This pin is a 5-V reference output that requires a 0.22-µF ceramic bypass capacitor to the AGND pin. This reference is used to power internal circuits and can supply a limited external load current. Pulling this pin low shuts down PWM action and initiates a VDD restart.
AGND	8	G	Analog ground and the ground return of PWMH and RUN drivers. Return all analog control signals to this ground.
CS	9	I	This is the current-sense input pin. This pin couples to the current-sense resistor through a line-compensation resistor to control the peak primary current in each switching cycle. An internal current source on this pin, proportional to the converter's input voltage, creates an offset voltage across the line-compensation resistor to balance the over-power protection (OPP) threshold level across input line. The CS pin can also provide an alternative OTP function, when the FLT pin is being used for the line input-OVP. A small-signal diode in series with an NTC resistor is connected between PWMH pin and CS pin to form the OTP detection. When PWMH is high, the NTC resistor and the line-compensation resistor become a resistor divider from 5 V and creates a temperature dependent voltage on CS pin. When CS pin voltage is higher than 1.2 V in PWMH on state for 2 consecutive cycles, the OTP fault on CS pin is triggered.
RUN	10	O	This output pin is high when the controller is in the run state. This output is low during start-up, wait, and fault states. A 2.2-µs timer delays the initiation of PWML switching after this pin has gone high and S13-pin voltage is above its 10-V power-good threshold. The pull-up driving capability of both RUN and PWMH pins allows bias power management of a digital isolator through a common-cathode small-signal diode, so the power consumption can be reduced in the wait state.
PGND	11	G	Low-side ground return of the PWML driver to the primary switch. The internal level shifter allows the common return impedance to be eliminated and improves higher frequency operation by decoupling the additional voltage spike on the current-sense resistor and layout parasitic inductance of the gate driving loop. For a silicon (Si) power FET, this pin can be connected to the source for a smaller gate driving loop. For a GaN power IC with a logic PWM input, this pin can be connected to AGND. For a GaN-based gate-injection transistor (GIT), this pin can be directly connected to the separate source pin of a GIT GaN device, which enhances the turn-off speed.
PWML	12	O	Primary switch gate driver output. The high-current capability (-0.5A/+1.9A) of PWML enables driving of a silicon power MOSFET with higher capacitive loading, a GIT GaN with continuous on-state current, or a GaN power IC with logic input. The maximum voltage level of PWML is clamped to the P13 pin voltage.
S13	13	O	S13 is a switched bias-voltage source coupled to P13 through an internal 2.8-Ω switch controlled by the RUN pin. When RUN is high, the S13 decoupling capacitor is charged up to 13 V by an internal current limiter. The S13 pin voltage must increase above 10 V to initiate PWML switching. When RUN is low, S13 is discharged by its load. The power-on delay of any device powered by S13 must be less than 2 µs to be responsive to PWML. A 22-nF ceramic capacitor between S13 and the driver ground is recommended. S13 can also perform power management on a PFC controller at the same time through a diode, such that PFC can be disabled at very light-load condition.
P13	14	O	P13 is a regulated 13-V bias-voltage source derived from V_{VDD}. During V_{VDD} startup, P13 pin is connected to the VDD pin internally, so an external high-voltage depletion MOSFET, such as BSS126, can provide controlled startup current to charge the VDD capacitor. After the initial startup, P13 recovers back to 13-V regulation. A 1-µF ceramic bypass capacitor is required from P13 to AGND. A 20-V Zener diode between P13 and AGND is recommended to protect this pin from overstress, such as if the connection between this pin and the depletion MOSFET gate is fail-open or if line surge energy is coupled to this pin.
PWMH	15	O	PWM output signal used to control the gate of a secondary-side synchronous rectifier (SR) MOSFET through an external isolating gate driver. The driving capability is designed to bias a level-shifting isolator through a small-signal diode, or can also transmit the signal to secondary-side driving circuitry through a pulse transformer. The maximum voltage level of PWMH is clamped to REF.

Table 5-1. Pin Functions (continued)

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
SWS	16	I	This sensing input is used to monitor the switch-node voltage as it nears zero volts in normal operation for ZVS auto-tuning. The source of a high-voltage depletion-mode MOSFET, such as BSS126, is coupled to this pin through a current-limiting resistor so only the useful switching characteristic below 15 V is monitored. During start-up, this pin is connected to the VDD pin internally to allow the depletion-mode MOSFET to provide start-up current. The external current-limit resistor and a small bidirectional TVS across gate and source should be added to protect the V_{GS} from potential abnormal voltage stress. The resistor should be higher than 500 Ω and less than 820 Ω. The clamping voltage of TVS should be less than the MOSFET voltage rating but greater than 15 V. Moreover, the resistor and a 22-pF ceramic capacitor between the SWS pin and the bulk input capacitor ground form a small sensing delay to help the internal detection circuit to identify the ZVS characteristic correctly.
XCD	17, 18	I	X-cap Discharge input pins with 2-mA maximum discharge current capability. A line zero-crossing (LZC) threshold of 6.5 V on XCD is used to detect AC-line presence. When LZC is not detected within an 84-ms test period, the discharge current is enabled for a maximum period of 300 ms followed by a no-current blanking time of 700 ms. When AC-line recovers and LZC is detected again, the controller can reset the fault state almost immediately and will attempt to restart without waiting to fully discharge the bulk input capacitor. For the auto-recovery fault protections, if the controller is in 1.5-s auto-recovery fault state, LZC can reset the timer and speed up the restart attempt. The two redundant XCD pins help to provide the X-cap discharge function even when one pin is in fail-open condition. To form the discharge path, an anode of two high-voltage diode rectifiers is connected to each X-cap terminal, the two diode cathodes are connected together to a 26-kΩ high-voltage current-limiting resistance, and the drain-to-source connection of a high-voltage depletion MOSFET couples the resistance to the XCD pins. Two series 13-kΩ SMD resistors in 1206 size can be used as the current limiting device, and share the potential transient voltage from the AC-line. A 600-V rated MOSFET such as BSS126 is needed as the high voltage blocking device. The MOSFET gate is connected to the P13 pin, so the XCD pins can obtain enough signal headroom for LZC detection. If the X-cap discharge function is not needed, XCD pins must be connected to AGND pin to disable the function, and the diode-resistor-MOSFET path must be removed.
VDD	19	P	Controller bias power input. A ceramic capacitor with 10-µF or 15-µF capacitance is recommended, and the minimum voltage rating is 25 V.
GTP1	20	G	Ground This Pin. This pin must be connected to AGND for proper operation of the device.
GTP2	21	G	Ground This Pin. This pin must be connected to AGND for proper operation of the device.
GTP3	22	G	Ground This Pin. This pin must be connected to AGND for proper operation of the device.
VS	23	I	This voltage-sensing input pin is coupled to an auxiliary winding of the converter's transformer via a resistor divider. The pin and associated external resistors are used to monitor the output and input voltages and switching edges of the converter at different moments within each switching cycle. Parasitic capacitance between VS and any net, including AGND, must be minimized to avoid adverse effects on output voltage sensing, edge detection, and the dead-time calculation.
SET	24	I	This pin is used to configure the controller to be optimized for gallium nitride (GaN) power FETs or silicon (Si) power FETs on the primary side. Depending on the setting, it will optimize parameters of the ZVS control loop, dead-time adjustment, and protection features. When pulled high to REF pin, it is optimized for Si FETs. When pulled low to AGND, it is optimized for GaN FETs.
Thermal Pad		G	The thermal pad (TP) must be connected to AGND.

(1) I = input, O = output, I/O = input or output, FB = feedback, G = ground, P = power

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
Input Voltage	VDD		38	V
	SWS	–6	38	
	SWS (transient, negative pulse width of 20 ns max., duty cycle ≤ 1%)	–10	38	
	VDD-SWS	–20	38	
	CS	–0.3	3.6	
	VS	–0.75	7	
	VS (transient, 100 ns max.)	–1	7	
	PGND	–1	4	
	PGND (transient, 25 ns max.)		5	
	RTZ, BUR, SET, RDM, IPC, FLT, FB	–0.3	7	
	XCD	–0.3	30	
Output Voltage	REF, PWMH, RUN	–0.3	7	V
	P13, S13, PWML	–0.3	20	
Source Current	REF, P13, RTZ, RDM, IPC		Self–limiting	mA
	S13 (average)		15	
	VS		2	
	VS (transient, 100 ns max.)		2.5	
	FB		1	
	RUN (continuous)		5	
	PWML (continuous)		50	
	PWMH (continuous)		10	
	CS (transient, 30 ns max.)		1	
Sink Current	RUN (continuous)		8	mA
	PWML (continuous)		50	
	PWMH (continuous)		10	
	SWS		Self–limiting	
	XCD		25	
	FLT		0.3	
Operating junction temperature, T_J		–40	150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002(1)	±2000	V
		Charged device model (CDM), per AEC Q100-011	±500	

(1) AEC Q100-002 indicates that HBM stressing must be in accordance with the ANSI/ESDA/JEDC JS-001 specification.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{VDD}	Bias supply operating voltage	14		34	V
C_{VDD}	VDD capacitor	10			µF
C_{P13}	P13 bypass capacitor	1			µF
C_{REF}	REF bypass capacitor	0.22			µF
T_J	Operating junction temperature	–40		140	°C

6.4 Thermal Information

THERMAL METRIC(1)		UCC28781-Q1 RTW (WQFN) 24 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	43.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	31.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	20.3	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	0.5	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	20.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	5.7	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.5 Electrical Characteristics

Unless otherwise stated: V_{VDD} = 20 V, R_{RDM} = 115 kΩ, R_{RTZ} = 140 kΩ, V_{BUR} = 1.2 V, V_{SET} = 0 V, R_{NTC} = 50 kΩ, V_{VS} = 4 V, V_{SWS} = 0 V, I_{FB} = 0 µA, C_{PWML} = 0 pF, C_{PWMH} = 0 pF, C_{REF} = 0.22 µF, C_{P13} = 1 µF, and -40ºC < T_J = T_A < 125ºC

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
VDD INPUT						
$I_{RUN(STOP)}$	Supply current, run state	No switching	0.88	2.2	2.66	mA
$I_{RUN(SW)}$	Supply current, run state	Switching, I_{VSL} = 0 µA	2.45	3	3.55	mA
I_{WAIT}	Supply current, wait state	I_{FB} = -85 µA, I_{VDD} only	465	540	658	µA
I_{START}	Supply current, start state	V_{VDD} = $V_{VDD(ON)}$ - 100 mV, V_{VS} = 0 V	150	235	301	µA
I_{FAULT}	Supply current, fault state	fault state		500	630	µA
$I_{VDD(LIMIT)}$	VDD startup current limit during startup	V_{VDD} increasing, V_{SWS} - V_{VDD} = 1 V, V_{VDD} = 16.5 V	1.2	2	2.53	mA
$V_{VDD(ON)}$	VDD turnon threshold	V_{VDD} increasing	16.2	17	17.91	V
$V_{VDD(OFF)}$	VDD turnoff threshold	V_{VDD} decreasing	9.94	10.6	11.17	V
$V_{VDD(PCT)}$	Offset to power cycle for long output voltage overshoot	Offset above $V_{VDD(OFF)}$, I_{FB} = -85 µA	1.54	2.2	2.98	V
P13 OUTPUT						
V_{P13}	P13 voltage level including load regulation	0 mA to 60 mA out of P13, run state, V_{VDD} = 20 V	12.0	12.8	13.6	V
$I_{P13(START)}$	Max sink current of P13 pin during startup	V_{P13} = 14 V	1.53	2.2	3.04	mA
$I_{P13(MAX)}$	Current sourcing limit of P13 pin	P13 shorted to AGND, V_{VDD} = 20 V	103.3	133	160	mA
$VR13_{(LINE)}$	Line regulation of V_{P13}	V_{VDD} = 15 V to 35 V	-6	2	8.7	mV
$V_{P13(OV)}$	Over voltage fault threshold above V_{P13}		1.35	2	2.54	V
R_{P13}	Dropout resistance of P13 regulator switch between VDD and P13 pins	(V_{VDD} - V_{P13}) / 30 mA, V_{VDD} = 11 V, 30 mA out of P13	8.5	13	22.7	Ω
S13 OUTPUT						

Unless otherwise stated: V_{VDD} = 20 V, R_{RDM} = 115 kΩ, R_{RTZ} = 140 kΩ, V_{BUR} = 1.2 V, V_{SET} = 0 V, R_{NTC} = 50 kΩ, V_{VS} = 4 V, V_{SWS} = 0 V, I_{FB} = 0 µA, C_{PWML} = 0 pF, C_{PWMH} = 0 pF, C_{REF} = 0.22 µF, C_{P13} = 1 µF, and -40ºC < T_J = T_A < 125ºC

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
R_{S13}	$R_{DS(on)}$ of internal disconnect switch between P13 and S13 pins	(V_{P13} - V_{S13}) / 30 mA, V_{VDD} = 11 V, 30 mA out of S13	2.1	2.8	3.82	Ω
V_{S13_OK}	S13_OK threshold to enable switching	V_{RUN} = 5 V	9.63	10.2	10.7	V
$I_{S13(MAX)}$	Current sourcing limit of S13 pin	S13 shorted to AGND, V_{VDD} = 20 V	260.7	350	452.5	mA
REF OUTPUT						
V_{REF}	REF voltage level	I_{REF} = 0 A	4.9	5	5.13	V
$I_{REF(MAX)}$	Current sourcing limit of REF pin	REF shorted to AGND, V_{VDD} = 20 V	14.3	17	20.3	mA
$VR5_{(LINE)}$	Line regulation of V_{REF}	V_{VDD} = 12 V to 35 V	-7	-3	1	mV
$VR5_{(LOAD)}$	Load regulation of V_{REF}	0 mA to 1 mA out of REF, Change in V_{REF}	-16	0.1	25	mV
VS INPUT						
V_{VSNC}	Negative clamp level	I_{VSL} = -1.25 mA, voltage below ground	221	287	344	mV
V_{ZCD}	Zero-crossing detection (ZCD) level	V_{VS} decreasing	12.4	35	67.2	mV
I_{VSB}	Input bias current	V_{VS} = 4 V	-0.23	0	0.31	µA
$V_{VS(SM1)}$	VS threshold voltage in SM1 startup mode		242.4	282	318.3	mV
$V_{VS(SM2)}$	VS threshold voltage in SM2 startup mode		458.3	500	543	mV
$V_{VSLV(UP)}$	VS upper threshold out of low output voltage mode (LV mode)	V_{VS} increasing	2.41	2.49	2.6	V
$V_{VSLV(LR)}$	VS lower threshold into low output voltage mode (LV mode)	V_{VS} decreasing	2.3	2.39	2.49	V
t_{ZC}	Zero-crossing timeout delay		1.95	2.3	2.73	µs
$t_{D(ZCD)}$	Propagation delay from ZCD high to PWML 10% high	V_{VS} step from 4 V to -0.1 V	23	50	81	ns
CS INPUT						
$V_{CST(MAX)}$	Peak-power threshold on CS pin out of LV mode	I_{VSL} = 0 µA, V_{VS} ≥ $V_{VSLV(UP)}$	767.4	801	836.4	mV
		I_{VSL} = -333 µA, V_{VS} ≥ $V_{VSLV(UP)}$	650	727	788.7	mV
		I_{VSL} = -666 µA, V_{VS} ≥ $V_{VSLV(UP)}$	570	600	651.8	mV
		I_{VSL} = -1.25 mA, V_{VS} ≥ $V_{VSLV(UP)}$	537.2	570	612	mV
$V_{CST(MAX)\_LV}$	Peak-power threshold on CS pin in LV mode	I_{VSL} = 0 mA, V_{VS} ≤ $V_{VSLV(LR)}$	593.7	628	663.9	mV
		I_{VSL} = -666 µA, V_{VS} ≤ $V_{VSLV(LR)}$	540	570	609.5	mV
		I_{VSL} = -1.25 mA, V_{VS} ≤ $V_{VSLV(LR)}$	511.2	540	584.7	mV
$V_{CST(MIN)}$	Minimum CS threshold voltage	V_{CS} increasing, I_{FB} = -85 µA	120.7	153	200.1	mV
K_{LC}	Line-compensation current ratio	I_{VSL} = -1.25 mA, I_{VSL} / current out of CS pin	21.6	25	29	A/A
$V_{CST(EMI)}$ (1)	EMI dithering magnitude on CS pin out of LV mode	(V_{BUR} / $K_{BUR-CST}$) < V_{CST} < $V_{CST(MAX)}$, I_{VSL} > -646 µA, V_{VS} ≥ $V_{VSLV(UP)}$	78.4	96	113.6	mV
$V_{CST(EMI)\_LV}$ (1)	EMI dithering magnitude on CS pin in LV mode	(V_{BUR} / $K_{BUR-CST}$) < V_{CST} < $V_{CST(MAX)}$, I_{VSL} > -646 µA, V_{VS} ≤ $V_{VSLV(LR)}$	29.3	36	42.7	mV
$V_{CST(SM1)}$	CS threshold voltage in SM1 startup mode	V_{VS} < $V_{VS(SM1)}$	177.5	200	222.9	mV
$V_{CST(SM2)}$	CS threshold voltage in SM2 startup mode	V_{VS} < $V_{VS(SM2)}$	470.4	500	531.4	mV
t_{CSLEB}	Leading-edge-blanking time	V_{SET} = 5 V, V_{CS} = 1 V	171.2	190	216.1	ns
		V_{SET} = 0 V, V_{CS} = 1 V	94.4	108	125	ns
$t_{D(CS)}$	Propagation delay of CS comparator high to PWML 90 % low	V_{CS} step from 0 V to 1 V	10	26	37	ns
f_{DITHER} (1)	EMI dithering frequency on CS pin	(V_{BUR} / $K_{BUR-CST}$) < V_{CST} < $V_{CST(OPP)}$, I_{VSL} > -646 µA	20	23	27	kHz
BUR INPUT and Low-power MODE						
$K_{BUR-CST}$	Ratio of V_{BUR} to V_{CST}	V_{BUR} between 0.7 V and 2.4 V	3.82	3.98	4.09	V/V

Unless otherwise stated: V_{VDD} = 20 V, R_{RDM} = 115 kΩ, R_{RTZ} = 140 kΩ, V_{BUR} = 1.2 V, V_{SET} = 0 V, R_{NTC} = 50 kΩ, V_{VS} = 4 V, V_{SWS} = 0 V, I_{FB} = 0 µA, C_{PWML} = 0 pF, C_{PWMH} = 0 pF, C_{REF} = 0.22 µF, C_{P13} = 1 µF, and -40ºC < T_J = T_A < 125ºC

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{BUR(LPM)}$	Bias source current of V_{BUR} offset in LPM		2.09	2.65	3.16	µA
$I_{BUR(AAM)}$	Bias sink current of V_{BUR} offset in AAM	V_{CST} > V_{BUR} / $K_{BUR-CST}$	3.76	4.85	5.81	µA
$f_{BUR(UP1)}$	First upper threshold of burst frequency in ABM		30.7	34.4	38.5	kHz
$f_{BUR(UP2)}$	Second upper threshold of burst frequency in ABM	V_{VS} = 2.2 V	41.8	51.2	58.9	kHz
$f_{BUR(LR)}$	Lower threshold of burst frequency in ABM		21.3	24.5	28.1	kHz
f_{LPM}	Burst frequency in low-power mode		23.3	25	26.9	kHz
IPC INPUT and SBP2 MODE						
$V_{CST\_IPC(UP)}$	Highest programmable V_{CST} range of SBP2 by IPC pin	V_{IPC} = 5 V	373.8	405	438.5	mV
K_{IPC}	Ratio of the programmable IPC voltage to V_{CST}	V_{IPC} between 1.8 V and 3.8 V	59.3	64	68.4	mV/V
$V_{CST\_IPC(LR)}$	Lowest programmable V_{CST} range of SBP2 by IPC pin	V_{IPC} = 1 V	247.5	273	307.7	mV
$V_{CST\_IPC(MIN)}$	Minimum V_{CST} of SBP2 by grounding IPC pin	V_{IPC} = 0 V	128.1	154	191.5	mV
$I_{IPC(SBP2)}$	Bias source current of V_{IPC} offset in SBP2	I_{FB} = -85 µA	40.7	49	55.7	µA
$f_{SBP2(UP)}$	Upper threshold of burst frequency in SBP2		6	8.5	13.4	kHz
$f_{SBP2(LR)}$	Lower threshold of burst frequency in SBP2	V_{IPC} = 2 V	1	1.7	2	kHz
RUN						
V_{RUNH}	RUN pin high-level	I_{RUN} = -0.2 mA	4.6	4.78	5	V
V_{RUNL}	RUN pin low-level	I_{RUN} = 1 mA	0.1	0.25	0.3	V
$I_{SRC(RUN)}$	RUN peak source current	V_{RUN} = 2.3 V	33	44	52	mA
		V_{RUN} = 3 V	14	20	25	mA
$t_{R(RUN)}$	Turn-on rise time of RUN pin, from 0 V to 2.5 V	C_{LOAD} = 22 nF, V_{RUN} from 0 V to 2.5 V	0.2	0.79	1	µs
$t_{F(RUN)}$	Turn-off fall time of RUN pin, 90 % to 10 %	C_{LOAD} = 10 pF		20	32	ns
PWML						
V_{PWMLH}	PWML pin high-level	I_{PWML} = -1 mA	12.1	12.85	13.6	V
V_{PWMLL}	PWML pin low-level	I_{PWML} = 1 mA		0.002	0.1	V
$I_{SRC(PWML)}$ (1)	PWML peak source current	V_{PWML} = 0 V	0.25	0.5	0.8	A
$I_{SNK(PWML)}$ (1)	PWML peak sink current	V_{PWML} = 13 V	1.2	1.9	2.8	A
$R_{SRC(PWML)}$	PWML pull-up resistance	I_{PWML} = -20 mA	3.1	4.3	6.1	Ω
$R_{SNK(PWML)}$	PWML pull-down resistance	I_{PWML} = 20 mA	0.5	1.1	1.9	Ω
$t_{R(PWML)}$	Turn-on rise time of PWML pin, 10 % to 90 %	C_{LOAD} = 1.5 nF		30	53	ns
$t_{F(PWML)}$	Turn-off fall time of PWML pin, 90 % to 10 %	C_{LOAD} = 1.5 nF		9	20	ns
$t_{D(RUN-PWML)}$	Delay from RUN high to PWML high	V_{S13} > 11 V	1.92	4.7	7.43	µs
$t_{ON(MIN)}$	Minimum on-time of PWML in LPM	V_{SET} = 5 V, I_{FB} = -85 µA, V_{CS} = 1 V	68	105	180	ns
PWMH						
V_{PWMHH}	PWMH pin high-level	I_{PWMH} = -1 mA	4.39	4.66	4.83	V
V_{PWMHL}	PWMH pin low-level	I_{PWMH} = 1 mA	0.1	0.198	0.21	V
$I_{SRC(PWMH)}$	PWMH peak source current	V_{PWMH} = 2.5 V	16.5	21	26.2	mA
		V_{PWMH} = 3.5 V	3.8	6	7.6	mA
$t_{R(PWMH)}$	Turn-on rise time of PWMH pin, 10 % to 90 %	C_{LOAD} = 10 pF		8	24	ns

Unless otherwise stated: V_{VDD} = 20 V, R_{RDM} = 115 kΩ, R_{RTZ} = 140 kΩ, V_{BUR} = 1.2 V, V_{SET} = 0 V, R_{NTC} = 50 kΩ, V_{VS} = 4 V, V_{SWS} = 0 V, I_{FB} = 0 µA, C_{PWML} = 0 pF, C_{PWMH} = 0 pF, C_{REF} = 0.22 µF, C_{P13} = 1 µF, and -40ºC < T_J = T_A < 125ºC

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{F(PWMH)}$	Turn-off fall time of PWMH pin, 90 % to 10 %	C_{LOAD} = 10 pF		22	29	ns
$t_{D(VS-PWMH)}$	Dead time between VS high and PWMH 10 % high		10	18	28	ns
PROTECTION						
V_{OVP}	Over-voltage threshold	V_{VS} increasing	4.4	4.55	4.67	V
V_{OCP}	Over-current threshold	V_{CS} increasing	1.14	1.22	1.27	V
$K_{OPP-PPL}$	Ratio of over-power threshold to peak-power threshold	$V_{CST(OPP)}$ / $V_{CST(MAX)}$, and $V_{CST(OPP)\_LV}$ / $V_{CST(MAX)\_LV}$	0.72	0.75	0.78	V/V
$I_{VSL(RUN)}$	VS line-sense run current	Current out of VS pin increasing	313	365	408.6	µA
$I_{VSL(STOP)}$	VS line-sense stop current	Current out of VS pin decreasing	255	305	336.4	µA
K_{VSL}	VS line sense ratio	$I_{VSL(STOP)}$ / $I_{VSL(RUN)}$	0.72	0.836	0.9	A/A
$R_{RDM(TH)}$	R_{RDM} threshold for CS pin fault		35	55	70	kΩ
$T_{J(STOP)}$ (1)	Thermal-shutdown temperature	Internal junction temperature	125	162		°C
t_{OPP}	OPP fault timer	I_{FB} = 0 A	130	164	210	ms
t_{BO}	Brown-out detection delay time	I_{VSL} < $I_{VSL(STOP)}$	28.8	55	85.2	ms
t_{CSF1}	Maximum PWML on-time for detecting CS pin fault	V_{SET} = 5 V	1.6	2.05	2.5	µs
t_{CSF0}	Maximum PWML on-time for detecting CS pin fault	R_{RDM} < $R_{RDM(TH)}$ for V_{SET} = 0 V	0.85	1.05	1.27	µs
t_{FDR}	Fault reset delay timer	OCP, OPP, OVP, SCP or CS pin fault	1.2	1.5	2.4	s
FLT INPUT						
V_{NTCTH}	NTC shut-down voltage	FLT voltage decreasing	0.47	0.5	0.52	V
R_{NTCTH}	NTC shut-down resistance	R_{NTC} decreasing	8.9	9.91	11.18	kΩ
R_{NTCR}	NTC recovery resistance	R_{NTC} increasing	21.2	23	26.4	kΩ
I_{FLT}	Input bias current for V_{FLT} at V_{IOVPTH}	V_{FLT} = 4.5 V	-0.1	0	0.1	µA
V_{IOVPTH}	Shut-down voltage of input OVP	FLT voltage increasing	4.3	4.5	4.67	V
V_{IOVPR}	Hysteresis of input OVP	FLT voltage increasing	57.7	74	87	mV
$t_{FLT(NTC)}$	Delay time of NTC fault		14	50	100	µs
$t_{FLT(IOVP)}$	Delay time of input OVP fault		555	750	917	µs
V_{FLTZ}	Clamp voltage of FLT pin	I_{FLT} = 150 µA	5.08	5.5	5.61	V
RTZ INPUT						
K_{TZ}	t_Z compensation ratio	ratio of t_Z at I_{VSL} = -200 µA to t_Z at I_{VSL} = -733 µA	1.27	1.41	1.54	s/s
$t_{Z(MAX)}$	Maximum programmable dead time from PWMH low to PWML high	R_{RTZ} = 280 kΩ, I_{VSL} = -1 mA, V_{SET} = 5 V	397.8	478	592.8	ns
$t_{Z(MIN)}$	Minimum programmable dead time from PWMH low to PWML high	R_{RTZ} = 78.4 kΩ, I_{VSL} = -1 mA, V_{SET} = 0 V	56.1	70	89.1	ns
t_Z	Dead time from PWMH low to PWML high	I_{VSL} = -200 µA	152.2	175	212.7	ns
		I_{VSL} = -450 µA	129.2	150	190	ns
		I_{VSL} = -733 µA	109.7	125	147.2	ns
SWS INPUT						
$V_{TH(SWS)}$	SWS zero voltage threshold	V_{SET} = 5 V	8.1	8.5	9.1	V
		V_{SET} = 0 V	3.7	4.04	4.4	V
$t_{D(SWS-PWML)}$	Time between SWS low to PWML 10 % high	V_{SWS} step from 5 V to 0 V	11.4	17	26	ns
FB INPUT						
$I_{FB(SBP)}$	Maximum control FB current	I_{FB} increasing	64.2	75	87.1	µA

Unless otherwise stated: V_{VDD} = 20 V, R_{RDM} = 115 kΩ, R_{RTZ} = 140 kΩ, V_{BUR} = 1.2 V, V_{SET} = 0 V, R_{NTC} = 50 kΩ, V_{VS} = 4 V, V_{SWS} = 0 V, I_{FB} = 0 µA, C_{PWML} = 0 pF, C_{PWMH} = 0 pF, C_{REF} = 0.22 µF, C_{P13} = 1 µF, and -40ºC < T_J = T_A < 125ºC

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{FB(REG)}$	Regulated FB voltage level		4.02	4.25	4.53	V
R_{FBI}	FB input resistance		7.4	8.3	9.6	kΩ
dI_{COMP}/dt(1)	Slope of internal ramp compensation current		0.192	0.214	0.236	A/s
I_{COMP}	Magnitude of internal ramp compensation current		4	6.75	8	µA
RDM INPUT						
$t_{DM(MAX)}$	Maximum PWMH width with maximum tuning	V_{SWS} = 12 V	6.0	6.95	7.53	µs
$t_{DM(MIN)}$	Minimum PWMH width with minimum tuning	V_{SWS} = 0 V	3.0	3.43	3.77	µs
XCD INPUT						
$V_{XCD(LR)}$	XCD lower zero-crossing threshold		5.9	6.62	7.2	V
$V_{XCD(UP)}$	XCD upper zero-crossing threshold		6.8	7.5	7.9	V
$I_{XCD(0)}$	Leakage current in XCD wait state	V_{XCD} = 15 V		0.3	1.7	µA
$I_{XCD(1)}$	First-step XCD sense current	V_{XCD} = 15 V	0.32	0.4	0.46	mA
$I_{XCD(2)}$	Second-step XCD sense current	V_{XCD} = 15 V	0.61	0.775	0.91	mA
$I_{XCD(3)}$	Third-step XCD sense current	V_{XCD} = 15 V	0.73	1.15	1.6	mA
$I_{XCD(4)}$	Fourth-step XCD sense current	V_{XCD} = 15 V	1.2	1.53	1.81	mA
$I_{XCD(MAX)}$	Maximum XCD discharge current	V_{XCD} = 15 V	1.65	2	2.5	mA
$V_{XCD(OVP)}$	Clamp voltage of XCD OVP	I_{XCD} = 20 mA	23	26	30	V
$t_{XCD(STEP)}$	Dwell time for each XCD sense step		9	12	14.6	ms
$t_{XCD(MAX)}$	Maximum XCD discharge time		230.4	300	373.3	ms
$t_{XCD(WAIT)}$	XCD wait time			700	1071	ms

(1) Ensured by design, not tested in production

6.6 Typical Characteristics

V_{VDD} = 20 V, R_{RDM} = 115 kΩ, R_{RTZ} = 140 kΩ, V_{SET} = 0 V, and $T_J = T_A$ = 25 ºC (unless otherwise noted)

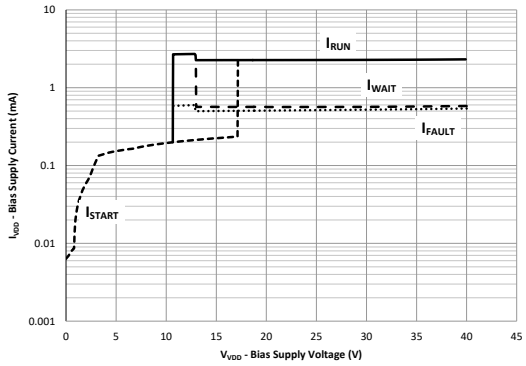


Figure 6-1. VDD Bias-Supply Current vs. VDD Bias-Supply Voltage

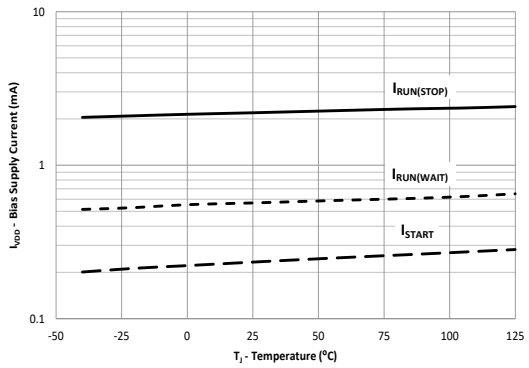


Figure 6-2. VDD Bias-Supply Current vs. Temperature

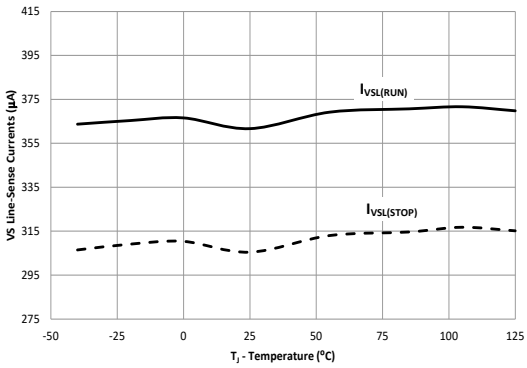


Figure 6-3. VS Line-Sense Currents vs. Temperature

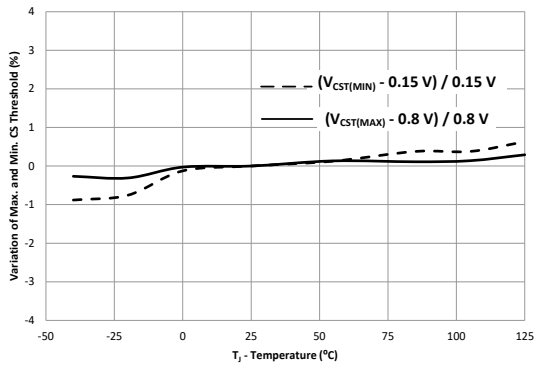


Figure 6-4. Percentage Variation of Maximum and Minimum CS Thresholds vs. Temperature

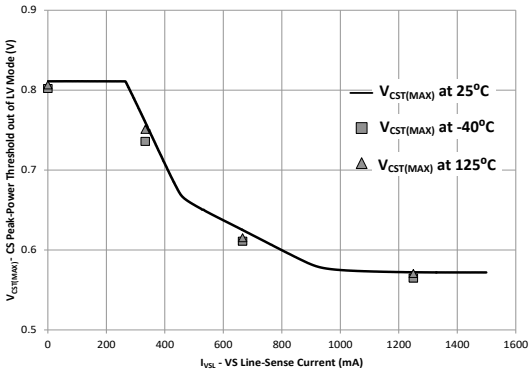


Figure 6-5. CS Peak-Power Threshold for V_{VS} > $V_{VSLV(UP)}$ vs. VS Line-Sense Currents

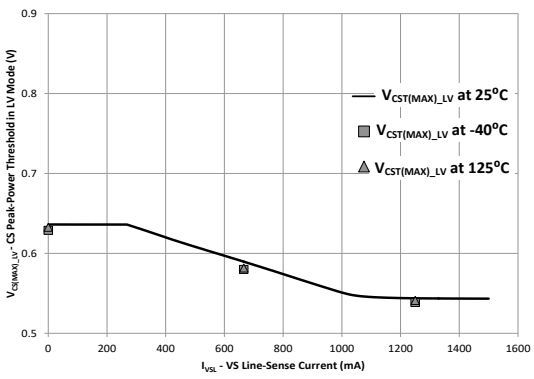


Figure 6-6. CS Peak-Power Threshold for V_{VS} < $V_{VSLV(LR)}$ vs. VS Line-Sense Currents

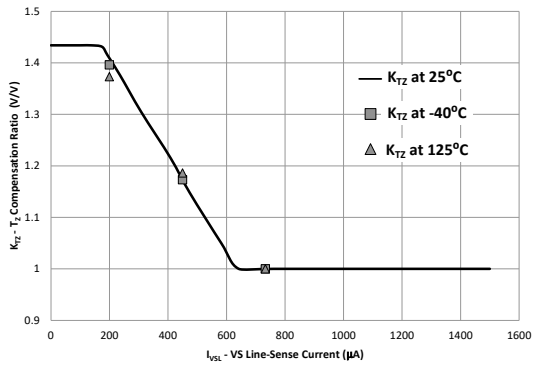


Figure 6-7. t_Z Compensation Ratio (K_{TZ}) vs. VS Line-Sense Currents

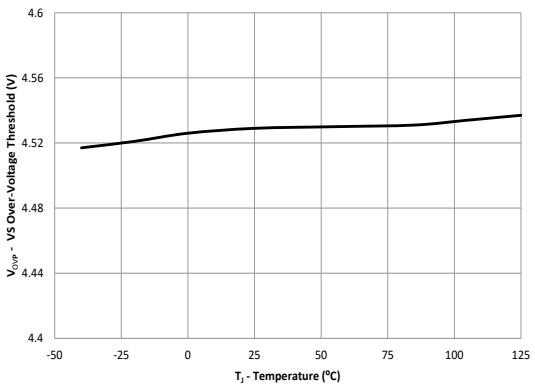


Figure 6-8. VS Over-Voltage Threshold vs. Temperature

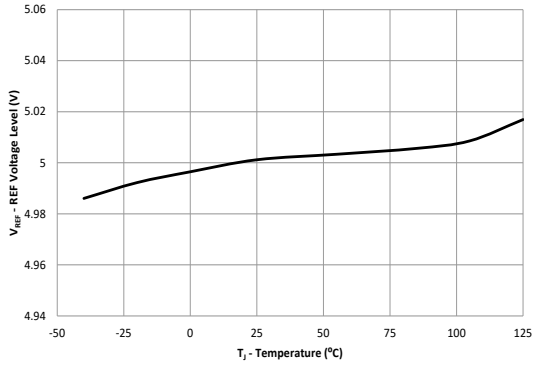


Figure 6-9. REF Voltage vs. Temperature

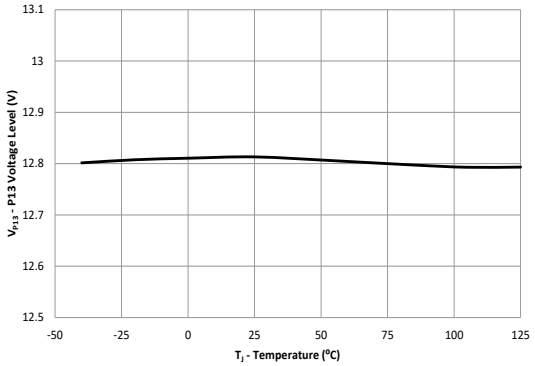


Figure 6-10. P13 Voltage vs. Temperature

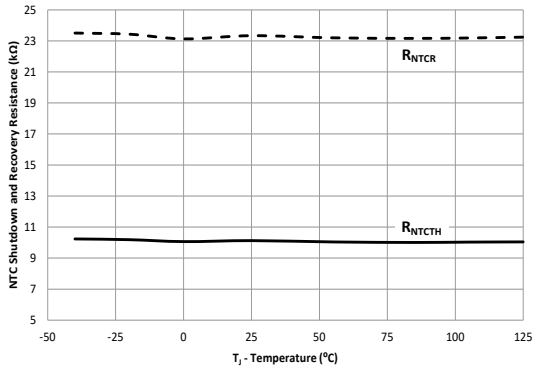


Figure 6-11. FLT OTP Thresholds vs. Junction Temperature

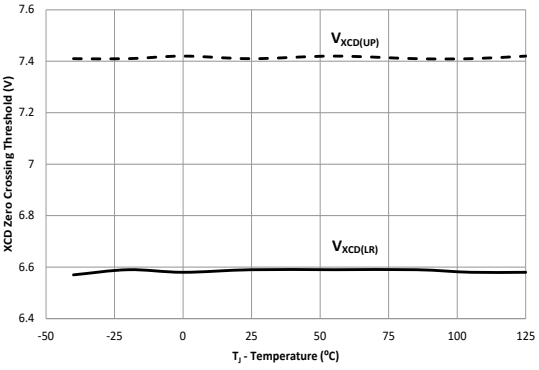


Figure 6-12. XCD Thresholds vs. Junction Temperature

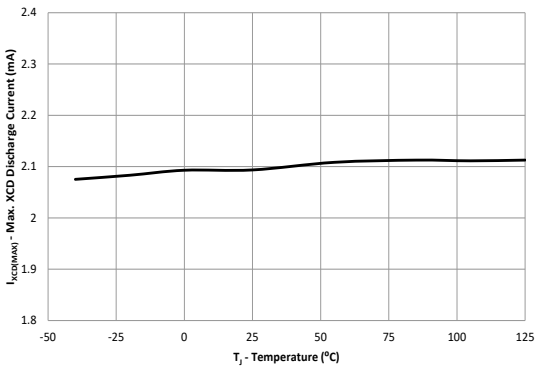


Figure 6-13. Max. XCD Discharge Current vs. Junction Temperature

7 Detailed Description

7.1 Overview

The UCC28781-Q1 is a transition-mode zero-voltage-switching flyback (ZVSF) controller equipped with advanced control schemes to enable significant size reduction of passive components for higher power density and higher average efficiency. Its control law is optimized for Silicon (Si) and Gallium Nitride (GaN) power FETs in a single-switch flyback configuration at high frequencies. In burst mode at very light loads the switching frequency may increase up to 1.5 MHz.

The ZVSF control of the UCC28781-Q1 is capable of auto-tuning the on-time of a secondary-side synchronous rectifier switch (Q_{SR}) by using a unique lossless ZVS-sensing network connected between the switch-node voltage (V_{SW}) and the SWS pin. The ZVSF controller is designed to adaptively achieve targeted full-ZVS or partial-ZVS conditions for the primary-side main switch (Q_L) with minimum circulating energy over wide operating conditions. Auto-tuning eliminates the risk of losing ZVS due to component tolerance, temperature, and input/output voltage variations, since the Q_{SR} on-time is corrected cycle-by-cycle.

Dead-times between PWML (controls Q_L) and PWMH (controls Q_{SR}) are optimally adjusted to help minimize the circulating energy required for ZVS as operating conditions change. Therefore, the overall system efficiency is improved and more consistent in mass production of the soft-switching topology. The programming features of the RTZ, RDM, BUR, IPC, and SET pins provide rich flexibility to optimize the power stage efficiency across a range of output power and operating frequency levels.

The UCC28781-Q1 uses five different steady-state operating modes to maximize efficiency over wide load and line ranges:

1. At higher load levels, adaptive amplitude modulation (AAM) adjusts the peak primary current.
2. In the medium-load range, adaptive burst mode (ABM) modulates the pulse count of each burst packet.
3. In the light-load range, low power mode (LPM) reduces the peak primary current of each two-pulse burst packet.
4. During very light-load conditions, stand-by power mode 1 (SBP1) minimizes the power loss.
5. During no-load conditions, stand-by power mode 2 (SBP2) minimizes the power loss.

During the system transient events such as the output load step down and output voltage overshoots, V_{VDD} may be reduced close to the 10.5-V UVLO-off threshold. In such cases, a sixth non-steady-state mode called survival mode (SM) is triggered to maintain V_{VDD} above 13 V and to reduce the size of the hold-up VDD capacitor.

The switching frequency-dither function is active in AAM to help reduce conducted-EMI noise and allow EMI filter size reduction. The 23-kHz dithering pattern and magnitude are designed to avoid audible noise, minimize efficiency influence, and desensitize the effect of the output voltage feedback loop response effect on the EMI attenuation. The dither function at low line can be programmed into disable mode based on the brown-in voltage setting, so the option provides design flexibility to balance the worst-case low-line efficiency and EMI. The dither fading feature smoothly disables the dither signal when the output load is close to the transition point between AAM and ABM. The 23-kHz dither frequency is high enough to allow a higher control-loop bandwidth for improved load transient response without distorting the dither signal and impairing EMI.

The unique burst mode control in ABM, LPM, and two SBP modes maximizes the light-load efficiency of the ZVSF power stage while avoiding the concerns of conventional burst operation - such as high output ripple and audible noise. The internal ramp compensation can stabilize the burst control loop without an external compensation network. The burst control provides an enable signal through the RUN pin to dynamically manage the static current of the SR gate-driver and also adaptively disables the drive signal of Q_{SR}. The internal drivers of RUN and PWMH can supply and disconnect the 5-V bias voltage to a digital isolator through a small-signal diode. The disconnect switch inside the S13 pin can directly control the 13-V bias voltage to a low-side GaN driver. These power management functions with RUN, PWMH, and S13 pins can be used to minimize the quiescent power consumed by those devices during burst off time, further improving the converter's light-load efficiency and reducing its stand-by power.

The S13 and IPC pins of the UCC28781-Q1 can be adapted to manage an upstream PFC stage to maximize the light-load efficiency of higher power applications. The S13 pin can supply a 13-V bias voltage to the PFC controller whenever the ZVSF controller is in the run state. The pin disconnects the bias voltage during the wait

states of the burst mode operation. When the burst frequency is reduced in very light load conditions, the bias voltage will decay below UVLO and shut down PFC controller, so the power loss from PFC can be eliminated.

The PWML output is a strong driver for a Si power MOSFET with high capacitive loading, a GaN-based gate injection transistor (GIT) with continuous on-state current, or a GaN power IC with logic input. The maximum voltage level of PWML is clamped at 13 V to balance the conduction loss reduction and gate charge loss of Si MOSFET. A dedicated driver ground return pin (PGND) minimizes the parasitic impedance and noise coupling of the PWML gate-drive loop to achieve faster switching speed and reduced turn-off loss of Q_L. The short 15-ns propagation delay and narrow 110-ns minimum on-time enable more accurate ZVS control and higher switching frequency operation.

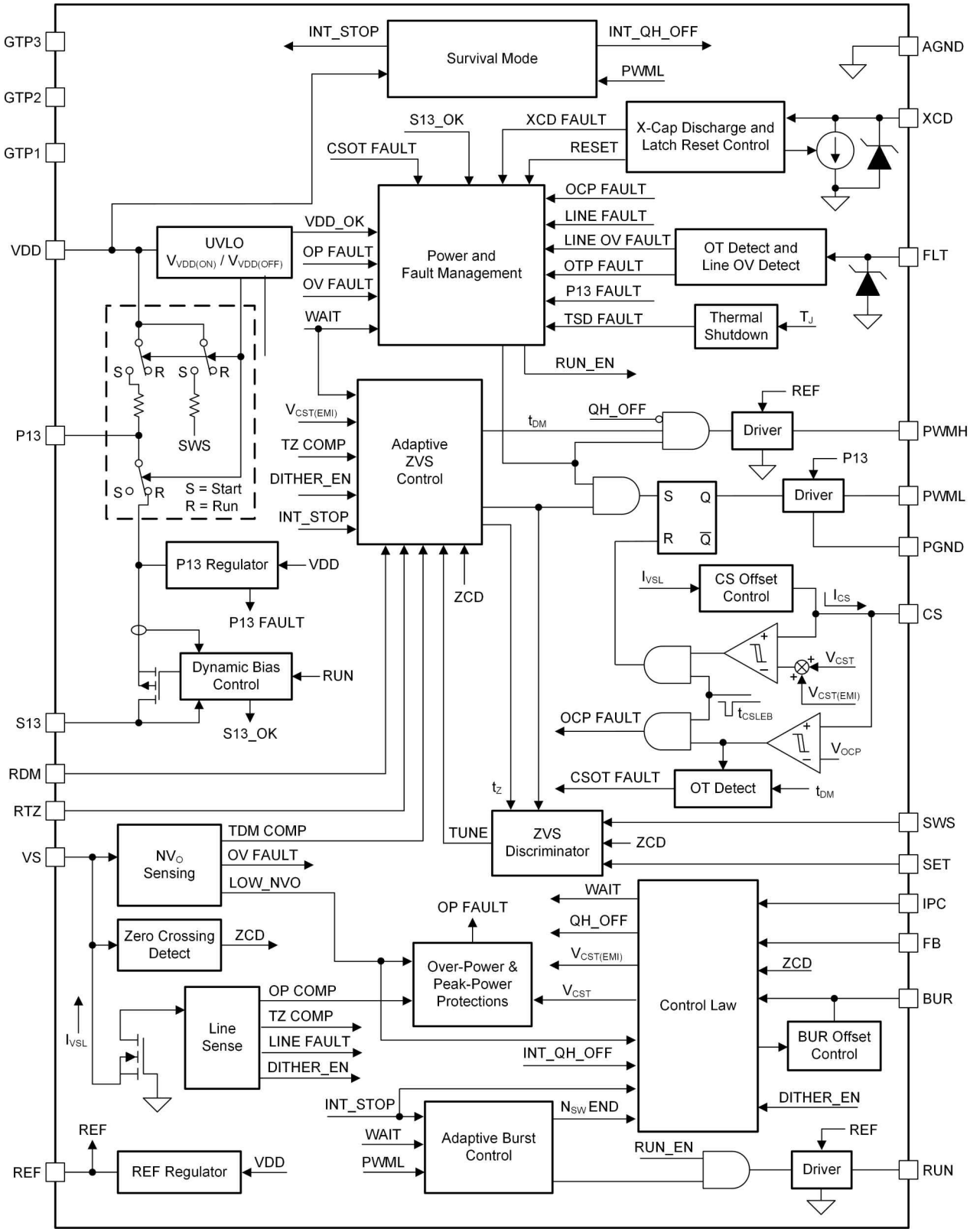
During initial power up or VDD restart, the ZVSF stops switching, so UCC28781-Q1 starts up the VDD supply voltage with an external high-voltage depletion-mode MOSFET between the ZVSF switch node and the SWS pin. Fast startup is achieved with low stand-by power overhead, compared with using the conventional high-voltage startup resistance to VDD. Moreover, the P13 pin biases the gate of the depletion-mode FET to also allow this MOSFET to be used in lossless ZVS-sensing. This arrangement avoids additional sensing devices.

The enhanced switching control of UCC28781-Q1 mitigates excessive drain-to-source voltage stress on a synchronous rectifier (SR) caused by temporary continuous conduction mode (CCM), so the power loss of an SR snubber can be reduced for higher efficiency. Additional PWML timing controls can avoid premature Q_L turn-on before the magnetizing current reaches to zero through an improved zero-crossing detection (ZCD) scheme of the VS pin.

The UCC28781-Q1 also integrates more robust protection features tailored to maximize system reliability and safety. These features include active X-capacitor discharge, internal soft start, brown in/out, output over-voltage (OVP), input line over-voltage (IOVP), output over-power (OPP), system over-temperature (OTP), switch over-current (OCP), output short-circuit protection (SCP), and pin faults. All fault responses are auto-recovery, which means that the controller will attempt to restart after the shut-down time elapses.

The X-capacitor discharge function can actively discharge the residual voltage on X2 safety capacitors to a safe level after AC-line voltage removal is detected through the XCD pins of UCC28781-Q1 and its external sensing circuit. If the AC-line voltage recovers within 2 seconds after the line removal, the controller will reset the fault state immediately and will attempt to restart without waiting to fully discharge the bulk input capacitor or VDD capacitor. Grounding the two XCD pins disables this function and eliminates the sensing circuit. Unlike other conventional flyback controllers, UCC28781-Q1 provides the design flexibility of using the X-capacitor discharge function based on application power level as it is decoupled from VDD startup and brown-in/out detection functions. Since those two functions are implemented on the SWS and VS pins, respectively, UCC28781-Q1 maintains the two functions even when the XCD-related components are fully removed.

7.2 Functional Block Diagram



7.3 Detailed Pin Description

7.3.1 BUR Pin (Programmable Burst Mode)

The voltage at the BUR pin (V_{BUR}) sets a target peak current-sense threshold at the CS pin ($V_{CST(BUR)}$) which programs the onset of adaptive burst mode (ABM). V_{BUR} also determines the clamped peak current level of switching cycles in each burst packet. When V_{BUR} is set higher, ABM will start at heavier output load conditions with higher peak primary current, so the benefit is higher light-load efficiency but the side effect is larger burst-mode output voltage ripple. Therefore, 50% to 60% of output load at high line is the recommended highest load condition to enter ABM ($I_{o(BUR)}$) for both Si and GaN-based designs. The gain between V_{BUR} and $V_{CST(BUR)}$ is a constant gain of $K_{BUR-CST}$, so setting $V_{CST(BUR)}$ just requires properly selecting the resistor divider on the BUR pin formed by R_{BUR1} and R_{BUR2}. V_{BUR} should be set between 0.7 V and 2.4 V. If V_{BUR} is less than 0.7 V, $V_{CST(BUR)}$ holds at 0.7 V / $K_{BUR-CST}$. If V_{BUR} is higher than 2.4 V, $V_{CST(BUR)}$ stays at 2.4 V / $K_{BUR-CST}$.

$$R_{BUR2} = \frac{R_{BUR1} K_{BUR-CST} V_{CST(BUR)}}{V_{REF} - K_{BUR-CST} V_{CST(BUR)}} = \frac{4 \times R_{BUR1} V_{CST(BUR)}}{5V - 4 \times V_{CST(BUR)}} \quad (1)$$

In order to enhance the mode transition between ABM and LPM, a programmable offset voltage ($\Delta V_{BUR(LPM)}$) is generated on top of the V_{BUR} setting in ABM through an internal 2.7-µA current source ($I_{BUR(LPM)}$), as shown in Figure 7-1. In ABM, V_{BUR} is set through the resistor voltage divider to fulfill the target average efficiency. On transition from ABM to LPM, $I_{BUR(LPM)}$ is enabled in LPM and flows out of the BUR pin, so $\Delta V_{BUR(LPM)}$ can be programmed based on the Thevenin resistance on the BUR pin, which can be expressed as

$$\Delta V_{BUR(LPM)} = I_{BUR(LPM)} (R_{BUR1} // R_{BUR2}) \quad (2)$$

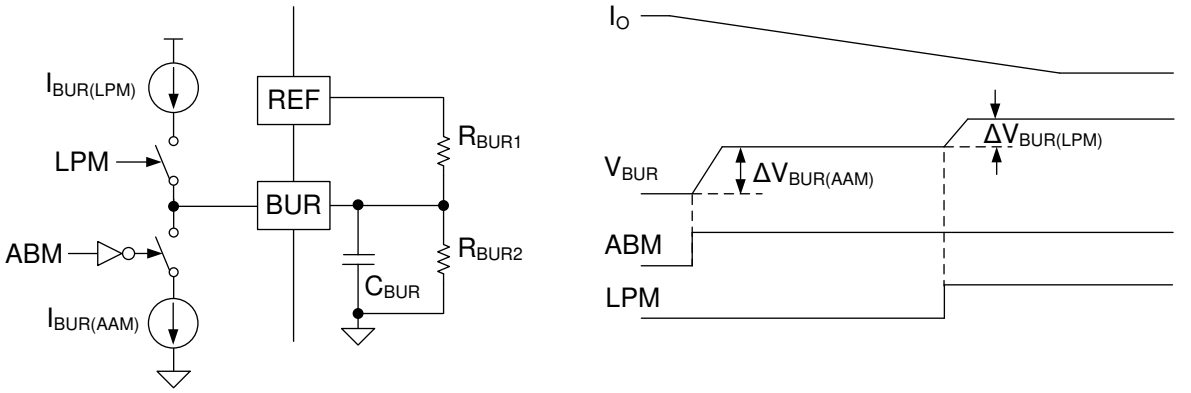


Figure 7-1. Hysteresis Voltage Generation on BUR Pin

When V_{BUR} steps higher on transition into LPM, the initial peak magnetizing current in LPM is increased with larger energy per switching cycle in each burst packet. This increases the output voltage which forces higher feedback current to restore regulation. Higher feedback current causes UCC28781-Q1 to stay in LPM, forming a hysteresis effect. If $\Delta V_{BUR(LPM)}$ is designed too small, it is possible that mode toggling between LPM and ABM can occur resulting in audible noise. For that situation, $\Delta V_{BUR(LPM)}$ greater than 100 mV is recommended.

To minimize the effects of external noise coupling on V_{BUR}, a filter capacitor on the BUR pin (C_{BUR}) may be needed. C_{BUR} needs to be properly designed to minimize the delay in generating ΔV_{BUR} during mode transitions. It is recommended that C_{BUR} should be sized small enough to ensure $\Delta V_{BUR(LPM)}$ settles within 40 µs, corresponding to the burst frequency of 25 kHz in LPM (f_{LPM}). Based on three RC time constants, representing 95% of a settled steady-state value from a step response, the design guide for C_{BUR} is expressed as

$$C_{BUR} \le 40\mu s \times \frac{R_{BUR1} + R_{BUR2}}{3R_{BUR1}R_{BUR2}} \quad (3)$$

In order to enhance the mode transition between ABM and AAM, a programmable offset voltage ($\Delta V_{BUR(AAM)}$) is generated to lower the V_{BUR} with an internal 5-µA pull-down current ($I_{BUR(AAM)}$), as shown in Figure 7-1. After transition from ABM to AAM, $I_{BUR(AAM)}$ is enabled in AAM and flows into the BUR pin, so $\Delta V_{BUR(AAM)}$ is also programmed based on the Thevenin resistance on the BUR pin, which can be expressed as

$$\Delta V_{BUR(AAM)} = I_{BUR(AAM)}(R_{BUR1} // R_{BUR2}) \quad (4)$$

When V_{BUR} reduces after transition to AAM, the initial peak magnetizing current in AAM is reduced with less energy per switching cycle, which forces controller to continu operating in AAM. If $\Delta V_{BUR(AAM)}$ is too small, it is possible that either mode toggling between ABM and AAM or low-frequency ABM burst packets less than 20 kHz can occur and result in audible noise concern. For that situation, $\Delta V_{BUR(AAM)}$ greater than 150 mV is recommended. In some power stage designs, LPM in hard switching condition may cover a wider output load current range, so the light-load efficiency in LPM may be lower than ABM with ZVS condition. Besides, the ABM-to-AAM mode transition may be affected potentially when the load current condition of LPM-to-ABM transition is too close to the load current condition of ABM-to-AAM transition.

In order to optimize the output load current range in LPM, lower $V_{BUR(ABM)}$, smaller $\Delta V_{BUR(LPM)}$, larger R_{OPP}, and smaller C_{CS} help to reduce the peak magnetizing current in LPM. If the LPM energy needs to be further reduced but V_{BUR} in AAM is limited by the 0.7-V minimum programmable level, the optional application circuit in Figure 7-2 can be considered. When the output load current is reduced, duty cycle of each burst packet becomes smaller, so as the duty cycle of RUN-pin voltage. C_{BUR} is discharged by the RUN driver through the small-signal diode (D_{BUR}) and the current limit resistor (R_{RUN}). Proper selection of R_{RUN} value can further reduce $V_{BUR(ABM)}$ when the load current is reduced close to the transition point from ABM to LPM. One example BUR-pin setting is R_{BUR1} = 182 kΩ, R_{BUR2} = 37.4 kΩ, C_{BUR} = 330 pF, and R_{RUN} = 20 kΩ.

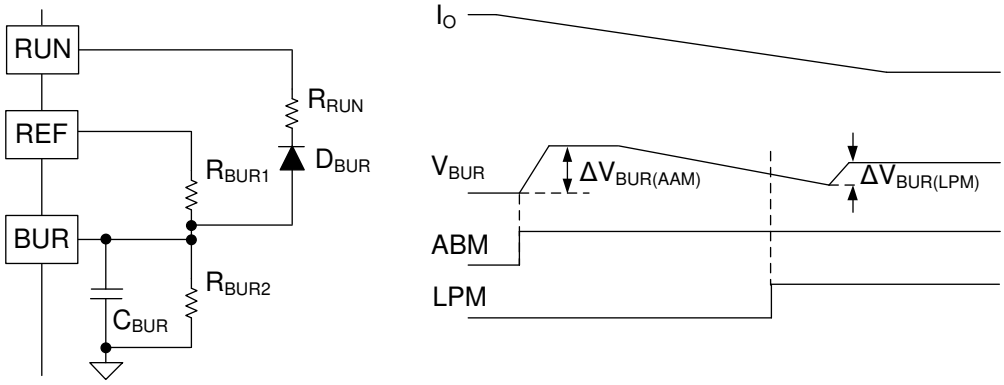


Figure 7-2. Optional Application Circuit to Reduce V_{BUR} in LPM

7.3.2 FB Pin (Feedback Pin)

The FB pin usually connects to the collector of an optocoupler output transistor through an external current-limiting resistor (R_{FB}). A maximum of 20 kΩ for R_{FB} is recommended. The feedback network of UCC28781-Q1 is shown in Figure 7-3. A high-quality ceramic by-pass capacitor between FB pin and REF pin (C_{FB}) is required for decoupling I_{FB} from switching noise interference. A minimum of 220 pF is recommended for C_{FB} . An internal 8-kΩ resistor (R_{FBI}) at the FB pin in conjunction with the external C_{FB} forms an effective low-pass filter. Section 8 provides a detailed design guide on the secondary-side compensation network of V_O feedback loop, to improve the load transient response and also limit the I_{FB} ripple of ABM mode within the recommended range.

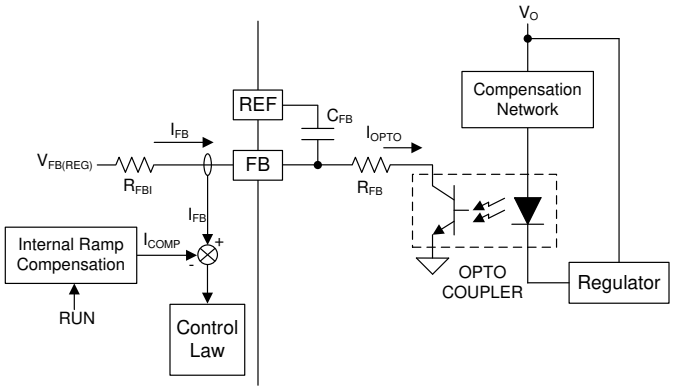


Figure 7-3. External Feedback Network Connected to the FB Pin

Depending on the operating mode, the controller interprets the current flowing out of the FB pin (I_{FB}) to regulate the output voltage. For AAM and LPM modes based on peak current control, I_{FB} is converted into an internal peak current-sense threshold (V_{CST}) to modulate the amplitude of the current-sense signal on the CS pin. For example, when the output voltage (V_O) is lower than the regulation level set by the shunt regulator, the absolute current level of I_{FB} reduces, causing a higher V_{CST} to increase more power to the output load. In ABM, the burst control loop takes over the V_O regulation, where V_{CST} is clamped to $V_{CST(BUR)}$ and the ripple component of I_{FB} participates in the modulation of the burst off time.

Figure 7-4 illustrates the operating principle of the ABM. A burst of switching pulses raises the output voltage V_O which increases I_{FB}. At the end of the burst, the load current discharges the output capacitor, which decreases V_O and I_{FB}. UCC28781-Q1 injects a noise-free internal ramp compensation current (I_{COMP}) superimposed on I_{FB} in order to stabilize the ABM operation. When the RUN pin is high, I_{COMP} is reset to 0 µA. When the RUN pin goes low, I_{COMP} is gradually increased to 6 µA with a positive slope of 0.214 A/s. The summation of I_{FB} and I_{COMP} is compared with $I_{TH(FB)}$ to trigger the next burst event. The magnitude and sharp slope of I_{COMP} help to push switching ripple and high-frequency noise component of I_{OPTO} away from $I_{TH(FB)}$.

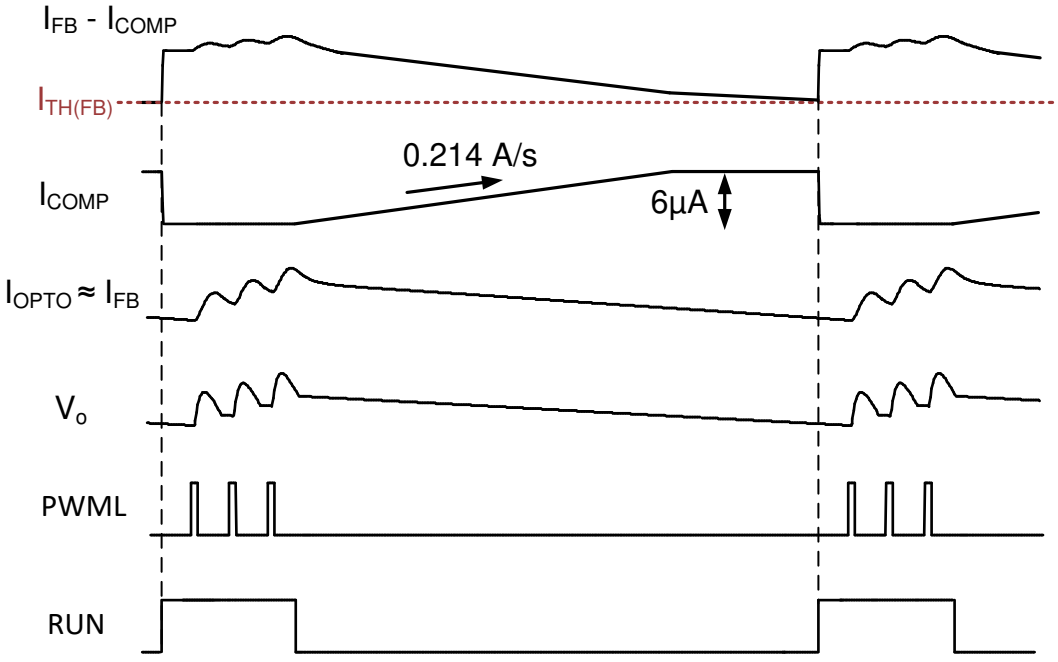


Figure 7-4. Concept of Burst Control with an Internal Ramp Compensation

7.3.3 REF Pin (Internal 5-V Bias)

The output of the internal 5-V regulator of the controller is connected to the REF pin. REF provides bias current to most of the functional blocks within the UCC28781-Q1. It requires a high-quality ceramic by-pass capacitor (C_{REF}) to AGND to decouple switching noise and to reduce the voltage transients as the controller transitions from wait state to run state. The minimum C_{REF} value is 0.22 µF, and a high quality dielectric material should be used, such as X7R.

The output short-circuit current ($I_{S(REF)}$) of the REF regulator is self-limited to approximately 17 mA. 5-V bias is only available after the under-voltage lock-out (UVLO) circuit enables the operation of UCC28781-Q1 when V_{VDD} reaches $V_{VDD(ON)}$.

This pin can be used to perform an external shutdown function. A small-signal switch can be used to pull this pin voltage below the power-good threshold of 4.5V so the controller will stop switching, force a VDD restart cycle, and turn off the REF current.

7.3.4 VDD Pin (Device Bias Supply)

The VDD pin is the primary bias for the internal 5-V REF regulator, internal 13-V P13 regulator, other internal references, and the undervoltage lock-out (UVLO) circuit. As shown in Figure 7-5, the UVLO circuit connected to the VDD pin controls the internal power-path switches among VDD, P13, and SWS pins, in order to allow an external depletion-mode MOSFET (Q_S) to be able to perform both V_{VDD} startup and switch-node voltage (V_{SW}) sensing for ZVS control after startup. During startup, SWS and P13 pins are connected to VDD pin allowing Q_S to charge the VDD capacitor (C_{VDD}) from the V_{SW}.

After the VDD startup completes, the ZVS discriminator block and switching logic are enabled. Then, the transformer starts delivering energy to the output capacitor (C_O) every switching cycle, so both output voltage (V_O) and auxiliary winding voltage (V_{AUX}) increase.

As V_{AUX} is high enough, the auxiliary winding takes over to power V_{VDD}. The UVLO circuit provides a turn-on threshold of $V_{VDD(ON)}$ at 17 V and turn-off threshold of $V_{VDD(OFF)}$ at 10.6 V. For fixed output voltage designs, the wide V_{VDD} range can accommodate lower values of VDD capacitor (C_{VDD}) and support shorter power-on delays.

For a fixed output voltage design, the rectified V_{AUX} is directly connected to the VDD pin. As V_{VDD} reaches $V_{VDD(ON)}$, the SWS pin is disconnected from the VDD pin by the internal power path switch, so the C_{VDD} size has to be sufficient to hold V_{VDD} higher than $V_{VDD(OFF)}$ until the positive auxiliary winding voltage is high enough to take over bias power delivery during V_O soft start. Therefore, the calculation of minimum capacitance ($C_{VDD(MIN)}$) needs to consider the discharging effect from the sink current of the UCC28781-Q1 during switching in its run state ($I_{RUN(SW)}$), the average operating current of driver (I_{DR}), and the average gate charge current of half-bridge FETs (I_{Qg}) throughout the longest duration of V_O soft-start ($t_{SS(MAX)}$) sequence.

$$C_{VDD(min)} = \frac{\left(I_{RUN(SW)} + I_{DR} + I_{Qg}\right) \times t_{SS(max)}}{V_{VDD(on)} \times V_{VDD(off)}} \tag{5}$$

$t_{SS(MAX)}$ estimation should consider the averaged soft-start current ($I_{SEC(SS)}$) on the secondary side of the converter, load current on the output ($I_{O(SS)}$) during start-up (if any), maximum output capacitance ($C_{O(MAX)}$), and a 0.7-ms time-out potentially being triggered in the startup sequence. Include 1 ms in the equation to be the worst-case condition of the 0.7-ms timer.

$$t_{SS(max)} = \frac{C_{O(max)} \times V_O}{I_{SEC(SS)} - I_{O(SS)}} + 1\ \text{ms} \tag{6}$$

During the V_O soft-start sequence, V_{CST} reaches the maximum current threshold on the CS pin ($V_{CST(MAX)}$) , so $I_{SEC(SS)}$ at the minimum voltage of the input bulk capacitor ($V_{BULK(MIN)}$) can be approximated as:

$$I_{SEC(SS)} = \frac{\left(N_{PS} \times V_{CST(max)}\right)}{2 \times R_{CS}} \times \frac{V_{BULK(min)}}{V_{BULK(min)} + N_{PS} \times \left(V_O + V_F\right)} \tag{7}$$

where

- R_{CS} is the current sense resistor
- N_{PS} is primary-to-secondary turns ratio
- V_F is the forward voltage drop of the secondary rectifier

7.3.5 P13 and SWS Pins

The P13 pin provides a regulated voltage to the gate of the depletion-mode MOSFET (Q_S), enabling Q_S to serve both V_{VDD} start-up and loss-less ZVS-sensing from the high-voltage switch node (V_{SW}) through the SWS pin. During V_{VDD} start-up, the UVLO circuit controls two power-path switches connecting SWS and P13 pins to VDD pin with two internal current-limit resistors (R_{DDS} and R_{DDH}), as shown in Figure 7-5. In this configuration, Q_S behaves as a current source to charge the VDD capacitor (C_{VDD}). R_{DDS} is set at 5 kΩ when V_{VDD} < 1.8 V to limit the maximum fault current under a VDD short-to-GND condition. R_{DDS} is reduced to 500 Ω when V_{VDD} > 1.8 V to allow V_{VDD} to charge faster. The maximum charge current (I_{SWS}) is affected by R_{DDS}, the external series resistance (R_{SWS}) from SWS pin to Q_S, and the threshold voltage of Q_S ($V_{TH(Qs)}$). I_{SWS} can be calculated as

$$I_{SWS} = \frac{V_{TH(Qs)}}{R_{DDS} + R_{SWS}} \quad (8)$$

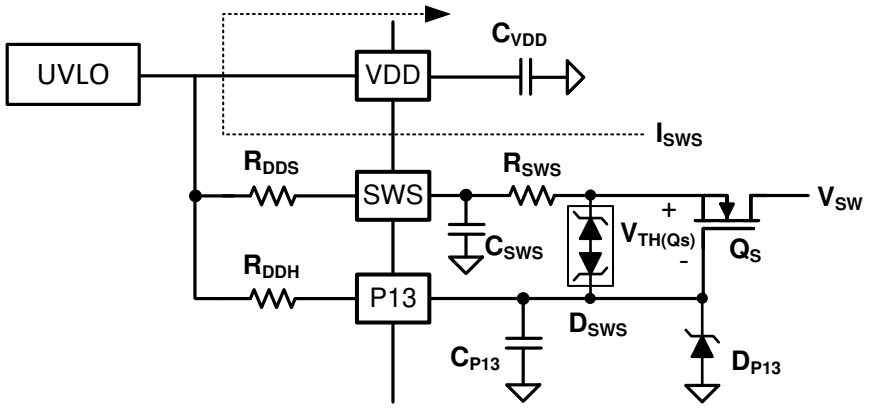


Figure 7-5. Operation of the VDD Startup Circuit

After V_{VDD} reaches $V_{VDD(ON)}$, the two power-path switches open the connections between SWS, P13, and VDD pins. At this point, a third power-path switch connects an internal 13-V regulator to the P13 pin for configuring Q_S to perform loss-less ZVS sensing. Because the Q_S gate is fixed at 13 V, when the drain pin voltage of Q_S becomes higher than the sum of Q_S threshold voltage ($V_{TH(Qs)}$) and the 13-V gate voltage, Q_S turns off and the source pin voltage of Q_S can no longer follow the drain pin voltage change. This gate control method makes Q_S act as a high-voltage blocking device with the drain pin connected to V_{SW}. When the controller is switching, whenever V_{SW} is lower than 13 V, Q_S turns on and forces the source pin voltage to follow V_{SW}, becoming a replica of the V_{SW} waveform at the lower voltage level, as illustrated in Figure 7-6.

The limited window for monitoring the V_{SW} waveform is sufficient for ZVS control of the UCC28781-Q1, since the ZVS tuning threshold ($V_{TH(SWS)}$) is set at 8.5 V for V_{SET} = 5 V and set at 4 V for V_{SET} = 0 V. The 8.5-V threshold is the auto-tuning target of the internal adaptive ZVS control loop for realizing a partial-ZVS condition using Si primary switches. On the other hand, performing full ZVS operation is more suitable with GaN primary switches. Using a 4-V threshold helps to compensate for sensing delay between V_{SW} and the SWS pin.

The internal 13-V regulator requires a high-quality ceramic by-pass capacitor (C_{P13}) between the P13 pin and AGND pin for noise filtering and providing compensation to the P13 regulator. The minimum C_{P13} value is 1 µF and an X7R-type dielectric capacitor with 25-V rating or better is recommended. The controller enters a fault state if the P13 pin is open or shorted to AGND during V_{VDD} start-up, or if V_{P13} overshoot is higher than $V_{P13(OV)}$ of 15 V in run state. The output short-circuit current of P13 regulator ($I_{P13(MAX)}$) is self-limited to approximately 130 mA.

Since the P13 pin interfaces to the external depletion-FET, during input surge or EFT testing the Cgd of the depletion-FET can inject charge into the P13 pin and may cause an over-voltage stress. Under such condition it is recommended to place an 18-V Zener diode (D_{P13}) on the P13 pin to clamp its voltage below its abs-max level.

During AAM and ABM if the negative magnetizing current is large enough, a GaN device may operate in the reverse conduction condition before it turns on each switching cycle, so V_{SW} may be around -5 V for a brief inteval and it appears on the SWS pin. The SWS-pin design of UCC28781-Q1 can sustain –6 V (continuous) and –10 V (transient) stress to enhance the robust operation of the GaN power stage.

During this interval, Q_S is in the on-state and its body diode may conduct for a short time when the voltage drop across the on-state resistance of Q_S is high enough. The external R_{SWS} can limit the forward current flowing through the Q_S body diode, so the reverse recovery charge of the body diode can be significantly reduced. Too high of R_{SWS} value weakens the start-up charge current of C_{VDD} and results in a longer start-up time. R_{SWS} can be expected be slightly higher than 500 Ω. A small back-to-back TVS across BSS126 gate-to-source should be added to protect the gate-to-source voltage from potential abnormal voltage stress. Ensure that the TVS clamping voltage is less than the BSS126 gate-to-source voltage rating but does not conduct below 15 V.

R_{SWS} and a ceramic capacitor (C_{SWS}) between the SWS pin and the bulk input capacitor ground form a small sensing delay to help the internal detection circuit to identify the ZVS characteristic correctly. The delay is to ensure that the ZCD detection on the VS pin happens earlier than the ZVS detection on the SWS pin, such that the ZVS control can auto-tune the PWMH on-time in the proper direction. The minimum value of C_{SWS} is 22 pF.

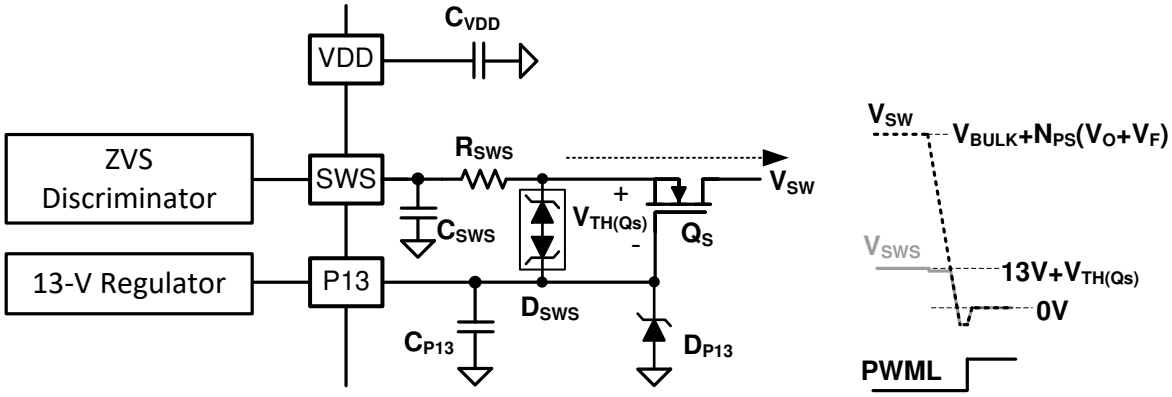


Figure 7-6. ZVS Sensing by Reusing the VDD Startup Circuit

7.3.6 S13 Pin

As shown in Power Management Function for a GaN Power IC and PFC Controller , the S13 pin (switched 13-V rail) is used to perform bias-power management for a primary-side GaN power IC, along with an example application where it also powers a PFC controller. This configuration enables to minimize the power-loss contribution to so-called "tiny-load" input power and stand-by power.

S13 is sourced by P13 through an internal 2.8-Ω switch controlled by the RUN pin. Figure 7-8 illustrates the power-up sequence of the S13 pin. When RUN is high, the S13 decoupling capacitor is charged up to 13 V and the charge current is controlled by an internal soft-start current limiter. The S13-pin voltage must increase above the 10-V power-good threshold ($V_{S13(OK)}$) in order to initiate PWML switching of each burst cycle. When RUN is low, V_{S13} is discharged by the loading on S13. The power-on delay of the GaN power IC on the S13 pin must be less than 2 µs to be responsive to PWML. If not, the VDD or P13 pin may be a more suitable bias supply for devices with long power-on delay, but the wait-state power consumption will be compromised. A 22-nF ceramic capacitor as $C_{S13(ZVSF)}$ is recommended. If the S13 pin is not used, it can be connected to the P13 pin in order to eliminate the delay effect on PWML switching in every low-frequency burst cycle.

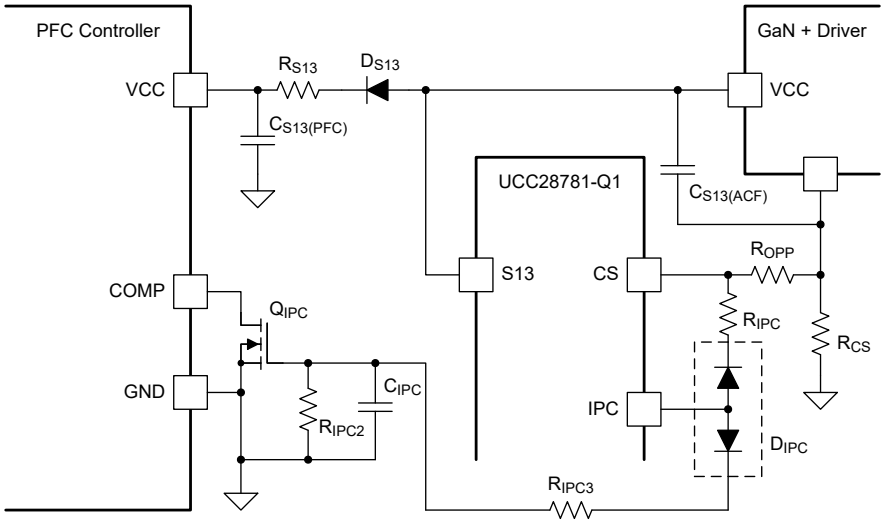


Figure 7-7. Power Management Function for a GaN Power IC and PFC Controller

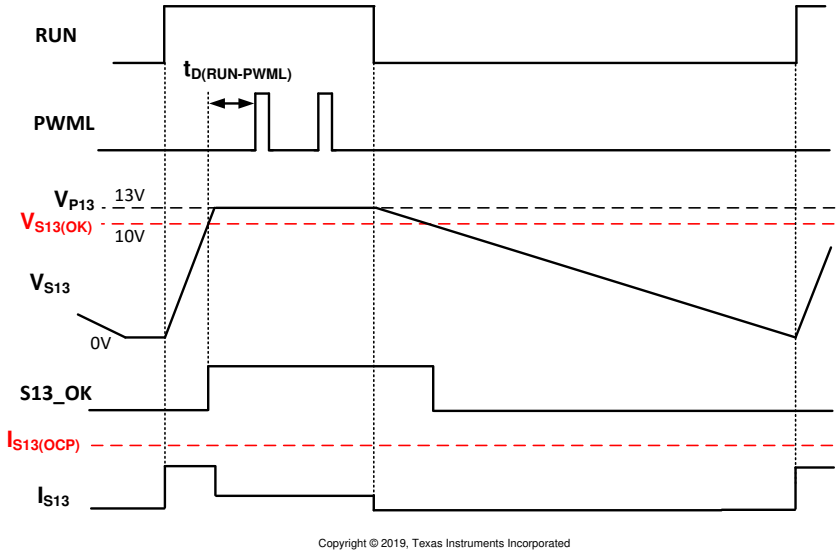


Figure 7-8. Power-up Sequence of the S13 Pin

When the S13 pin supplies both the GaN power IC and a PFC controller at the same time, a low-voltage rectifier diode (D_{S13}) between the S13 pin and the PFC controller bias VCC pin is needed, so the local decoupling capacitor for each powered device can be separated. The decoupling capacitor of the PFC controller ($C_{S13(PFC)}$) is usually larger than the one for a GaN power IC, such that the bias voltage of the GaN power IC will discharge more quickly without affecting the PFC bias voltage and PFC output voltage regulation. If the S13 pin supplies a PFC controller only, the rectifier diode is not needed.

During start-up before VDD reaches the $V_{VDD(ON)}$ threshold, the S13 switch stays off, so the S13-pin loading will not consume any of the charging current of VDD capacitor flowing from SWS pin to VDD pin, thereby enabling a fast start-up sequence. Under this condition, the PFC controller will be off resulting in a lower PFC bus voltage below 400 V.

7.3.7 IPC Pin (Intelligent Power Control Pin)

Under certain conditions, the IPC pin provides a 50-µA current from an internal source ($I_{IPC(SBP2)}$) which is controlled by logic as shown in Figure 7-9. The voltage on the VS pin is sampled during the demagnetization time to obtain an indication of the reflected output voltage (NVO). When the VS-pin voltage is lower than the

2.4-V lower LV mode threshold ($V_{VSLV(LR)}$), the LOW_NVO logic signal is pulled high, and the current source is enabled during the run state of all normal control modes (SBP1, SBP2, LPM, ABM, and AAM).

When the sampled VS-pin voltage is higher than the 2.5-V upper LV mode threshold ($V_{VSLV(UP)}$), the LOW_NVO logic signal becomes low. In the LOW_NVO = 0 V case, the 50-µA current source is enabled in the run state of SBP2 mode only.

To minimize stand-by power, the 50-µA source is always disabled during the wait state of any control mode. Additionally, if V_{VDD} falls lower than the 13-V survival-mode threshold, the INT_STOP logic signal is pulled high and the current source is disabled during survival mode operation, irrespective of the V_{VS} level.

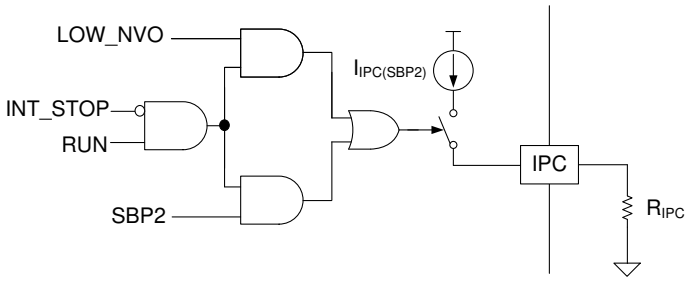


Figure 7-9. Control Circuit Diagram to the IPC-Pin Current Source

The multi-function IPC pin can be programmed to obtain one or more of the following benefits:

1. Reduction of input power for special light-load and stand-by conditions
2. Improvement of light-load efficiency at lower output voltages, such as 5 V and 9 V
3. Reduction of burst-mode output ripple at lower output voltages
4. Reduction of the over-power limit at lower output voltages
5. Power management of a PFC controller, together with the S13 pin

To implement the benefit No. 1, connect a resistor R_{IPC} from IPC pin to AGND pin. The 50-µA current source establishes a voltage (V_{IPC}) across R_{IPC} to program an increase in the CS-pin peak primary current threshold at very light loads. The transfer function between V_{IPC} and the CS threshold (V_{CST_IPC}) in SBP2 mode is illustrated in Figure 7-10.

Proper sizing of R_{IPC} to AGND can further reduce the burst frequency in SBP2 for so-called *tiny-load* power and for stand-by power.

When V_{IPC} is less than 0.9 V (or IPC is shorted to AGND), V_{CST_IPC} threshold stays at the minimum level of 0.15 V. When V_{IPC} is set between 0.9 V and 1.8 V, V_{CST_IPC} is clamped at 0.27 V. For V_{IPC} between 1.8 V and 3.8 V, there is a linear programmable V_{CST_IPC} range between 0.27 V and 0.4 V. When V_{IPC} is greater than 3.8 V, V_{CST_IPC} remains clamped to 0.4 V. Be aware that high settings of V_{CST_IPC} may, in some cases, introduce higher output ripple in deep light-load condition or provoke audible noise.

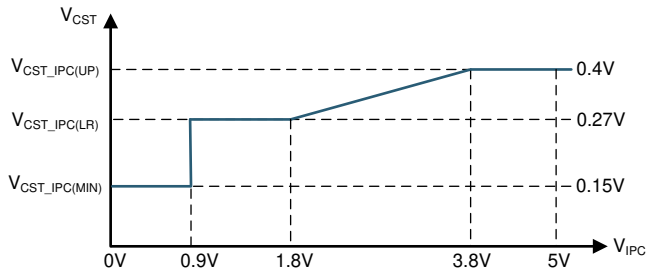


Figure 7-10. IPC Transfer Function to Program the SBP2 Peak Current Threshold

Because the enable status of the IPC current source contains the very useful output voltage information from the LOW_NVO logic state, the IPC pin can be used to further optimize power stage performance over a wide output voltage range. To gain benefits No.2, No. 3, and No. 4 of the IPC function, connect R_{IPC} between the IPC pin and the CS pin, so that the current source can create additional CS-pin offset voltage on R_{OPP} when V_{VS} < 2.4 V. With higher CS offset, the operating range of the V_{CST} signal will be higher than the actual power stage peak current. This forces the controller to operate in AAM mode for a wider actual output load range, and forces the burst-mode threshold down to a lower power level.

Figure 7-11 shows the side effect of the IPC-to-CS connection if the R_{IPC} setting is the same. Because the controller enables 50 µA in the run state of SBP2, the lower peak magnetizing current of the IPC-to-CS connection makes the SBP2 burst frequency higher and results in weakening the stand-by power improvement. Therefore, a higher R_{IPC} is needed to increase V_{CST_IPC} to compensate the peak current change.

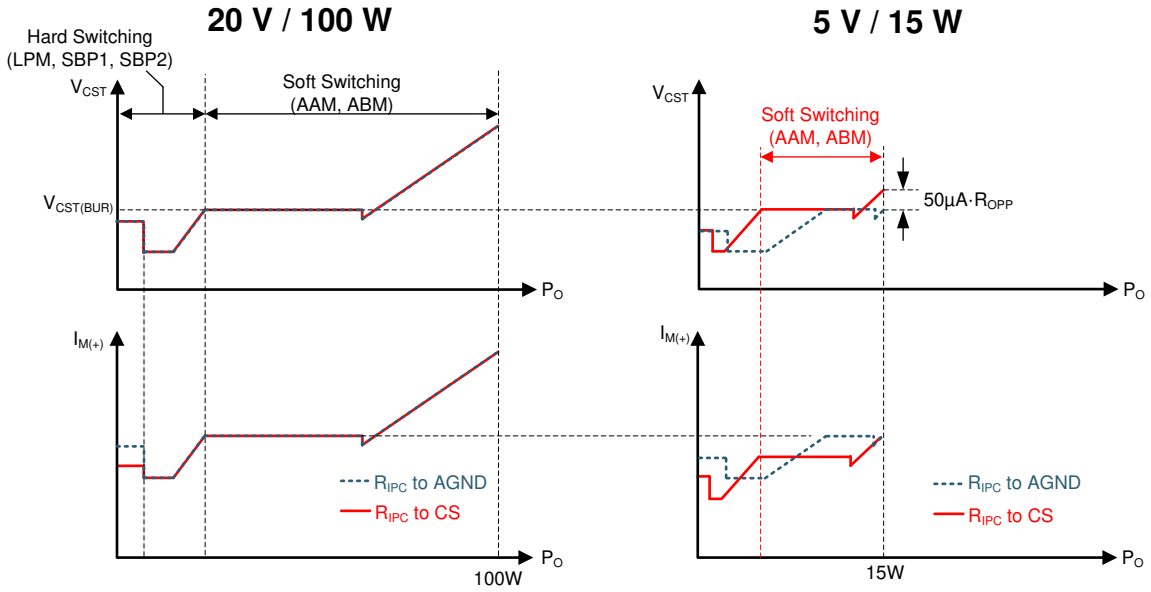


Figure 7-11. Effect of the CS-pin Offset Voltage from the IPC Pin

For benefit No. 5, the IPC pin can also be used to disable a PFC controller (if used) at all load conditions for lower voltage outputs to further improve the light-load efficiency . As shown in Power Management Function for a GaN Power IC and PFC Controller, the diode D_{IPC} in series with R_{IPC} is placed between IPC and CS pins, and V_{IPC} established at IPC is used to drive a small-signal switch Q_{IPC} to disable the PFC controller such as UCC28056.

When V_{IPC} is higher than its threshold voltage, Q_{IPC} can pull low the COMP pin voltage of a PFC controller, so its switching is disabled. As a consequence, PFC output voltage drops from the typical 400-V regulation level to the peak value of the AC line. This lowers the bulk voltage, which reduces the ZVS energy, which increases power stage efficiency for low voltage outputs. Furthermore, the power loss of the PFC power stage is out of the efficiency equation. One design example for those components are $C_{S13(ZVSF)}$ = 22 nF, $C_{S13(PFC)}$ = 0.22 µF, C_{IPC} = 10 nF, R_{IPC} = 69.8 kΩ, R_{IPC2} = 10 MΩ, and R_{IPC3} = 20 kΩ. Choose Q_{IPC} with threshold voltage less than 1.5 V to ensure that V_{IPC} is sufficient to achieve low on-resistance ($R_{DS(on)}$) even at very low burst frequencies.

7.3.8 RUN Pin (Driver and Bias Source for Isolator)

The RUN pin is a logic-level output signal which enables PWM switching when active high. When RUN is low, all PWML and PWMH switching is disabled and the controller enters a low-current wait state.

In addition to enabling switching, RUN is capable of sourcing considerable current to bias an external gate driver and perform a power management function on the primary side of a digital isolator. It generates a 5-V logic output when the driver should be active, and pulls down to less than 0.5 V when the driver should be disabled.

During the off-time of any burst mode, the RUN pin serves as a power-management function to dynamically reduce the static bias current of the isolator/ driver, so light-load efficiency can be further improved and stand-by power can be minimized.

As RUN goes high, while its voltage is less than 3 V, a 44-mA peak pull-up current is supplied from the internal P13 regulator. With this current, the RUN driver can quickly charge the primary-side decoupling capacitor of a digital isolator above its UVLO(ON) threshold. A Schottky diode can block discharge of this capacitor when RUN goes low. When the RUN voltage goes above 3 V, P13 stops providing current and the pull-up is supplied from the REF regulator, so the peak driving capability will be limited in order to avoid triggering the over-current protection of the REF regulator. When RUN is low for a long burst off-time, the decoupling capacitor of the digital isolator will be gradually discharged below its UVLO(OFF) threshold, so the isolator power loss can be minimized.

There are three delays between RUN going high to the first PWML pulse going high in each burst packet. The first delay is a fixed 2.2-µs delay time, intended to provide an appropriate "wake-up" time for the controller and the gate driver to transition from a wait state to a run state. The second delay is gated by the 10-V power-good threshold of the S13 pin. PWML will not go high until S13 voltage exceeds 10 V. The third delay is another 2.2-µs timeout, t_{ZC} in the electrical table, intended to turn on the low-side switch of the first switching cycle per burst packet around the valley point of DCM ringing by waiting for the zero-crossing detection (ZCD) on the auxiliary winding voltage (V_{AUX}). If ZCD is detected (on the VS input) before the t_{ZC} timeout elapses, PWML is immediately driven. If no ZCD is detected, PWML is driven when t_{ZC} elapses. The first two delays can be concurrent; the third delay is sequential.

Therefore, the minimum total delay time is 2.2 µs typically if V_{S13} > 10 V and ZCD is detected immediately after the 2.2-µs wake-up time. If V_{S13} < 10 V, the total delay time with tolerance over temperature is listed as $t_{D(RUN-PWML)}$ in the electrical table.

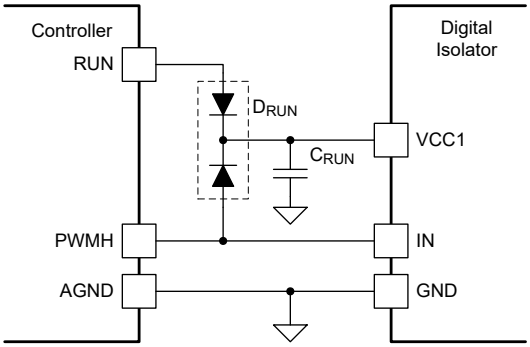


Figure 7-12. Power Management Circuit

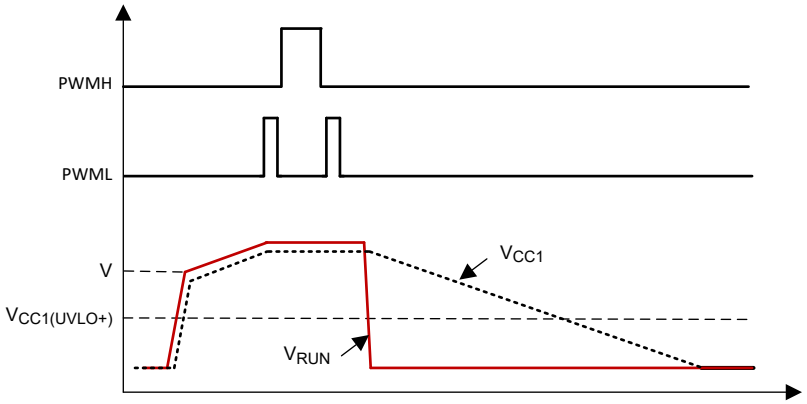


Figure 7-13. Power Management Waveform

7.3.9 PWMH and AGND Pins

The PWMH pin controls the gate of an SR MOSFET through an external isolating gate-driver. PWMH may also be used to bias the primary-side of the gate-driver. The PWMH driver ground return is referenced to the AGND pin. The maximum voltage level of PWMH is clamped to 5-V REF level. As PWMH goes high, when its voltage is less than 3 V, up to 21-mA peak pull-up current may be supplied from the P13 regulator. When the PWMH voltage goes above 3 V, the pull-up is supplied from the REF regulator instead, so the peak driving capability is limited to less than 6 mA to avoid tripping the over-current protection of the REF regulator.

As shown in Figure 7-12, since the RUN driver charges the decoupling capacitor of a digital isolator first through one small-signal diode at the beginning of every burst cycle, the sourcing current of PWMH is sufficient to send the control signal to the isolator and supply the continuous isolator operating current together with the RUN driver at the same time through another small-signal diode. The high peak driving capability of PWMH provides the flexibility of signal transmission through a digitally isolated gate-driver with opto-compatible input.

It is prudent to choose an isolated gate-driver with minimal power-up delay on both input and output sides to avoid missing several PWMH pulses for SR control.

AGND pin is the ground return for all the analog control signals, RUN driver, and PWMH driver. It is required to implement a careful layout separation from other noisy ground return paths, such as PGND and power stage ground. The thermal pad should be connected to the AGND pin directly and could be a Kelvin connection point to the related external components. For details of the grounding layout guideline and noise decoupling techniques, one can refer to the Section 8.1 of this datasheet.

7.3.10 PWML and PGND Pins

The PWML pin is the primary-side switch gate-drive, for which ground return is referenced to the PGND pin. The strong driver with 0.5-A peak source and 1.9-A peak sink capability can control either a silicon power MOSFET with a higher gate-to-source capacitance, a cascode GaN, an E-mode gate-injection-transistor (GIT) GaN with continuous on-state current, or a GaN power IC with logic PWM input.

The maximum voltage level of PWML is clamped to the P13 pin voltage. The 13-V clamped gate voltage provides an optimal gate-drive for low on-state resistance and lower gate-driving loss. An external gate resistor in parallel with a fast recovery diode can be used to further reduce the turn-on speed without compromising the turn-off switching loss. Slower turn-on speed of the primary switch mitigates the voltage stress across the secondary-side rectifier when the SR switch is disabled in deep light-load condition, and reduces the switching-node dV/dt to a safe level for reducing stress on the high-voltage isolating SR driver. A decoupling capacitor much larger than the PWML capacitive loading should be placed between P13 and PGND pins to decouple the gate-drive loop to allow operation at higher switching frequency. The 15-ns propagation delay of the PWML driver enables a higher frequency operation and more consistent ZVS switching.

Figure 7-14 and Figure 7-15 shows the example PWML driving network for a GIT GaN device and for a silicon MOSFET. Resistor R_{G2} controls the turn-on speed. The turn-off speed can be maintained by the two fast recovery diodes, D_{G1} and D_{G2}. R_{G1} provides a continuous driving path to maintain the on state and low on-resistance ($R_{DS(on)}$) of a GIT GaN. C_G avoids the small R_{G2} from affecting the on state current. PGND can be directly connected to the separate source terminal of a GIT GaN to achieve a kelvin connection, so the driver loop parasitic inductance can be decoupled.

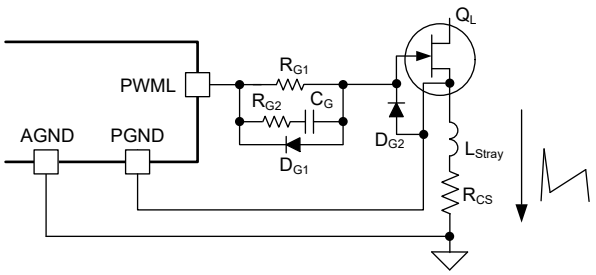


Figure 7-14. Driving a GIT GaN Device

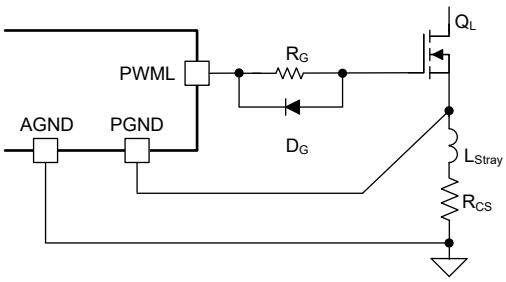


Figure 7-15. Driving a Si MOSFET

An internal low-voltage level shifter is included between PGND and the ground return pin for analog control signals (AGND), so PGND can be connected separately to the top of the current sense resistor (R_{CS}) to achieve a Kelvin connection. When hard switching condition occurs, the lumped parasitic capacitor on the switch node is discharged, so a positive voltage spike is created across R_{CS}. In soft switching condition, the negative magnetizing current flowing through R_{CS} can create a negative voltage spike on R_{CS}. The level shifter is designed to handle 5-V positive transient spike and -1-V negative stress between PGND pin and AGND pin.

7.3.11 SET Pin

Due to different capacitance non-linearity between Si and GaN power FETs as well as different propagation delays of their drivers, the SET pin is provided to program critical parameters of UCC28781-Q1 for the two different power stages.

Firstly, this pin sets the zero-voltage threshold ($V_{TH(SWS)}$) at the SWS input pin to be one of two different auto-tuning targets for ZVS control. When SET pin is tied to AGND, $V_{TH(SWS)}$ is set at its low level of 4 V for

realizing full ZVS, which allows the low-side switch (Q_L) to be turned on when the switch-node voltage drops close to 0 V. When SET pin is tied to REF pin, $V_{TH(SWS)}$ is set at 8.5 V for implementing partial ZVS, which makes Q_L turn on at around 8.5 V.

Secondly, the SET pin also selects the current-sense leading-edge blanking time (t_{CSLEB}) to accommodate different delays of the gate drivers; 110 ns for V_{SET} = 0 V and 190 ns for V_{SET} = 5 V.

Thirdly, the minimum PWML on-time ($t_{ON(MIN)}$) in low-power mode and standby-power mode is 110 ns for V_{SET} = 0 V, and is 100 ns for V_{SET} = 5 V.

Finally, the maximum PWML on-time to detect CS pin fault (t_{CSF}) is adjusted. t_{CSF} for V_{SET} = 5 V (t_{CSF1}) is set at 2 µs. t_{CSF} for V_{SET} = 0 V (t_{CSF0}) depends on the value of R_{RDM}. t_{CSF0} is configured to 2 µs when $R_{RDM} \geq R_{RDM(TH)}$ and to 1 µs when $R_{RDM} < R_{RDM(TH)}$.

7.3.12 RTZ Pin (Sets Delay for Transition Time to Zero)

The dead-time between PWMH falling edge and PWML rising edge (t_Z) serves as the wait time for V_{SW} transition from its high level down to the target ZVS point. Since the optimal t_Z varies with V_{BULK}, the internal dead-time optimizer automatically extends t_Z as V_{BULK} is less than the highest voltage of the input bulk capacitor ($V_{BULK(MAX)}$). The circulating energy for ZVS can be further reduced, obtaining higher efficiency at low line versus a fixed dead-time over a wide line voltage range. A resistor on the RTZ pin (R_{RTZ}) programs the minimum t_Z ($t_{Z(MIN)}$) at $V_{BULK(MAX)}$, which is the sum of the propagation delay of the synchronous rectifier driver ($t_{D(DR)}$) and the minimum resonant transition time of V_{SW} falling edge ($t_{LC(MIN)}$).

$$R_{RTZ} = K_{RTZ} \times t_{Z(min)} = K_{RTZ} \times \left(t_{D(DR)} + t_{LC(min)}\right) \quad (9)$$

where

- K_{RTZ} is equal to 11.2×10^{11} (unit: F^{-1}) for V_{SET} = 0 V
- K_{RTZ} is equal to 5.6×10^{11}(unit: F^{-1}) for V_{SET} = 5 V

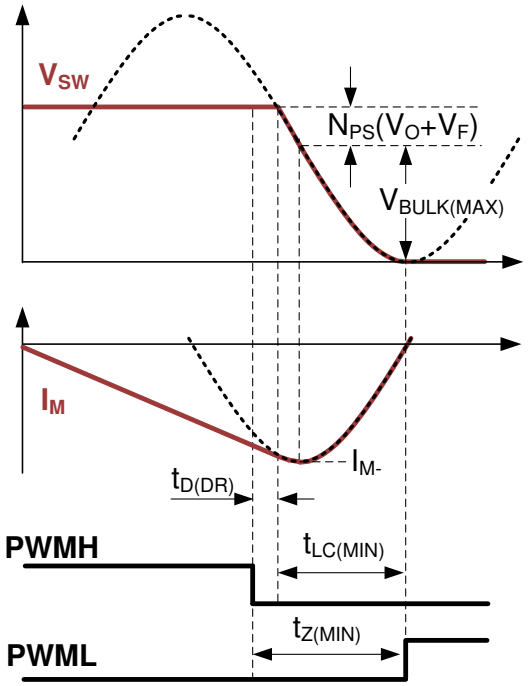


Figure 7-16. RTZ Setting for the Falling-edge Transition of V_{SW}

As illustrated in Figure 7-16, when PWMH turns off Q_{SR} after $t_{D(DR)}$ delay, the negative magnetizing current (i_{M-}) becomes an initial condition of the resonant tank formed by magnetizing inductance (L_M) and the switch-node capacitance (C_{SW}). C_{SW} is the total capacitive loading on the switch-node, including the junction capacitance (C_{OSS}) of the primary switch, reflected secondary-side capacitance, intra-winding capacitance of the transformer,

the snubber capacitor, and parasitic capacitance of the PCB traces between switch-node and ground. Unlike a conventional valley-switching flyback converter, the resonance of the Zconverter at high line does not begin at the peak of the sinusoidal trajectory. The transition time of V_{SW} takes less than half of the resonant period. The following $t_{LC(MIN)}$ expression quantifies the transition time for R_{RTZ} calculation, where an arccosine term represents the initial angle at the beginning of resonance. As an example, the value of π minus the arccosine term at $V_{BULK(MAX)}$ of 375 V, V_O of 20 V, and N_{PS} of 5 is around 0.585π, which is close to one quarter of the resonant period.

$$t_{LC(MIN)} = [\pi - \cos^{-1}(\frac{N_{PS}(V_O + V_F)}{V_{BULK(MAX)}})] \times \sqrt{L_M C_{SW}} \quad (10)$$

7.3.13 RDM Pin (Sets Synthesized Demagnetization Time for ZVS Tuning)

The R_{RDM} resistor provides the power stage information to the t_{DM} optimizer for auto-tuning the on-time of PWMH to achieve ZVS within a given t_Z discharge time. The following equation calculates the resistance, based on the knowledge of the primary magnetizing inductance (L_M), auxiliary-to-primary turns ratio (N_A/N_P), the values of the resistor divider (R_{VS1} and R_{VS2}) from the auxiliary winding to VS pin, and the current sense resistor (R_{CS}). Among those parameters, L_M contributes the most variation due to its typically wider tolerance. The optimizer is equipped with wide enough on-time tuning range of PWMH to cover tolerance errors. Therefore, just typical values are enough for the calculation.

$$R_{RDM} = \frac{N_A \times R_{VS2}}{N_P \times (R_{VS1} + R_{VS2})} \times \frac{K_{DM} \times L_M}{R_{CS}} \quad (11)$$

where

- K_{DM} is equal to 5.0×10^9 (unit: F^{-1}) for both V_{SET} = 5 V and V_{SET} = 0 V

7.3.14 XCD Pin

The XCD pin performs the X-capacitor discharge function in conjunction with the recommended external detection circuit, shown in Figure 7-17.

Note

The XCD application circuit must be connected to an AC input but not to a DC input, in order to avoid the thermal stress on those sensing components caused by enabling the discharge current repetitively.

If the XCD function is not needed, directly shorting the two XCD pins to the AGND pin disables the XCD pin function, so the controller wait-state current is further reduced. The external sensing circuit must be removed. (see Figure 7-18)

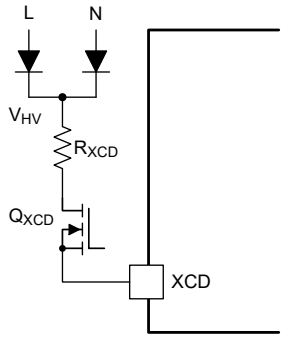


Figure 7-17. X-cap Discharge Circuit

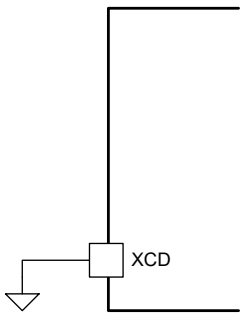


Figure 7-18. Disable XCD Functions

To form the discharge path in the first circuit, the anode nodes of two high-voltage diode rectifiers are connected to each X-cap terminal, the two diode cathodes are connected together to a 26-kΩ current limit resistance

(R_{XCD}), and the drain-to-source of a high-voltage depletion MOSFET (Q_{XCD}) couples the resistance to XCD pins. Since R_{XCD} needs to sustain the high voltage drop from the XCD-pin current, two series 13-kΩ SMD resistors in 1206 size with 26-kΩ total resistance are required to meet the voltage de-rating. A 600-V rated MOSFET such as BSS126 is needed as the high voltage blocking device. The MOSFET gate is connected to the P13 pin, so the highest voltage level of the XCD pins is limited to the sum of the P13-pin voltage and the threshold voltage of BSS126. The voltage level gives sufficient headroom over the 6.5-V line zero-crossing (LZC) threshold.

In case of single-fault event where one XCD pin is in fail-open condition, the redundant XCD pin helps to maintain the X-cap discharge function. In case of the single-fault event of BSS126 involving its drain-to-source in fail-short condition, an internal 26-V clamp helps to protect the XCD pin from exceeding its voltage rating. The current-limiting resistance (R_{XCD}) limits the fault current below the maximum clamping capability, however the value of R_{XCD} should avoid reducing the normal discharge current. A total resistance of 26 kΩ ±5% meets both criteria. The internal clamping function can also help to dissipate some of the line surge energy accumulated on the XCD pins in order to limit the pin voltage below its 30-V rating.

After the AC line is disconnected, X-capacitors in the EMI filters on the AC side of the diode-bridge rectifier must have means to discharge its residual voltage to a safe level within a certain time. Typically a high voltage discharge resistor bank is placed in parallel with the capacitor to form a discharge path. The value of the resistance is chosen to discharge the capacitance within the required time period. However, if the capacitance is large enough, the necessary lower value of discharge resistance will increase the standby power. The controller provides an active X-capacitor discharge function with 2-mA maximum discharge current capability to reduce the standby power. The discharge current is activated only when the detection criteria for the AC-line removal condition is met. The 6.5-V line zero-crossing (LZC) threshold on XCD pins is used to detect AC-line presence. When LZC is missing over an 84-ms detection timeout period, the discharge current is enabled for a maximum period of 300 ms followed by a 700-ms blanking time with no current. To detect the zero crossing reliably, as well as to save power consumption, a stair-case test current shown in Figure 7-19 is generated within the 84-ms detection time. The worst-case discharge current and timing are designed to discharge the X-capacitor up to 1 µF.

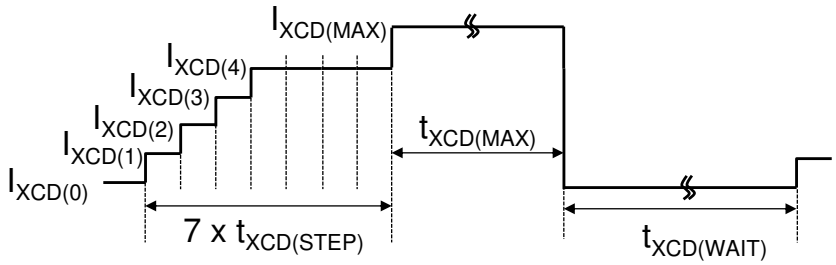


Figure 7-19. Step-current Profile into the XCD Pins for the X-cap Discharge Function

The four test current levels are designed to overcome the impact of leakage current from the bridge diode over a wide line range. Without enough test current level in a 12-ms period, the diode leakage current will prevent the XCD-pin voltage from reaching close to the 6.5-V LZC threshold. A higher AC line voltage or a higher diode junction temperature requires a higher test current due to the increased diode leakage current. When the AC line is connected, the four stair-case current levels and the 700-ms time out after the completion of LZC detection helps to minimize the average current sink from AC main and thereby the static power loss. For the first three current levels, every 12-ms time-out event commands the test current to increment. The last test current level has to be sustained for 48 ms without LZC, before triggering the 2-mA discharge mode. Whenever LZC is detected, any higher-level test-current steps are aborted and the 700-ms wait-state is initiated. Figure 7-20 shows the flow chart of X-capacitor discharge.

Note that the XCD-LATCH referenced in Figure 7-20 is a latch that is set when loss of AC line is confirmed. When set, this state allows X-capacitor discharge to proceed.

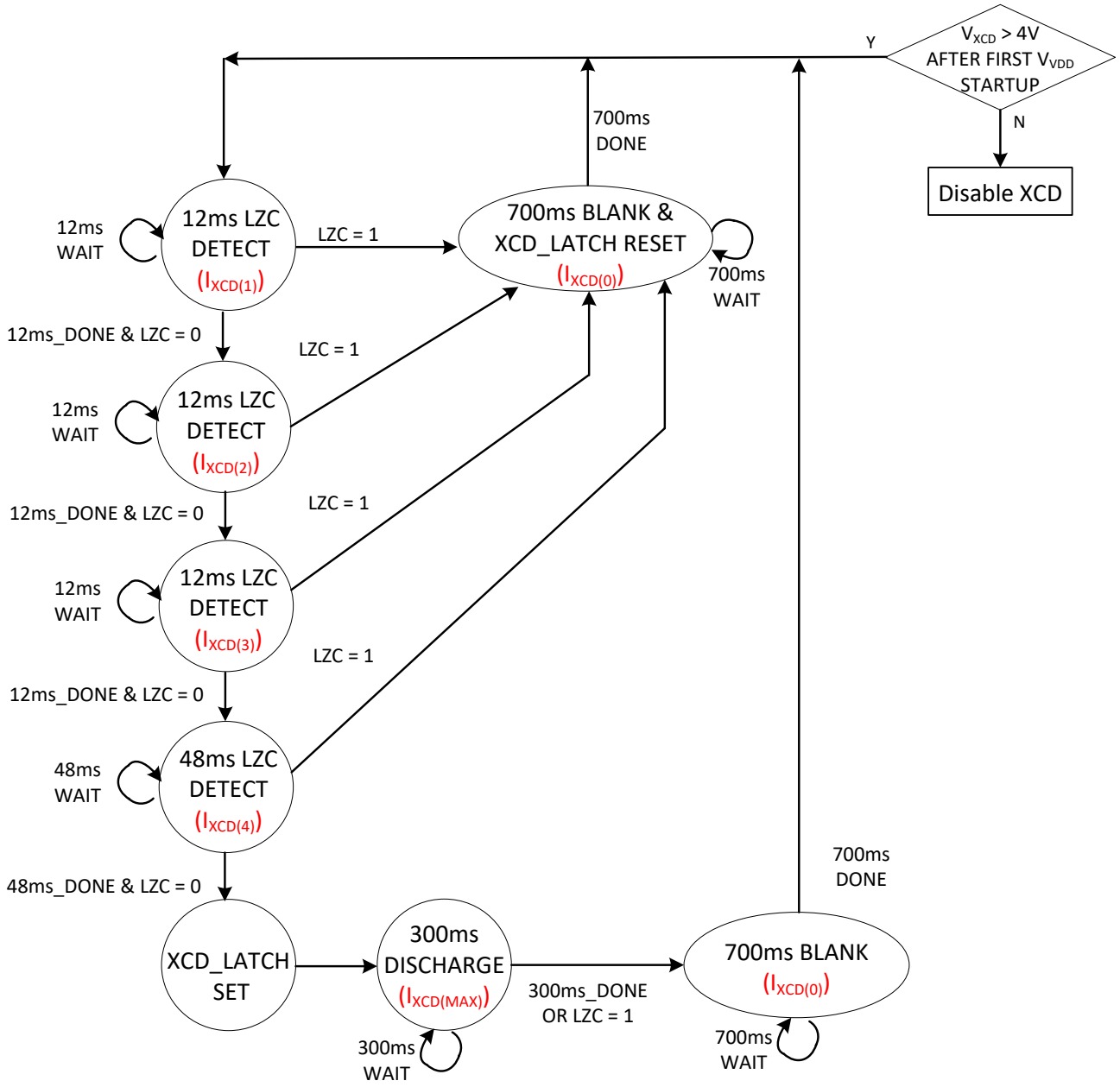


Figure 7-20. The State Diagram of the XCD-pin Function

Whenever any system protection is triggered, the converter switching is terminated and V_{VDD} restart cycle occurs between $V_{VDD(ON)}$ and $V_{VDD(OFF)}$. In this mode, the XCD pin function continues to operate, since the internal circuitry is separately biased from V_{VDD} instead of from V_{REF}.

Shorting the XCD pins to AGND disables the XCD function. After V_{VDD} first reaches $V_{VDD(ON)}$, an 80-µA test current is sourced out of the XCD pin in order to reliably identify the XCD-pin short with a low-impedance path to the AGND pin. If XCD is shorted to AGND, any path to L and N must be open to prevent R_{XCD} from overheating. When V_{XCD} is lower than 4 V before the RUN-pin first pulls high, the XCD function is disabled and the internal circuit will stop sourcing current from V_{VDD}.

7.3.15 CS, VS, and FLT Pins

The CS pin is the current-sense input. The internal peak current control loop limits the highest magnetizing current, and Section 7.4.4 in this datasheet describes the peak current change in different operating modes.

The VS pin is a multi-function sensing input, which detects the input voltage, the output voltage, and the zero-current-detection (ZCD) through the auxiliary winding voltage, to optimize ZVSF performance and provide critical protections.

The FLT pin is a dual-purpose fault detection pin for either over-temperature protection or input over-voltage protection, depending on how the external circuit is configured.

The system protection functions of these three pins are introduced in Section 7.4.12.

7.4 Device Functional Modes

7.4.1 Adaptive ZVS Control with Auto-Tuning

Figure 7-21 shows the simplified block diagram explaining the ZVS control of UCC28781-Q1 controller. A high-voltage sensing network provides a replica of the switch node voltage waveform (V_{SW}) with a limited "visible" lower voltage range that the SWS pin can handle. The ZVS discriminator identifies the ZVS condition and determines the adjustment direction for the on-time of PWMH (t_{DM}) by detecting if V_{SW} reaches a predetermined ZVS threshold, $V_{TH(SWS)}$, within t_Z, where t_Z is the targeted zero voltage transition time of V_{SW} controlled by the PWMH-to-PWML dead-time optimizer.

In Figure 7-21, V_{SW} of the current switching cycle in the dashed line has not reached $V_{TH(SWS)}$ after t_Z expires. The ZVS discriminator sends a TUNE signal to increase t_{DM} for the next switching cycle in the solid line, such that the negative magnetizing current (I_{M-}) can be increased to bring V_{SW} down to a lower level in the same t_Z. After a few switching cycles, the t_{DM} optimizer settles and locks into ZVS operation of the low-side switch (Q_L). In steady-state, there is a fine adjustment on t_{DM}, which is the least significant bit (LSB) of the ZVS tuning loop. This small change of t_{DM} in each switching cycle is too small to significantly move the ZVS condition away from the desired operating point. Figure 7-22 demonstrates how fast the ZVS control can lock into ZVS operation. Before the ZVS loop is settled, controller starts in a valley-switching mode as t_{DM} is not long enough to create sufficient I_{M-}. Within 15 switching cycles, the ZVS tuning loop settles and begins toggling t_{DM} with an LSB.

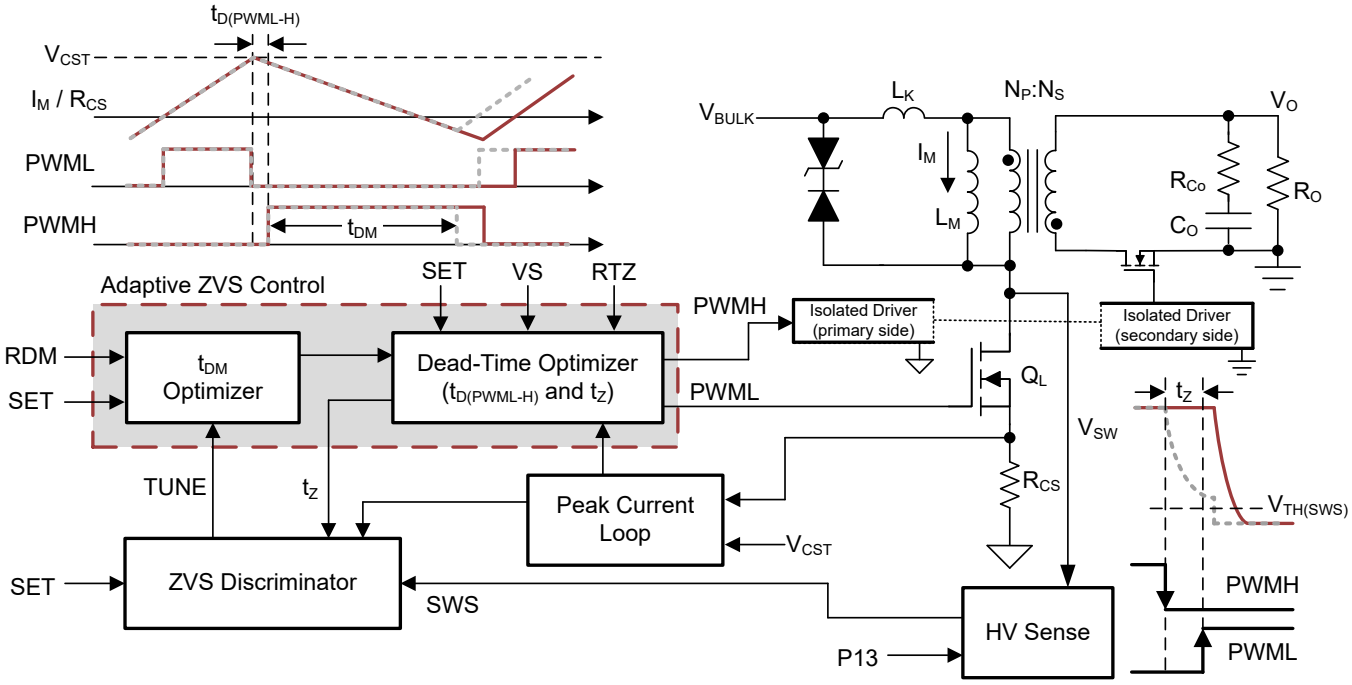


Figure 7-21. Block Diagram of Adaptive ZVS Control

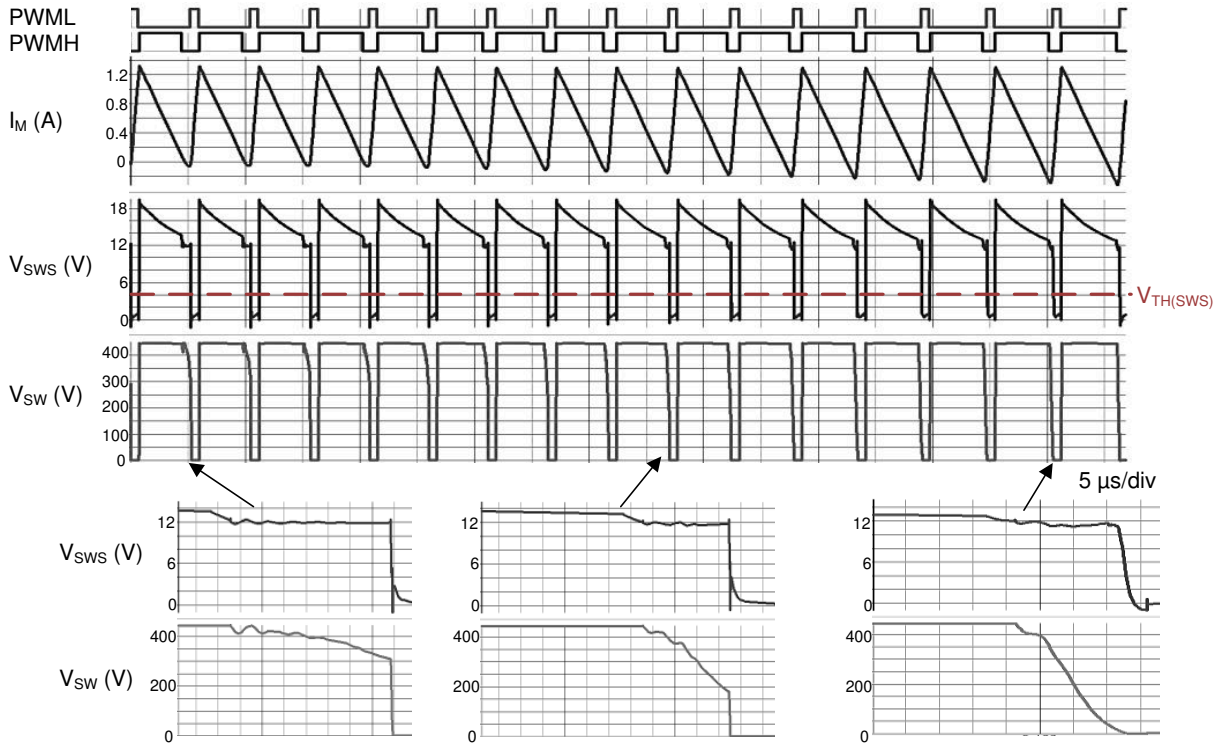


Figure 7-22. Auto-Tuning Process of Adaptive ZVS Control

7.4.2 Dead-Time Optimization

The dead-time optimizer in Figure 7-21 controls the two dead-times: the dead-time between PWMH falling edge and PWML rising edge (t_Z), as well as the dead-time between PWML falling edge and PWMH rising edge ($t_{D(PWML-H)}$).

The adaptive control law for t_Z utilizes the line feed-forward signal to extend t_Z as V_{BULK} reduces, as shown in Figure 7-23. The VS pin senses V_{BULK} through the auxiliary winding voltage (V_{AUX}) when the primary side switch (Q_L) is on. The auxiliary winding creates a line-sensing current (I_{VSL}) out of the VS pin flowing through the upper resistor of the voltage divider on VS pin (R_{VS1}). Minimum t_Z ($t_{Z(MIN)}$) is set at $V_{BULK(MAX)}$ through the RTZ pin. When I_{VSL} is lower than 666 µA, t_Z linearly increases and the maximum t_Z extension is 140% of $t_{Z(MIN)}$.

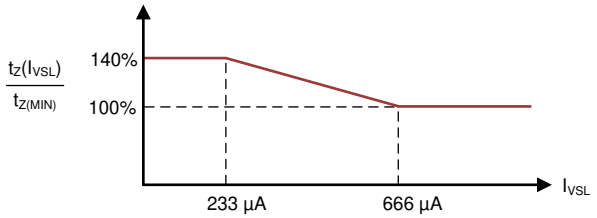


Figure 7-23. t_Z Control Optimized for Wide Input Voltage Range

The control law for $t_{D(PWML-H)}$ is adaptive with the slope variation of the switching node voltage, regardless of the SET-pin voltage as shown in Figure 7-24.

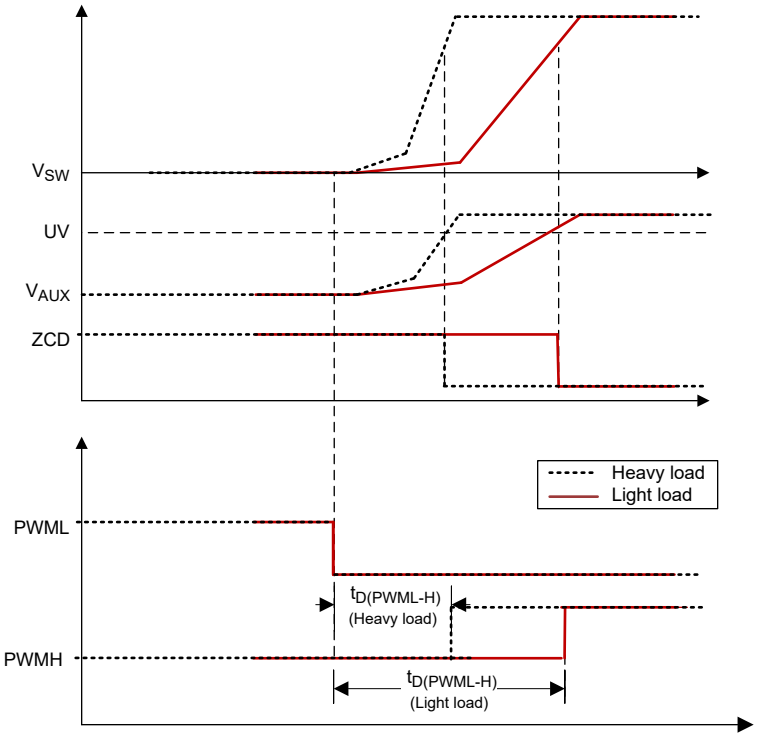


Figure 7-24. $t_{D(PWML-H)}$ Control Optimized for GaN and Si FETs

7.4.3 EMI Dither and Dither Fading Function

The frequency dither function in AAM reduces the conducted EMI noise and results in EMI filter size reduction. Conventionally, the dither carrier frequency is in the range of hundreds of Hz. However, when the control loop bandwidth is pushed higher in order to improve the load transient response, the control loop will be able to correct the disturbance from the dither signal, and weakens the EMI frequency spreading effectiveness. Even though increasing the dither frequency to few kHz can reduce the influence of the control loop, the audible noise issue will occur. For UCC28781-Q1, since itis able to run at a higher switching frequency in AAM, the dither frequency can be optimized at 23 kHz, so as to avoid audible noise and desensitize the loop response effect on the EMI attenuation.

UCC28781-Q1 enhances the response of the ZVS control loop, such that the ZVS performance can be maintained in most switching cycles even under a strong EMI dither condition. A triangular dither signal is superimposed on the feedback voltage signal V_{CST}, The novel feed-forward control method is applied to allow the ZVS loop to correct the timing error much faster, so ZVS can be maintained and the efficiency will not suffer.

Conventionally, the dither magnitude is fixed across the whole output voltage range. Since the higher output voltage condition needs to deliver a higher output power, the EMI issue is typically more severe, so a stronger dither signal is needed for more conducted EMI reduction. In the lower output voltage condition, the output ripple specification is usually much tighter, so a strong dither signal may aggravate the output voltage ripple and create the design tradeoff. For UCC28781-Q1, the two-level dither magnitude is adjusted automatically based on the output voltage level, so the perturbed output ripple at the lower output voltage condition can be reduced to meet a more stringent ripple requirement, and the strong dither can still be applied to the higher output voltage condition for the better EMI performance. Specifically, when V_{VS} is lower than 2.4 V during the demagnetization time (the LOW_NVO logic signal is high), the peak-to-peak dither magnitude on CS pin is reduced to around 36 mV. When V_{VS} is higher than 2.5 V, the peak-to-peak dither magnitude on CS pin is increased to around 98 mV.

Since the low-line efficiency usually determines the power stage thermal limit, the efficiency will drop further when EMI dither is enabled. Since the bulk capacitor ripple voltage at low line is bigger than at high line and AAM mode forces variable frequency operation, the line frequency causes nature dither frequency anyway even without applying the internal EMI dither. Therefore, taking advantage of AAM mode, the dither function at low line can be disabled based on the brown-in voltage setting, so the option provides design flexibility to trade-off the

worst-case low-line efficiency and EMI. Specifically, when i_{VSL} is higher than 646 µA, the EMI dither function is enabled. When i_{VSL} is lower than 580 µA, the EMI dither function is disabled. If the brown-in point is set at 75 Vac, this means that the EMI dither is disabled for 90 Vac and 115 Vac.

The dither fading feature allows the dither signal to be smoothly disabled, when the output load current is close to the transition point between AAM and ABM. As shown in Figure 7-25, $V_{CST(MAX)}$ and $V_{CST(BUR)}$ are used as the two voltage-clamping targets to the perturbed V_{CST} signal. When the V_{CST} reaches $V_{CST(MAX)}$, the top of the V_{CST} ripple content is clipped by the internal clamp circuit, so the influence of the EMI dither on the peak power capability can be eliminated. When the V_{CST} reaches $V_{CST(BUR)}$, the bottom of the V_{CST} ripple content is clipped by an another internal clamp circuit, so the influence of the EMI dither on the ABM waveform is removed.

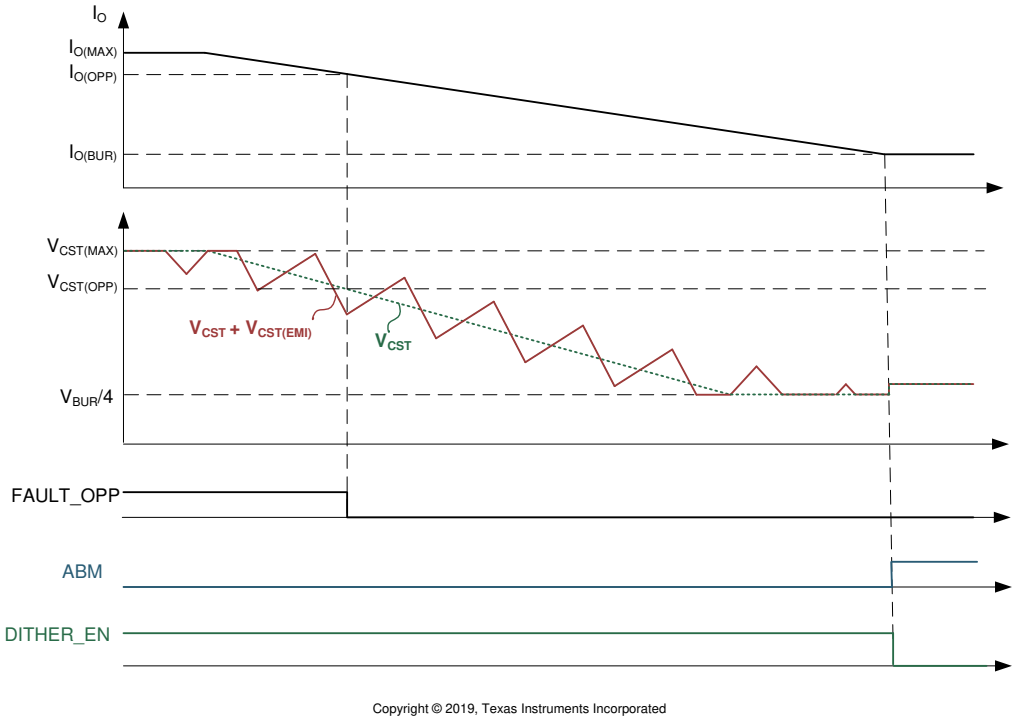


Figure 7-25. Dither Fading Feature in AAM

7.4.4 Control Law Across Entire Load Range

The UCC28781-Q1 offers six modes of operation summarized in Table 7-1. Starting from heavier load, the AAM mode forces PWML and PWMH into complementary switching with ZVS tuning enabled. ABM mode generates a group of PWML and PWMH pulses as a burst packet, and adjusts the burst off-time to regulate the output voltage. At the same time, the converter confines the burst frequency variation above 20 kHz by adjusting the number of PWML and PWMH pulses per packet to mitigate audible noise and reduce burst output ripple. In LPM, SBP1, and SBP2 modes, PWMH and the ZVS tuning loop are disabled, so the converter operates in valley-switching mode. The survival mode is to maintain V_{VDD} higher than $V_{VDD(OFF)}$ during a long interval of no switching.

Table 7-1. Functional Modes

	MODE	OPERATION	PWMH	ZVS
AAM	Adaptive Amplitude Modulation	PWML and PWMH in complementary switching	Enabled	Yes
ABM	Adaptive Burst Mode	Variable $f_{BUR} > f_{BUR(LR)}$, PWML and PWMH in complementary switching	Enabled	Yes
LPM	Low Power Mode	Fix $f_{BUR} \approx f_{LPM}$, valley-switching	Disabled	No
SBP1	First StandBy Power Mode	Variable f_{BUR} between $f_{SBP2(LR)}$ and $f_{SBP2(UP)}$, valley-switching	Disabled	No

Table 7-1. Functional Modes (continued)

	MODE	OPERATION	PWMH	ZVS
SBP2	Second StandBy Power Mode	Variable $f_{BUR} < f_{SBP2(UP)}$ as $V_{BUR} < 0.9$ V; Variable $f_{BUR} < f_{SBP2(LR)}$ as $V_{BUR} > 0.9$ V; Both are in valley-switching	Disabled	No
INT_STOP	Survival Mode	When $V_{VDD} < V_{VDD(OFF)} + V_{VDD(PCT)}$, a series of PWML pulses followed by a long PWMH pulse is generated	Enabled in the last switching cycle of a survival-mode burst packet	No

Figure 7-26 and Figure 7-28 show the critical parameter changes among the five operating modes, where V_{CST} is the peak current threshold compared with the current-sense voltage from the CS pin, f_{SW} is the switching frequency of PWML, f_{BUR} is the burst frequency, and N_{SW} is the pulse number of PWML cycles per burst packet. Figure 7-26 represents the control mode difference under the two VS-pin voltage ranges, when the IPC-pin voltage is less than 0.9 V or IPC is connected to AGND. Figure 7-28 illustrates the modified control mode, when the IPC-pin voltage setting is higher than 0.9 V. The following section explains the detailed operation of each mode. The following section discusses VS-pin voltage and IPC-pin voltage effects.

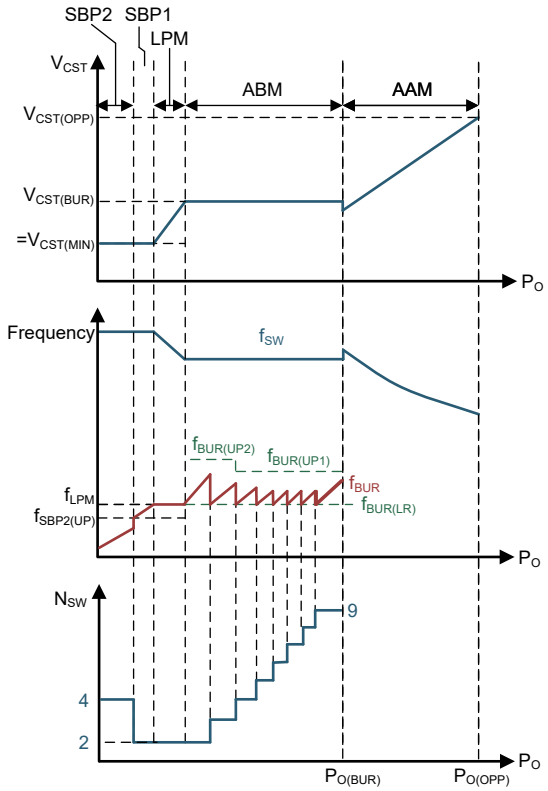


Figure 7-26. Control law for $V_{VS} > V_{VSLV(UP)}$ (LOW_NVO = 0)

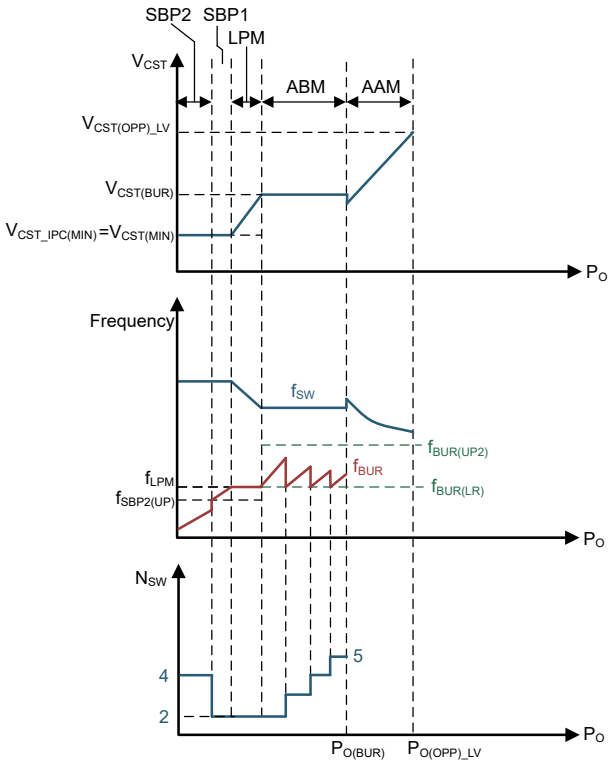


Figure 7-27. Control law for $V_{VS} < V_{VSLV(LR)}$ (LOW_NVO = 1)

Control Law Under Different Load Sweep Direction as $V_{IPC} > 0.9$ V and $V_{VS} > V_{VSLV(UP)}$

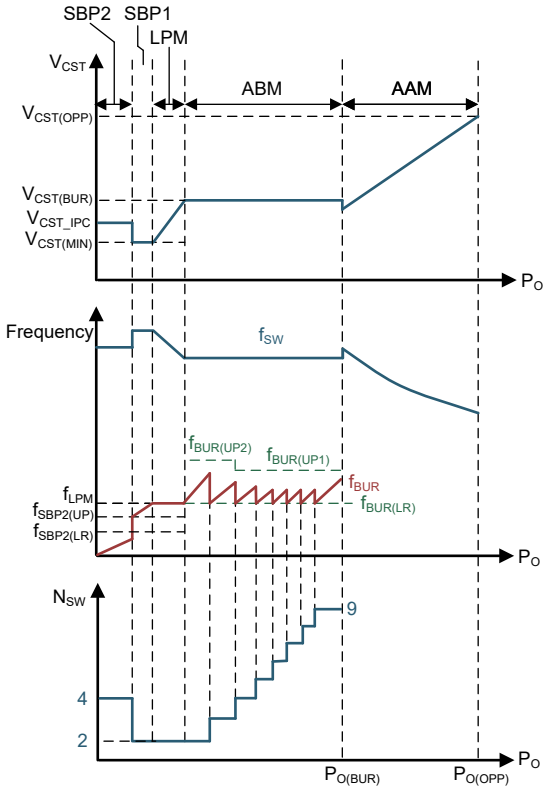


Figure 7-28. Full Load to Light Load

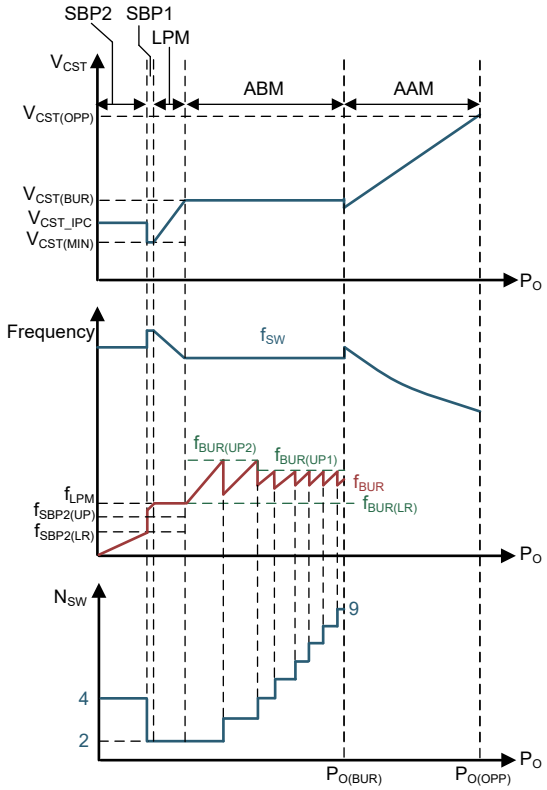


Figure 7-29. Light Load to Full Load

7.4.5 Adaptive Amplitude Modulation (AAM)

The switching pattern in AAM forces PWML and PWMH to alternate in a complementary fashion with dead-time in between, as shown in Figure 7-30. As the load current reduces, the negative magnetizing current (I_{M-}) stays the same, while the positive magnetizing current (I_{M+}) reduces by the internal peak current loop to regulate the output voltage. I_{M+} generates a current-feedback signal (V_{CS}) on the CS pin through a current-sense resistor (R_{CS}) in series with Q_L source and a peak current threshold (V_{CST}) in the current loop controls the peak current variation. Due to the nature of transition-mode (TM) operation, lowering the peak current with lighter load conditions results in higher switching frequency. When the load current increases to an over-power condition ($I_{O(OPP)}$) where V_{CST} correspondingly reaches an OPP threshold ($V_{CST(OPP)}$) of the peak current loop, the OPP fault response will be triggered after a 160-ms timeout. The RUN signal stays high in AAM, so the half-bridge driver remains active.

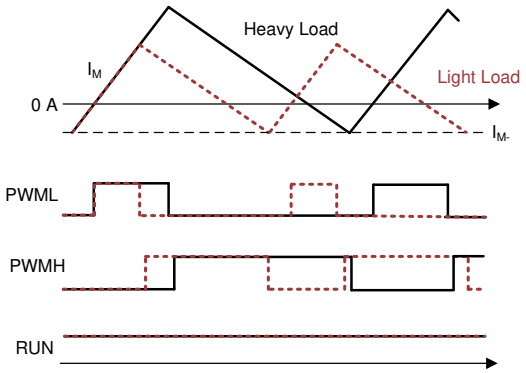


Figure 7-30. PWM Pattern in AAM

7.4.6 Adaptive Burst Mode (ABM)

As the load current reduces to $I_{O(BUR)}$ where V_{CS} reaches the $V_{CST(BUR)}$ threshold, the control mode transitions to ABM starts and V_{CS} is clamped. The peak magnetizing current and the switching frequency (f_{SW}) of each switching cycle are fixed for a given input voltage level. $V_{CST(BUR)}$ is programmed by the BUR pin voltage (V_{BUR}). The PWM pattern of ABM is shown in Figure 7-31. When RUN goes high, a delay time between RUN and PWML ($t_{D(RUN-PWML)}$) is given to allow both the gate driver and the UCC28781-Q1 controller time to wake up from a wait state to a run state. The first PWML pulse turns on Q_L close to a valley point of the DCM ringing on the switch-node voltage (V_{SW}) by sensing the condition of zero crossing detection (ZCD) on the auxiliary winding voltage (V_{AUX}).

The following switching cycles operate in a ZVS condition, since PWMH is enabled. As the number of PWML pulses (N_{SW}) in the burst packet reaches its target value, the RUN pin pulls low after the ZCD of the last switching cycle is detected, and forces the isolated gate driver and controller into a wait state for the quiescent current reduction of both devices. In this mode, the minimum off-time of the RUN signal is 2.2 µs and the minimum on-time of PWML is limited to the leading-edge blanking time (t_{CSLEB}) of the peak current loop. However, more grouped pulses means more risk of higher output ripple and higher audible noise. The following equation estimates how burst frequency (f_{BUR}) varies with output load and other parameters.

$$f_{BUR} = \frac{I_O}{I_{O(BUR)}} \times \frac{f_{SW}}{N_{SW}} \tag{12}$$

As $I_O < I_{O(BUR)}$, f_{BUR} can become lower than the audible noise range if N_{SW} is fixed. In ABM, N_{SW} is modulated to ensure f_{BUR} stays above 20 kHz by monitoring f_{BUR} in each burst period. As I_O decreases, f_{BUR} decreases and reaches a predetermined low-level frequency threshold ($f_{BUR(LR)}$) of 25 kHz. The ABM loop commands N_{sw} of both PWML and PWMH to be reduced by one pulse to maintain f_{BUR} above $f_{BUR(LR)}$. At the same time, the burst frequency ripple on the output voltage reduces as N_{SW} drops with the load reduction. As I_O increases, f_{BUR} becomes higher and reaches a predetermined high-level frequency threshold ($f_{BUR(UP)}$). The ABM loop commands N_{SW} to be increased by one pulse to push f_{BUR} back below $f_{BUR(UP)}$.

The maximum N_{SW} and the $f_{BUR(UP)}$ thresholds are modified based on the output voltage condition, i.e., the positive VS-pin voltage level. When the V_{VS} sampled at the PWMH falling edge is less than the 2.4-V threshold ($V_{VSLV(LR)}$), the maximum N_{SW} is 5 pulses and the $f_{BUR(UP2)}$ is 50 kHz. When the sampled V_{VS} is higher than the 2.5-V threshold ($V_{VSLV(UP)}$), the maximum N_{SW} is 9 pulses, the $f_{BUR(UP2)}$ is 50 kHz for $N_{SW} \leq 3$, and the $f_{BUR(UP1)}$ is 34 kHz for $N_{SW} > 3$. The IPC-pin voltage does not affect the parameters in ABM mode.

This algorithm maximizes the number of pulses in each burst packet to improve light-load efficiency, while also limiting the burst output ripple and audible noise. As I_O is close to the boundary between AAM and ABM, the two burst packets with the maximum pulse count may start to bundle together. In order to mitigate the output ripple and audible noise concerns, when the bundled burst packet appears two times within eight sequential burst cycles, the 5-µA current sink into the BUR pin is enabled to reduce V_{BUR} . The less energy per cycle with a lower V_{BUR}will force the control loop to transition from ABM to AAM smoothly in order to allow the peak current increase to maintain the output voltage regulation.

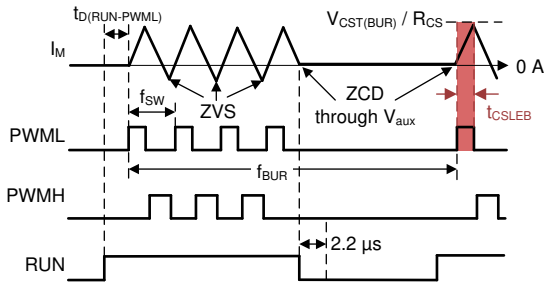


Figure 7-31. PWM Pattern in ABM

7.4.7 Low Power Mode (LPM)

As N_{SW} drops to two in ABM and the condition of f_{BUR} less than $f_{BUR(LR)}$ is qualified under two consecutive burst periods, the controller enters into LPM mode and disables PWMH. The purpose of LPM is to provide a soft peak current transition between $V_{CST(BUR)}$ and $V_{CST(MIN)}$. LPM fixes N_{SW} at two and sets f_{BUR} equal to f_{LPM} of 25 kHz. In LPM mode, V_{CST} is controlled to regulate the output voltage. At the start of each burst packet, after RUN pulls high, $t_{D(RUN-PWML)}$ is used to wake up both the isolated gate driver and the controller. With PWMH disabled, the two PWML pulses turn on Q_L close to valley-switching by sensing ZCD. When ZCD is detected again at the end of the second pulse, the RUN pin goes low and the controller enters its low-power wait state. For LPM mode with the SET pin connected to REF, the minimum on-time of PWML can be further reduced to $t_{ON(MIN)}$, to allow the peak magnetizing current to be reduced below the level limited by t_{CSLEB} of the peak current loop. In this condition, operation of the LPM control loop is changed from a current-mode control to a voltage-mode control, so the on-time adjustment of PWML is not limited to t_{CSLEB}. With this feature, before f_{BUR} starts to fall below f_{LPM} and enters the audible frequency range of SBP mode, the peak current is low enough to limit the magnitude of audible excitation.

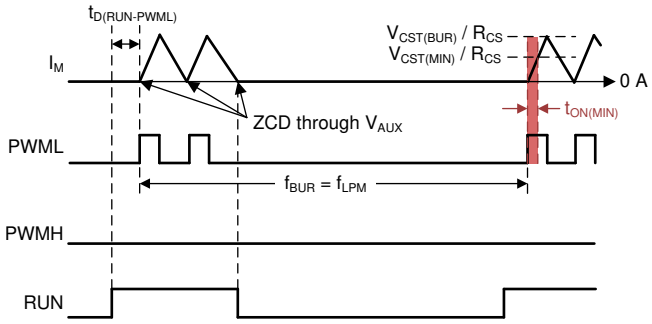


Figure 7-32. PWM Pattern in LPM

7.4.8 First Standby Power Mode (SBP1)

As V_{CST} drops to $V_{CST(MIN)}$, UCC28781-Q1 enters into SBP1 mode and PWMH continues to stay disabled. The purpose of SBP1 is to lower f_{BUR} in order to minimize power loss. SBP1 fixes N_{SW} at two and V_{CST} to $V_{CST(MIN)}$, while the burst off-time is adjusted to regulate the output voltage. As f_{BUR} is well below f_{LPM}, the switching-related loss can be minimized. In addition, lowering f_{BUR} forces both the isolated gate driver and controller to remain in wait states longer to minimize the static power loss. The equivalent static current of the controller in SBP can be represented as

$$I_{VDD(SBP)} = (I_{RUN} - I_{WAIT}) \times \left(\frac{2}{f_{SW(SBP)}} + t_{D(RUN-PWML)}\right) \times f_{BUR} + I_{WAIT} \quad (13)$$

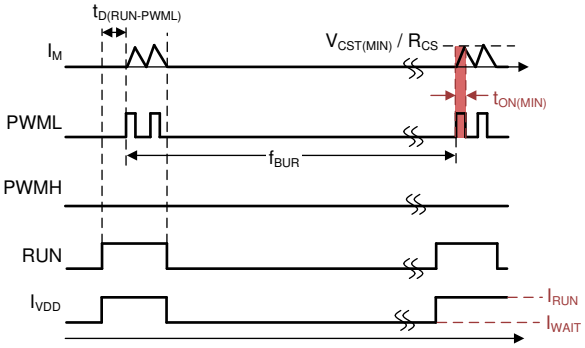


Figure 7-33. PWM Pattern in SBP1

7.4.9 Second Standby Power Mode (SBP2)

When f_{BUR} is below the 8.5-kHz upper burst frequency threshold ($f_{SBP2(UP)}$), UCC28781-Q1 exits SBP1 mode and enters into SBP2 mode. Compared with the SBP1 mode, the pulse count is doubled and V_{CST} can be

programmed by the IPC pin. The V_{CST} programmable range in SBP2 is between 0.27 V and 0.4 V. The purpose of SBP2 is to further lower f_{BUR} in order to minimize standby power.

The f_{BUR} condition to trigger the mode transition from SBP2 to SBP1 depends on the IPC pin voltage setting as well. If V_{IPC} is set lower than 0.9 V or the IPC pin is shorted to AGND, V_{CST} is equal to $V_{CST\_IPC(MIN)}$, and the mode transition occurs when f_{BUR} is increased above the same 8.5-kHz threshold. On the other hand, if V_{IPC} is set higher than 0.9 V, V_{CST} is higher than 0.27 V, and the mode transition occurs when f_{BUR} is increased above the 1.7-kHz lower burst frequency threshold ($f_{SBP2(LR)}$). The purpose of skipping the burst frequency range between 1.7 kHz and 8.5 kHz is to avoid the most sensitive audible frequency range to the human ear. The frequency skipping is only enabled, when the peak current is set higher by V_{IPC} > 0.9 V.

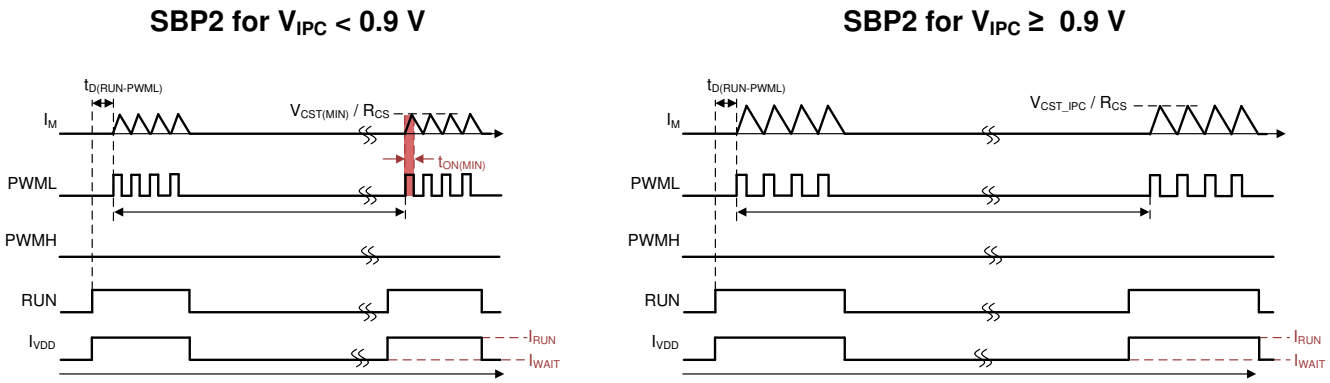


Figure 7-34. PWM Pattern in SBP2

7.4.10 Startup Sequence

Figure 7-35 shows the simplified block diagram related with the VDD startup function of UCC28781-Q1, and Figure 7-36 addresses the startup sequence. Table 7-2 describes specific startup waveform time periods.

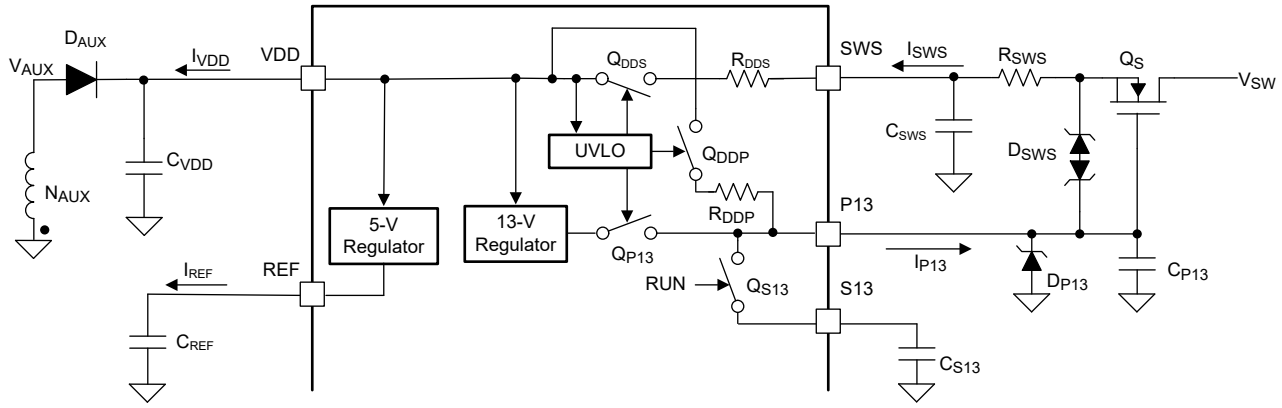


Figure 7-35. Functional Startup Block Diagram

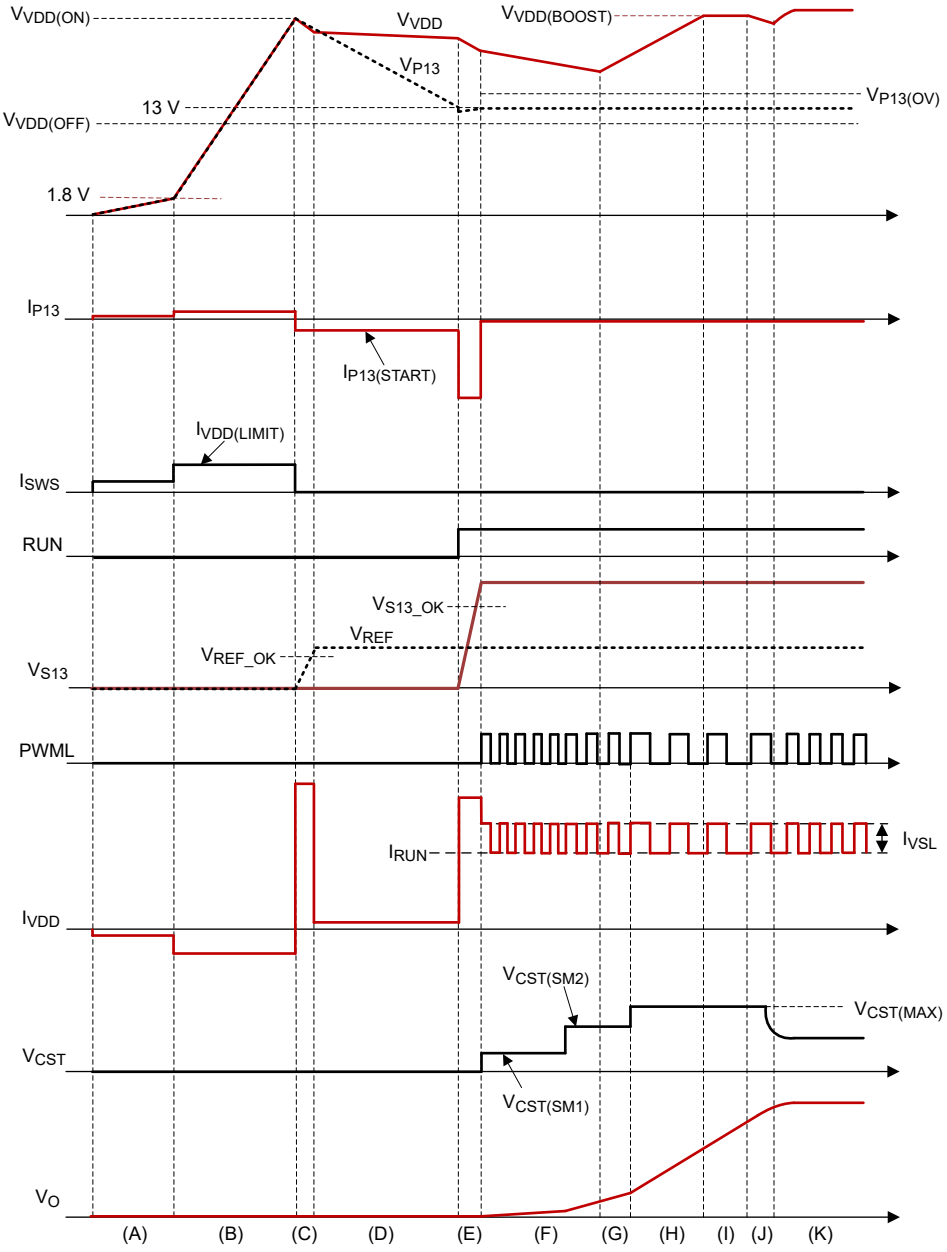


Figure 7-36. Startup Timing Waveforms

Table 7-2. Startup Time Intervals

TIME PERIOD	DESCRIPTION
A	The UVLO circuit commands the two internal power-path switches (Q_{DDS} and Q_{DDP}) to close the connections between SWS, VDD, and P13 pins through two serial current-limiting resistors (R_{DDS} and R_{DDP}). The depletion-mode MOSFET (Q_S) starts sourcing charge current (I_{SWS}) safely from the high-voltage switch-node voltage (V_{SW}) to the VDD capacitor (C_{VDD}). Before V_{VDD} reaches 1.8 V, I_{SWS} is limited by the high-resistance R_{DDS} of 5 kΩ to prevent potential device damage if C_{VDD} or VDD pin is shorted to ground.
B	After V_{VDD} rises above 1.8 V, R_{DDS} is reduced to a smaller resistance of 0.5 kΩ. I_{SWS} is increased to charge C_{VDD} faster. The maximum charge current during VDD startup can be quantified by Equation 8.

Table 7-2. Startup Time Intervals (continued)

TIME PERIOD	DESCRIPTION
C	As V_{VDD} reaches $V_{VDD(ON)}$ of 17 V, the ULVO circuit turns-off Q_{DDS} to disconnect the source pin of Q_S to C_{VDD}, and turns-off Q_{DDP} to break the gate-to-source connection of Q_S, so Q_S loses its current-charge capability. V_{VDD} then starts to drop, because the 5-V regulator on REF pin starts to charge up the reference capacitor (C_{REF}) to 5 V, for which the maximum charge current ($I_{SE(REF)}$) is self-limited at around 17 mA. After V_{REF} is settled, the UVLO circuit turns-on another power-path switch (Q_{P13}), so an internal 13-V regulator is connected to the P13 pin. The voltage on the P13 pin capacitor (C_{P13}) starts to be discharged by the regulator.
D	While discharging the recommended 1 µF on C_{P13} , the sink current of the 13-V regulator ($I_{P13(START)}$) is self-limited at around 2.2 mA, so it takes longer than 10 µs to settle to 13 V. If V_{P13} reaches 13 V in less than 10 µs, the P13 pin open fault is triggered to protect the device. Once V_{P13} has settled to 13 V without the fault event, RUN pin goes high and the controller enters a run state with $I_{VDD} = I_{RUN}$.
E	There is a minimum 2.2-µs delay from RUN going high to PWML starting to switch in order to wake-up the isolated gate driver and UCC28781-Q1. In this interval, the 2.8-Ω power path switch between the P13 pin and the S13 pin is enabled, so the S13-pin decoupling capacitor (C_{S13}) is charged up and the charge current is supplied from C_{P13} and the P13 regulator. If 2.2-µs delay is timed out before V_{S13} reaches to the 10-V power good threshold (V_{S13_OK}), the PWML switching instance is further delayed.
F	This is the soft-start region of peak magnetizing current. The first purpose is to limit the supply current if the output is short. The second purpose is to push the switching frequency higher than the audible frequency range during repetitive startup situations. At the beginning of V_O soft-start, the peak current is limited by two V_{CST} thresholds. The first V_{CST} startup threshold ($V_{CST(SM1)}$) is clamped at 0.2 V and the following second threshold ($V_{CST(SM2)}$) is 0.5 V. When $V_{CST} = V_{CST(SM1)}$, PWMH is disabled if the sampled VS pin voltage (V_{VS}) < 0.28 V, and the first five PWML pulses are forced to stay at this current level. After the sampled V_{VS} exceeds 0.28 V and the first five PWML pulses are generated, the peak current threshold changes from $V_{CST(SM1)}$ to $V_{CST(SM2)}$. In case of the inability to build up V_O with $V_{CST(SM1)}$ at the beginning of the V_O soft-start due to excessively large output capacitor and/or constant-current output load, there is an internal time-out of 0.7 ms to force V_{CST} to switch to $V_{CST(SM2)}$.
H	When V_{VS} rises above 0.5 V, V_{CST} is allowed to reach $V_{CST(MAX)}$, so the ramp rate of V_O startup becomes faster. When PWML is in a high state, I_{VDD} can be larger than I_{RUN}, because the 5-V regulator provides the line-sensing current pulse (I_{VSL}) on the VS pin to sense V_{BULK} condition.
J	When V_O gets close to the target regulation level, V_{CST} starts to reduce from $V_{CST(MAX)}$.
K	V_O and V_{CST} settle, and the auxiliary winding takes over the VDD supply.

7.4.11 Survival Mode of VDD (INT_STOP)

When an output voltage overshoot occurs during step-down load transients, the V_O feedback loop commands the UCC28781-Q1 controller to stop switching quickly by increasing I_{FB}, in order to prevent additional energy from aggravating the overshoot. Since V_{VDD} drops during this time, the typical way to prevent a controller from shutting down is to oversize the VDD capacitor (C_{VDD}) so as to hold V_{VDD} above $V_{VDD(OFF)}$. Instead, the controller is equipped with survival-mode operation to hold V_{VDD} above $V_{VDD(OFF)}$ during a transient event. Therefore, the size of C_{VDD} can be significantly reduced and the PCB footprint for the auxiliary power can be minimized. Specifically, there is a ripple comparator to regulate V_{VDD} above a 13-V threshold, which is $V_{VDD(OFF)}$ plus $V_{VDD(PCT)}$ in the electrical table. The ripple regulator is enabled when the V_O feedback loop requests the controller to stop switching due to V_O overshoot.

The regulator initiates unlimited PWML pulses when V_{VDD} drops lower than 13 V, and stops switching after V_{VDD} rises above 13 V. Since V_{VDD} is lower than the reflected output voltage overshoot, most of the magnetizing energy is delivered to the auxiliary winding and brings V_{VDD} above 13 V quickly. After V_O moves back to the regulation level, V_O feedback loop forces the controller to begin switching again by reducing I_{FB}, and the PWML and PWMH pulses are then controlled by the normal operating mode.

To prevent the controller from getting stuck in survival mode continuously or toggling between SBP and survival mode at zero load, follow these guidelines for the auxiliary power delivery path to VDD.

- The normal V_{VDD} level under regulated V_O must be designed to be above the 13-V threshold by an appropriate turns count for the auxiliary winding.
- C_{VDD} should not be over-sized, but designed just large enough to hold $V_{VDD} > V_{VDD(OFF)}$ under the longest V_O soft-start time.
- An auxiliary resistor in series with the auxiliary rectifier diode (D_{AUX}) should not be too large of value, because the lower series impedance can help the VDD capacitor to charge faster.

- Ensure good coupling between the auxiliary winding (N_{AUX}) and the secondary winding (N_S) of the transformer.
- Ensure that the DC resistance of the auxiliary winding is less than 0.1 ohm.

7.4.12 System Fault Protections

The UCC28781-Q1 provides extensive protections on different system fault scenarios. The protection features are summarized in Table 7-3.

Table 7-3. System Fault Protection

PROTECTION	SENSING	THRESHOLD	DELAY TO ACTION	ACTION BY UCC28781-Q1
VDD UVLO	VDD voltage	$V_{VDD(OFF)} \le V_{VDD} \le V_{VDD(ON)}$	None	UVLO reset
Brown-in detection	VS current	$I_{VSL} \le I_{VSL(RUN)}$	4 PWML pulses	UVLO reset
Brown-out detection	VS current	$I_{VSL} \le I_{VSL(STOP)}$	t_{BO} (60ms) plus 3 confirming PWML pulses	UVLO reset
Over-power protection (OPP)	CS voltage	$V_{CST(OPP)} \le V_{CST} \le V_{CST(MAX)}$	t_{OPP} (160 ms)	t_{FDR} restart (1.5s)
Peak-power limit (PPL)	CS voltage	$V_{CST} \le V_{CST(MAX)}$		
Over-current protection (OCP)	CS voltage	$V_{CS} \ge V_{OCP}$	3 PWML pulses	t_{FDR} restart
Output short-circuit protection (SCP)	CS, VS, and VDD voltages	(1) $V_{VDD} = V_{VDD(OFF)}$ & $V_{CST} \ge V_{CST(OPP)}$; (2) $V_{VDD} = V_{VDD(OFF)}$ & $V_{VS} \le V_{VS(SM2)}$	$\le t_{OPP}$	t_{FDR} restart
Output over-voltage protection (OVP)	VS voltage	$V_{VS} \ge V_{OVP}$	3 PWML pulses	t_{FDR} restart
Over-temperature protection on FLT pin (OTP)	FLT voltage	$R_{NTC} \le R_{NTCTH}$	$t_{FLT(NTC)}$ (50 µs)	UVLO reset until $R_{NTC} \ge R_{NTCR}$
Over-temperature protection on CS pin (OTP)	CS voltage	$V_{CS} \ge V_{OCP}$	2 PWMH pulses	t_{FDR} restart
Input over-voltage protection (IOVP)	FLT voltage	$V_{FLT} \ge V_{IOVPTH}$	$t_{FLT(IOVP)}$ (750 µs)	UVLO reset until $V_{FLT} < V_{IOVPTH} - V_{IOVPR}$
Thermal shutdown	Junction temperature	$T_J \ge T_{J(STOP)}$	3 PWML pulses	UVLO reset

7.4.12.1 Brown-In and Brown-Out

The VS pin senses the negative voltage level of the auxiliary winding during the on-time of the primary-side switch (Q_L) to detect an under-voltage condition of the input DC or AC line. When the bulk voltage (V_{BULK}) is too low, UCC28781-Q1 stops switching and no V_O restart attempt is made until the input line voltage is back into normal range. As Q_L turns on with PWML, the negative voltage level of the auxiliary winding voltage (V_{AUX}) is equal to V_{BULK} divided by primary-to-auxiliary turns ratio (N_{PA}) of the transformer, which is N_P / N_A. During this time, the voltage on VS pin is clamped to about 250 mV below AGND. As a result, V_{AUX} can create a line-sensing current (I_{VSL}) out of the VS pin flowing through the upper resistor of the voltage divider on VS pin (R_{VS1}). With I_{VSL} proportional to V_{BULK}, it can be used to compare against two under-voltage thresholds, $I_{VSL(RUN)}$ and $I_{VSL(STOP)}$.

The following discussion, equations, and figures involving brown-in and brown-out thresholds are based on AC-line input conditions, but are generally applicable to DC input voltages as well. For an application using a DC input, substitute $V_{DC(BI)}$ for $V_{AC(BI)}$, $V_{DC(BO)}$ for $V_{AC(BO)}$ and remove the $\sqrt{2}$ factor from each equation and figure in this section.

The target brown-in AC voltage ($V_{AC(BI)}$) can be programmed by the proper selection of R_{VS1}. For every UVLO cycle of VDD, there are at least four initial test pulses from PWML to check I_{VSL}condition. I_{VSL} of the first test pulse is ignored. If $I_{VSL} \le I_{VSL(RUN)}$ is valid for the next three consecutive test pulses, the controller stops

switching, the RUN pin goes low, and a new UVLO start cycle is initiated after V_{VDD} reaches $V_{VDD(OFF)}$. On the other hand, if $I_{VSL} > I_{VSL(RUN)}$ occurs, V_O soft start sequence is initiated.

$$R_{VS1} = \frac{V_{AC(BI)}\sqrt{2}}{N_{PA} \times I_{VSL(RUN)}} = \frac{N_A}{N_P}\frac{V_{AC(BI)}\sqrt{2}}{365\mu A} \tag{14}$$

The brown-out AC voltage ($V_{AC(BO)}$) is set internally by approximately 83% of $V_{AC(BI)}$, which provides enough hysteresis to compensate for possible sensing errors through the auxiliary winding.

$$V_{AC(BO)} = \frac{I_{VSL(STOP)}}{I_{VSL(RUN)}} V_{AC(BI)} = 0.83 \times V_{AC(BI)} \tag{15}$$

A 60-ms timer (t_{BO}) is used to bypass the effect of line ripple content on the I_{VSL} sensing. Only when the $I_{VSL} \le I_{VSL(STOP)}$ condition lasts longer than 60 ms (i.e. typically three line cycles of 50 Hz) and 3 additional switching cycles verify the condition, the brown-out fault is triggered. If switching is interrupted, the brown-out fault will remain pending without shut-down until the 3 verification cycles complete. The fault is reset after V_{VDD} reaches $V_{VDD(OFF)}$. Figure 7-37 shows an example of the timing sequence of brown-out and brown-in protections for the case of an actual input brown-out condition. An application with DC input that has considerable ripple on the bulk voltage will behave similar to the AC-line bulk-ripple case.

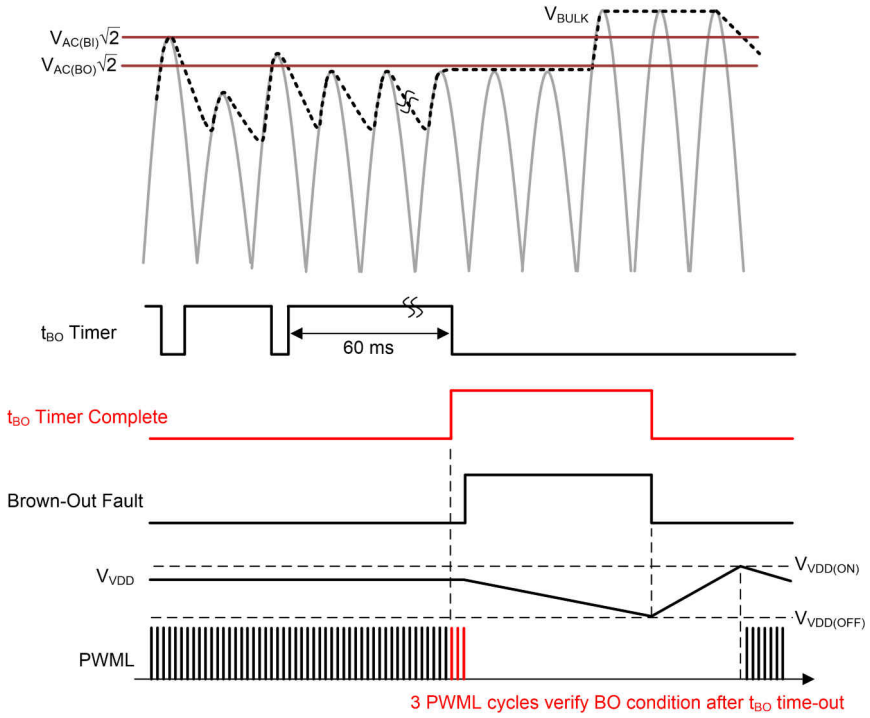


Figure 7-37. Timing Diagram of Brown-Out/Brown-In Response on AC Line Events

The t_{BO} timer is started at the moment $I_{VSL} \le I_{VSL(STOP)}$ is detected during the PWML on-time. The timer is cleared when $I_{VSL} > I_{VSL(STOP)}$ is detected. In the case of an overshoot voltage on the output, switching will stop until the output voltage recovers to the regulation level. If the t_{BO} timer is triggered by $I_{VSL} \le I_{VSL(STOP)}$ while in the valley of the bulk ripple voltage, and then switching is stopped the status of I_{VSL} cannot be detected and updated. The timer cannot be cleared without switching to sample I_{VSL}, and the 60-ms timer may elapse even though no brown-out condition exists. To prevent an unwarranted shut-down, the 3 additional switching cycles sample the condition once switching does resume, to verify or dismiss the pending apparent brown-out fault. An extended output overshoot condition longer than t_{BO} can result from a sudden load drop combined with a drop

in the regulation reference due to reduction of cable compensation. Figure 7-38 shows an example of the timing sequence for the case of an apparent brown-out cancelled by 3 verifying pulses.

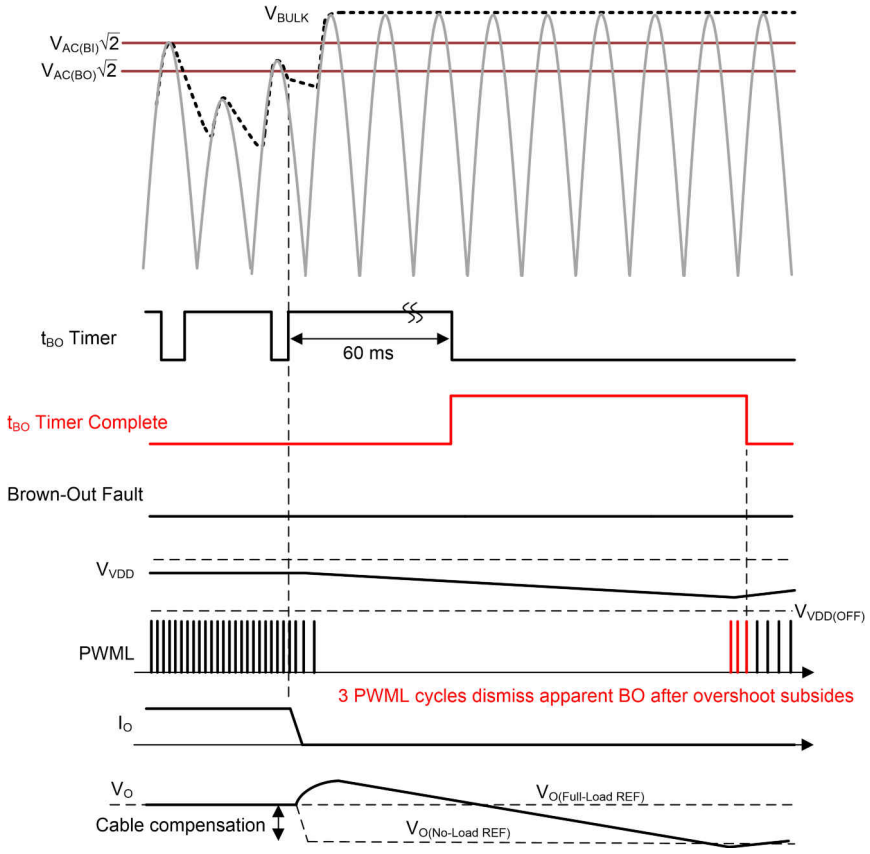


Figure 7-38. Timing Diagram of Brown-Out Response on Extended Output Overshoot

7.4.12.2 Output Over-Voltage Protection (OVP)

The VS pin is used to sense the positive voltage level of the auxiliary winding voltage (V_{AUX}) to detect an over-voltage condition of V_O. When an OVP event is triggered, the auto-recovery version of OVP stops switching and there is a 1.5-s fault recovery time (t_{FDR}) before any V_O restart attempt is made. As Q_L turns off, the settled V_{AUX} is equal to (V_O+V_F) x N_{AS}, where N_{AS} is the auxiliary-to-secondary turns ratio of the transformer, N_A / N_S, and V_F is the forward voltage drop of the secondary-side rectifier. The VS pin senses V_{AUX} through a voltage divider formed by R_{VS1} and R_{VS2}. The pin voltage (V_{VS}) is compared with an internal OVP threshold (V_{OVP}). If $V_{VS} \geq V_{OVP}$ condition is qualified for three consecutive PWML pulses, the controller stops switching, brings RUN pin low, and initiates the 1.5-s time delay. During this long delay time, only the UVLO-cycle of V_{VDD} is active, and there are no test pulses of PWML. After the 1.5-s timeout is completed and V_{VDD} reaches the next $V_{VDD(OFF)}$, a normal start sequence begins. The calculation of R_{VS2} is

$$R_{VS2} = \frac{R_{VS1} \times V_{OVP}}{N_{AS} \times (V_{O(OVP)} + V_F) - V_{OVP}} = \frac{R_{VS1} \times 4.5V}{(N_A / N_S)(V_{O(OVP)} + V_F) - 4.5V} \quad (16)$$

The long t_{FDR} timer (1.5 s) helps to protect the power stage components from the large current stress during every restart and allows some time for V_O to discharge in the case of light-load or no-load, before attempting restart.

7.4.12.3 Input Over Voltage Protection (IOVP)

The UCC28781-Q1 provides an input OVP function on the FLT pin. Figure 7-39 shows the application circuit for the input OVP sensing. A resistor divider senses the bulk capacitor voltage, and the IOVP fault is triggered when

V_{FLT} > 4.5 V for longer than 750 µs. The 750 µs delay helps to desensitize the abrupt bulk voltage spike during the line surge condition, such that the output voltage will not drop accidentally. After the IOVP fault is asserted, the switching will be terminated immediately and V_{VDD} will restart. When V_{VDD} reaches $V_{VDD(ON)}$ of the following VDD cycle, the controller will check V_{FLT} first before switching, to avoid the switching device from being exposed to a high-voltage stress condition. The fault will be cleared when V_{FLT} < 4.43 V.

If longer than 750 µs delay is required, a filter capacitor between the FLT pin and AGND pin can create additional programmable delay. If the filter capacitor is too large, it may trigger the OTP fault on the FLT pin, if the ramp up time for V_{FLT} to rise above V_{NTCTH} is longer than $t_{FLT(NTC)}$ after the RUN pin is pulled high. The resistor divider design does not need to consider the offset voltage effect from the 50 µA current source out of the FLT pin, because the controller will disable the current source once V_{FLT} > 2.5 V.

The goal of the internal 5.5-V clamp device on the FLT pin is to protect the pin from exceeding the voltage limit when one of the IOVP upper sensing resistor fails short. The maximum clamp current is 150 µA, so the resistor divider design needs to consider this limitation.

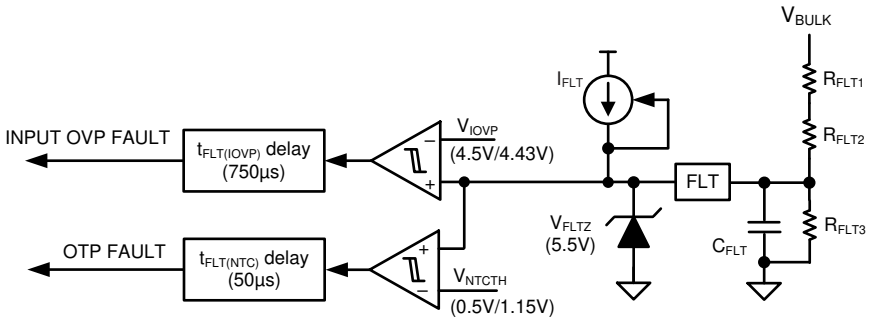


Figure 7-39. Bulk Capacitor Voltage Sensing for Input OVP

7.4.12.4 Over-Temperature Protection (OTP) on FLT Pin

The UCC28781-Q1 uses an external NTC resistor (R_{NTC}) tied to the FLT pin to program a thermal shutdown temperature near the hotspot of the converter. The NTC shutdown threshold (V_{NTCTH}) of 0.5 V with an internal 50-µA current source flowing through R_{NTC} results in a 10-kΩ thermistor shutdown threshold. If the NTC resistance stays lower than 10 kΩ for more than 50 µs, an OTP fault event is triggered. The 50-µs delay ($t_{FLT(NTC)}$) allows a filter capacitor (C_{FLT}) to be placed between the FLT pin and the AGND pin, when the NTC resistor is located far away from the controller but close to the hot spot. To avoid the OTP fault from false trigger as RUN goes high, C_{FLT} should be designed to allow V_{FLT} increased above V_{NTCTH} within $t_{FLT(NTC)}$. On the other hand, if the NTC resistor is close to the controller and there is no potential noise coupling path to the sensing traces, C_{FLT} is not needed.

For auto-recovery mode, the 0.5-V threshold is increased to 1.15 V after the OTP fault, so the NTC resistance has to increase above 23 kΩ to reset the OTP fault. This threshold change provides a safe temperature hysteresis to help the hot-spot temperature cool down before the next V_O restart attempt, reducing the thermal stress to the components. If the FLT pin is not used, the pin can be left floating but can not be connected to REF pin, since the line OVP will be falsely triggered.

The thermal issue in the heavy output load condition is the main design consideration for OTP, and the heavy load operating mode, AAM, allows the controller to stay in the run state continuously, so the 50-µs delay allows V_{FLT} to trigger OTP. Based on the practical BUR-pin setting, 50% to 60% load is operated in AAM. The 50-µA current source is disabled in the burst off time of the light load modes such as ABM, LPM, SBP1, and SBP2, in order to save standby power. However, when the run state becomes shorter than the 50-µs in these modes but the current source is disabled in the wait state, the OTP will not be able to trigger because there is not enough time to detect the fault. Therefore, if certain design considerations still require the OTP to be armed in light load modes, a second OTP configuration can be considered by reusing the 4.5-V threshold of input OVP. As shown

in Figure 7-40, the upper NTC resistor and the lower resistor form a resistor divider from the REF pin to the FLT pin. The 750-µs delay is independent to the wait state condition of controller, so the OTP fault can still be triggered in the light load mode. This configuration provides auto-recovery mode only.

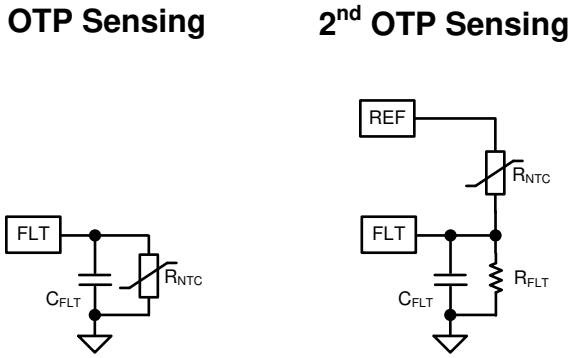


Figure 7-40. Two Connections to Implement OTP on the FLT Pin

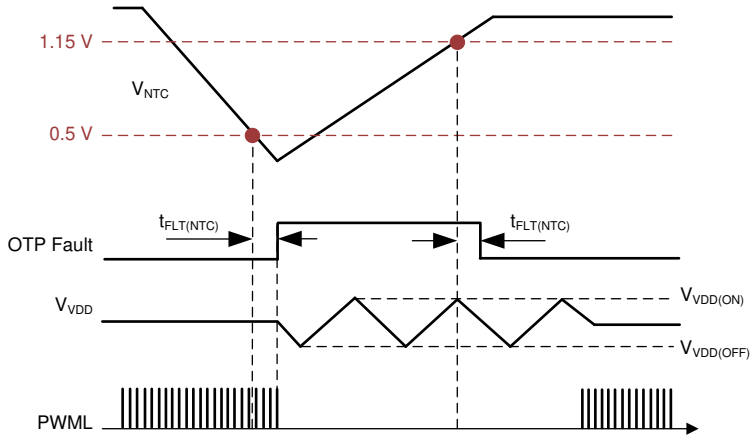


Figure 7-41. OTP Timing Diagram for a NTC between the FLT Pin and AGND Pin

7.4.12.5 Over-Temperature Protection (OTP) on CS Pin

In case the FLT pin is already used for the input OVP sensing, UCC28781-Q1 provides the third and fourth OTP functions on the CS pin. The two configurations do not affect the current sense signal on the CS pin and the OPP level, because the two sensing circuits are only biased after PWML is off. Figure 7-42 shows the two application circuits. For the third OTP configuration, when the PWMH pin is pulled high, R_{NTC} and R_{OPP} form a resistor divider to create a temperature-dependent voltage signal on the CS pin. When the voltage exceeds the 1.2-V threshold sampled before the end of the demagnetization time (T_{DM}) for two successive cycles, the OTP fault will be triggered. The OTP sensing circuit will not affect the operation of the peak current loop, since the PWMH is pulled low in the PWML on time duration. For auto-recovery mode, the long 1.5-s timer starts and the controller stays in fault state without switching. This long recovery time provides a temperature hysteresis to help the hot-spot temperature cool down before the next V_O restart attempt. Compared with the first OTP configuration on the FLT pin, this configuration allows the OTP armed in both AAM and ABM, so the OTP can still be triggered at around 25% output load. Compared with the second OTP configuration from FLT pin, this configuration supports both auto-recovery and latch-off modes.

The fourth configuration with a small-signal PMOS is the most comprehensive way to cover a wide output load range and support both auto-recovery and latch-off modes at the same time. The RUN pin is used to bias the sensing circuit, and the PMOS gate is controlled by the PWML pin to only allow the detection to occur when PWML is low.

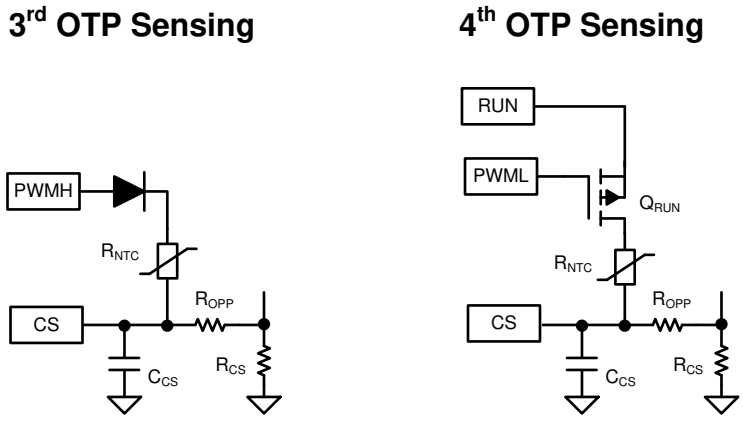


Figure 7-42. Two Connections to Implement OTP on the CS Pin

7.4.12.6 Programmable Over-Power Protection (OPP)

The over-power protection (OPP) allows operation in an over-power condition for a limited amount of time, so the UCC28781-Q1 can support a power stage design with temporary peak power requirements. As shown in Figure 7-43, when V_{CST} is higher than the threshold voltage of the OPP curve ($V_{CST(OPP)}$), a 160-ms timer starts. For the auto-recovery mode, if V_{CST} remains higher than $V_{CST(OPP)}$ continuously for 160 ms, the 1.5-s timer starts and the controller stays in fault state without switching. This long recovery time reduces the average current during a sustained over-power event. The system benefits includes the reduction of thermal stress in high density adapters and the protection of its output cable.

The OPP function uses I_{VSL} as a line feed-forward signal to vary $V_{CST(OPP)}$ depending on V_{BULK}, in order to make the OPP trigger point constant over a wide line voltage range. The UCC28781-Q1 allows programmability of the OPP curve by adding a line-compensation offset voltage on the CS pin through a resistor (R_{OPP}) connected between the CS pin and current-sense resistor (R_{CS}). An internal current source flowing out of CS pin creates the offset voltage on R_{OPP}. This current level is equal to I_{VSL} divided by a constant gain of K_{LC}. As R_{OPP} increases, the OPP trigger point becomes lower at high line, so lower peak magnetizing current is allowed to run continuously.

The OPP function uses V_{VS} as an output voltage feed-forward signal to modify the line-dependent $V_{CST(OPP)}$ curve into the two different sets, such that the OPP trigger point can be more consistent across a wide output voltage range. The higher OPP threshold under V_{VS} > 2.5 V contains two piece-wise linear regions, and the lower OPP threshold under V_{VS} < 2.4 V contains one piece-wise linear region.

The highest threshold of OPP curve ($V_{CST(OPP1)}$) of 0.6 V helps to determine R_{CS} value at $V_{BULK(MIN)}$.

$$R_{CS} = \frac{V_{CST(OPP1)}}{\frac{P_{O(OPP)}}{V_{BULK(MIN)}\eta}\frac{2}{D_{MAX}} - \frac{V_{BULK(MIN)}t_{D(CST)}}{L_M}} \tag{17}$$

where $P_{O(OPP)}$ is the output power that triggers OPP, and $t_{D(CST)}$ is the sum of all delays in the peak current loop which contributes additional peak current overshoot. $t_{D(CST)}$ consists of propagation delay of the low-side driver, current sense filter delay (R_{OPP} x C_{CS}), internal CS comparator delay ($t_{D(CS)}$), and nonlinear capacitance delay of Q_L. After R_{CS} is determined, R_{OPP} can be adjusted to keep a similar OPP point at highest line. Note that setting the OPP trigger point too far away from the full power may introduce more challenge on the thermal design, since the converter runs continuously with more power as long as the corresponding peak current is slightly less than OPP threshold.

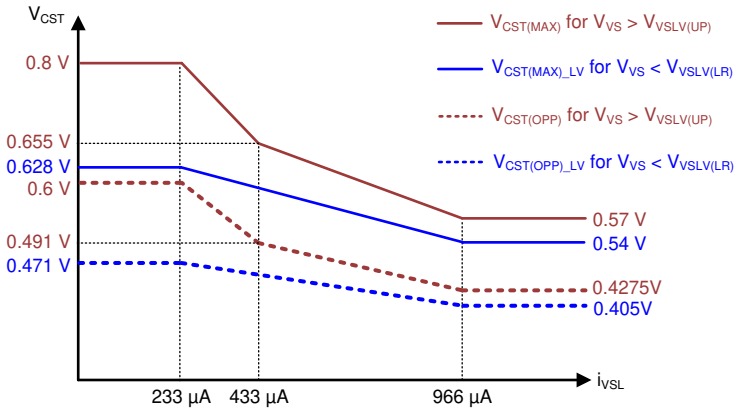


Figure 7-43. V_{CST} OPP curve across I_{VSL}

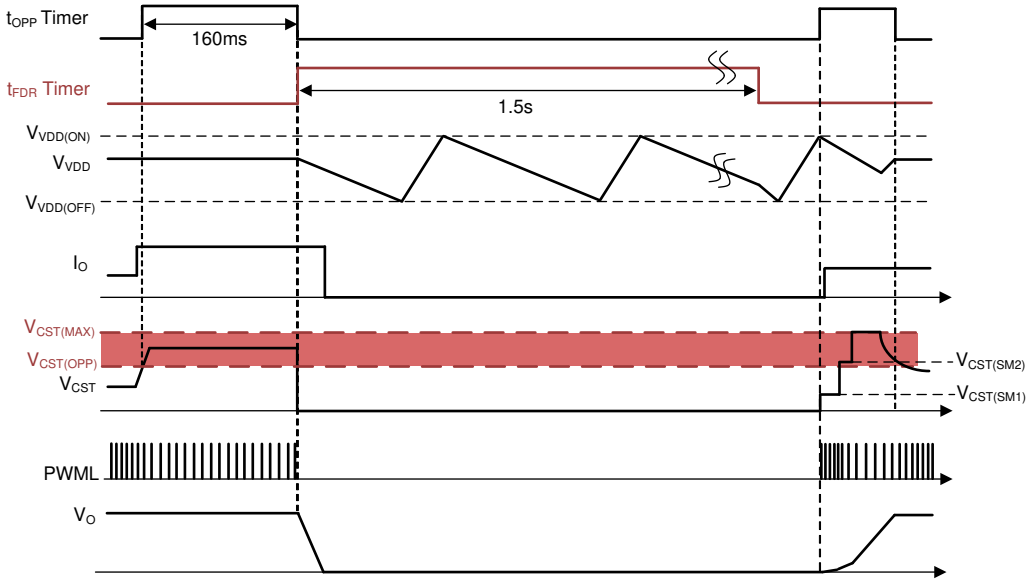


Figure 7-44. Timing Diagram of OPP

7.4.12.7 Peak Power Limit (PPL)

The peak current threshold of the OPP curve is used to initiate the 160-ms timer, while the peak power limit (PPL) determines the highest controllable peak current of the peak current loop, $V_{CST(MAX)}$. Regardless of V_{VS}, the ratio between $V_{CST(MAX)}$ and $V_{CST(OPP)}$ is fixed at approximately 4/3. In other words, this feature provides the highest *short duration* peak power ($P_{O(MAX)}$) that the converter can deliver. The line-dependent PPL curve is able to achieve a consistent peak power level over a wide input voltage range. As an example, to supply a highest peak power of 150% of nominal rated load, choose an R_{CS} value that ensures that the peak current threshold at 150% load and $V_{BULK(MIN)}$ must not be above $V_{CST(MAX)}$. Then, the threshold of the OPP power ($P_{O(OPP)}$) can be programmed to approximately 112% to support 150% peak power design, based on the following equation.

$$P_{O(OPP)} = \frac{V_{CST(OPP1)}}{V_{CST(max)}} \times P_{O(max)} = \frac{0.6\ V}{0.8\ V} \times P_{O(max)} \quad (18)$$

Additionally, before V_O reaches steady-state regulation during V_O soft-start, the highest V_{CST} can also reach $V_{CST(MAX)}$. The transformer maximum flux density must have sufficient design margin to the high-temperature saturation limit of the core material at the peak current while in PPL.

7.4.12.8 Output Short-Circuit Protection (SCP)

When a short-circuit is applied to the converter output, the peak current reaches the PPL limit and triggers the 160-ms OPP fault timer. During this event, the VDD recharge supply is lost due to the auxiliary winding voltage being close to 0 V. Without additional short-circuit detection, if V_{VDD} reaches $V_{VDD(OFF)}$ before the 160-ms timeout, the 1.5-s recovery time for the OPP fault cannot be triggered but only a UVLO recycle is performed. To remedy this scenario, as V_{VDD} reaches $V_{VDD(OFF)}$, the UCC28781-Q1 checks two additional parameters to identify the short-circuit event at the output, and triggers the fault response without waiting for 160 ms to expire. Specifically, when V_{VDD} reaches $V_{VDD(OFF)}$, if either V_{CST} is greater than the OPP threshold ($V_{CST(OPP)}$) or the VS-pin voltage is less than 0.5 V, the 1.5-s recovery delay is initiated for auto-recovery mode. With this additional layer of intelligence, the average load current during continued short-circuit event can be greatly reduced, and thus also the thermal stress on the power supply.

7.4.12.9 Over-Current Protection (OCP)

The UCC28781-Q1 operates with cycle-by-cycle primary-peak current control. The normal operating range of the CS pin threshold is between $V_{CST(MIN)}$ and $V_{CST(MAX)}$. If the voltage on CS exceeds the 1.2-V over-current level at any instant after the internal leading edge blanking time (t_{CSLEB}) and before the end of the transformer demagnetization, for three consecutive PWML cycles, the device stops switching, RUN pin goes low, and the OCP fault response is triggered. Similar to OVP, OPP, and SCP, only the UVLO-cycle of VDD is active and there are no test PWML pulses at all. For auto-recovery, when V_{VDD} reaches the next $V_{DD(OFF)}$ after the 1.5-s time-out is completed a normal start sequence begins.

7.4.12.10 External Shutdown

The REF pin may be used as an external shutdown function by shorting this pin to AGND with a small-signal control switch. This provides an additional design flexibility for the control function extension with external circuitry. When the REF-pin voltage drops lower than its internal power good threshold (approximately 4.5 V), the switching action will be terminated and V_{VDD} will drop to $V_{VDD(OFF)}$, and the controller begins the UVLO restart cycle.

As long as the REF pin is shorted to AGND continuously, the UVLO restart cycle will repeat and switching action is inhibited until the external pull-down on REF is released. During the switch-short condition on REF, the falling slope of V_{VDD} will drop faster than normal case due to the 17-mA over-current limit of the REF regulator which discharges the VDD capacitor faster than the normal I_{VDD} currents in the run and wait states.

7.4.12.11 Internal Thermal Shutdown

The internal over-temperature shutdown threshold is higher than 125°C. If the junction temperature of the device reaches this threshold, the device initiates a UVLO reset and restart fault cycle. If the temperature is still high at the end of the UVLO cycle, the protection cycle repeats. This internal protection is not suitable as a substitute for the NTC for hot-spot temperature protection. An NTC thermistor provides more accurate temperature sensing and may be placed in a remote location for less compromise on PCB layout.

7.4.13 Pin Open/Short Protections

As summarized in Table 7-4, UCC28781-Q1 strengthens the protections of several critical pins under "open" and "short" conditions, such as CS, P13, RDM, and RTZ pins. The pin protections are all in auto-recovery modes. All "short" conditions are defined as short-circuits to AGND.

Table 7-4. Protections for Open and Short of Critical Pins

PROTECTION	SENSING	CONDITION	DELAY TO ACTION	ACTION
CS pin short	PWML on-time at first PWML pulse only	> 2 µs (V_{SET} = 5 V)	none	t_{FDR} restart (1.5 s)
		> 2 µs (V_{SET} = 0 V, $R_{RDM} \geq R_{RDM(TH)}$)		
		> 1 µs (V_{SET} = 0V, $R_{RDM} < R_{RDM(TH)}$)		
CS pin open	CS voltage	$V_{CS} \geq V_{OCP}$	3 PWML pulses	t_{FDR} restart (1.5 s)
P13 pin open	P13 voltage at $UVLO_{ON}$	V_{P13} drops to 14 V within 10 µs	none	UVLO reset
P13 pin over voltage	P13 voltage	$V_{P13} \geq V_{P13(OV)} + V_{P13(REG)}$	3 PWML pulses	UVLO reset
RDM pin short	RDM current at $UVLO_{ON}$	V_{RDM} = 0 V, self-limited I_{RDM}	none	UVLO reset
RDM pin open	RDM current at $UVLO_{ON}$	RDM = Open	none	UVLO reset
RTZ pin short	RTZ current at $UVLO_{ON}$	V_{RTZ} = 0 V, self-limited I_{RTZ}	none	UVLO reset
RTZ pin open	RTZ current at $UVLO_{ON}$	RTZ = Open	none	UVLO reset
XCD pin over voltage	XCD voltage	$V_{XCD} > V_{XCD(OVP)}$	750 µs	UVLO reset

7.4.13.1 Protections on CS pin Fault

UCC28781-Q1 identifies a fail-short event on the CS pin by monitoring the on-time pulse width of the first PWML pulse after V_{VDD} startup is completed. As shown in Figure 7-36, the normal first on-time pulse width should be limited by the clamped $V_{CST(SM1)}$ level of 0.2 V and the rising slope of the current-loop feedback signal from the current-sense resistor (R_{CS}) to the CS pin. When the current feedback path is gone due to a CS pin short to GND, the peak magnetizing current increases and potentially can damage the power stage. Therefore, a maximum on-time of the first PWML pulse for V_{SET} = 5 V, t_{CSF1} of 2 µs in the electrical table, is used to limit the first peak-current stress of the silicon-based converter and then will trigger a CS pin short protection which initiates the t_{FDR} recovery of 1.5 s in auto-recovery mode.

Additionally, t_{CSF0} in the electrical table confines the maximum on-time of the first PWML pulse on the GaN-based converter with V_{SET} = 0 V. There are two corresponding values based on two predetermined ranges of the RDM pin setting in order to provide the protection over a wider switching frequency range. Specifically, t_{CSF0} is set at 2 µs with R_{RDM} higher than the $R_{RDM(TH)}$ threshold of 55 kΩ, while t_{CSF0} is reduced to 1 µs under $R_{RDM} < R_{RDM(TH)}$. Since a GaN-based converter is capable of operating at higher switching frequency with lower magnetizing inductance (L_M), it is possible that the peak current can be increased higher than a lower switching-frequency design under the same $V_{CST(SM1)}$ level and same on-time of PWML. The RDM pin can provide a good indication of the switching frequency range of a GaN power stage, since the lower L_M requires smaller R_{RDM} setting. With a different t_{CSF0} setting, the CS pin fault adapts to a wide switching frequency range.

Unlike a CS pin short protection which senses only the first on-time pulse width of PWML only, CS pin open protection monitors the fail-open condition cycle-by-cycle. An internal 4-µA current source out of the CS pin is used to pull the CS pin voltage up to 3.3 V as the CS pin exhibits high impedance during a fail-open condition. If the CS voltage is higher than the 1.2-V threshold of the OCP limit and lasts for three consecutive PWML pulses, the CS pin open protection is triggered which initiates the 1.5-s recovery.

7.4.13.2 Protections on P13 pin Fault

As shown in Figure 7-36, after V_{VDD} reaches $V_{VDD(ON)}$, an internal 13-V regulator on the P13 pin should force V_{P13} back to the regulation level before PWML starts switching. If the recommended P13-pin capacitor (C_{P13}) of 1 µF and the connection to the depletion-mode MOSFET (Q_S) are in place, the settling time of V_{P13} to 14 V is much longer than 10 µs with a limited 1.9-mA sink current of the regulator ($I_{P13(START)}$) to discharge C_{P13}.

The first fault scenario is that if C_{P13} is too small, or the P13 pin is open, the pin is not able to control Q_S correctly for the high-voltage sensing function of ZVS control, so no switching action will be performed. When either two situations happen, V_{P13} settles to 13 V very quickly instead. Therefore, after a 10-µs delay from the instant of V_{VDD} reaching $V_{VDD(ON)}$, UCC28781-Q1 checks if V_{P13} is below 14 V for the pin-fault detection, and then performs one UVLO cycle of VDD directly without switching as the protection response.

The above protection is to prevent the controller from generating PWM signals. However, when the P13 pin is open and disconnected from the Q_S gate, the source voltage of Q_S keeps increasing. To protect the P13-pin open event, a small Zener diode (D_{P13}) between Q_S gate to AGND should be used to limit the Q_S source voltage. D_{P13} should be higher than $V_{VDD(ON)}$, so as to prevent interference with normal VDD startup. A 20-V Zener diode is recommended.

The second fault scenario is the over-voltage condition of P13 pin after the converter starts switching. When the switch-node voltage (V_{SW}) rises with a high dV/dt condition, there is a charge current flowing through the junction capacitance of Q_S, and part of the current can charge up C_{P13}. If the overshoot is too large, the voltage on the SWS pin also increases due to the nature of depletion-mode MOSFET operation. UCC28781-Q1 detects the overshoot event on P13 pin with a 15-V over-voltage threshold cycle-by-cycle. When V_{P13} is higher than 15 V for three consecutive PWML pulses, the P13 over-voltage protection is triggered which performs one UVLO cycle of VDD.

The third fault scenario is an P13 pin short event at the beginning of VDD startup, and Q_S is unable to charge up the VDD capacitor to $V_{DD(ON)}$, so there is no chance to enable the controller.

7.4.13.3 Protections on RDM and RTZ pin Faults

Since RDM and RTZ pins are the critical programming pins for ZVS control, UCC28781-Q1 offers both open-circuit and short-to-GND protections for those pins. At initial start-up when V_{VDD} reaches $V_{VDD(ON)}$ and before switching begins, a fixed voltage level is applied to each pin and the corresponding current level flowing out of the pin is sensed to detect a pin-fault condition. As a result, too small of a current represents the pin-open state, and too large of a current represents the pin-short state where the short-circuit current level is self-limited.

In general, maintain 2 kΩ < R_{RDM} < 500 kΩ and 20 kΩ < R_{RTZ} < 1.1 MΩ with ample margins to avoid triggering one of these faults. When a pin-fault condition is identified, no switching is allowed and one UVLO cycle of VDD is triggered as the protection response. The normal start-up sequence will proceed on the next VDD cycle after the fault condition is removed.

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

A typical application of a high-frequency zero-voltage switching flyback (ZVSF) converter, using the UCC28781-Q1 controller, is to enable high-density DC-to-DC or AC-to-DC power supply design which complies with stringent global and application-specific efficiency standards and high-density power packaging. Both Silicon (Si) and Gallium Nitride (GaN) power MOSFETs may be used, with appropriate gate drivers for either (if necessary).

8.2 Typical Application Circuit

The following application circuit implements a 60-W, 15-V Si-based ZVSF power stage with the SET pin connected to the REF pin.

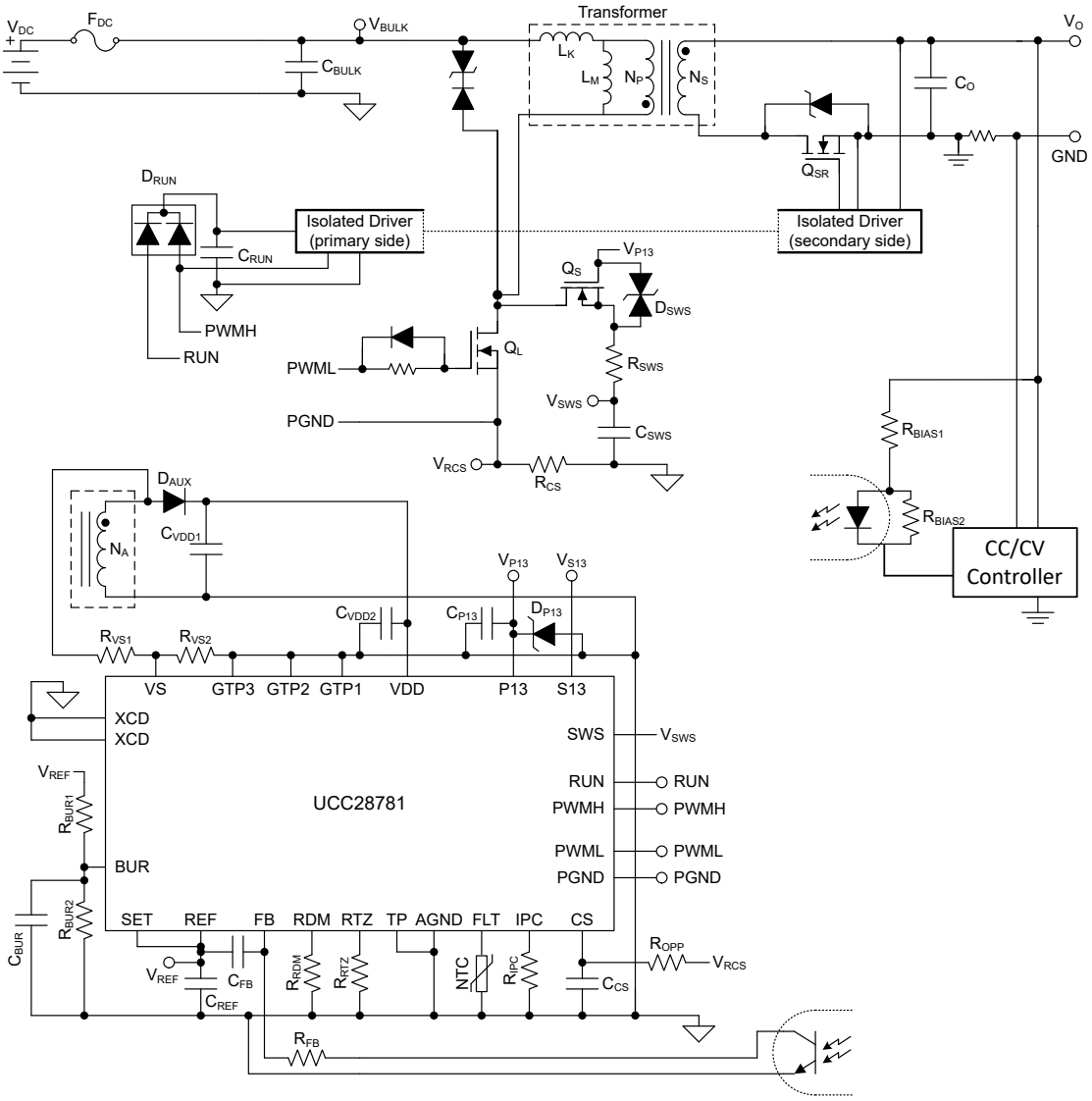


Figure 8-1. Typical Application Circuit

8.2.1 Design Requirements for a 60-W, 15-V ZVSF Bias Supply Application with a DC Input

Table 8-1. Electrical Performance Specifications using Si FET(1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT CHARACTERISTICS						
V_{IN}	Input line voltage (DC)		50	400	500	V
P_{STBY}	Input power at no-load, V_O = 15 V	V_{IN} = 500 V_{DC}, I_O = 0 A		47		mW
		V_{IN} = 250 V_{DC}, I_O = 0 A		36		mW
OUTPUT CHARACTERISTICS						
V_O	Output voltage	V_{IN} = 250 to 500 V_{DC}, I_O = 4.0 A to 0 A	14.7	15	15.3	V
		V_{IN} = 40 to 250 V_{DC}, I_O = 2.0 A to 0 A				
$I_{O(FL\_HI)}$	Full-load rated output current, high input range	V_{IN} = 250 to 500 V_{DC}			4	A
$I_{O(FL\_LO)}$	Full-load rated output current, low input range	V_{IN} = 40 to 250 V_{DC}			2	A
V_{O_pp}	Output ripple voltage, peak to peak, high input range	V_{IN} = 250 to 500 V_{DC}, I_O = 0 A to 4 A		350	500	mVpp
	Output ripple voltage, peak to peak, low input range	V_{IN} = 40 to 250 V_{DC}, I_O = 0 A to 2 A		200	300	
$P_{O(OPP)}$	Over-power protection threshold	V_{IN} = 40 to 500 V_{DC}			70	W
t_{OPP}	Over-power protection duration	V_{IN} = 40 to 500 V_{DC}, P_O > $P_{O(OPP)}$		160		ms
ΔV_O	Output voltage transient deviation at load-step	I_O steps between 0 A and $I_{O(FL\_HI)}$ at 100 Hz			±1000	mVpp
SYSTEM CHARACTERISTICS						
η_{FL}	Full-load efficiency(2)	V_{IN} = 500 V_{DC}, I_O = 4 A		0.932		
		V_{IN} = 250 V_{DC}, I_O = 2 A		0.937		
η_{avg}	4-point average efficiency(3)	V_{IN} = 500 V_{DC}		0.905		
		V_{IN} = 250 V_{DC}		0.919		
$\eta_{10\%}$	Efficiency at 10% load	V_{IN} = 500 V_{DC}, I_O = 10% of $I_{O(FL\_HI)}$		0.808		
		V_{IN} = 250 V_{DC}, I_O = 10% of $I_{O(FL\_LO)}$		0.835		
T_{AMB}	Ambient operating temperature range	V_{IN} = 90 to 264 V_{DC}, V_O = 20 V, I_O = 0 to 3.25 A		25°C		

(1) The performance listed in this table is based on the test results from a single board, using either DC input or AC input for their respective results.
(2) Power losses from external input and output cables are not included in efficiency results.
(3) Average efficiency of four load points: I_O = 100%, 75%, 50%, and 25% of $I_{O(FL)}$.

8.2.2 Detailed Design Procedure

8.2.2.1 Input Bulk Capacitance and Minimum Bulk Voltage

For off-line rectified-AC applications, the total input bulk capacitor (C_{BULK}) should be sized to provide energy from the peak of the minimum input AC-line rms voltage ($V_{IN(MIN)}$) to the minimum allowable voltage ($V_{BULK(MIN)}$) for the power conversion stage. Due to the transition-mode operation, too low of $V_{BULK(MIN)}$ selection results in higher rms current at $V_{IN(MIN)}$ and affects the full-load efficiency, while too high of $V_{BULK(MIN)}$ enlarges the volume of the bulk capacitor. This equation does not account for the hold-up time requirement over AC-line dips and drop-outs.

$$C_{BULK(MIN)} = \frac{\frac{P_O}{\eta} \times [0.5 + \frac{1}{\pi} \times \arcsin(\frac{V_{BULK(MIN)}}{\sqrt{2} \times V_{IN(MIN)}})]}{(2 \times {V_{IN(MIN)}}^2 - {V_{BULK(MIN)}}^2) \times f_{LINE}} \quad (19)$$

For DC-input applications, the value of C_{BULK} depends on the nature of the input:

- If the DC source is subject to brief interruptions (similar to dips and drop-outs of an AC-line), then the value of C_{BULK} is calculated in a similar manner as for $C_{BULK(MIN)}$ above. Δt_{DC_drop} represents the maximum expected interruption time of the DC input.

$$C_{BULK(MIN)} = \frac{\frac{P_O}{\eta} \times \Delta t_{DC\_drop}}{\left(V^2_{DC\_IN(MIN)} - V^2_{BULK(MIN)}\right)} \quad (20)$$

- If the DC source is consistently steady such as from a high-voltage battery, then the value of C_{BULK} should be sufficient to effectively by-pass the high-frequency primary switching current to avoid conducting significant EMI noise back to the source.C_{BULK} may be made up of more than one capacitor. Select standard values with sufficient margin to the calculated $C_{BULK(MIN)}$ to allow for tolerance and aging.

8.2.2.2 Transformer Calculations

8.2.2.2.1 Primary-to-Secondary Turns Ratio (N_{PS})

N_{PS} is a ratio of primary winding turns to secondary winding turns and although each winding must have a whole number of turns, the ratio of the two is not required to be a whole number. The choice of N_{PS} influences the design tradeoffs on the voltage ratings between primary and secondary switches, and the balance between the magnetic core and winding loss of the transformer, which are explained in more detail as follows:

1. Maximum N_{PS} ($N_{PS(MAX)}$) is limited by the maximum derated drain-to-source voltage of Q_L ($V_{DS\_QL(MAX)}$). In the expression below, ΔV_{CLAMP} is the total voltage deviation above V_{BULK} when the primary TVS or RCD clamp absorbs the leakage inductance energy of the trasnformer when Q_L turns off. V_O is the output voltage, and V_F is the forward voltage drop of the secondary rectifier.

$$N_{PS(MAX)} = \frac{V_{DS\_QL(MAX)} - V_{BULK(MAX)} - \Delta V_{CLAMP}}{V_O + V_F} \quad (21)$$

2. Minimum N_{PS} ($N_{PS(MIN)}$) is limited by the maximum derated drain-to-source voltage of the secondary rectifier ($V_{DS\_SR(MAX)}$). In the expression for $N_{PS(MIN)}$, ΔV_{SPIKE} should account for any additional voltage spike higher than $V_{BULK(MAX)}/N_{PS}$ that occurs when Q_{SR} is active and turns-off at non-zero current in AAM and ABM modes.

$$N_{PS(MIN)} = \frac{V_{BULK(MAX)}}{V_{DS\_SR(MAX)} - V_O - \Delta V_{SPIKE}} \quad (22)$$

3. The winding loss distribution between the primary and secondary side of the transformer is the final consideration. As N_{PS} increases, primary RMS current reduces, while secondary RMS current increases. Conversely, as N_{PS} decreases, primary RMS current increases, while secondary RMS current reduces.

8.2.2.2.2 Primary Magnetizing Inductance (L_M)

After N_{PS} is chosen, L_M can be estimated based on minimum switching frequency ($f_{SW(MIN)}$) at $V_{BULK(MIN)}$, maximum duty cycle (D_{MAX}), and output power at highest nominal output voltage, nominal full-load current ($P_{O(FL)}$). The choice of $f_{SW(MIN)}$ should consider the expected range of switching frequency as bulk voltage increases from minimum to maximum and as load falls from maximum to the burst mode threshold. K_{RES} represents the duty cycle loss to wait for the switch-node voltage transition from the reflected output voltage to zero. Typically, f_{SW} may extend to 200% to 300% $f_{SW(MIN)}$ or higher. A K_{RES} value of 5% to 6% is used as an initial estimate for GaN-based power stages, while ~10% is more appropriate for Si-based designs. The selection of minimum switching frequency ($f_{SW(MIN)}$) should consider the impact on full-load efficiency and EMI filter design.

$$D_{MAX} = \frac{N_{PS}(V_O + V_F)}{V_{BULK(MIN)} + N_{PS}(V_O + V_F)} \tag{23}$$

$$L_M = \frac{D_{MAX}{}^2 V_{BULK(MIN)}{}^2 \eta}{2P_{O(FL)}} \times \frac{(1 - K_{RES})}{f_{SW(MIN)}} \tag{24}$$

8.2.2.2.3 Primary Winding Turns (N_P)

The number of turns on the primary winding (N_P) of the transformer is determined by two design considerations:

1. The maximum flux density (B_{MAX}) must be kept below the saturation limit (B_{SAT}) of the chosen magnetic core under the highest peak magnetizing current ($I_{M+(MAX)}$) condition, the cross-sectional area (A_E) of the core, and highest core temperature. When I_{FB} = 0 A, such as during V_O soft-start or step-up load transient, the peak magnetizing current reaches $I_{M+(MAX)}$, since $V_{CST} = V_{CST(MAX)}$ in those conditions. $I_{M+(MAX)}$ can be estimated based on the output power triggering an OPP fault ($P_{O(OPP)}$) with $V_{CST} = V_{CST(OPP1)}$ at $V_{BULK(MIN)}$.

$$I_{M+(MAX)} = \frac{2P_{O(OPP)}}{D_{MAX} V_{BULK(MIN)} \eta} \frac{V_{CST(MAX)}}{V_{CST(OPP1)}} \tag{25}$$

$$B_{MAX} = \frac{L_M I_{M+(MAX)}}{N_P A_E} < B_{SAT} \tag{26}$$

2. The AC flux density (ΔB) affects the core loss of the transformer. For a transition-mode ZVS flyback, the core loss is usually highest at high line, since the switching frequency is highest, duty cycle is smallest, and peak-to-peak magnetizing current swing is greatest for a given load condition. The following equation is the ΔB calculation including the contribution of negative magnetizing current (I_{M-}), used to put into the Steinmetz equation for more accurate core loss estimation. For $V_{BULK} \geq N_{PS}(V_O+V_F)$, I_{M-} is calculated with V_{BULK} divided by the characteristic impedance of L_M and the lumped time-related switch-node capacitance (C_{SW}). I_{M-} is always a negative value. The expression of f_{SW} is derived based on the triangular approximation of the magnetizing current, which also considers the effect of I_{M-} over wide DC or AC input line conditions.

$$I_{M-} = -\sqrt{\frac{C_{SW}}{L_M}} V_{BULK} \tag{27}$$

$$I_{IN} = \frac{P_{O(FL)}}{\eta} \frac{1}{V_{BULK}} \tag{28}$$

$$D = \frac{N_{PS}(V_O + V_F)}{V_{BULK} + N_{PS}(V_O + V_F)} \tag{29}$$

$$f_{SW} = \frac{D^2 V_{BULK}}{2L_M I_{IN} - DL_M I_{M-} + DV_{BULK} \times 0.5\pi\sqrt{L_M C_{SW}}} \quad (30)$$

$$I_{M+} = \sqrt{\frac{2P_{O(FL)}}{\eta L_M f_{SW}} + I_{M-}{}^2} \quad (31)$$

$$\Delta B = \frac{L_M (I_{M+} - I_{M-})}{N_P A_E} \quad (32)$$

For the ΔB calculation, remember that I_{M-} is a negative value and that ΔB is a peak-to-peak flux swing. Core loss is based on ½ of ΔB.

8.2.2.2.4 Secondary Winding Turns (N_S)

After N_P is chosen, N_S can be calculated using the target N_{PS}. N_S and N_P are adjusted to the nearest suitable integers.

$$N_S = \frac{N_P}{N_{PS}} \quad (33)$$

Once N_P and N_S are finalized, the actual N_{PS} is recalculated. With the new N_{PS} value, Section 8.2.2.2.2 and follow-on parameters are also recalculated to reflect the updated N_{PS} parameter change.

8.2.2.2.5 Auxiliary Winding Turns (N_A)

Turns of the auxiliary winding (N_A) is an integer value usually chosen to provide a nominal V_{VDD} that satisfies all devices powered from V_{VDD}, such as a gate driver, or the UCC28781-Q1. N_A is determined by the following design considerations:

1. V_{VDD} must be lower than the maximum rating voltage of VDD pin ($V_{VDD(MAX)}$) at maximum output voltage and rectifier forward drop ($V_{O(MAX)}$ + V_F). $V_{VDD(MAX)}$ is also limited by the lowest maximum voltage rating of any other devices connected to the VDD pin. For designs with a fixed output voltage or a narrow output range, the maximum Auxiliary winding turns ($N_{A(max)}$) is given by the following equation.

$$N_{A(MAX)} = \frac{V_{VDD(MAX)}}{V_{O(MAX)} + V_F} N_S \quad (34)$$

2. The nominal V_{VDD} calculation must consider the impact on the stand-by power. Higher V_{VDD} results in a static loss increase with the total bias current of all devices connected to the VDD pin.
3. V_{VDD} should be higher than the 13-V threshold voltage of survival mode (which is the sum of $V_{VDD(off)}$ and $V_{VDD(PCT)}$) at the minimum sustained output voltage ($V_{O(min)}$). ΔV here represents the voltage difference between the nominal V_{VDD} and the survival-mode threshold. A minimum of 3 V is a recommended design margin for ΔV.

$$N_{A(MIN)} = \frac{V_{VDD(OFF)} + V_{VDD(PCT)} + \Delta V}{V_{O(MIN)} + V_F} N_S \quad (35)$$

$N_{A(min)}$ must also accommodate the highest $V_{VDD(off)}$ threshold of other devices powered by VDD, if any. Select an integer value for N_A between the lowest $N_{A(MAX)}$ and the highest $N_{A(MIN)}$ with consideration of #2. For best performance, design the DC resistance of the auxiliary winding to be < 0.1 Ω.

8.2.2.2.6 Winding and Magnetic Core Materials

Besides the choice of AC flux density (ΔB) with L_M and N_P, the core loss of the transformer can also be significantly reduced by proper selection of the magnetic core material. For converters operating at full-load

switching frequencies up to 250 kHz, ferrite materials such as Ferroxcube 3C97 or 3C98, for example, exhibit low core-loss density. For converters operating at full-load switching frequencies over 400 kHz, materials such as 3F36 from Ferroxcube and N49 from TDK/Epcos exhibit low core-loss density. Other ferrite materials with equivalent or similar loss characteristics may also be used.

Litz wire is recommended for both primary and secondary windings, in order to reduce the R_{AC} losses caused by high-frequency proximity effect and skin effect of the windings. Choose a suitable insulation class for the windings based on the expected and measured maximum operating temperature under sustained over-stress conditions.

8.2.2.3 Calculation of ZVS Sensing Network

There are three components in the application circuit to help the depletion MOSFET (Q_S) perform ZVS sensing safely: C_{SWS}, R_{SWS}, and D_{SWS}. Design considerations and selection guidelines for the values of these components are given here.

At the rising edge of the switch-node voltage, the fast dV/dt may couple through the drain-to-source capacitance of Q_S ($C_{OSS(Qs)}$) and generate a charge current that flows into the circuit loading on the Q_S source pin. The result may be a possible voltage overshoot on both the SWS pin and across the gate-to-source of Q_S ($V_{GS(Qs)}$) because the gate is tied to P13. The SWS pin, having an absolute maximum voltage rating of 38 V, can handle higher voltage stress than $V_{GS(Qs)}$. Therefore, carefully select a capacitor (C_{SWS}) between the SWS pin and GND to prevent the voltage overshoot from damaging the Q_S gate. Because $C_{OSS(Qs)}$ and C_{SWS} form a voltage divider, the minimum C_{SWS} ($C_{SWS(min)}$) can be derived as

$$C_{SWS(min)} = \frac{C_{OSS(Qs)} \times \left[V_{BULK(MAX)} + N_{PS}(V_O + V_F)\right]}{V_{P13} + V_{GS_{MAX(Qs)}}} \quad (36)$$

where

- $V_{GS\_MAX(Qs)}$ is the de-rated maximum gate-to-source voltage of Q_S
- V_{P13} is the steady-state voltage level of 13 V

Without resistive damping, both the charge current on the rising edge of V_{SW} and the discharge current on the falling edge of V_{SW} may oscillate with the parasitic series inductance within the ZVS sensing network resonating with C_{SWS}. Therefore, a series resistor (R_{SWS}) between SWS pin and source-pin of Q_S is used to dampen any high-frequency ringing, helping to obtain a cleaner sensing signal on the SWS pin and preventing any high-frequency current from interfering with other noise-sensitive signals. R_{SWS} can be expressed as:

$$R_{SWS} > \sqrt{\frac{L_{SWS}}{C_{SWS} + C_{Dz}}} \quad (37)$$

where

- L_{SWS} is the lumped parasitic inductance including the packaging of Q_S and PCB traces of Q_S and C_{SWS} return path
- C_{Dz} is the junction capacitance of any zener diode applied across C_{SWS}, if used (usually not necessary).

For most applications, use a resistor value slightly higher than 500 Ω. The resistor and a 22-pF ceramic capacitor between the SWS pin and the bulk input capacitor ground form a small sensing delay to help the internal detection circuit to identify the ZVS characteristic correctly.

Based on the above design guide, even though R_{SWS} and C_{SWS} may be sufficient to manage the voltage overshoot in normal operation, a low-capacitance bi-directional TVS diode (D_{SWS}) across BSS126 gate and source is highly recommended to serve as a safety backup of the ZVS sensing network. Regular Zener diodes are not suitable due to high capacitance and slow clamping response. Ensure the clamping voltage of D_{SWS} is less than BSS126 voltage rating but greater than 15 V.

A general recommendation is to use a 50-V 22-pF C0G-type ceramic capacitor for C_{SWS}, a 510-Ω chip resistor for R_{SWS}, and a bi-directional TVS diode with clamp voltage of 18 V for D_{SWS}. Too large of R_{SWS} or C_{SWS} introduces a sensing delay between the actual V_{SW} and the SWS pin, causing the ZVS control to unnecessarily

extend t_{DM} in order to pull down V_{SW} earlier than expected before the end of t_Z . As shown in Figure 7-5, the larger R_{SWS} is, the smaller supply current to charge the VDD capacitor. If the reduced charge current (I_{SWS}) is lower than the total consumed current from the controller (I_{START}) and from the external circuitry on the VDD and P13 pins, V_{VDD} may not be able to reach $V_{VDD(ON)}$ and the controller can not initiate any switching event.

8.2.2.4 Calculation of BUR Pin Resistances

Referring back to Section 7.3.1, it is recommended that ABM is entered at no higher than 50% to 60% of full load. Equation 1 and Equation 2, or Equation 1 and Equation 4, provide two equations for calculating two unknowns for the BUR-pin resistor values. However, choose the target values of $V_{CST(BUR)}$, $\Delta V_{BUR(AAM)}$, and $\Delta V_{BUR(LPM)}$ first. Because the ratio of $I_{BUR(AAM)}$ to $I_{BUR(LPM)}$ is fixed at 1.852 (5 µA / 2.7 µA), it is necessary to target $\Delta V_{BUR(AAM)}$ = 185 mV to ensure that $\Delta V_{BUR(LPM)}$ = 100 mV, per guidance in Section 7.3.1.

The procedure to determine the value of $V_{CST(BUR)}$ is quite complex and is not provided in this datasheet. Instead, a soon-to-be-released *UCC28781 Excel Calculator Tool* automatically calculates this value based on user input and determines the V_{BUR} target voltage V_{BUR_tgt}. Using this target value, it further determines the appropriate values for R_{BUR2} and R_{BUR1} to meet the BUR pin targets based on user selections for the following set of equations.

Expected values are used to determine recommended resistances, then actual resistances are selected from standard value series and the resulting actual voltages are calculated from the selected resistor values. Actual voltage results should be close to the targeted values.

Calculate expected $\Delta V_{BUR(LPM)}$ value based on $\Delta V_{BUR(AAM)}$ target value.

$$\Delta V_{BUR(LPM)} = I_{BUR(LPM)} \times \left(\frac{R_{BUR1} \times R_{BUR2}}{R_{BUR1} + R_{BUR2}} \right) \tag{38}$$

Calculate the expected value for the parallel combination of R_{BUR1} with R_{BUR2}.

$$R_{BUR1} \left|\right| R_{BUR2} = \frac{\Delta V_{BUR(AAM)}}{I_{BUR(AAM)}} \tag{39}$$

Calculate the recommended value for R_{BUR1} and choose a standard 1% tolerance value for R_{BUR1_act} that is close to the recommended value.

$$R_{BUR1\_rec} = \frac{\Delta V_{BUR(AAM)}}{I_{BUR(AAM)}} \times \left(\frac{V_{REF}}{V_{BUR\_tgt} + \Delta V_{BUR(AAM)}} \right) \tag{40}$$

Calculate the recommended value for R_{BUR2} using R_{BUR1_act} and choose a standard 1% tolerance value for R_{BUR2_act} that is close to the recommended value.

$$R_{BUR2\_rec} = R_{BUR1} \times \left[\frac{\left(V_{BUR\_tgt} + \Delta V_{BUR(AAM)} \right)}{V_{REF} - \left(V_{BUR\_tgt} + \Delta V_{BUR(AAM)} \right)} \right] \tag{41}$$

Calculate the actual values for V_{BUR}, $\Delta V_{BUR(AAM)}$, and $\Delta V_{BUR(LPM)}$ using R_{BUR1_act} and R_{BUR2_act}.

$$V_{BUR\_act} = V_{REF} \times \left(\frac{R_{BUR2}}{R_{BUR1} + R_{BUR2}} \right) - I_{BUR(AAM)} \times \left(\frac{R_{BUR1} \times R_{BUR2}}{R_{BUR1} + R_{BUR2}} \right) \tag{42}$$

$$\Delta V_{BUR(AAM)} = I_{BUR(AAM)} \times \left(\frac{R_{BUR1} \times R_{BUR2}}{R_{BUR1} + R_{BUR2}} \right) \tag{43}$$

$$\Delta V_{BUR(LPM)} = I_{BUR(LPM)} \times \left(\frac{R_{BUR1} \times R_{BUR2}}{R_{BUR1} + R_{BUR2}} \right) \tag{44}$$

Finally, verify that the total summation of the BUR voltage with hysteresis does not exceed the BUR-pin upper clamp voltage of 2.4 V.

$$V_{BUR\_act} + \Delta V_{BUR(AAM)} + \Delta V_{BUR(LPM)} \leq 2.4\ V \quad (45)$$

8.2.2.5 Calculation of Compensation Network

The UCC28781-Q1 integrates two control concepts to benefit high-efficiency operation: peak current-mode control and burst-ripple control. The peak current loop in AAM can be analyzed based on linear control theory, so the compensation target is to obtain enough phase margin and gain margin for the given small-signal characteristic of a zero-voltage switching flyback converter. For transition-mode operation, the power stage can be modeled as a voltage-controlled current source charging an output capacitor (C_O) with an equivalent-series resistance (R_{Co}) and the output load (R_O) as shown in Figure 8-2. The first-order plant characteristic and high switching frequency operation in AAM make the peak current loop easier to stabilize than when in ABM.

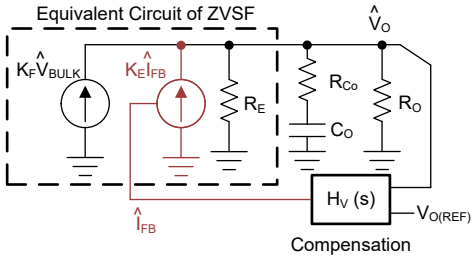


Figure 8-2. Small-Signal Model of ZVSF in AAM Loop

The adaptive burst mode (ABM) uses ripple-based control, so the linear control theory for AAM cannot be applied. As illustrated in Figure 7-4, the internal ramp compensation feature of the controller stabilizes the ABM control loop, so the external compensation network can be simplified.

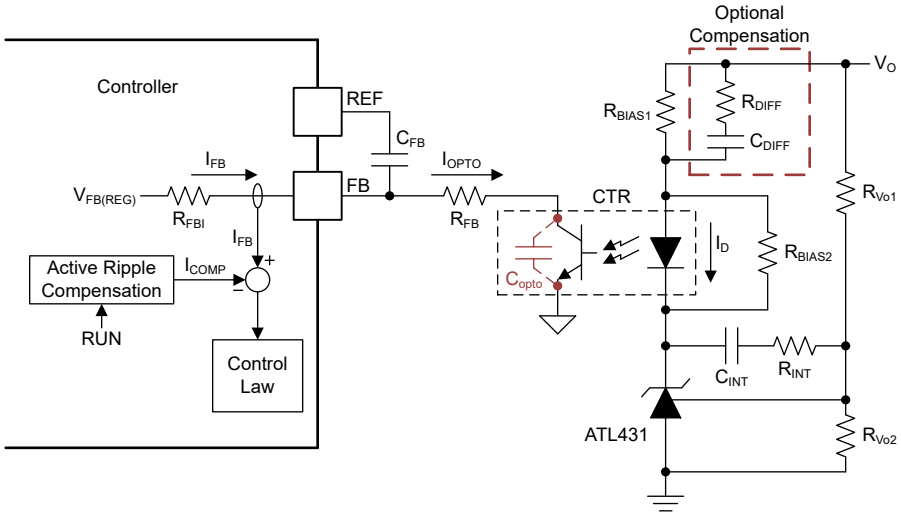


Figure 8-3. Compensation Network, $H_V(s)$

The transfer function from I_{FB} to V_O guides the pole/zero placement of the general secondary-side compensation network in Figure 8-3. In the primary-side control circuitry, two poles at ω_{FB} and ω_{OPTO} introduce phase-delay on I_{FB}. ω_{FB} pole is formed by the external filter capacitor C_{FB} and the parallel resistance of the internal R_{FBI} and the external current-limiting resistor (R_{FB}). ω_{OPTO} pole is formed by the parasitic capacitance of the optocoupler output (C_{OPTO}) and the series resistance of R_{FBI} and R_{FB}. For C_{FB} = 220 pF, R_{FBI} = 8 KΩ, and R_{FB} = 20 KΩ, the delay effect of ω_{FB} pole located at 139 kHz is negligible. C_{OPTO} is in the range of a few nanoFarads contributed by the Miller effect of the collector-to-base capacitance of the BJT in the optocoupler output, so ω_{OPTO} pole is located at less than 10 kHz.

If the control loop bandwidth needs to be designed at higher frequency for a faster transient response, the phase delay effect of ω_{OPTO} on the stability margin must be taken into account. Therefore, an RC network (R_{DIFF} and C_{DIFF}) in parallel with R_{BIAS1} is used to compensate the phase-delay of the optocoupler, which introduces an

extra pole/zero pair located at ω_{P1} and ω_{Z1} respectively. The basic design guide is to place the ω_{Z1} zero close to the ω_{OPTO} pole, and to place ω_{P1} pole away from highest f_{BUR}. On the other hand, if the stability margin and transient response are sufficient to meet the requirements without R_{DIFF} and C_{DIFF}, then these two components are optional for the controller.

$$\frac{I_{FB}(s)}{V_O(s)} = \frac{CTR}{R_{BIAS1}} \frac{1+(s/\omega_{Z0})}{(s/\omega_{Z0})} \frac{1}{1+(s/\omega_{P1})} \frac{1+(s/\omega_{Z1})}{1+(s/\omega_{OPTO})} \frac{1}{1+(s/\omega_{FB})} \tag{46}$$

$$\omega_{Z0} = \frac{1}{(R_{Vo1}+R_{INT})C_{INT}} \tag{47}$$

$$\omega_{Z1} = \frac{1}{(R_{DIFF}+R_{BIAS1})C_{DIFF}} \tag{48}$$

$$\omega_{P1} = \frac{1}{R_{DIFF}C_{DIFF}} \tag{49}$$

$$\omega_{OPTO} = \frac{1}{(R_{FB}+R_{FBI})C_{OPTO}} \tag{50}$$

$$\omega_{FB} = \frac{1}{(R_{FBI}//R_{FB})C_{FB}} \tag{51}$$

The step-by-step design procedure of the compensator without R_{DIFF} and C_{DIFF} is:

1. R_{FB} selection needs to consider both the output voltage regulation and compensation challenge on the low-frequency pole at ω_{OPTO}. R_{FB} should be less than the maximum value of 28 kΩ to provide a sufficient feedback current of 95 μA for the output voltage regulation in SBP2 mode, under the worst-case $V_{FB(REG)}$ and R_{FBI}. However, R_{FB} = 28 kΩ and C_{OPTO} = 2 nF result in an ω_{OPTO} pole located at 2.8 kHz. This low-frequency pole may reduce phase margin at the cross-over frequency. If the control bandwidth is around this frequency range, R_{FB} value should be designed even lower to move the pole to a higher frequency.

$$R_{FB(MAX)} = \frac{V_{FB(REG)} - V_{CE(OPTO)}}{I_{FB(SBP)}} - R_{FBI} \tag{52}$$

2. R_{BIAS1} is determined based on a given current transfer ratio (CTR) of the optocoupler, $\Delta V_{O(ABM)}$, and target 4~5 μA of ΔI_{FB} as example. At collector currents less than 100 μA, the CTR of most optocouplers can be as low as 10%, or 0.1 (used in this example), although some high performance devices can have higher CTR.

$$R_{BIAS1} = \frac{CTR}{\Delta I_{FB}} \times \Delta V_{O(ABM)} = \frac{0.1}{5\ \mu A} \times \Delta V_{O(ABM)} \tag{53}$$

3. R_{INT} selection is not designed for the small-signal compensation, but to resolve the slow large-signal response of the shunt regulator. Specifically, after a step-down load change from heavy load to no load occurs, the output voltage overshoot and the long settling time forces ATL431 to reduce the cathode voltage continuously by the integrator configuration until the output voltage gets back to normal regulation level. If the load step-up transient happens before the output voltage is settled from the previous load step-down event, the low voltage across ATL431 becomes the initial voltage level for the integrator to move to a new steady-state. Because the time for ATL431 to move from lower voltage to a high voltage delays i_{FB} reduction, the controller response from SBP mode to AAM mode is delayed as well, which slows down the energy delivery to the output and results in a large voltage undershoot.
   To resolve this problem, R_{INT} behaves like a current-limiting resistor for C_{INT}, which slows down the reduction of the cathode voltage of ATL431. R_{INT} needs to be adjusted based on the voltage undershoot requirement under the highest repetitive rate of load change.

8.2.3 Application Curves

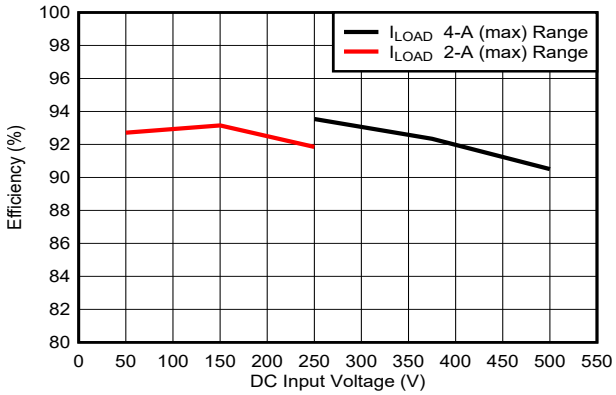


Figure 8-4. 4pt-Average Efficiency vs. DC Input Voltage

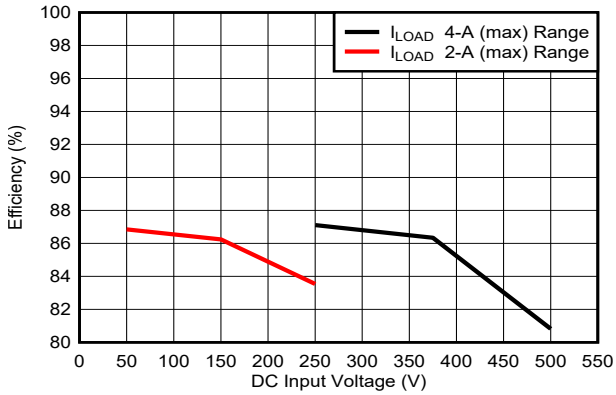


Figure 8-5. 10%-Load Efficiency vs. DC Input Voltage

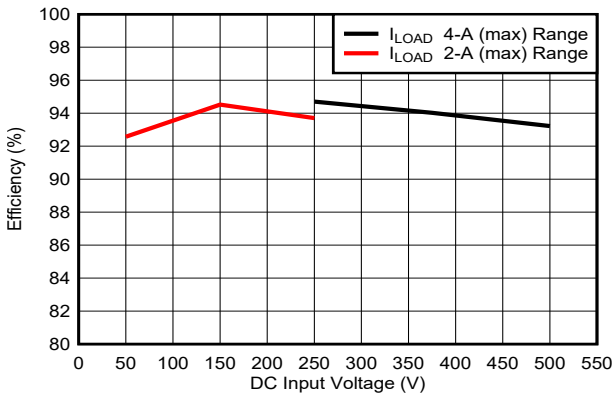


Figure 8-6. Full-Load Efficiency vs. DC Input Voltage

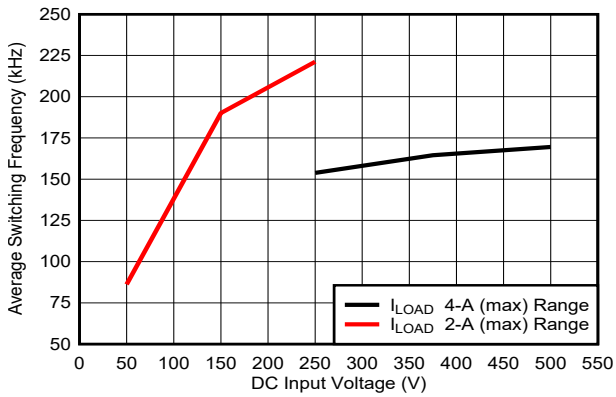


Figure 8-7. Average Switching Frequency at Full-Load vs. DC Input Voltage

9 Power Supply Recommendations

The UCC28781-Q1 controller is intended to control zero-voltage-switching flyback (ZVSF) converters in high-efficiency, high DC input voltage applications, and can work in *universal* AC input range (85 V_{AC} to 265 V_{AC}, 47 Hz to 63 Hz) applications as well. An external depletion-mode MOSFET, connected between the switch node of the converter and the SWS + P13 pins of this controller, is required to charge the VDD capacitor during start-up and to perform ZVS sensing during normal operation.

When the V_{VDD} reaches the UVLO turn-on threshold at 17 V, the VDD rail should be kept within the bias supply operating voltage range listed in the *Recommended Operating Conditions* table. To avoid the possibility that the device might stop switching, V_{VDD} must not be allowed to fall below the UVLO turn-off threshold at 10.6 V.

The rectifier on the output winding must be a synchronous-rectifier (SR) MOSFET in order to generate the negative magnetizing current necessary to achieve ZVS for high efficiency. The current rating of this SR MOSFET should be appropriate for the peak current flowing during the demagnetization interval at maximum loading. In addition to the output voltage plus reflected bulk voltage impressed across the SR during PWML on-time, consideration for additional voltage spikes from various transient conditions should be made. Sources of voltage spikes on the SR include: hard switching of the primary-side MOSFET and non-ZCS turn-off of the SR-MOSFET.

Regardless of the cause of each of these spike sources, it is important to ensure that the peak voltage across the SR does not exceed its maximum rating. This limitation can be accomplished in several ways:

- choose a MOSFET with a higher voltage rating
- add a snubber or voltage clamp across the SR, or
- investigate each cause and mitigate the associated spike separately

The simplest approach may be to include a TVS clamp across the rectifier.

10 Layout

10.1 Layout Guidelines

The ZVSF converter designed with the UCC28781-Q1 virtually eliminates switching loss with minimum circulating energy, so higher switching frequencies, efficiencies, and greater power densities can be achieved. However, when designing for higher switching frequencies, good layout practices as discussed below should be followed to ensure a reliable and robust design.

10.1.1 General Considerations

Designing for high power density requires consideration of noise coupling and thermal management. A four-layer PCB structure is highly recommended to use inner layers to help reduce current-loop areas and provide heat-spreading for surface-mount semiconductors.

- Provide internal-layer copper areas to improve heat dissipation of high-power SMDs, particularly for switching MOSFETs and power diodes. Use multiple thermal-vias to conduct heat from outer pads to inner-layers and supporting copper areas.
- To avoid capacitive noise coupling, do not cross outer-layer signals over copper areas that carry high-frequency switching voltage.
- To avoid inductive noise coupling, keep switching current loops as small as possible, and do not run signal tracks in parallel with such loops.
- Arrange the conducted-EMI filter components such that they do not allow switching noise to bypass them and affect the input. Avoid running switching signals through the EMI filter area.
- Use multiple vias to connect high-current tracks and planes between layers.

Figure 10-1 summarizes the critical layout guidelines, and more detail is further elaborated in the descriptions below.

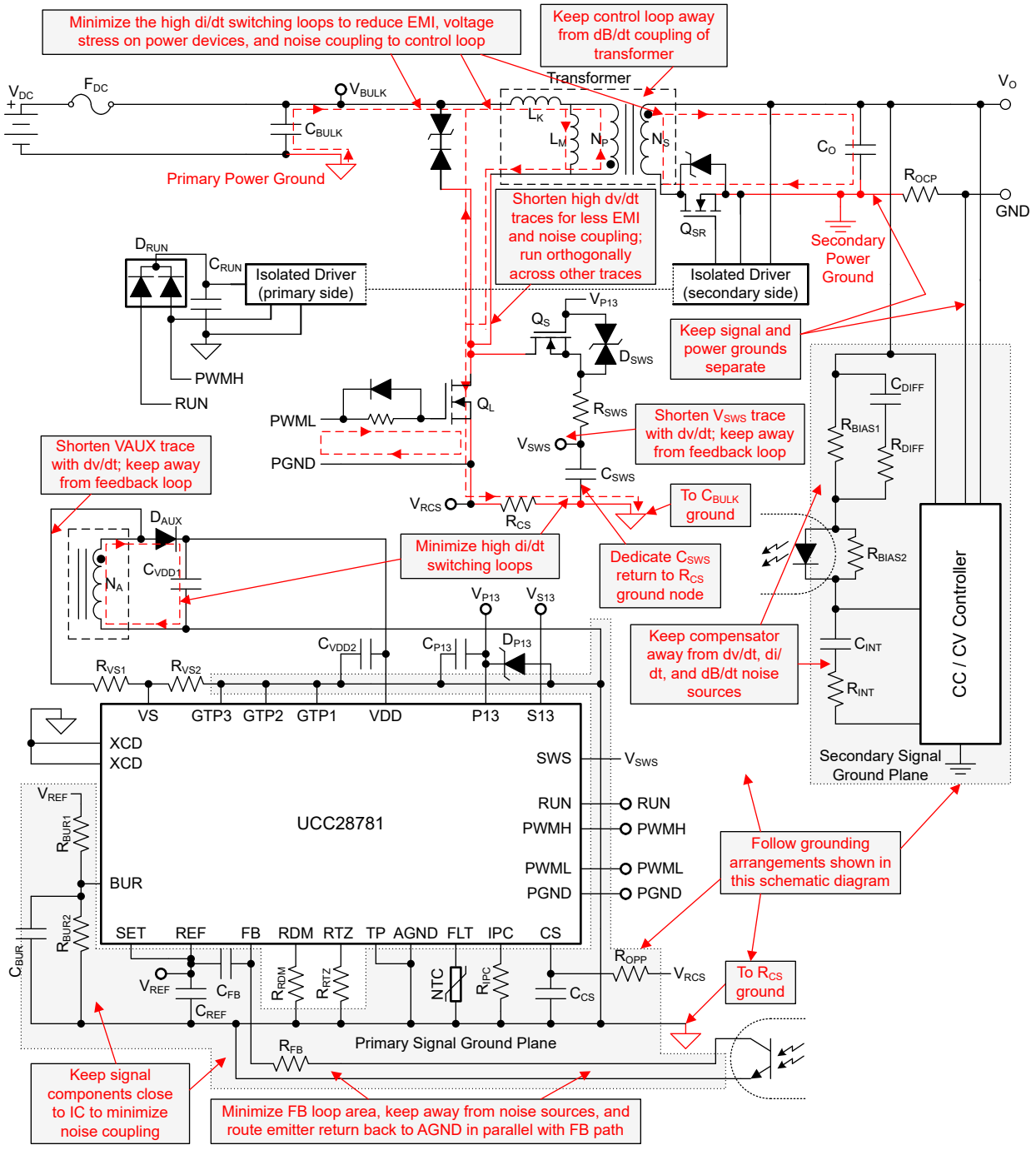


Figure 10-1. Typical Schematic with Layout Considerations

10.1.2 RDM and RTZ Pins

Minimize stray capacitance to RDM and RTZ pins.

- Place R_{RDM} and R_{RTZ} as close as possible between the controller pins and AGND pin.
- Avoid putting a ground plane or any other tracks under RDM and RTZ pins to minimize parasitic capacitance. This can be accomplished by putting cutouts and/or keepouts in the layers below these pins.

10.1.3 SWS Pin

Minimize potential stray noise coupling from SWS pin to noise-sensitive signals.

- Keep some distance between SWS network and other connections.
- The RC damping network (R_{SWS}, C_{SWS}) and the TVS diode (D_{SWS}) should be as close to the source pin of Q_S as possible instead of SWS pin, so the gate-to-source pin of Q_S can be effectively protected.
- Keep the return path for di/dt current through C_{SWS} and D_{SWS} separate from the IC local GND and FB signal return paths. Return C_{SWS} back to the ground node at R_{CS}, not at the IC.

10.1.4 VS Pin

Minimize stray capacitance at the VS pin to reduce the time-delay effect on ZVS control.

- Avoid putting a GND plane under the VS pin to reduce parasitic capacitance. This can be accomplished by inserting a cutout in the plane (if any) below this pin's pad and the tracks and pads of components connected to VS. Minimize the track length of the VS net.
- Do not run other tracks or planes over or under the VS net.
- Do not run other tracks or planes under R_{VS1} and R_{VS2}.

10.1.5 BUR Pin

The resistor divider (R_{BUR1} and R_{BUR2}) and the filter capacitor (C_{BUR}) on the BUR pin should to be as close to the BUR pin and IC AGND as possible.

- It is recommended to provide shielding on the BUR-pin trace with ground planes to minimize the noise-coupling effect on peak current variation during burst-mode operation. This can be accomplished by adding a ground plane under the BUR traces and pins.

10.1.6 FB Pin

This pin can be noise-sensitive to capacitive coupling from the high dV/dt switch nodes, or the flux coupling from magnetic components and high di/dt switching loops.

- Minimize the loop area for the PCB traces from the opto-coupler to the FB pin in order to avoid the possible flux coupling effect. Run the opto-coupler emitter return track from AGND at the IC in parallel with the FB to collector path, to minimize loop-area.
- Keep PCB traces away from the high dv/dt signals, such as the switch node of the converter (V_{SW}), the auxiliary winding voltage (V_{AUX}), and the SWS-pin voltage (V_{SWS}). If possible, it is recommended to provide shielding for the FB trace with ground planes.
- The filter capacitor between FB pin and REF pin (C_{FB}) needs to be as close to the two IC pins as possible.
- The current-limiting resistor of FB pin (R_{FB}) should be as close to the FB pin as possible to enhance the noise rejection of nearby capacitively-coupled noise sources.

10.1.7 CS Pin

The OPP-programming resistor (R_{OPP}) and the filter capacitor (C_{CS}) should be as close to the CS pin as possible to improve the noise rejection of nearby capacitively-coupled noise sources, and to filter any ringing that may be present during non-ZVS conditions.

10.1.8 AGND Pin

The AGND pin is the bias-power and signal-ground connection for the controller. The effectiveness of the filter capacitors on the signal pins depends upon the integrity of this ground return.

- Place the decoupling capacitors for VDD, REF, CS, BUR, and P13 pins as close as possible to the device pins and AGND pin with short traces.
- The device ground and power-stage ground should meet at the return pin of the current-sense resistor (R_{CS}). Try to ensure that high frequency, high current from the power stage does not flow through the signal ground.
- The thermal pad of the QFN package should be tied to the AGND pin with a short trace, and be connected to the signal ground plane with multiple vias which becomes a low-impedance ground return of external components to the AGND pin.

10.1.9 PGND Pin

The PGND pin is the gate-drive return for the PWML signal. It is NOT a ground return; do not confuse it as a power ground pin. It is not connected to AGND within the device.

- The PGND signal is normally connected to the source pin of the low-side switching device, and run in parallel with PWML to minimize loop area.
- In certain cases, PGND may be connected to AGND at a location where PWML return currents do not create ground noise to disturb control signals referenced to AGND.
- For the individual low-side GaN power IC with logic PWM input, it is recommended to connect PGND to the bottom of the current sense resistor (R_{CS}) directly.

10.1.10 Thermal Pad

The Thermal Pad (TP) is internally connected to the device substrate by an indeterminate impedance. Connect this pad externally to AGND at the AGND pin and at other pins that may also be tied to AGND for the application. This pad functions as a thermal dissipater for the device. Use multiple vias to connect this pad to other copper planes and areas to help dissipate heat and to maintain the lowest GND impedance for signal integrity.

10.2 Layout Example

The layout techniques described in previous sections are applied to the layout of the 60-W high-density DC-to-DC zero-voltage switching flyback converter. The schematic diagram of this converter is shown in the next three figures, and the pcb layers are shown in the following four figures.

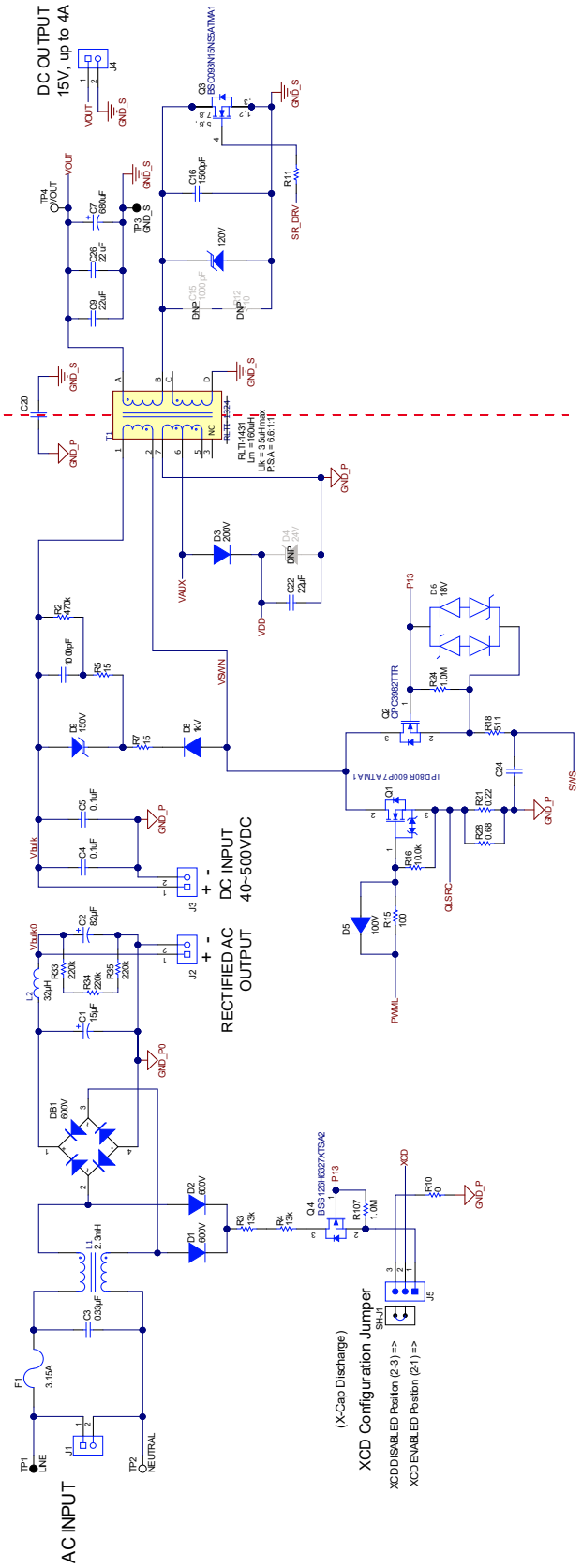


Figure 10-2. Power Stage of the 60-W EVM

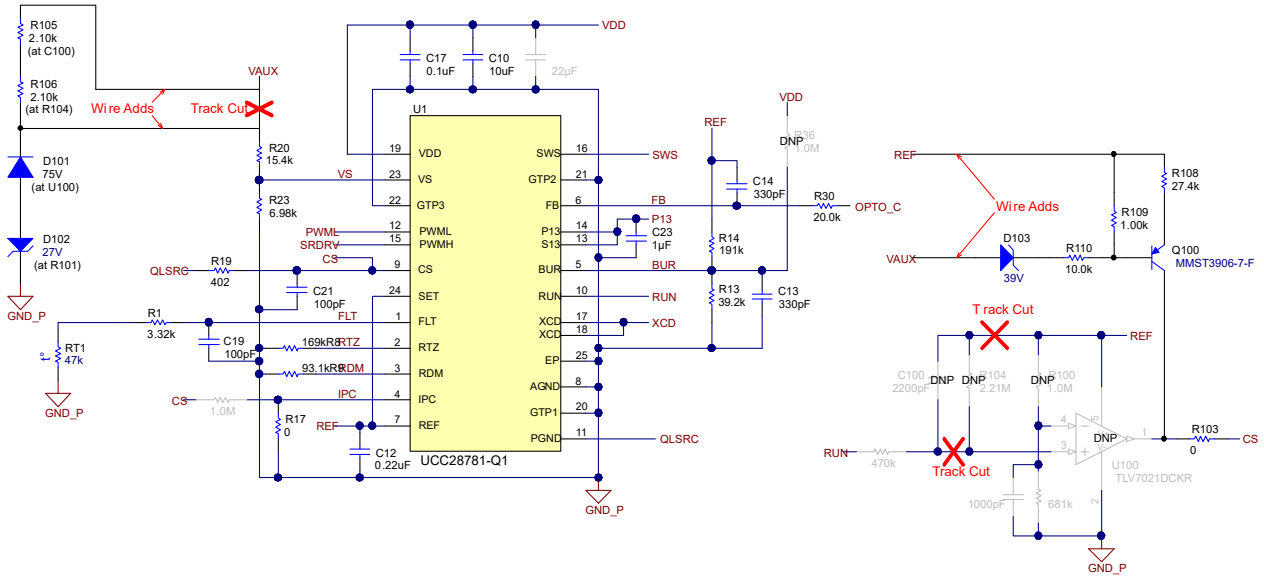


Figure 10-3. ZVSF Controller of the 60-W EVM

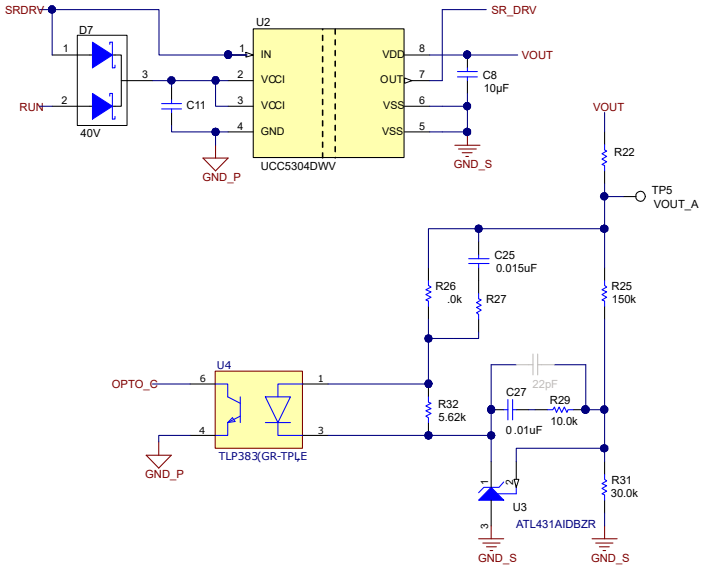


Figure 10-4. SR Drive and Feedback Circuits of the 60-W EVM

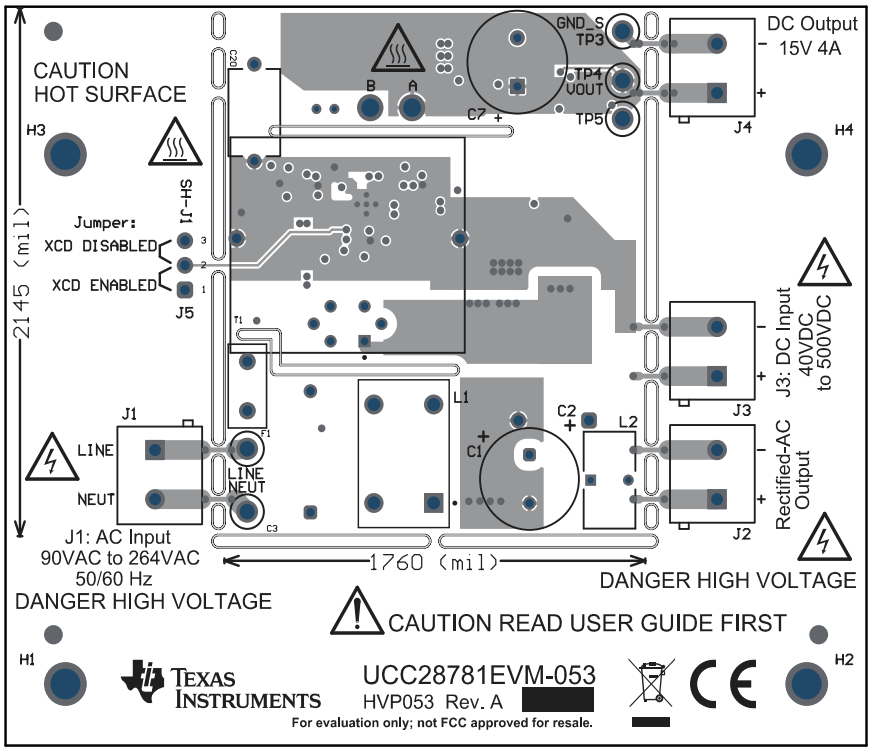


Figure 10-5. Top-Side Assembly and Top Layer of PCB

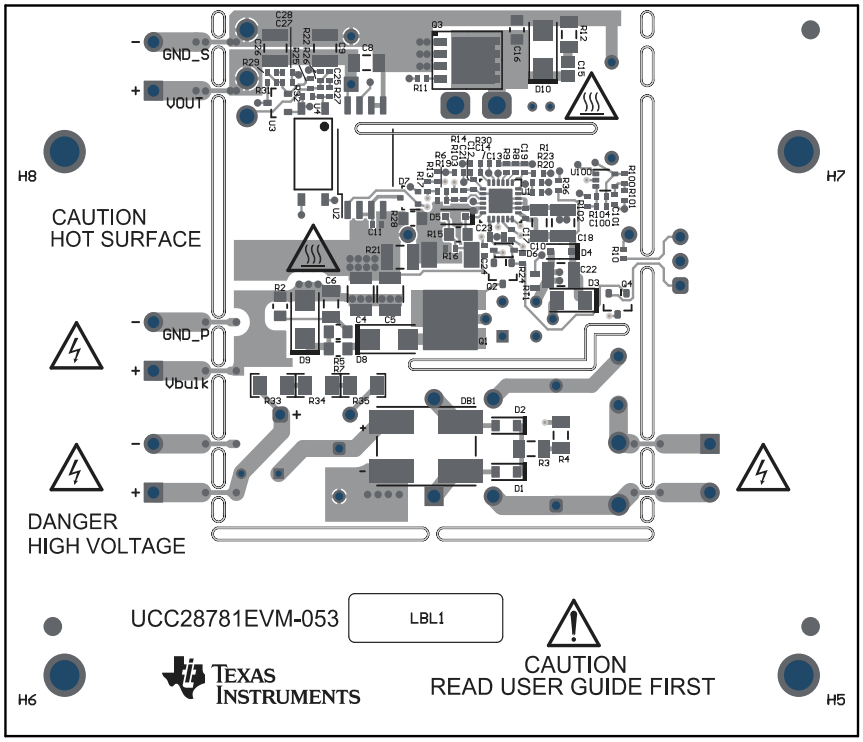


Figure 10-6. Bottom-Side Assembly and Bottom Layer of PCB

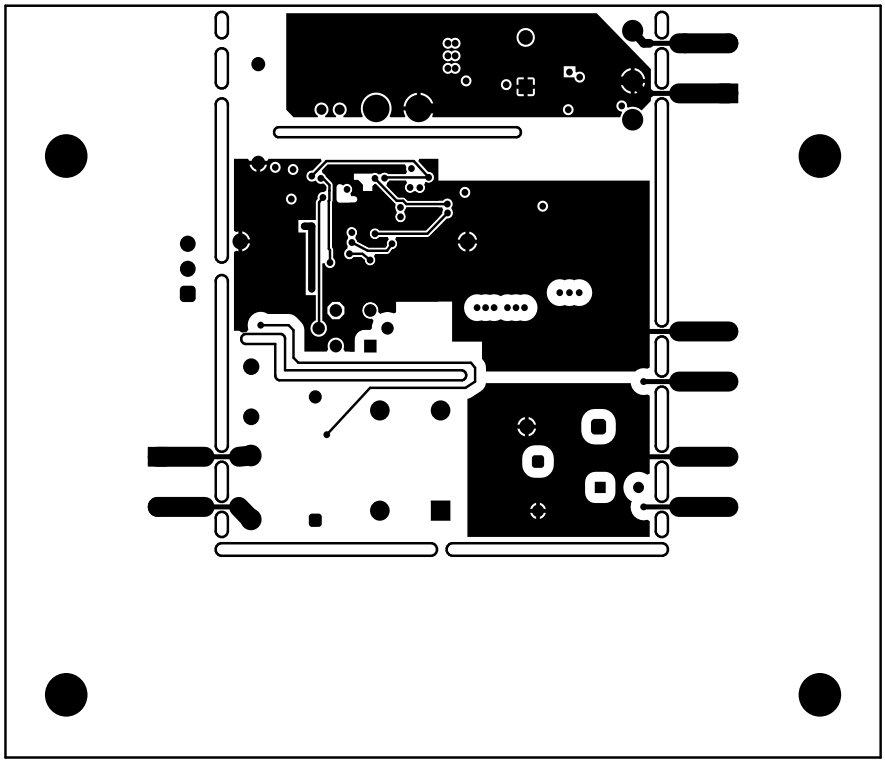
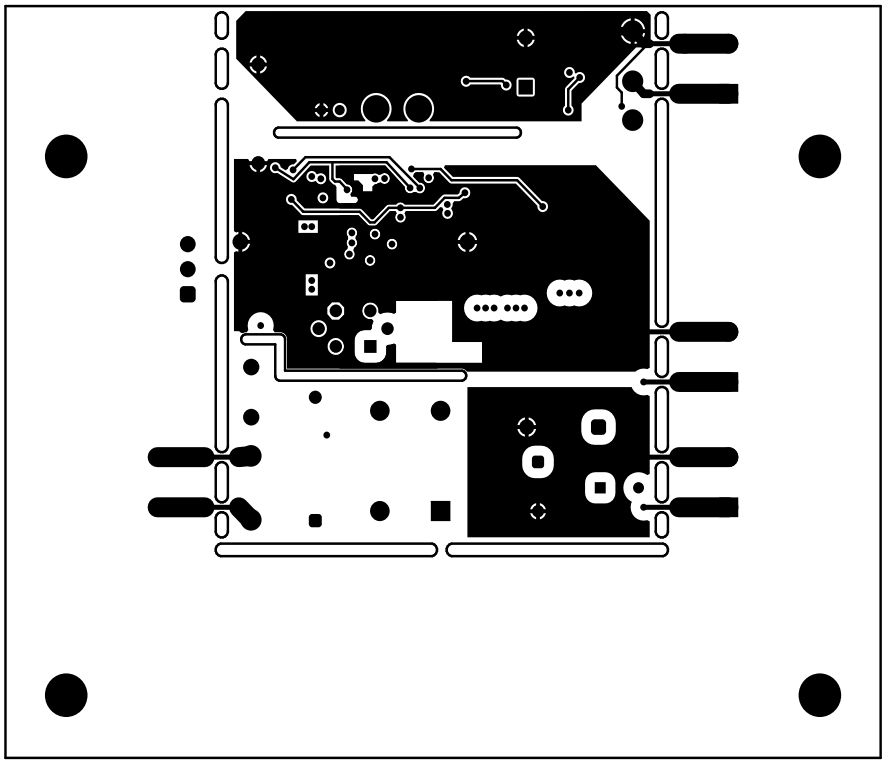


Figure 10-7. Inner Layer 1 (Second Layer) of PCB

Inner Layer 2 (Third Layer) of PCB



11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

11.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

11.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.5 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
UCC28781QRTWRQ1	Active	Production	WQFN (RTW) | 24	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	U28781Q
UCC28781QRTWRQ1.A	Active	Production	WQFN (RTW) | 24	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	U28781Q

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

OTHER QUALIFIED VERSIONS OF UCC28781-Q1 :

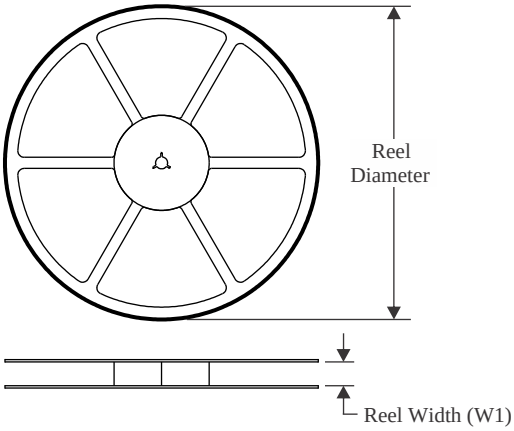
- Catalog : UCC28781

NOTE: Qualified Version Definitions:

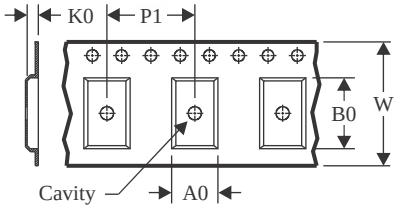
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

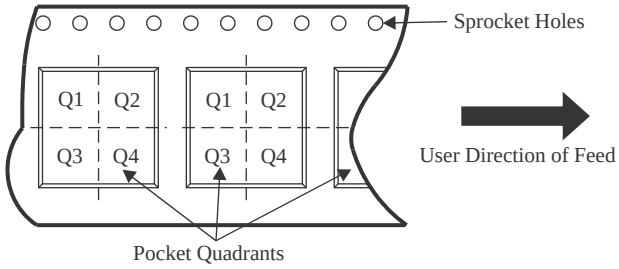


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

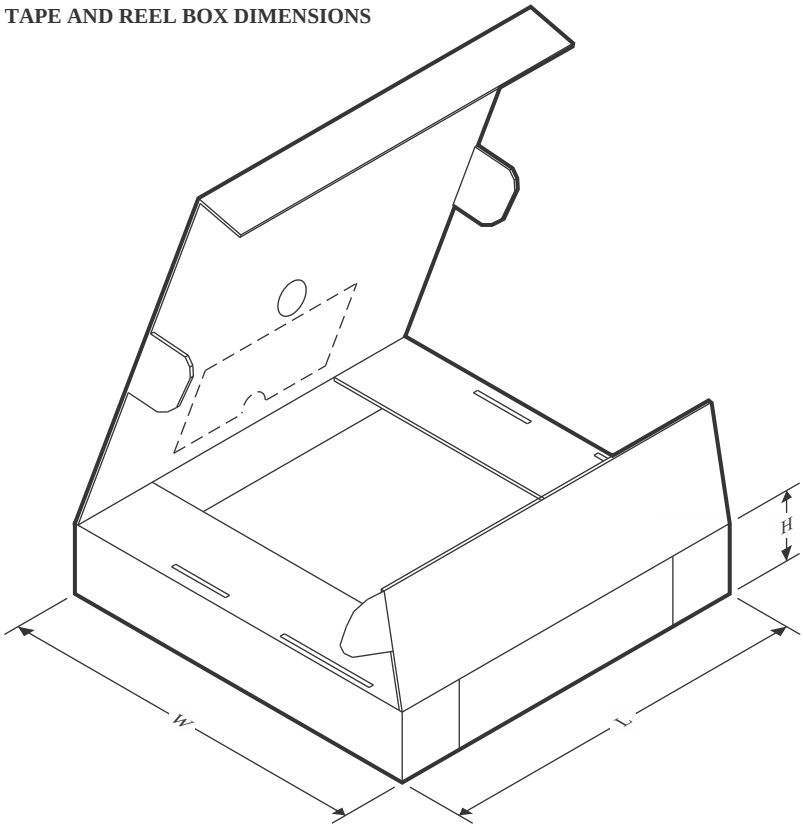
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UCC28781QRTWRQ1	WQFN	RTW	24	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UCC28781QRTWRQ1	WQFN	RTW	24	3000	367.0	367.0	35.0

GENERIC PACKAGE VIEW

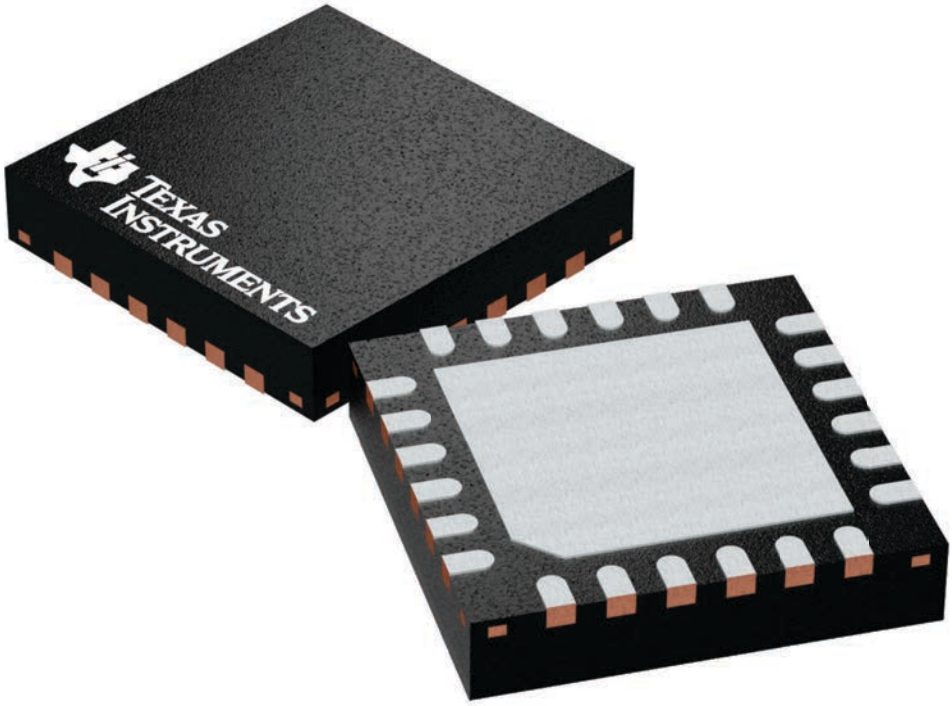
RTW 24

WQFN - 0.8 mm max height

4 x 4, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



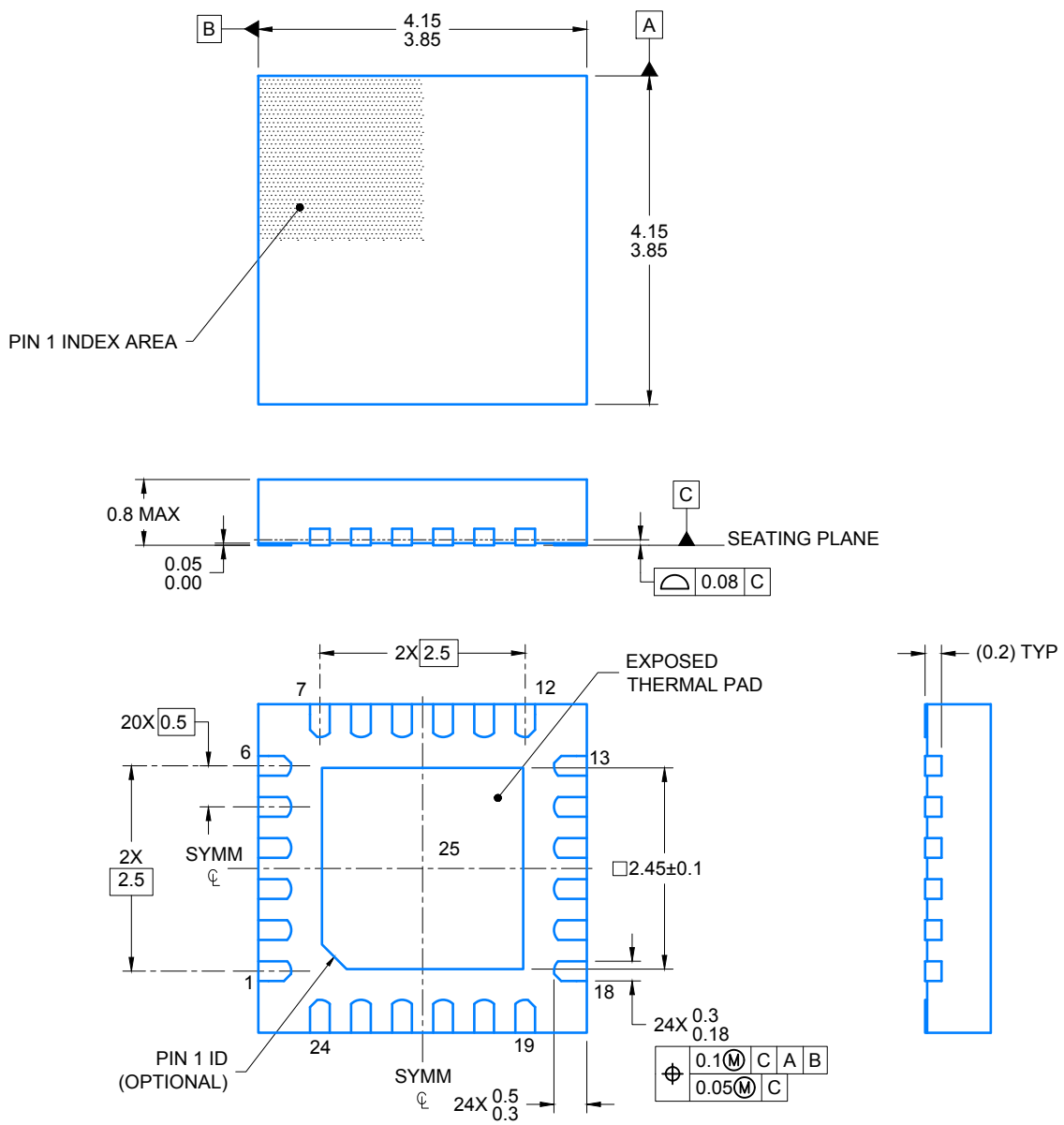
4224801/A

PACKAGE OUTLINE

RTW0024B

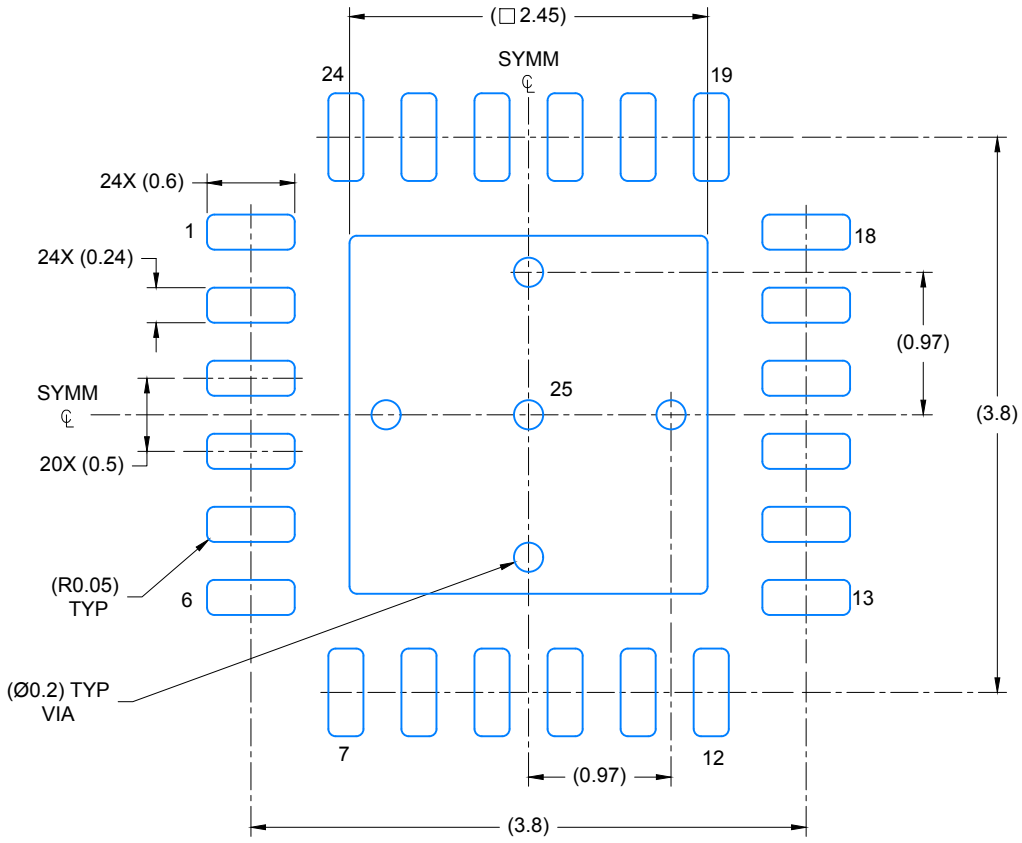
WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK-NO LEAD

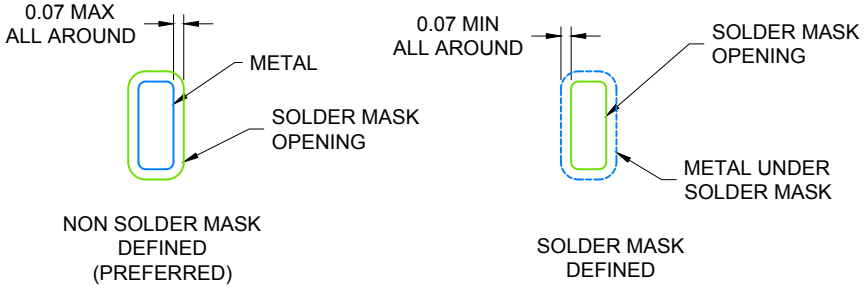


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
SCALE: 20X



SOLDER MASK DETAILS

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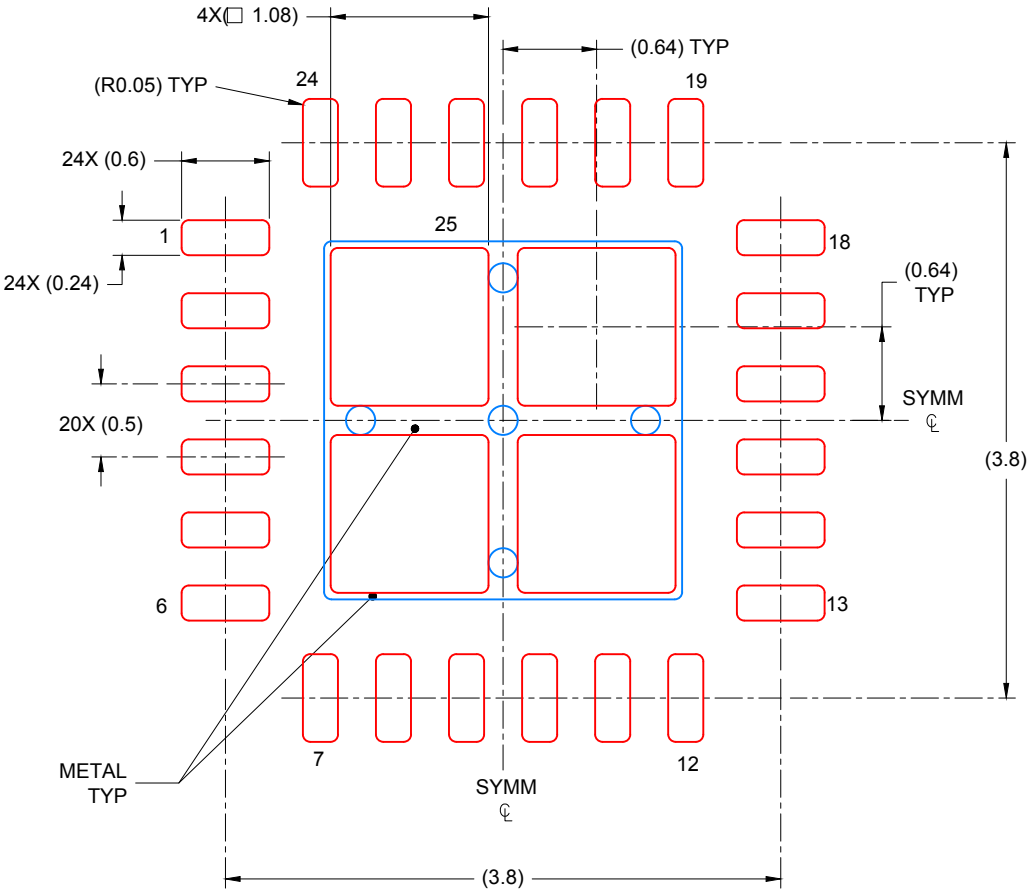
NOTES: (continued)

3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 25:
78% PRINTED COVERAGE BY AREA UNDER PACKAGE
SCALE: 20X

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NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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