Low Power Current Mode Push-Pull PWM

1 Features

- Qualified for automotive applications
- Dual output drive stages in push-pull configuration
- Current sense discharge transistor to improve dynamic response
- 130µA typical starting current
- 1mA typical run current
- Operation to 1MHz
- Internal soft start
- On-chip error amplifier with 2MHz gain bandwidth product
- On chip V_{DD} clamping
- Output drive stages capable of 500mA peak-source current, 1A peak-sink current
- Functional safety-capable
  - Documentation available to aid functional system design

2 Applications

- High-efficiency switch-mode power supplies
- Telecom DC/DC converters
- Point-of-load power modules
- Low-cost push-pull and half-bridge applications

3 Description

The UCC2808A-xQ1 is a family of BiCMOS push-pull pulse-width modulators that are high-speed and low-power. The UCC2808A-xQ1 contains all of the control and drive circuitry required for off-line or DC-to-DC fixed frequency current-mode switching power supplies with a minimal external part count.

The UCC2808A-xQ1 dual output drive stages are arranged in a push-pull configuration. Both outputs switch at half the oscillator frequency using a toggle flip-flop. The dead time between the two outputs is typically 60ns to 200ns, depending on the values of the timing capacitor and resistors, thus limiting each output stage duty cycle to less than 50%.

The UCC2808A-xQ1 family offers a variety of package options and choice of undervoltage lockout levels. The family has UVLO thresholds and hysteresis options for off-line and battery powered systems. Thresholds are shown in the orderable information table.

The UCC2808A-xQ1 is an enhanced version of the UCC2808 family. The significant difference is that the A versions feature an internal discharge transistor from the CS pin to ground, which is activated each clock cycle during the oscillator dead time. The feature discharges any filter capacitance on the CS pin during each cycle and helps minimize filter capacitor values and current sense delay.

Table 3-1. Package Information

DEVICE	PACKAGE(1)	PACKAGE SIZE(2)
UCC2808AQDR-1Q1	D (SOIC, 8)	4.90mm × 6.00mm
UCC2808AQDR-2Q1		

(1) For more information, see Section 11.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.

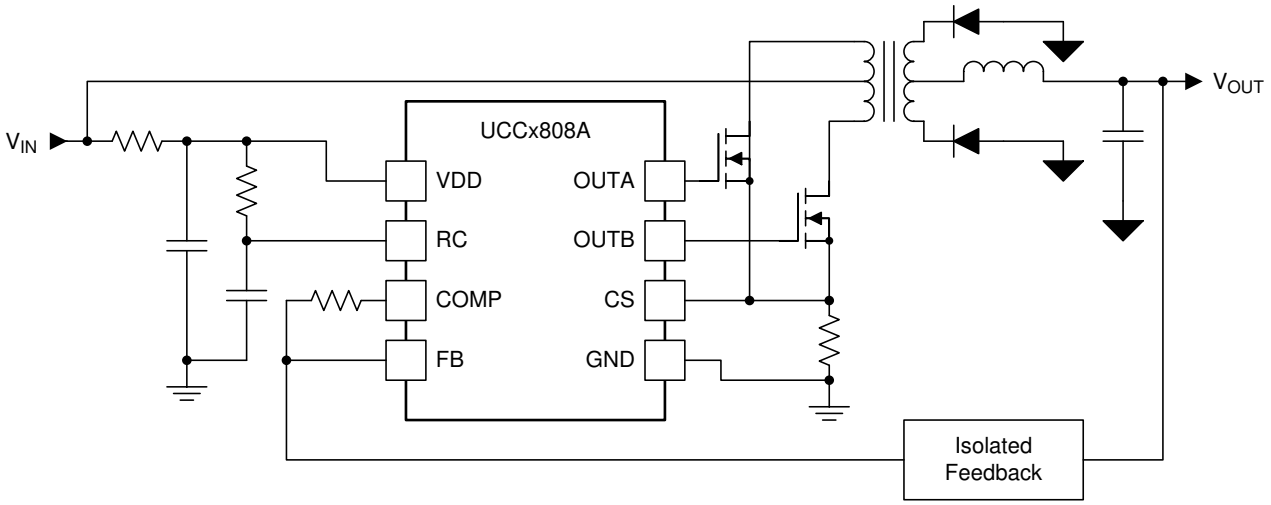


Table of Contents

4 Device Comparison Table

Device Comparison

T_A	UVLO OPTION	PACKAGE[1]		ORDERABLE PART NUMBER[2]	TOP-SIDE MARKING
–40°C to 125°C	12.5V/8.3V	D (SOIC, 8)	Tape and reel	UCC2808AQDR-1Q1	2D08-1
–40°C to 125°C	4.3V/4.1V	D (SOIC, 8)	Tape and reel	UCC2808AQDR-2Q1	2D08-2

(1) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.
(2) For the most current package and ordering information, see Section 11, or see the TI web site at www.ti.com.

5 Pin Configurations and Functions

D PACKAGE
(TOP VIEW)

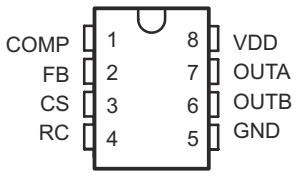


Table 5-1. Pin Functions

PIN		TYPE[1]	DESCRIPTION
NAME	NO.		
COMP	1	I/O	COMP is the output of the error amplifier and the input of the PWM comparator. See also Section 7.3.1.1.
CS	3	I	The input to the PWM, peak current, and overcurrent comparators. The overcurrent comparator is only intended for fault sensing. Exceeding the overcurrent threshold causes a soft start cycle. An internal MOSFET discharges the current sense filter capacitor to improve dynamic performance of the power converter.
FB	2	I	The inverting input to the error amplifier. For best stability, keep FB lead length as short as possible and FB stray capacitance as small as possible.
GND	5	G	Reference ground and power ground for all functions. Due to high currents, and high frequency operation of the UCC2808A-xQ1, a low impedance circuit board ground plane is highly recommended.
OUTA	7	I/O	Alternating high current output stages. Both stages are capable of driving the gate of a power MOSFET. Each stage is capable of 500mA peak-source current, and 1A peak-sink current. See also Section 7.3.1.2.
OUTB	6		
RC	4	I	The oscillator programming pin. The oscillator of the UCC2808Ax-Q1 tracks V_{DD} and GND internally, so that variations in power supply rails minimally affect frequency stability. See also Section 7.3.1.3.
VDD	8	P	The power input connection for this device. See also Section 7.3.1.4.

(1) I = Input, O = Output, I/O = Input or Output, G = Ground, P = Power.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		VALUE	UNIT
	Supply voltage (I_{DD} ≤ 10mA)	15	V
	Supply current(2)	20	mA
	OUTA/OUTB source current (peak)	–0.5	A
	OUTA/OUTB sink current (peak)	1	A
	Analog inputs (FB, CS)	–0.3 to V_{DD} 0.3, not to exceed 6	V
	Power dissipation at T_A = 25°C (D package)	650	mW
T_{stg}	Storage temperature	–65 to 150	°C
T_J	Junction temperature	–55 to 150	°C
	Lead temperature (soldering, 10 seconds)	300	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime

(2) Currents are positive into, negative out of the specified terminal. Consult the Packaging Section of the *Power Supply Control* data book for thermal limitations and considerations of packages.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002(1)	±2500	V
		Charged device model (CDM), per AEC Q100-011	±1500	

(1) AEC Q100-002 indicates that HBM stressing must be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{DD}	Supply voltage	UCC2808-1	13	14	V
		UCC2808-2	5	14	
T_J	Junction temperature	UCC2808-x	–40	125	°C

6.4 Thermal Information

THERMAL METRIC(1)		UCC2808A-xQ1 D (SOIC) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	118.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	63.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	65.9	°C/W
ψ_{JT}	Junction-to-top characterization parameter	14.6	°C/W
ψ_{JB}	Junction-to-board characterization parameter	65.0	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	—	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application note.

6.5 Electrical Characteristics

T_A = –40°C to 125°C for the UCC2808A-xQ1, V_{DD} = 10V(1), 1µF capacitor from V_{DD} to GND, R = 22kΩ, C = 330pF T_A = T_J, (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OSCILLATOR SECTION					
Oscillator frequency		175	194	213	kHz
Oscillator amplitude/V_{DD}	(2)	0.44	0.5	0.56	V/V
ERROR AMPLIFIER SECTION					
Input voltage	COMP = 2V	1.95	2	2.05	V
Input bias current		–1		1	µA
Open loop voltage gain		60	80		dB
COMP sink current	FB = 2.2V, COMP = 1V	0.3	2.5		mA
COMP source current	FB = 1.3V, COMP = 3.5V	–0.2	–0.5		mA
PWM SECTION					
Maximum duty cycle	Measured at OUTA or OUTB	48	49	50	%
Minimum duty cycle	COMP = 0V			0	%
CURRENT SENSE SECTION					
Gain	(3)	1.9	2.2	2.5	V/V
Maximum input signal	COMP = 5V(4)	0.45	0.5	0.55	V
CS to output delay	COMP = 3.5V, CS from 0mV to 600mV		100	200	ns
CS source current		–200			nA
CS sink current	CS = 0.5V, RC = 5.5V(5)	4	10		mA
Over current threshold		0.65	0.75	0.85	V
COMP to CS offset	CS = 0V	0.35	0.8	1.2	V
OUTPUT SECTION					
OUT low level	I = 100mA		0.5	1.1	V
OUT high level	I = −50mA, V_{DD} – OUT		0.5	1	V
Rise time	C_L = 1nF		25	60	ns
Fall time	C_L = 1nF		25	60	ns
UNDERVOLTAGE LOCKOUT SECTION					
Start threshold	UCC2808A−1(1)	11.5	12.5	13.5	V
	UCC2808A−2	4.1	4.3	4.5	V
Minimum operating voltage after start	UCC2808A−1	7.6	8.3	9	V
	UCC2808A−2	3.9	4.1	4.3	V
Hysteresis	UCC2808A−1	3.5	4.2	5.1	V
	UCC2808A−2	0.1	0.2	0.3	V
SOFT START SECTION					
COMP rise time	FB = 1.8V, rise from 0.5V to 4V		3.5	20	ms
OVERALL SECTION					
Startup current	V_{DD} < start threshold		130	260	µA
Operating supply current	FB = 0V, CS = 0V(6) (1)		1	2	mA
V_{DD} zener shunt voltage	I_{DD} = 10mA(7)	13	14	15	V

(1) For UCC2808A−1Q1, set V_{DD} above the start threshold before setting at 10V.
(2) Measured at RC. Signal amplitude tracks V_{DD}.
(3) Gain is defined by: A = $\Delta V_{COMP}/\Delta V_{CS}$, 0 ≤ V_{CS} ≤ 0.4V.
(4) Parameter measured at trip point of latch with FB at 0V.
(5) The internal current sink on the CS pin is designed to discharge an external filter capacitor. The pin is not intended to be a DC sink path.

(6) Does not include current in the external oscillator network.
(7) Start threshold and zener shunt threshold track one another.

6.6 Typical Characteristics

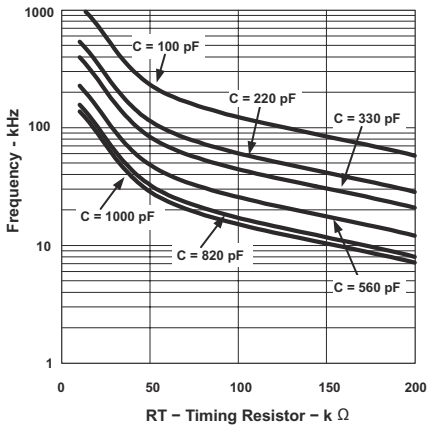


Figure 6-1. Oscillator Frequency vs External RC Values

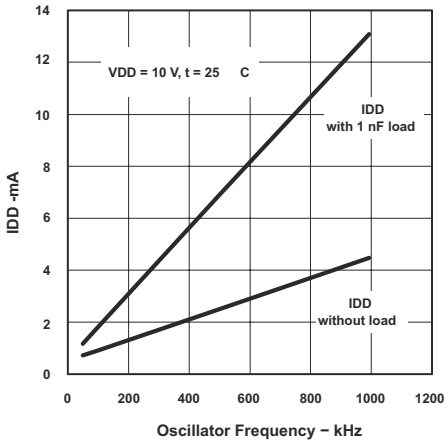


Figure 6-2. IDD vs Oscillator Frequency

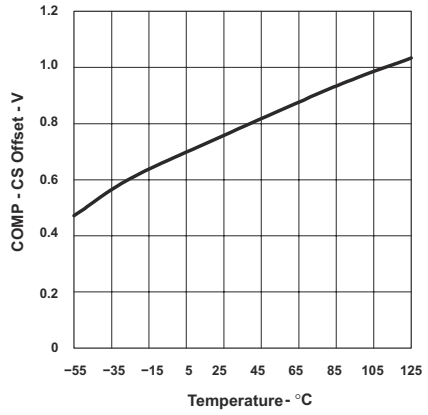


Figure 6-3. COMP To CS Offset vs Temperature

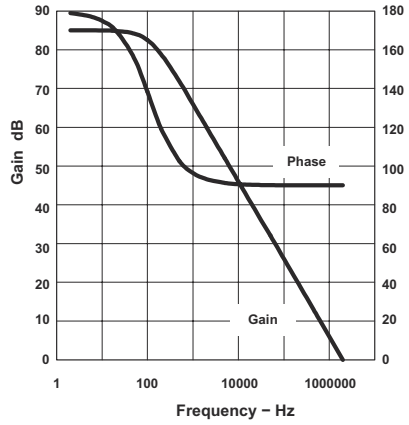


Figure 6-4. Error Amplifier Gain and Phase Response vs Frequency

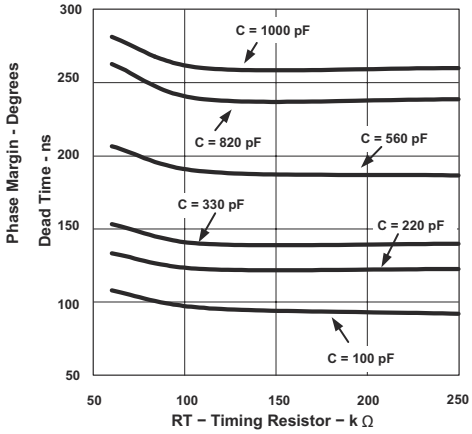


Figure 6-5. Output Dead Time vs External RC Values

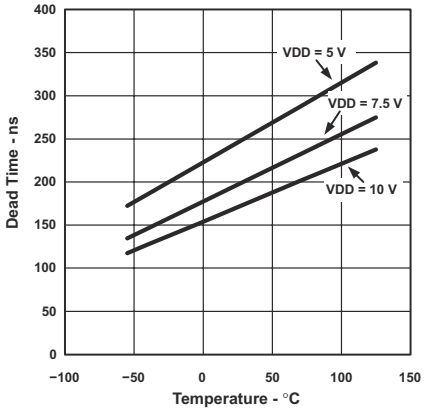


Figure 6-6. Dead Time vs Temperature

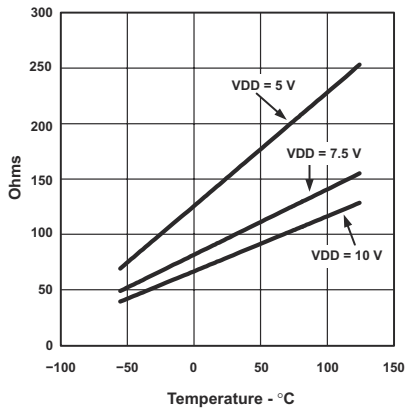


Figure 6-7. RC $R_{DS(on)}$ vs Temperature

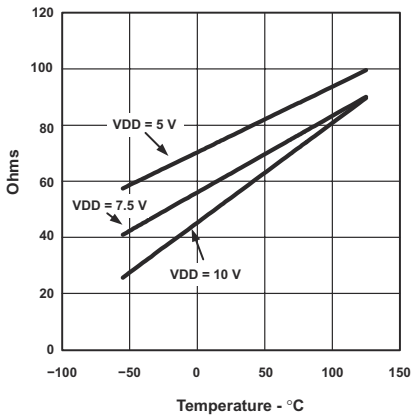


Figure 6-8. CS $R_{DS(on)}$ vs Temperature

7 Detailed Description

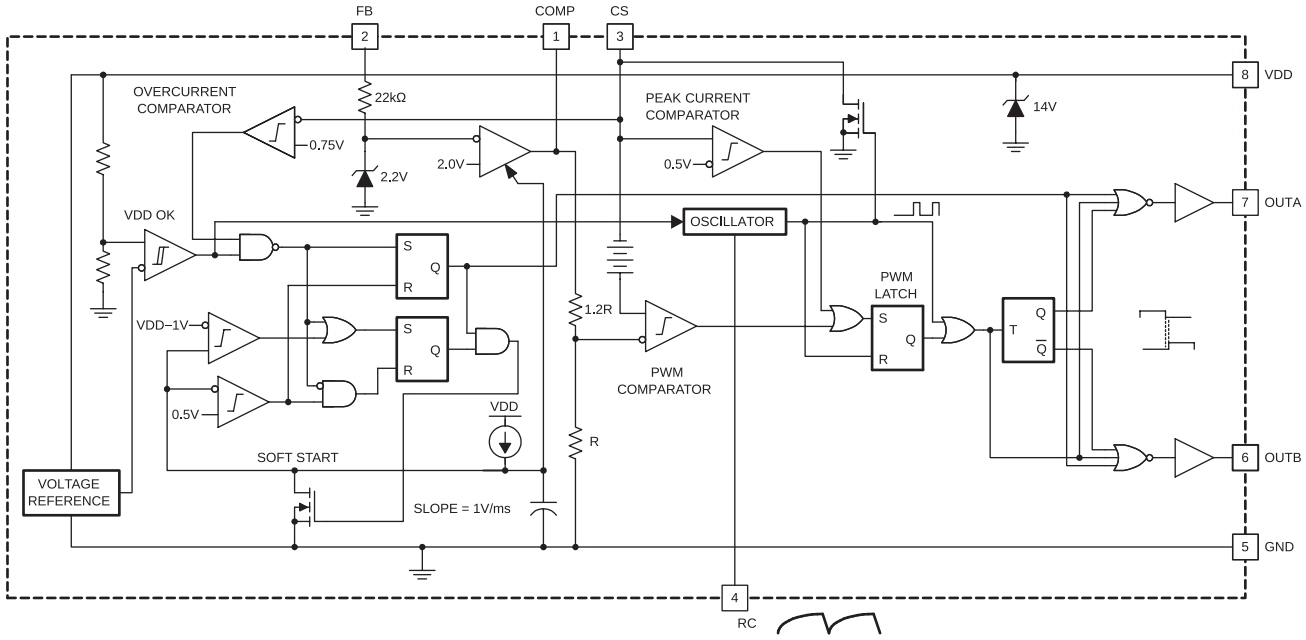
7.1 Overview

The UCC2808A-xQ1 device is a highly integrated, low-power current mode push-pull PWM controller. The controller employs low starting current and an internal control algorithm that offers accurate output voltage regulation in the presence of line and load variations. The UCC2808A-xQ1 family of parts has UVLO thresholds and hysteresis options for off-line and battery-powered systems.

Table 7-1. Undervoltage Lockout Levels

PART NUMBER	TURNON THRESHOLD	TURNOFF THRESHOLD
UCC2808A-1Q1	12.5V	8.3V
UCC2808A-2Q1	4.3V	4.1V

7.2 Functional Block Diagram



Note: The oscillator generates a sawtooth waveform on RC. During the RC rise time, the output stages alternate on time, but both stages are off during the RC fall time. The output stages switch a 1/2 the oscillator frequency, with specified duty cycle of < 50% for both outputs.

Figure 7-1. Block Diagram

7.3 Feature Description

7.3.1 Pin Descriptions

7.3.1.1 COMP Pin

The error amplifier in the UCC2808A-xQ1 is a true low-output impedance, 2MHz operational amplifier. As such, the COMP pin can both source and sink current. However, the error amplifier is internally current limited, so that zero duty cycle can be externally forced by pulling COMP to GND.

The UCC2808A-xQ1 family features built-in full-cycle soft start. Soft start is implemented as a clamp on the maximum COMP voltage.

7.3.1.2 OUTA and OUTB Pins

The output stages switch at half the oscillator frequency, in a push-pull configuration. When the voltage on the RC pin is rising, one of the two outputs is high, but during fall time, both outputs are off. The dead time between the two outputs, along with a slower output rise time than fall time, verifies that the two outputs are not on at the same time. Dead time is typically 60ns to 200ns and depends upon the values of the timing capacitor and resistor.

The high-current output drivers consist of MOSFET output devices, which switch from V_{DD} to GND. Each output stage also provides a very low impedance to overshoot and undershoot. In many cases, external Schottky-clamp diodes are not required.

7.3.1.3 RC Pin

The oscillator of the UCC2808Ax-Q1 tracks V_{DD} and GND internally, so that variations in power supply rails minimally affect frequency stability. Figure 7-2 shows the oscillator block diagram.

Only two components are required to program the oscillator: a resistor (tied to the V_{DD} and RC), and a capacitor (tied to the RC and GND). The approximate oscillator frequency is calculated in:

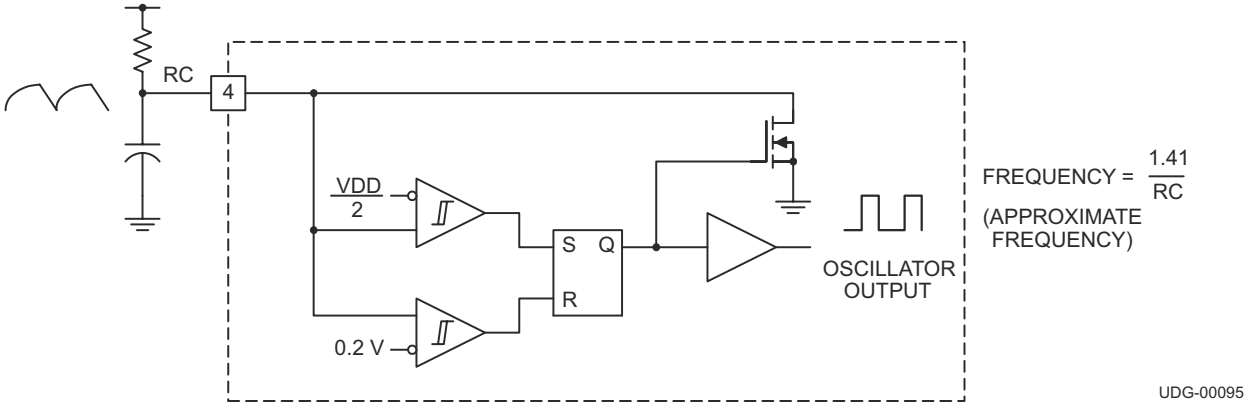
$$f_{OSCILLATOR} = \frac{1.41}{RC} \quad (1)$$

where

- Frequency is in hertz (Hz)
- Resistance is in Ω
- Capacitance is in farads (F)

The recommended range of timing resistors is between 10kΩ and 200kΩ and range of timing capacitors is between 100pF and 1000pF. Avoid timing resistors less than 10kΩ.

For best performance, keep the timing capacitor lead to GND, timing resistor lead from V_{DD}, and leads between timing components and RC as short as possible. Separate ground and V_{DD} traces to the external timing network are encouraged.



A. The oscillator generates a sawtooth waveform on RC. During the RC rise time, the output stages alternate on time, but both stages are off during the RC fall time. The output stages switch a 1/2 the oscillator frequency, with verified duty cycle of < 50% for both outputs.

Figure 7-2. Block Diagram for Oscillator

7.3.1.4 VDD Pin

The VDD pin is the power input connection for UCC2808A-xQ1. Although quiescent V_{DD} current is very low, total supply current is higher. The total supply current depends on OUTA and OUTB current and the programmed oscillator frequency. Total V_{DD} current is the sum of quiescent V_{DD} current and the average OUT current. With a known operating frequency and the MOSFET gate charge (Q_g), the average OUT current is calculated from:

$$I_{OUT} = Q_g \times F \quad (2)$$

where

- F = frequency

To prevent noise problems, bypass V_{DD} to GND with a ceramic capacitor as close to the chip as possible, along with an electrolytic capacitor. A 1µF decoupling capacitor is recommended.

7.4 Device Functional Modes

7.4.1 VCC

When VCC rises above 12.5V (for the UCC2808A-1Q1) or above 4.3V (for the UCC2808A-2Q1) the device is enabled. When any fault conditions are cleared, a soft-start condition is initiated and the gate driver outputs begin switching.

When VCC drops below 8.3V (for the UCC2808A-1Q1) or 4.1V (for the UCC2808A-2Q1) the device enters the UVLO protection mode and both gate drivers are actively pulled low.

7.4.2 Push-Pull or Half-Bridge Function

Because the UCCx2808A-xQ1 provide alternate 180° out-of-phase gate drive signals (OUTA and OUTB), these devices are great for use as a controller for push-pull or half-bridge topologies. For half-bridge topology, the UCCx2808A-xQ1 require a an external high side gate driver or pulse transformer on one or both of the OUTA and OUTB signals.

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

8.2 Typical Application

A 200kHz push-pull application circuit with a full-wave rectifier is shown in Figure 8-1. The output, V_O, provides 5V at 50W maximum and is electrically isolated from the input. Since the UCC2808A-xQ1 is a peak-current-mode controller, the 2N2907 emitter following amplifier (buffers the CT waveform) provides slope compensation, which is necessary for duty ratios greater than 50%. Capacitor decoupling is important with a single ground IC controller, and 1µF is suggested because 1µF is as close to the IC as possible. The controller supply is a series RC for start-up, paralleled with a bias winding on the output inductor used in steady state operation.

Isolation is provided by an optocoupler with regulation completed on the secondary side using the TL431 adjustable precision shunt regulator. Small signal compensation with tight voltage regulation is achieved using TL431 on the secondary side. Many choices exist for the output inductor depending on cost, volume, and mechanical strength. Several design options are iron powder, molypermalloy (MPP), or a ferrite core with an air gap. The main power transformer has a Magnetics® Inc. ER28 size core made of P material for efficient operation at this frequency and temperature. The input voltage ranges from 36V DC to 72V DC.

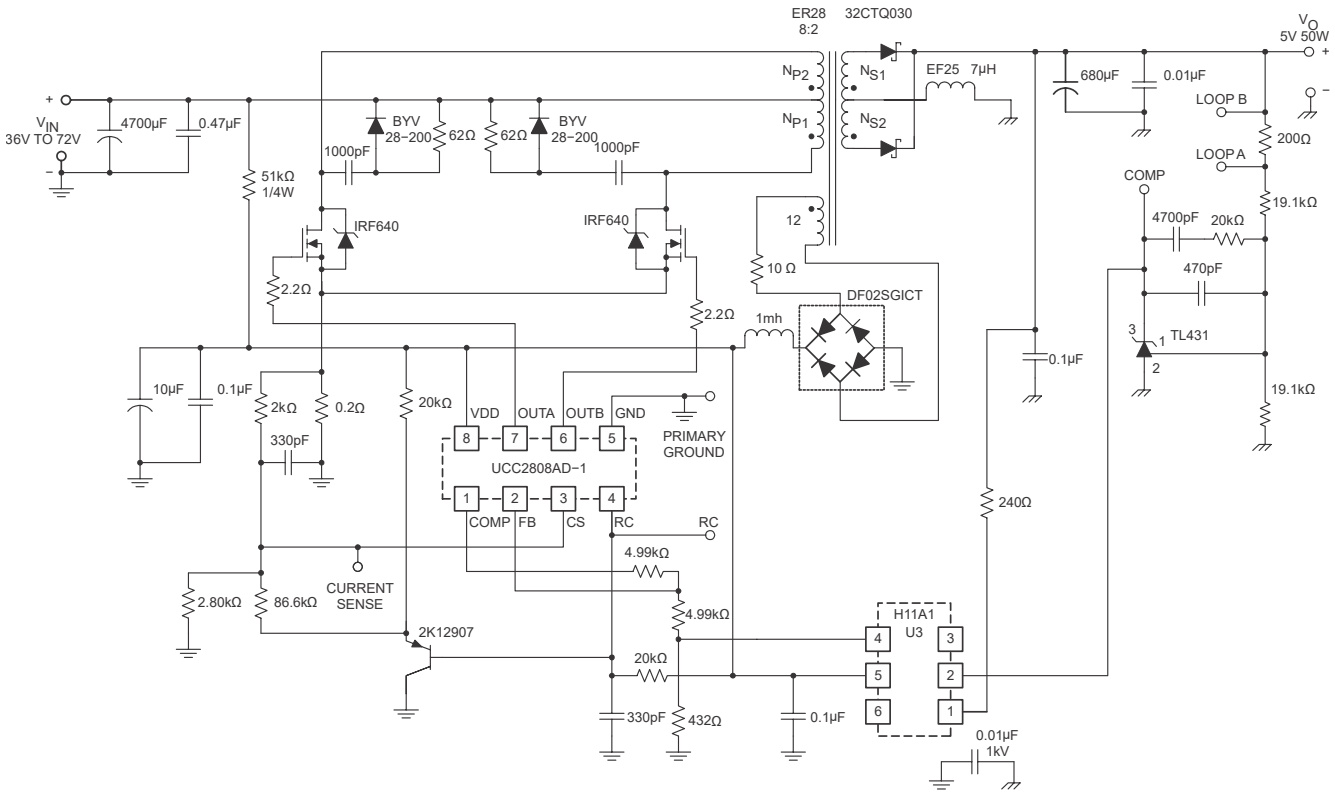


Figure 8-1. Typical Application Diagram: 48V In, 5V, 50W Output

8.2.1 Design Requirements

The following table lists the design parameters for the UCC2808A-x.

Table 8-1. Design Parameters

PARAMETER	VALUE
Output voltage	5V
Rated output power	50W
Input DC voltage range	36V to 72V
Switching frequency	210kHz

8.2.2 Detailed Design Procedure

The output, V_O, provides 5V at 50W maximum and is electrically isolated from the input. Because the UCC2808A-1Q1 is a peak current mode controller, the 2N2907 emitter-follower amplifier buffers the oscillator waveform (RC pin) and provides slope compensation to the current sense (CS) input. This configuration is necessary for duty cycle ratios greater than 50%.

Capacitor decoupling is provided on the VDD pin. TI recommends using a minimum decoupling capacitance of 10µF electrolytic and 0.1µF ceramic. Place the ceramic capacitor as close to the VDD pin as possible. The UCC2808A-1Q1 is initially powered up from the 36V to 72V input supply. After the power supply has started, an auxiliary winding on the main power transformer provides the bias supply.

Isolation is provided by an optocoupler with regulation accomplised on the secondary side using the TL431 precision programmable reference. The internal error amplifier of the UCC2808A-1Q1 is set up as a unity gain amplifier and the compensation network is provided on the secondary side.

Many choices exist for the output inductor depending on cost and size constraints. Design options are powdered iron, molypermalloy, or the ferrite core option that is used in this design. The power transformer is a low profile design, EFD25 size, using the Magnetics Inc. P material. This material is a good choice for low power loss at high switching frequency.

The switching frequency is set at 210kHz with the RC network on the RC pin.

8.2.3 Application Curves

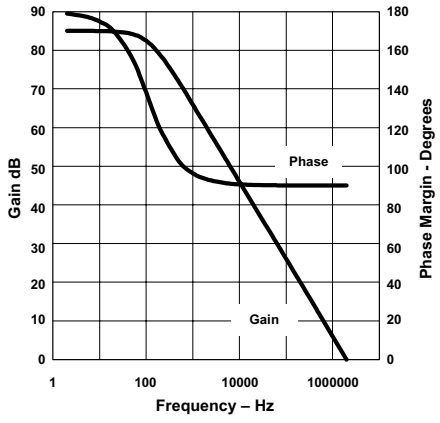


Figure 8-2. Error Amplifier Gain and Phase Response vs Frequency

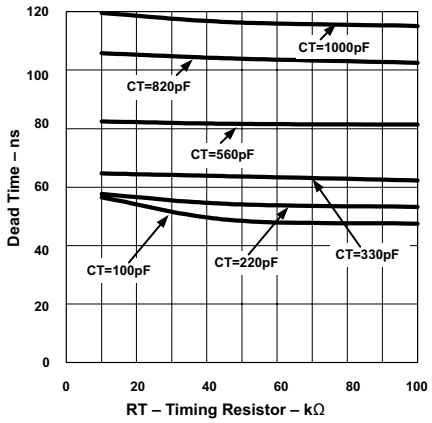


Figure 8-3. Dead Time vs Timing Resistor

8.3 Power Supply Recommendations

The VDD power terminal for these devices requires the placement of electrolytic capacitor as energy storage capacitor because of the 1A drive capability of the UCCx2808A-xQ1 controller. A low-ESR noise decoupling capacitor is also required; place this capacitor as close as possible to the VDD and GND pins. Ceramic

capacitors with stable dielectric characteristics over temperature are recommended. X7R is a good dielectric material for use here.

TI recommends a 10µF, 25V electrolytic capacitor.

8.4 Layout

8.4.1 Layout Guidelines

1. Place the VDD capacitor as close as possible between the VDD pin and GND of the UCC2808A-x, with the VDD capacitor tracked directly to both pins.
2. A small, external filter capacitor is recommended on the CS pin. Track the filter capacitor as directly as possible from the CS to GND pins.
3. The tracking and layout of the FB pin and connecting components is critical to minimize noise pickup and interference. Minimize the total surface area of traces on the FB net.
4. The OUTA and OUTB pins have a high-current source and sink capability. An external gate resistor is recommended to damp oscillations. A value of around 1 to 10 Ohms is recommended. A pulldown resistor on the gate to source is recommended to prevent the MOSFET gate from floating and turning on if there is an open-circuit fault in the gate drive path.

8.4.2 Layout Example

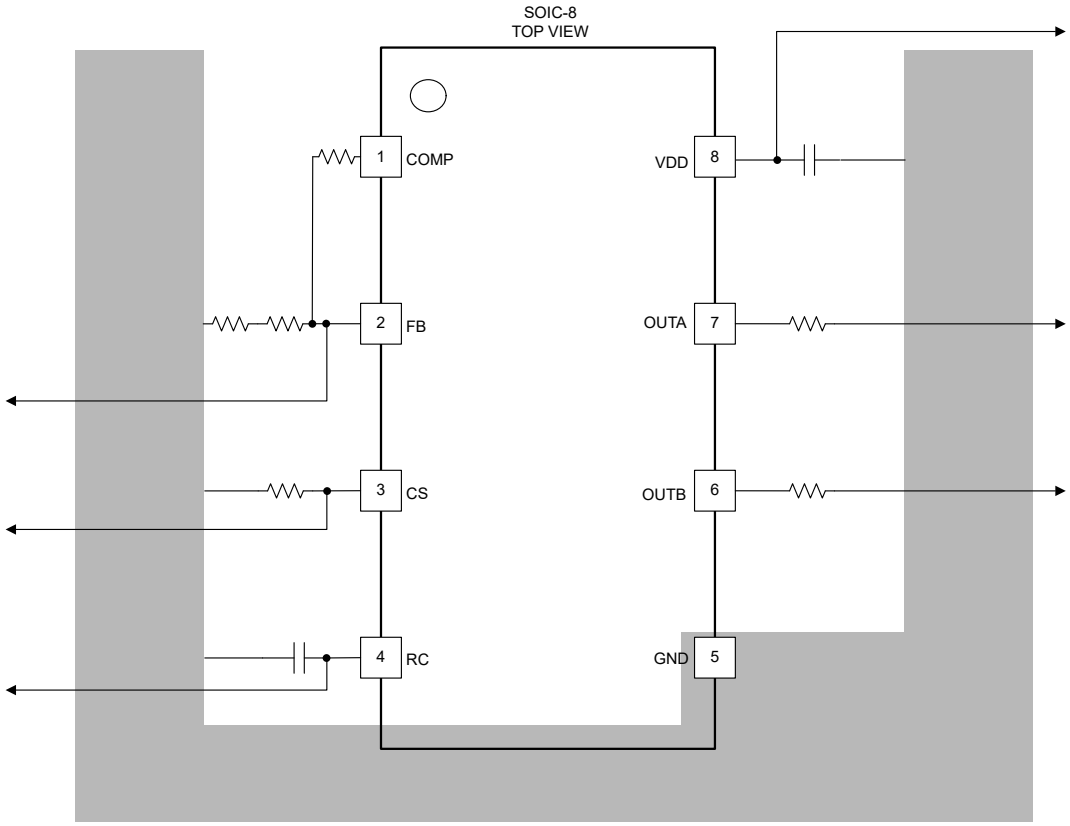


Figure 8-4. Recommended Layout

9 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

9.1 Documentation Support

9.1.1 Related Documentation

- Texas Instruments, *UCC2808A-xQ1* Functional Safety FIT Rate, FMD and Pin FMA
- Texas Instruments, *Semiconductor and IC Package Thermal Metrics* application note

9.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

9.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.
Magnetics® is a registered trademark of Magnetics, Inc.
All trademarks are the property of their respective owners.

9.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.5 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (July 2012) to Revision C (July 2025)	Page
• Updated the numbering formatting for tables, figures, and cross-references throughout the document	1
• Added sections to adhere to current standards	1
• Added functional safety capable information	1
• Deleted PW package information throughout the document	1
• Added *Thermal Information* table	5
• Added *Device Functional Modes* section	11

Changes from Revision A (April 2008) to Revision B (July 2012)	Page
• Changed top-side marking for SOIC (D) package from: UCC2808AD-1Q1 to: 2D08-1 and from: UCC2808AD-2Q1 to: 2D08-2	3

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
UCC2808AQDR-1G4Q1	Obsolete	Production	SOIC (D) | 8	-	-	Call TI	Call TI	-40 to 125	2D08-1 A-1Q1
UCC2808AQDR-1Q1	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2D08-1
UCC2808AQDR-1Q1.A	Active	Production	null (null) |	2500 | LARGE T&R	-	NIPDAU	Level-1-260C-UNLIM	See UCC2808AQDR-1Q1	2D08-1
UCC2808AQDR-2Q1	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2D08-2
UCC2808AQDR-2Q1.A	Active	Production	null (null) |	2500 | LARGE T&R	-	NIPDAU	Level-1-260C-UNLIM	See UCC2808AQDR-2Q1	2D08-2

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

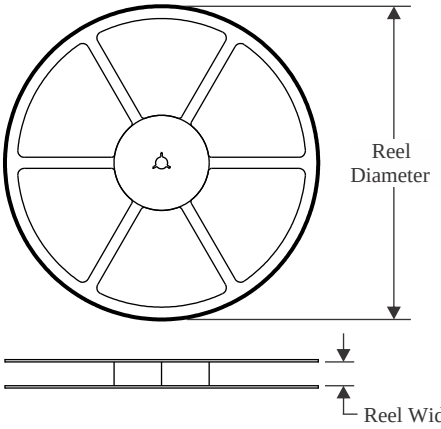
(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

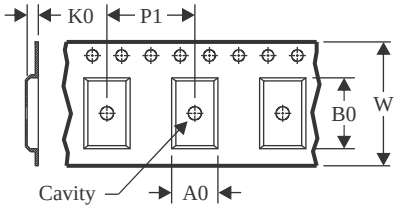
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

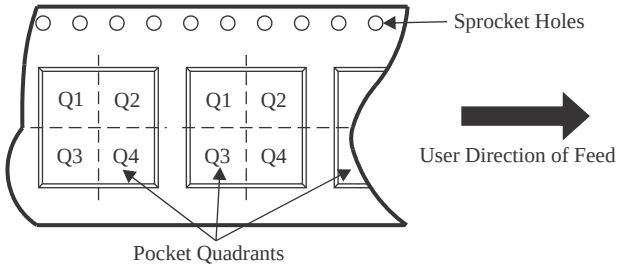


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

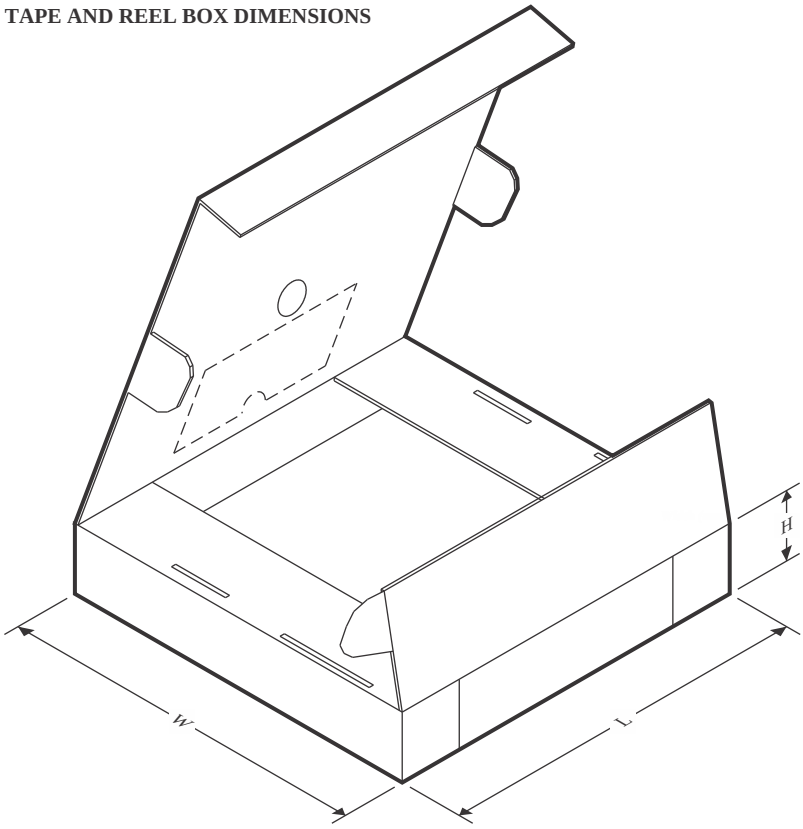
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

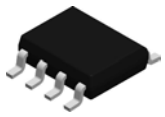
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UCC2808AQDR-1Q1	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UCC2808AQDR-2Q1	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UCC2808AQDR-1Q1	SOIC	D	8	2500	353.0	353.0	32.0
UCC2808AQDR-2Q1	SOIC	D	8	2500	353.0	353.0	32.0

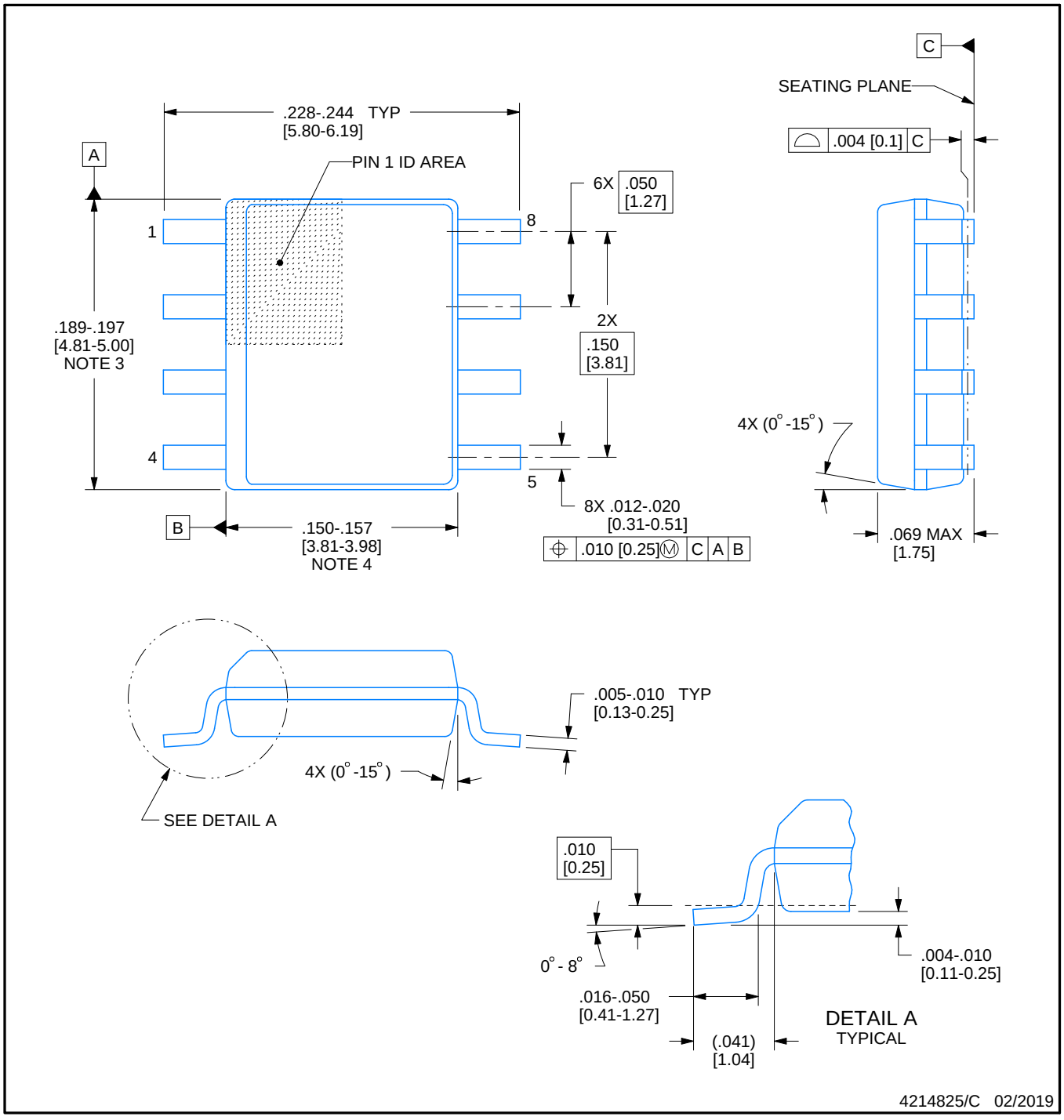


PACKAGE OUTLINE

D0008A

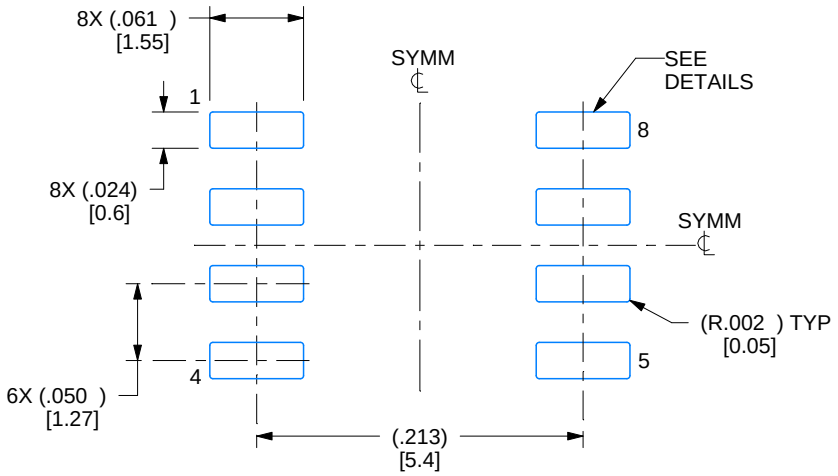
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

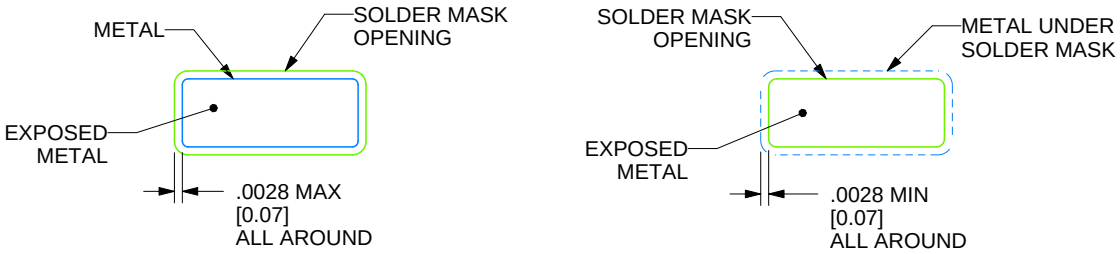


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

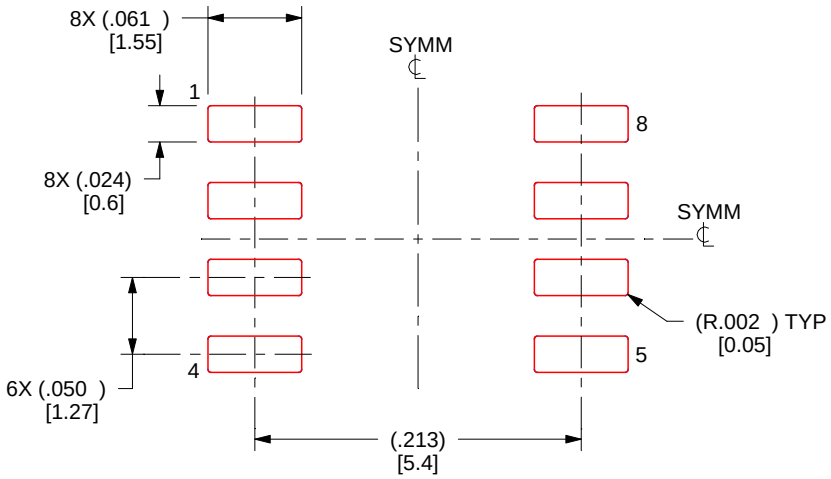
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265