UCC278X4-Q1 High-Speed, Automotive 230V Half-Bridge Driver with 3.5A, 4A Drive Strength and up to 100V/ns Noise Immunity

1 Features

- AEC-Q100 qualified for automotive applications
  - Device temperature grade 1
- Dual independent inputs for high-side and low-side drivers with interlock (UCC27834-Q1) or no interlock (UCC27884-Q1)
- Maximum bootstrap voltage of +230V (HB pin)
- 8.5V to 20V VDD bias recommended range
- Peak output current of 3.5A source, 4A sink
- Fast propagation delay (29ns typical)
- Tight propagation delay matching between HO/LO (<5ns max)
- dV/dt immunity of 100V/ns
- Low quiescent supply current draw of 150µA (typical) on VDD and 90µA (typical) on HB
- Built-in 8V UVLO protection for both high and low side channels
- Floating channel designed for bootstrap operation
- Available in standard SOIC-8 package
- All parameters specified over temperature range, –40°C to +150°C

2 Applications

- Motor drive (stepper motors, fans, power tools, robotics, drones, servos)
- E-bikes and E-scooters
- Solar boost and buck-boost MPPT
- Microinverters

3 Description

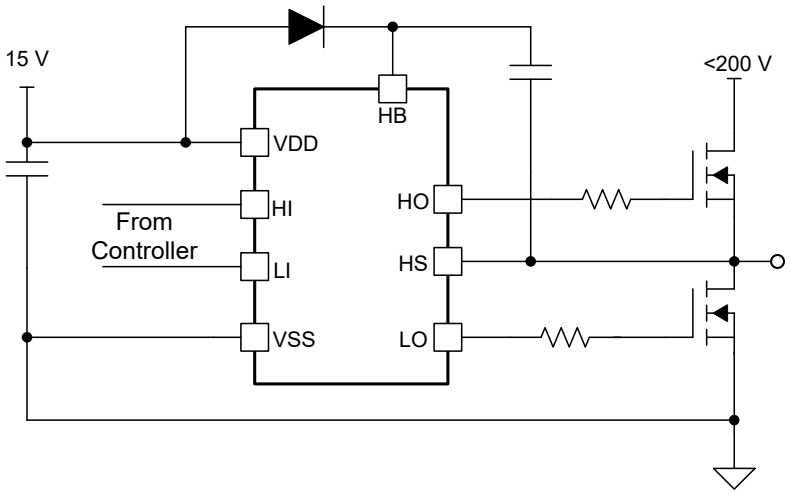
The UCC278X4-Q1 is a 230V half-bridge gate driver with 3.5A source, 4A sink current, targeted to drive power MOSFETs. The device consists of one ground-referenced channel (LO) and one floating channel (HO) which is designed to drive half-bridge configured MOSFETs operating with bootstrap power supplies. The device features fast propagation delays and excellent delay matching between both channels.The UCC278X4-Q1 allows a wide VDD operating voltage of 8.5V to 20V to support a wider range of gate voltage drive, as well as UVLO protection for both the low-side (VDD) and the high-side (HB) bias supplies. The UCC27834-Q1 includes an interlock function option to prevent both outputs from being turned on simultaneously

The device features robust drive with excellent noise and transient immunity including high dV/dt tolerance (100V/ns), and wide negative transient safe operating area (NTSOA) on the switch node (HS). The UCC278X4-Q1 is available in the SOIC-8 pin package and is rated to operate from –40°C to 150°C.

Package Information

PART NUMBER	PACKAGE(1)	BODY SIZE (NOM)
UCC27834D-Q1	D (SOIC 8)	3.91mm × 4.90mm
UCC27884D-Q1 (2)	D (SOIC 8)	3.91mm × 4.90mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.
(2) Product Preview



Simplified Schematic

Table of Contents

4 Pin Configuration and Functions

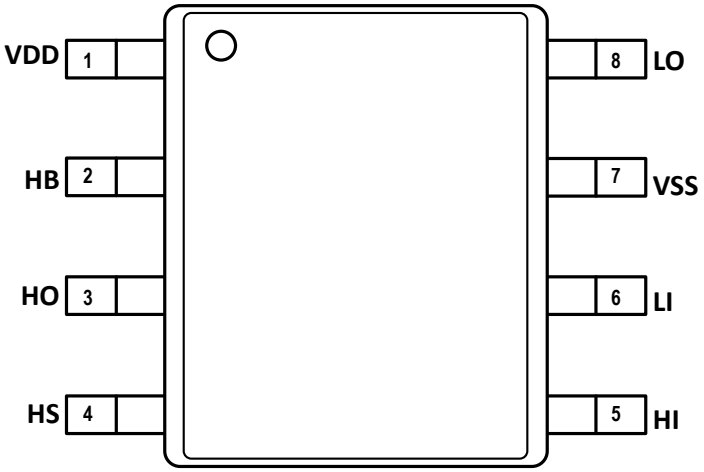


Figure 4-1. D Package 8-Pin SOIC Top View

Table 4-1. Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
VSS	7	–	Ground reference for inputs, VDD, and LO driver return
HB	2	I	High side floating supply. Bypass this pin to HS with a suitable capacitor to sustain bootstrap circuit operation, typically 10 times larger than the MOSFET effective gate capacitance.
HI	5	I	Logic input for high-side driver. If HI is unbiased or floating, HO is held low
HO	3	O	High-side driver output.
HS	4	–	Return for high-side floating supply.
LI	6	I	Logic input for low-side driver. If LI is unbiased or floating, LO is held low.
LO	8	O	Low-side driver output.
VDD	1	P	Bias supply input. Power supply for the input logic side of the device and also low-side driver output. Bypass this pin to VSS with a 1µF SMD capacitor (typically C_{VDD} needs to be 10 × C_{BOOT}).

5 Specifications

5.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted), all voltages are with respect to VSS (unless otherwise noted), currents are positive into and negative out of the specified terminal.(1)

PARAMETER			MIN	MAX	UNIT
V_{HI}, V_{LI}	Input voltages on HI and LI(2)		–0.3	23	V
V_{DD}	VDD supply voltage		–0.3	23	
V_{HB}	Voltage on HB		–0.3	230	
V_{HB}–V_{HS}	Bootstrap supply voltage		–0.3	23	
V_{HO}	Output voltage on HO	DC	HS–0.3	HB+0.3	V
		Transient, less than 100 ns(3)	HS–2	HB+0.3	
V_{LO}	Output voltage on LO	DC	–0.3	VDD+0.3	V
		Transient, less than 100 ns(3)	–2	VDD+0.3	
V_{HS}	Voltage on HS	DC	–18(4)	230	V
		Transient, less than 100 ns(3)	–23(4)	230	V
dV_{HS}/dt	Allowable offset supply voltage transient		–100	100	V/ns
T_J	Junction temperature		–40	150	°C
T_{stg}	Storage temperature		–65	150	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The maximum voltage on the input pins is not restricted by the voltage on the VDD pin.
(3) Values are verified by characterization on bench.
(4) At HB–HS = 15 V.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

All voltages are with respect to VSS, –40°C < TJ < 150°C, currents are positive into, negative out of the specified terminals

			MIN	NOM	MAX	UNIT
V_{DD}	VDD supply voltage		8.5		20	V
V_{HB}–V_{HS}	Bootstrap supply voltage		7.8		20	V
V_{HI}, V_{LI}	Input voltages on HI and LI		0		20	V
V_{HB}	Voltage on HB		3		HS + 20	V
V_{HS}	Voltage on HS	DC	3 – (V_{HB}–V_{HS})		200	V
V_{HS}		Transient, less than 100 ns	–(V_{HB}–V_{HS})		200	V
dV_{HS}/dt	Allowable offset supply voltage transient		–100		100	V/ns
T_A	Ambient temperature		–40		125	°C
T_J	Junction temperature		–40		150	°C

5.4 Thermal Information

THERMAL METRIC(1)		UCC278X4-Q1 (SOIC) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	114.0	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	54.0	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	62.8	°C/W
ψ_{JT}	Junction-to-top characterization parameter	8.5	°C/W
ψ_{JB}	Junction-to-board characterization parameter	61.9	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

5.5 Electrical Characteristics

At VDD=VHB=15V, VSS=VHS=0, all voltages are with respect to VSS, no load on LO and HO, –40°C < T_J < +150°C (unless otherwise noted). Currents are positive into and negative out of the specified terminal.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY BLOCK						
$V_{VDD\ ON}$	Turn-on threshold voltage of VDD		6.9	7.5	8.1	V
$V_{VDD\ OFF}$	Turn-off threshold voltage of VDD		6.4	7.0	7.6	
$V_{VDD\ HYS}$	Hysteresis of VDD			0.5		
$V_{VHB\ ON}$	Turn-on threshold voltage of VHB-VHS		6.2	6.8	7.4	
$V_{VHB\ OFF}$	Turn-off threshold voltage of VHB-VHS		5.7	6.3	6.9	
$V_{VHB\ HYS}$	Hysteresis of VHB-VHS			0.5		
I_{VDDO}	VDD operating current	HI=LI=0 to 5 V, f=500kHz, C_{LOAD} = 0		1100	2000	µA
I_{QVSS}	Quiescent VDD-VSS supply current	HI=LI=0 V or 5 V, DC on/off state		150	300	µA
I_{QBSO}	HB-HS operating supply current	HI=LI=0 to 5 V, f=500kHz, C_{LOAD} = 0		1000	1300	µA
I_{QBS}	Quiescent HB-HS supply current	HI=0 V or 5 V, HO in DC on/off state		90	180	µA
I_{BL}	Bootstrap supply leakage current (HB to VSS)	HB=HS=230 V, VDD=VSS=0 V		0.1	20	µA
INPUT AND ENABLE BLOCK						
V_{INH}	Input Pin (HI, LI,) high threshold		1.7	2.1	2.5	V
V_{INL}	Input Pin (HI, LI,) low threshold		0.7	1.0	1.3	V
V_{INHYS}	Input Pin (HI, LI,) threshold hysteresis			1.1		V
I_{INL}	HI, LI input low bias current	HI, LI=0 V	-5		5	µA
I_{INH}	HI, LI input high bias current	HI, LI=5 V	20		55	µA
R_{HI}	Pull down resistor on HI input pin	HI, LI=5 V	100		200	KΩ
R_{LI}	Pull down resistor on LI input pin	HI, LI=5 V	100		200	KΩ
OUTPUT BLOCK						
V_{DD}-V_{LOH}	LO output high voltage	LI = 5V, I_{LO}=-20mA		250	500	mV
V_{HB}-V_{HOH}	HO output high voltage	HI = 5V, I_{HO}=-20mA		250	500	mV
V_{LOL}	LO output low voltage	LI = 0V, I_{LO}=20mA		20	40	mV
V_{HOL}	HO output low voltage	HI = 0V, I_{HO}=20mA		20	40	mV
R_{LOL}, R_{HOL}	LO, HO output pull-down resistance	I_{LO}=I_{HO}=20mA		1	2	Ω
R_{LOH}, R_{HOH}	LO, HO output pull-up resistance	I_{LO}=I_{HO}=-20mA		12.6	25	
I_{GPK-} (1)	HO, LO output sink current	HI=LI=0V, HO=LO=15V, PW<10us		4		A
I_{GPK+} (1)	HO, LO output source current	HI=LI=5V, HO=LO=0V, PW<10us		3.5		

(1) Ensured by design, not tested in production

5.6 Dynamic Electrical Characteristics

At VDD=VHB=15V, VSS=VHS=0, all voltages are with respect to VSS, no load on LO and HO, –40°C<T_J< +150°C (unless otherwise noted). Currents are positive into and negative out of the specified terminal.

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
PROPAGATION DELAYS						
t_{DLFF}	VLI falling to VLO falling	C_{LOAD} = 0 pF, from V_{INL} of LI to 90% of LO falling		29	45	ns
t_{DHFF}	VHI falling to VHO falling	C_{LOAD} = 0 pF, from V_{INL} of HI to 90% of HO falling		29	45	ns
t_{DLRR}	VLI rising to VLO rising	C_{LOAD} = 0 pF, from V_{INH} of LI to 10% of LO rising		29	45	ns
t_{DHRR}	VHI rising to VHO rising	C_{LOAD} = 0 pF, from V_{INH} of HI to 10% of HO rising		29	45	ns
DELAY MATCHING						
t_{MON}	HI OFF, LI ON	T_J = 25°C, $\lvert t_{DHFF} - t_{DLRR} \rvert$			5	ns
t_{MON}	HI OFF, LI ON	T_J = -40°C to 150°C, $\lvert t_{DHFF} - t_{DLRR} \rvert$			5	ns
t_{MOFF}	LI OFF, HI ON	T_J = 25°C, $\lvert t_{DLFF} - t_{DHRR} \rvert$			5	ns
t_{MOFF}	LI OFF, HI ON	T_J = -40°C to 150°C, $\lvert t_{DLFF} - t_{DHRR} \rvert$			5	ns
OUTPUT RISE AND FALL TIME						
t_{R_LO}	LO rise time	C_{LOAD} = 1000 pF, from 10% to 90%		7.5		ns
t_{R_HO}	HO rise time	C_{LOAD} = 1000 pF, from 10% to 90%		7.5		ns
t_{F_LO}	LO fall time	C_{LOAD} = 1000 pF, from 90% to 10%		6.5		ns
t_{F_HO}	HO fall time	C_{LOAD} = 1000 pF, from 90% to 10%		6.5		ns
MISCELLANEOUS						
t_{ON}	Minimum HI/LI ON pulse that changes output state	0 V to 5 V input signal on HI & LI pins, C_{LOAD} = 1nF		11	20	ns
t_{OFF}	Minimum HI/LI OFF pulse that changes output state	5 V to 0 V input signal on HI & LI pins, C_{LOAD} = 1nF		11	20	ns

5.7 Timing Diagrams

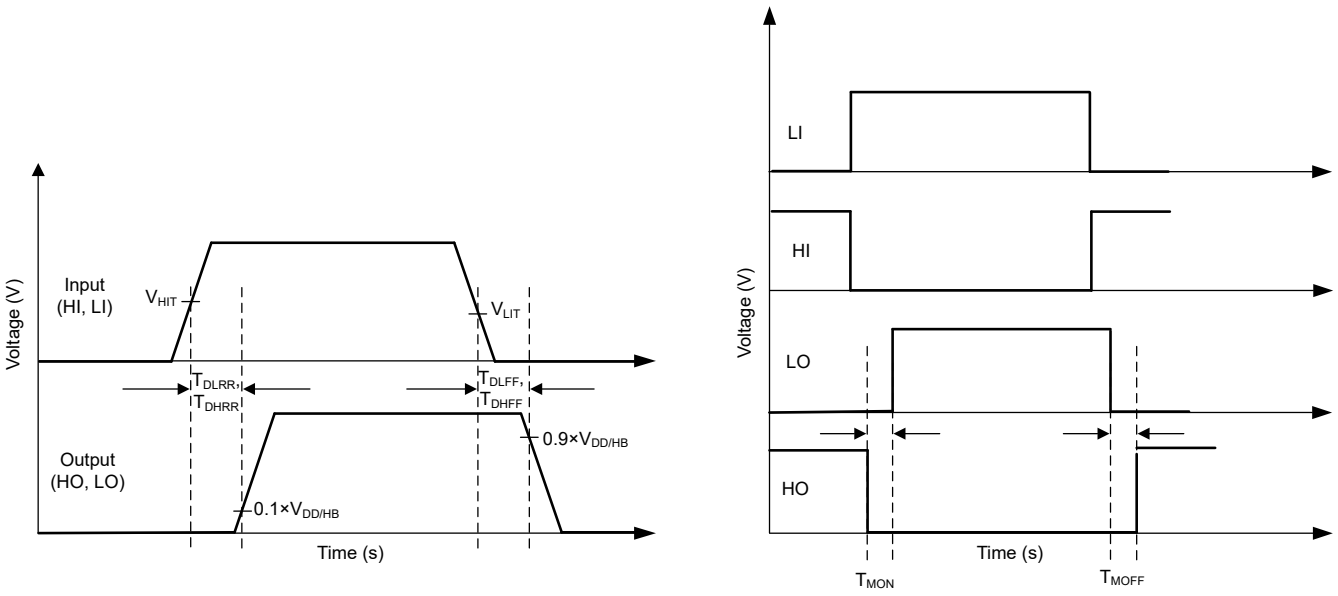


Figure 5-1. Timing Diagrams

5.8 Typical Characteristics

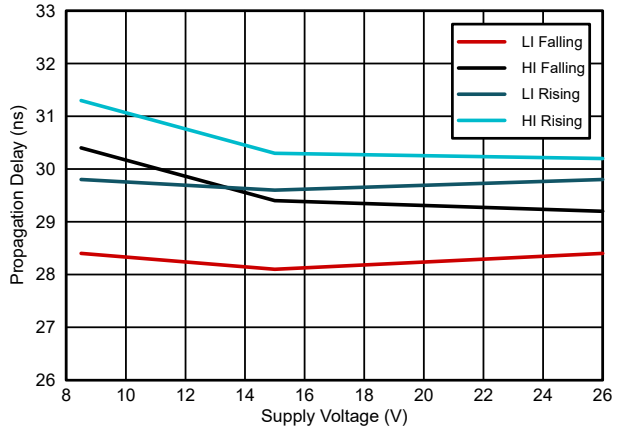


Figure 5-2. Propagation Delay vs Supply Voltage

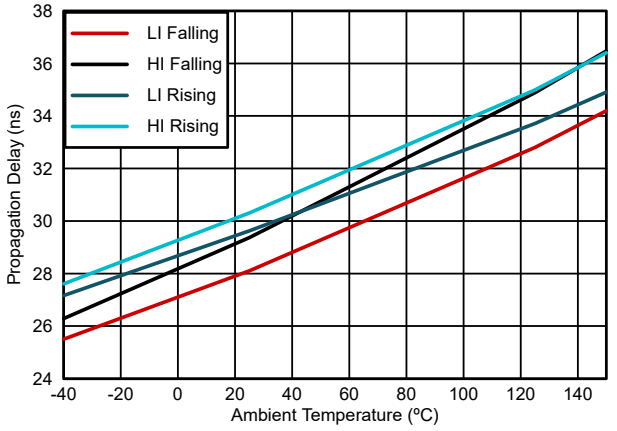


Figure 5-3. Propagation Delay vs Temperature

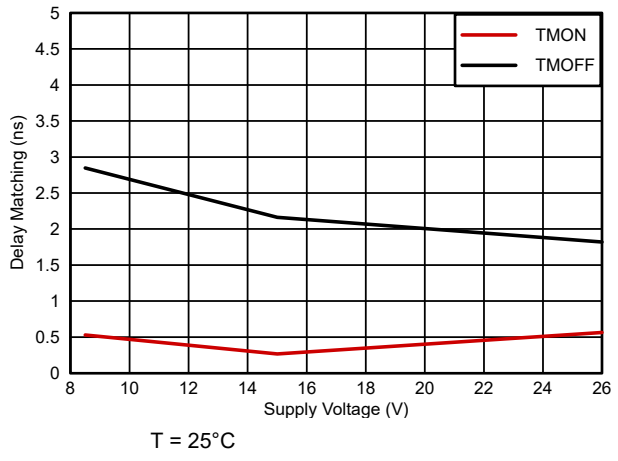


Figure 5-4. Delay Matching vs Supply Voltage

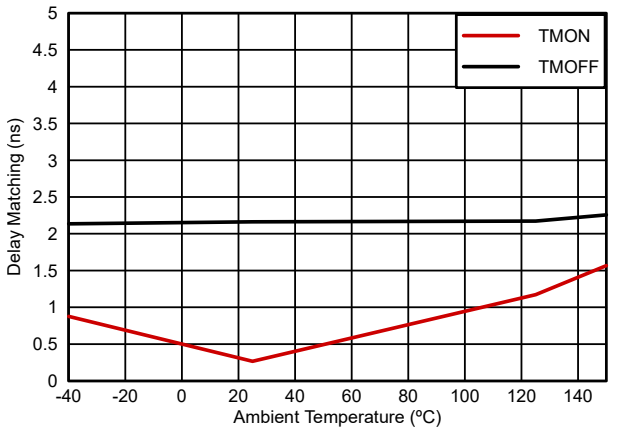


Figure 5-5. Delay Matching vs Temperature

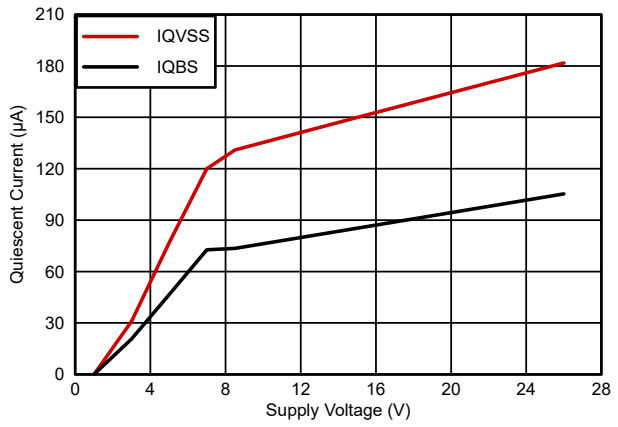


Figure 5-6. Quiescent Supply Current vs Supply Voltage

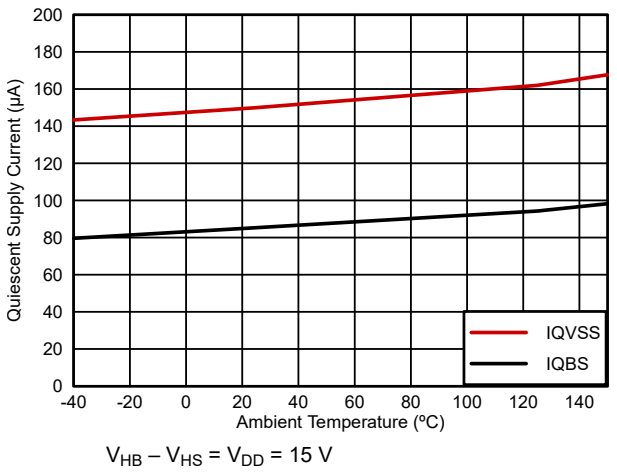
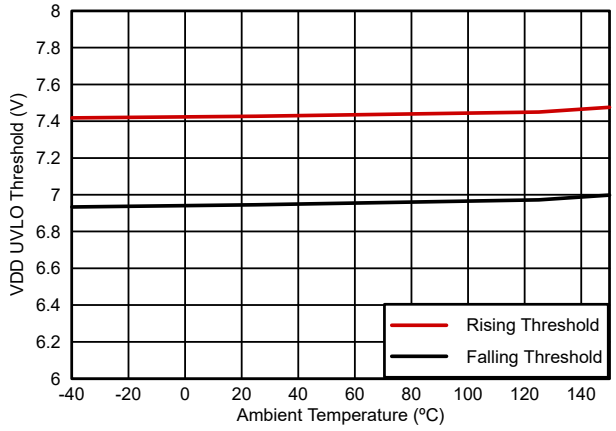


Figure 5-7. Quiescent Supply Current vs Temperature

5.8 Typical Characteristics (continued)



$V_{HB} – V_{HS} = V_{DD} = 15$ V

Figure 5-8. VDD UVLO Thresholds vs Temperature

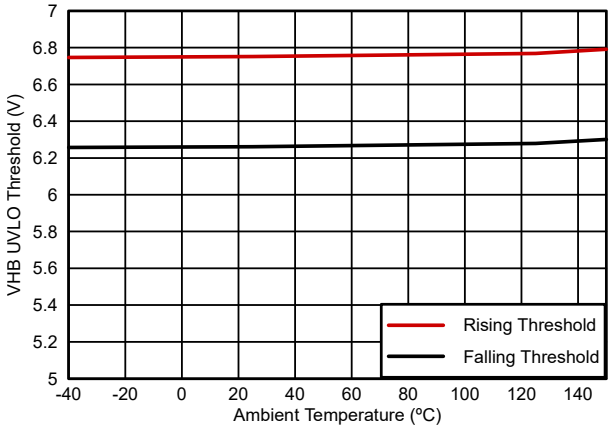


Figure 5-9. VHB UVLO Thresholds vs Temperature

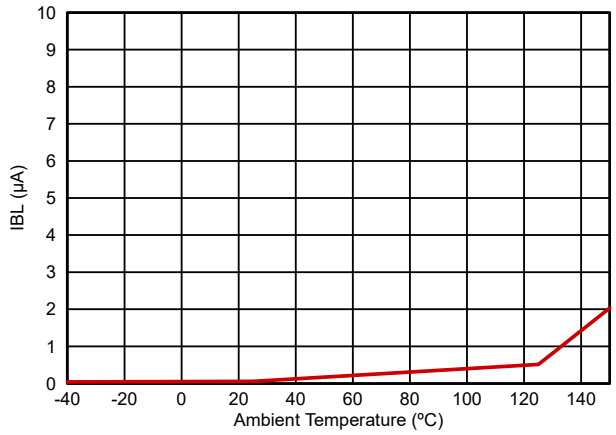
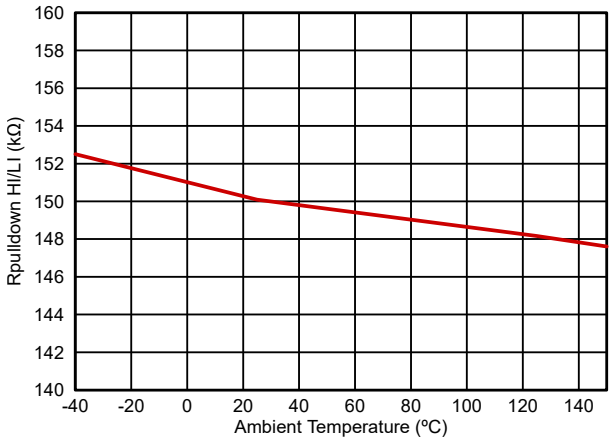
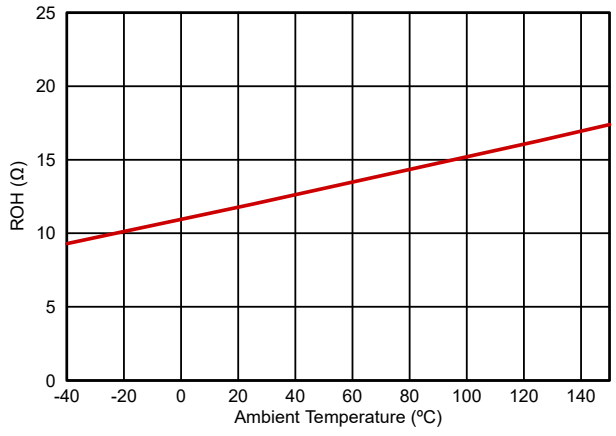


Figure 5-10. HB to VSS Leakage Current vs Temperature



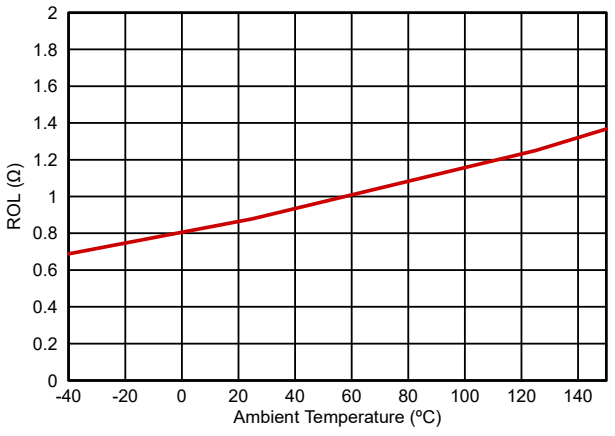
$V_{HB} – V_{HS} = V_{DD} = 15$ V

Figure 5-11. HI and LI Input Pulldown Resistance vs Temperature



$V_{HB} – V_{HS} = V_{DD} = 15$ V

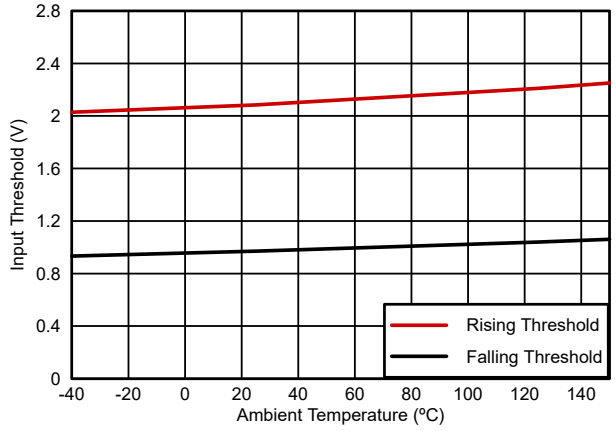
Figure 5-12. LO and HO Pull-up Resistance vs Temperature



$V_{HB} – V_{HS} = V_{DD} = 15$ V

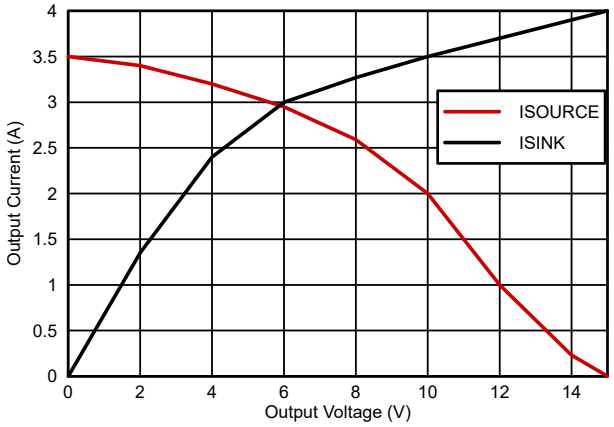
Figure 5-13. LO and HO Pull-down Resistance vs Temperature

5.8 Typical Characteristics (continued)



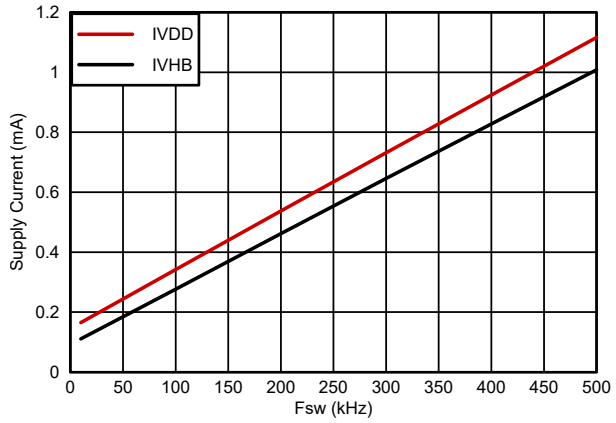
$V_{HB} – V_{HS} = V_{DD} = 15$ V

Figure 5-14. HI and LI Input Voltage Thresholds vs Temperature



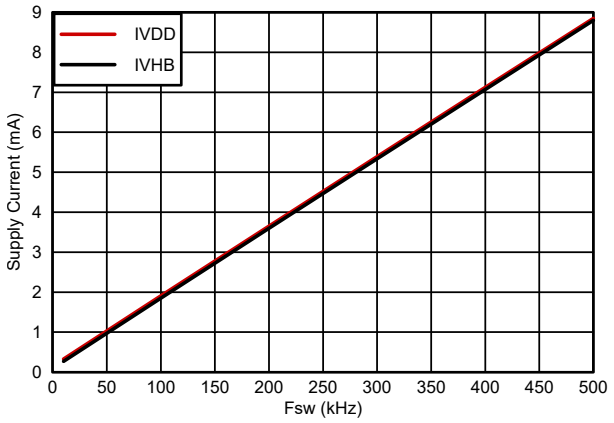
$V_{HB} – V_{HS} = V_{DD} = 15$ V

Figure 5-15. LO and HO Output Current vs Output Voltage



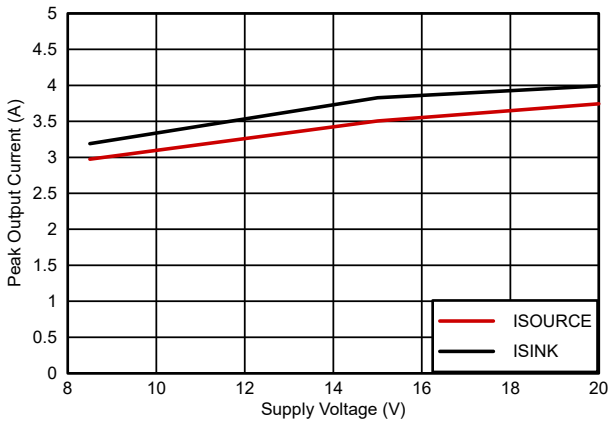
$V_{HB} – V_{HS} = V_{DD} = 15$ V, T = 25°C

Figure 5-16. No Load Supply Current vs Switching Frequency



$V_{HB} – V_{HS} = V_{DD} = 15$ V, T = 25°C, C_L = 1nF

Figure 5-17. Supply Current vs Switching Frequency



T = 25°C

Figure 5-18. LO and HO Peak Output Current vs Supply Voltage

6 Detailed Description

6.1 Overview

High-current, gate-driver devices are required in switching power applications for a variety of reasons. In order to implement fast switching of power devices and reduce associated switching power losses, a powerful gate-driver device is employed between the PWM output of control devices and the gates of the power semiconductor devices. Additionally, gate-driver devices are indispensable when having the PWM controller device directly drive the gates of the switching devices is not feasible. In the case of digital power supply controllers, this situation is often encountered because the PWM signal from the digital controller is often a 3.3V logic signal which is not capable of effectively turning on a power switch.

In bridge topologies, like hard-switched half bridge, hard-switched full bridge, half-bridge and full-bridge LLC, phase-shifted full bridge, and 2-transistor forward, the source and emitter pin of the top-side power MOSFET/ IGBT switch is referenced to a node whose voltage changes dynamically; that is, not referenced to a fixed potential, so floating-driver devices are necessary in these topologies.

The UCC278X4-Q1 is a half-bridge driver dedicated for DC-to-DC power supplies, inverters, and other half-bridge topologies. The high side is a floating driver that can be biased effectively using a bootstrap circuit, and can handle up to 230V. The driver can be used with 100% duty cycle as long as HB-HS can be maintained above UVLO of the high side.

The device features excellent propagation delays and delay matching between both channels aimed at minimizing pulse distortion in high-frequency switching applications. Each channel is controlled by its respective input pins (HI and LI), allowing full and independent flexibility to control on and off state of the output. The UCC278X4-Q1 includes protection features wherein the outputs are held low when inputs are floating or when the minimum input pulse width specification is not met. The driver inputs are CMOS and TTL compatible for easy interface to digital power controllers and analog controllers alike.

6.2 Functional Block Diagram

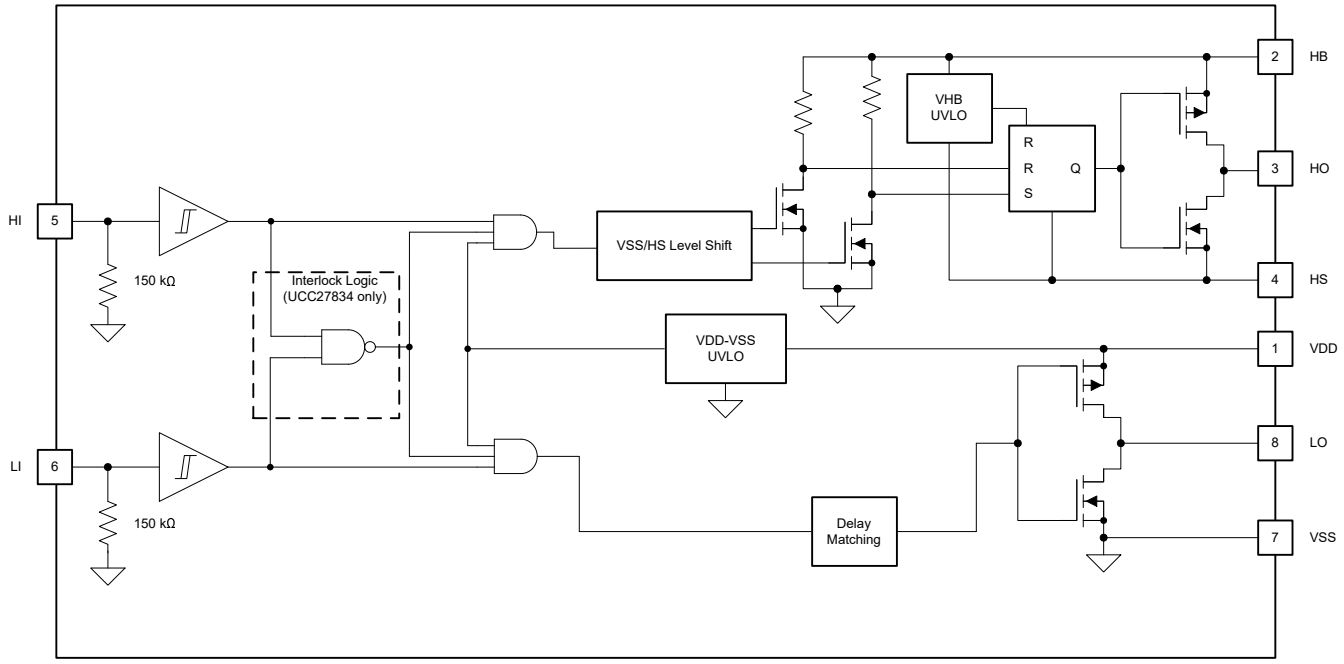


Figure 6-1. UCC278X4-Q1 Block Diagram

6.3 Feature Description

6.3.1 Input Stages and Interlock

The two inputs (HI and LI) operate independently. The independence allows for full control of two outputs compared to the gate drivers that have a single input. The UCC27834-Q1 device has input interlock or cross-conduction protection. Whenever both the inputs are high, the internal logic turns both the outputs (HO and LO) off. Once the device is in this mode, when one of the inputs goes low, the outputs follow the input logic. There is no other fixed time de-glitch filter implemented in the device and therefore propagation delay and delay matching are not sacrificed. In other words, there is no built-in dead-time due to the interlock feature.

The inputs are TTL-logic compatible. The device can also work with CMOS type control signals at its inputs as long as the signals meet the turn-on and turn-off threshold specifications of the device. Because the inputs are independent of supply voltage, they can be connected to outputs of either digital controller or analog controller. The inputs can accept wide slew rate signals and can withstand a wide input voltage range to increase the robustness and flexibility. A small RC filter at the inputs of the driver can further improve system robustness in noise prone applications. The inputs have internal pull down resistors with typical value of 150kΩ. Thus, when the inputs are floating, the outputs are held low.

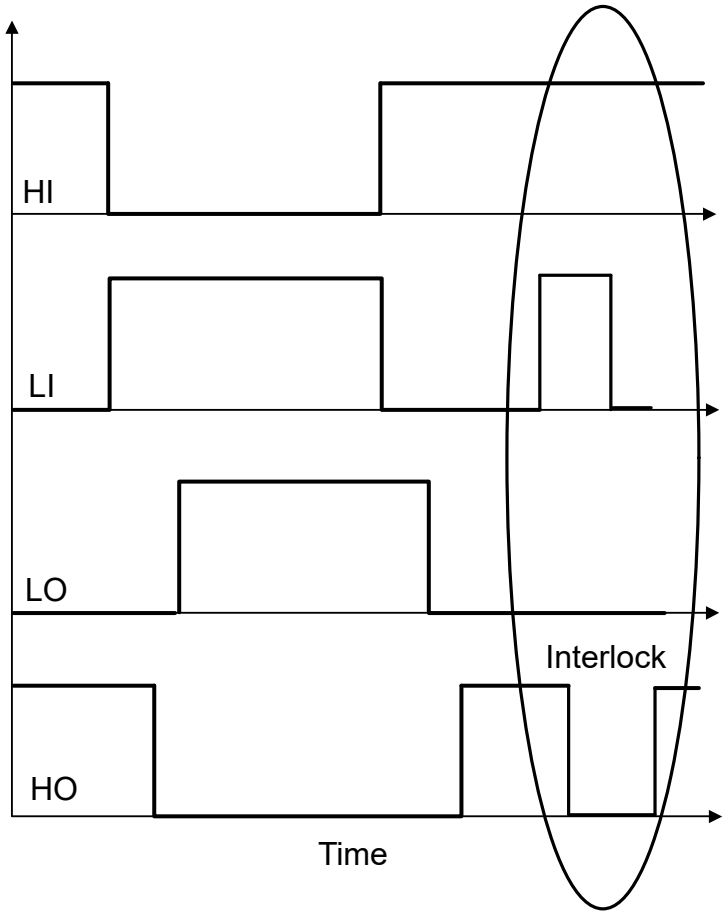


Figure 6-2. Interlock or Input Shoot-Through Protection (UCC27834-Q1)

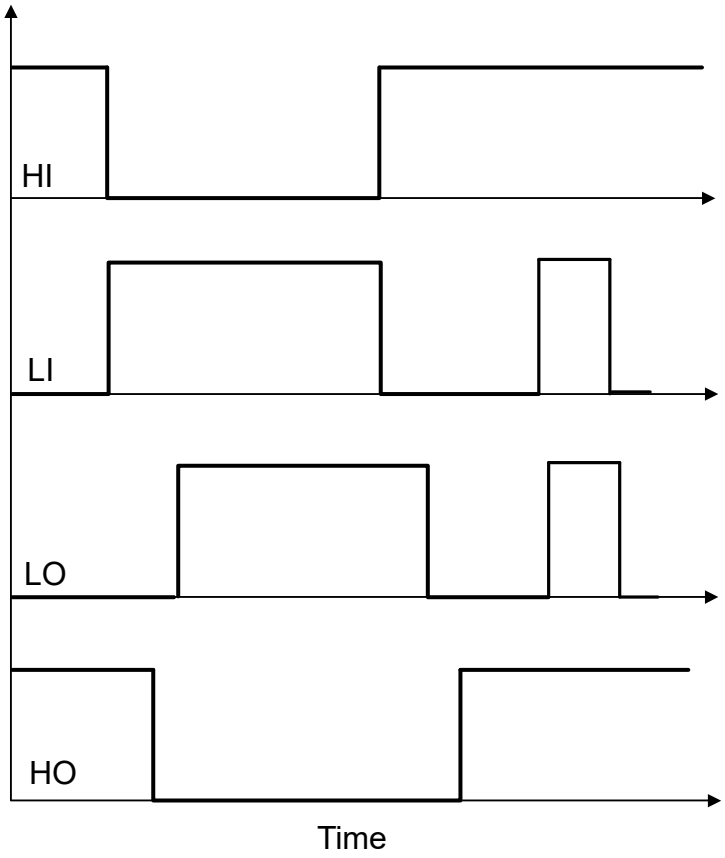


Figure 6-3. No Interlock or Input Shoot-Through Protection (UCC27884-Q1)

6.3.2 Undervoltage Lockout (UVLO)

Both the high-side and the low-side driver stages include UVLO protection circuitry which monitors the supply voltage ($V_{VDD–VSS}$) and the bootstrap capacitor voltage (V_{HB} to V_{HS}). The VDD UVLO circuit inhibits both LO and HO, while the HB UVLO circuit inhibits only HO. The UVLO circuits ensure each output remains low until sufficient supply voltage is available to turn on the external MOSFETs or IGBTs. The built-in UVLO hysteresis prevents chattering during supply voltage variations.

6.3.3 Level Shifter

The level shift circuit (refer to the functional block diagram in Figure 6-1) is the interface from the low-voltage input stage to the high-side driver stage which is referenced to the switch node (HS). The level shift allows control of the HO output referenced to the HS pin and provides excellent delay matching with the low-side driver. The delay matching of the UCC278X4-Q1 is summarized in Figure 5-5 and Figure 5-4.

6.3.4 Output Stage

The UCC278X4-Q1 device output stage features a unique architecture on the pull up structure which delivers the highest peak-source current when it is most needed during the Miller plateau region of the power-switch turn on transition (when the power switch drain or collector voltage experiences dV/dt). The output stage pull-up structure features a P-Channel MOSFET and an additional N-Channel MOSFET in parallel. The function of the N-Channel MOSFET is to provide a brief boost in the peak sourcing current enabling fast turn on. This is accomplished by briefly turning-on the N-Channel MOSFET during a narrow instant when the output is changing state from low to high.

The R_{OH} parameter (see Figure 5-12) is a DC measurement and it is representative of the on-resistance of the P-Channel device only. This is because the N-Channel device is held in the off state in DC condition and is turned on only for a narrow instant when output changes state from low to high.

Note

The effective resistance of the UCC278X4-Q1 pull-up stage during the turn-on instant is much lower than what is represented by R_{OH} parameter.

The pull-down structure in the UCC278X4-Q1 is simply composed of a N-Channel MOSFET. The R_{OL} parameter (see Figure 5-13), which is also a DC measurement, is representative of the impedance of the pull-down stage in the device.

Each output stage in the UCC278X4-Q1 is capable of supplying 3.5A peak source and 4A peak sink current pulses. The output voltage swings between (VDD and VSS) and (HB and HS) providing rail-to-rail operation.

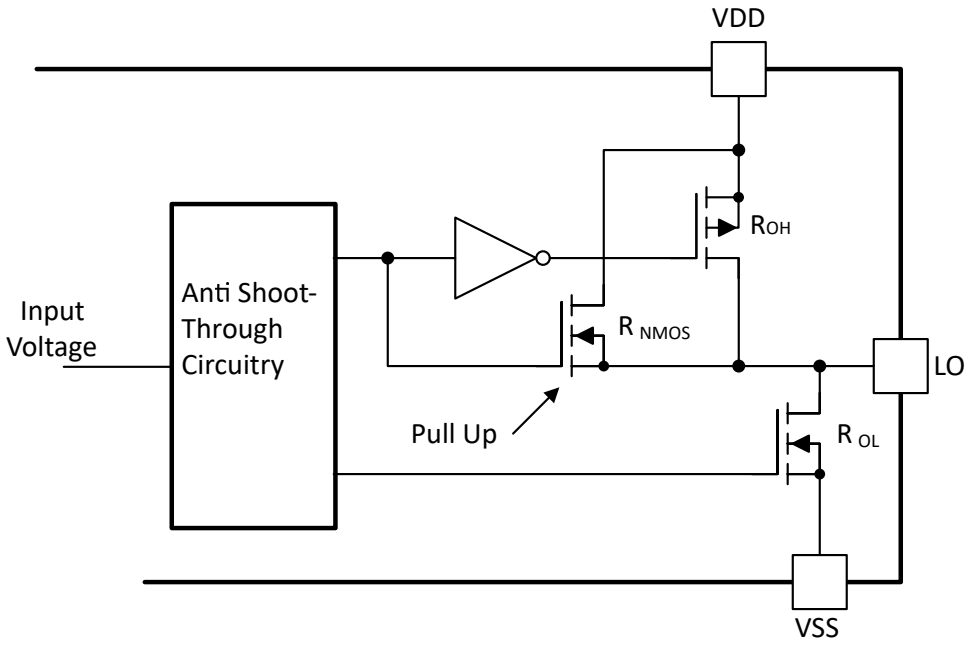


Figure 6-4. Output Stage Structure

6.3.5 Low Propagation Delays and Tightly Matched Outputs

The UCC278X4-Q1 features a fast, 29ns (typical) propagation delay (refer to Figure 5-2 and Figure 5-3) between input and output. The UCC278X4-Q1 also offers well-matched delay between the HO and LO channels (5ns max) enabling more precise dead-time control over operating conditions (refer to Figure 5-4 and Figure 5-5).

6.3.6 HS Node dV/dt

During typical switching operation of a half-bridge driver, the HS (also known as switch node) voltage swings between ground and the bus voltage. The UCC278X4-Q1 is rated to withstand HS transition rates of up to 100V/ns without signal distortion, logic errors, or damage. This level of dV/dt immunity enables UCC278X4-Q1 to operate in faster switching applications and systems using wide-bandgap power devices such as GaN FETs.

6.3.7 Operation Under Negative HS Voltage Condition

A typical half-bridge configuration with the UCC278X4-Q1 is shown in Figure 6-5. There are parasitic inductances in the power circuit from die bonding and pinning in QT/QB and PCB tracks of power circuit, the parasitic inductances are labeled $L_{K1,2,3,4}$.

During switching of HS, the current path of power circuit is changed to current path 2 from current path 1. This is known as current commutation. The current across L_{K3}, L_{K4} and body diode of QB pulls HS lower than VSS, like shown in the waveform in Figure 6-5. However, the UCC278X4-Q1 offers robust operation under these conditions of negative voltage on HS.

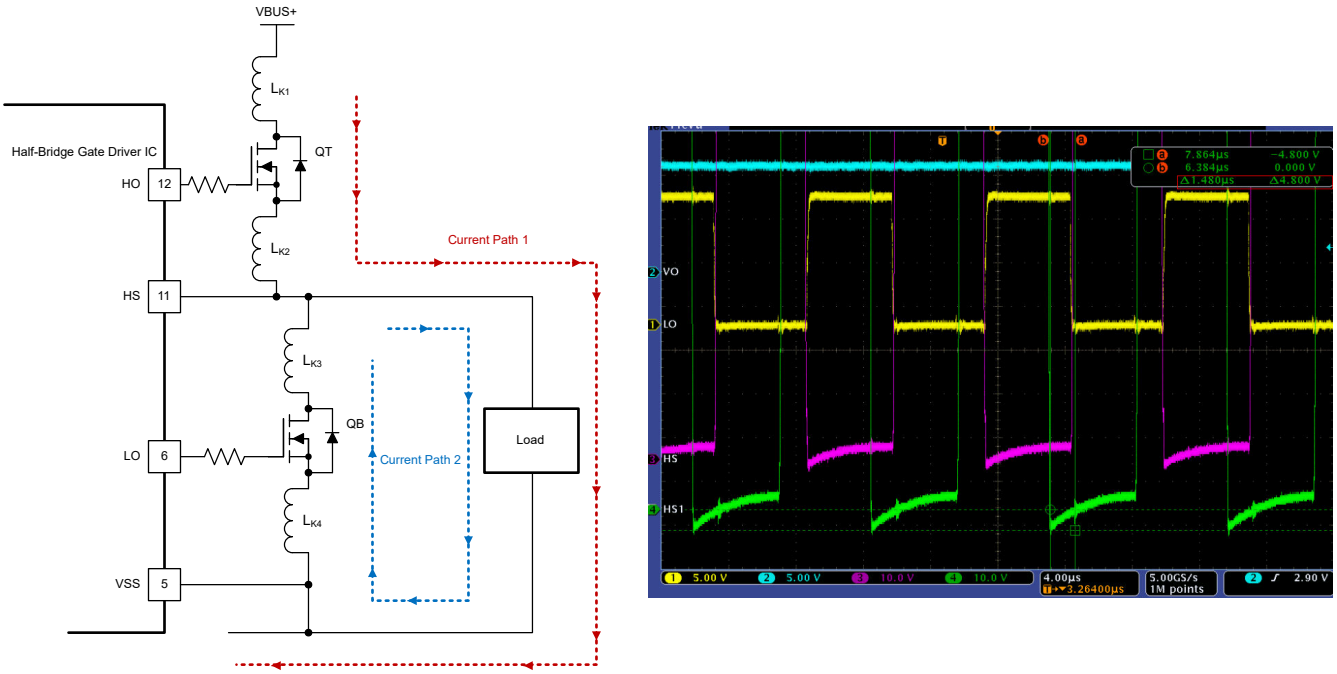


Figure 6-5. HS Negative Voltage In Half-Bridge Configuration

The level shifter circuit is referenced to VSS (refer to Figure 6-1), the voltage from HB to VSS is the supply voltage of the level shifter. When HS is a negative voltage with respect to VSS, the voltage of HB–VSS is decreased, as shown in Figure 6-6. There is a minimum operational supply voltage of the level shifter, if the supply voltage of level shifter is too low, the level shifter cannot pass the HI signal to HO. The minimum supply voltage of the level shifter of the UCC278X4-Q1 is 3V, so the recommended HS specification is dependent on HB-HS. The specification of minimum recommended HS is –9V at HB – HS = 12V.

In general, HS can operate until -9V when HB – HS = 12V. If HB–HS voltage is different, the minimum HS voltage changes accordingly.

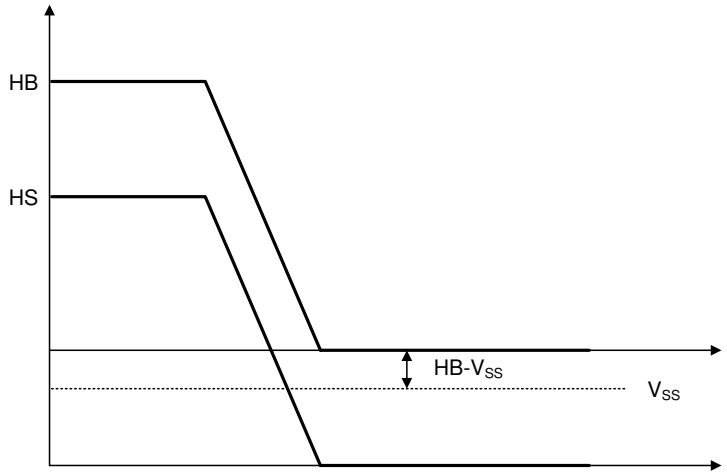


Figure 6-6. Level Shifter Supply Voltage with Negative HS

Note

HO logic operational for HS within –9V to 200V while HB – HS = 12V

The capability of a typical UCC278X4-Q1 device to operate under a negative voltage condition on the HS pin is reported in Figure 6-8. The test method is shown in Figure 6-7.

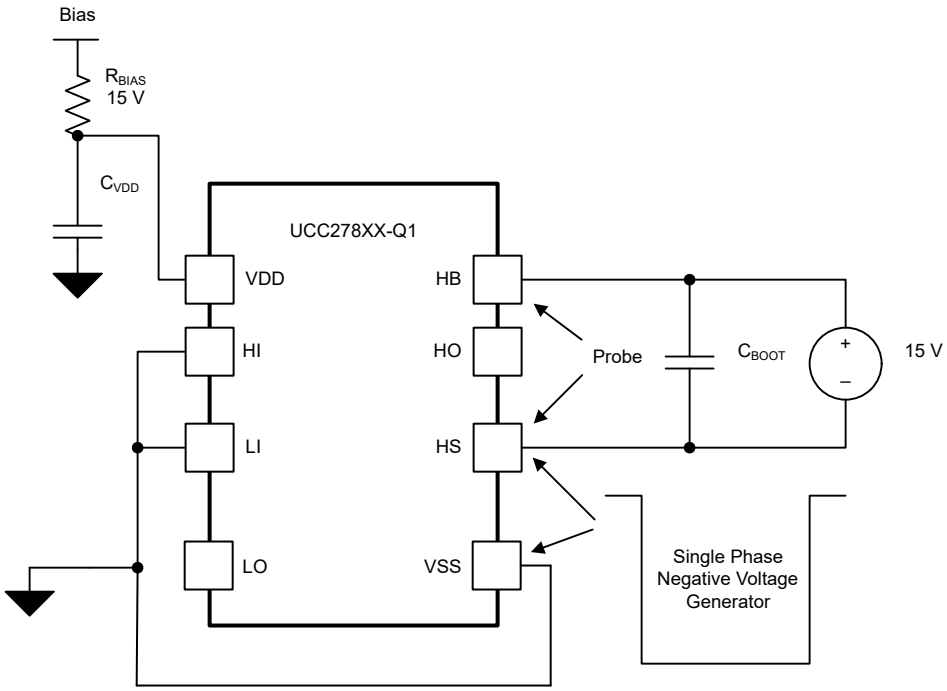


Figure 6-7. Negative Voltage Test Method

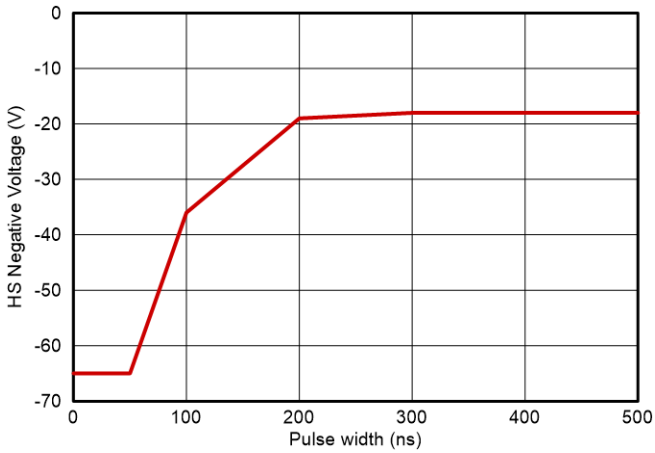


Figure 6-8. NTSOA (Negative Transient Safe Operating Area) Maximum Negative HS Voltage vs Pulse Width

The above curve is a typical curve based on limited units tested at 25°C and at V_{HB} –V_{HS}= 15 V. The curve gives a general guideline as to what negative transients the device can survive, but it is still recommended to limit the negative transients to within the device recommended specifications through layout and design.

6.4 Device Functional Modes

6.4.1 Input and Output Logic Table

The UCC278X4-Q1 features independent inputs, HI and LI, for controlling the state of the outputs, HO and LO, respectively. The device also features interlock functionality on some versions.

Table 6-1. Input/Output Logic Table
(Assuming no UVLO fault condition exists for VDD and VHB)

Inputs		UCC27834-Q1		UCC27884-Q1	
HI	LI	HO	LO	HO	LO
L	L	L	L	L	L
L	H	L	H	L	H
H	L	H	L	H	L
H	H	L	L	H	H

6.4.2 Operation Under 100% Duty Cycle Condition

The UCC278X4-Q1 allows constant on or constant off operation (0% and/or 100% duty cycle) as long as the VDD and VHB bias supplies are maintained above the UVLO thresholds. This is a challenge when bootstrap supplies are used for VHB. A floating bias supply such as an isolated supply or charge pump can be used to achieve 100% duty cycle operation.

7 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Application Information

To quickly switch power devices and reduce associated switching power losses, a gate driver is employed between the PWM output of a controller and the gates of a power semiconductor device. Also, gate drivers are indispensable when it is impossible for the PWM controller to directly drive the gates of the switching devices. With the advent of digital power, this situation will be encountered often because the PWM signal from the digital controller is often a 3.3V logic signal which cannot effectively turn on a power switch. Level shifting circuitry is needed to boost the 3.3V signal to the gate-drive voltage (such as 12V) in order to fully turn on the power device and minimize conduction losses. Traditional buffer drive circuits based on NPN/PNP bipolar transistors in totem-pole arrangement, being emitter follower configurations, prove inadequate with digital power because they lack level-shifting capability.

Gate drivers effectively combine both the level-shifting and buffer-drive functions. Gate drivers also fulfill other needs such as minimizing the effect of high-frequency switching noise by locating the high-current driver physically close to the power switch, and reducing power dissipation and thermal stress in controllers by moving gate charge power losses from the controller into the driver.

7.2 Typical Application

The circuit in Figure 7-1 shows a reference design example with UCC278X4-Q1 driving a typical half-bridge configuration which could be used in several common power converter topologies such as synchronous buck, synchronous boost, half-bridge/full bridge isolated topologies, and motor drive applications.

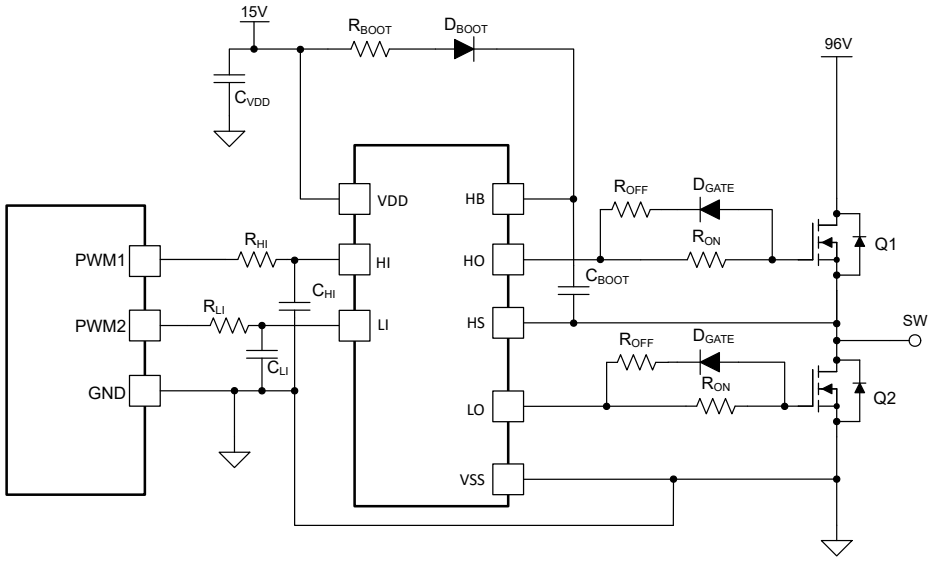


Figure 7-1. Typical Application Schematic

7.2.1 Design Requirements

Table 7-1 shows the reference design parameters for the example application: UCC278X4-Q1 for driving 200V MOSFETs in a high side-low side configuration.

Table 7-1. UCC278X4-Q1 Design Requirements

PARAMETER	VALUE	UNIT
Power Transistor	BSC13DN30NSFD	-
VDD	15	V
Input signal amplitude	3.3	V
Switching Frequency (f_{SW})	100	kHz
DC Link Voltage (V_{HV})	96	V

7.2.2 Detailed Design Procedure

This procedure outlines the steps to design a 200V half-bridge gate driver with 3.5A source and 4.0A sink current capability, targeted to drive power MOSFETs or IGBTs using the UCC278X4-Q1. Refer to Figure 7-1 for component names and network locations.

7.2.2.1 Selecting HI and LI Low Pass Filter Components (R_{HI}, R_{LI}, C_{HI}, C_{LI})

It is good practice to add a small RC filter between the PWM controller and input pin of the UCC278X4-Q1 to filter the high frequency noise, like R_{HI}/C_{HI} and R_{LI}/C_{LI} which is shown in Figure 7-1.

Such a filter should use a R_{HI}/R_{LI} in the range of 10Ω to 100Ω and a C_{HI}/C_{LI} between 10pF and 330pF. In the example, a R_{HI}/R_{LI} = 49.9Ω and a C_{HI}/C_{LI} = 33pF are selected.

7.2.2.2 Selecting Bootstrap Capacitor (C_{BOOT})

The bootstrap capacitor should be sized to have more than enough charge to drive the gate of FET Q1 high, without depleting the bootstrap capacitor more than 10%. A general rule is to size C_{BOOT} to be at least 10 times; as large as the equivalent FET gate capacitance (C_{gs}).

C_g is calculated based on the voltage driving the high side FET gate (V_{Q1g}) and the FET gate charge (Q_g). V_{Q1g} is approximately the bias voltage supplied to VDD subtracted by the forward voltage drop of the bootstrap diode (V_{BOOT}). In this design example, the estimated V_{Q1g} was approximately 14.4 V

$$V_{Q1g} \approx V_{DD} - V_{BOOT} = 14.4\ V \quad (1)$$

The FET used in this example had a specified Q_g of 33nC. Based on Q_g and V_{Q1g} the calculated C_g was 2.3nF.

$$C_g = \frac{Q_g}{V_{Q1g}} = \frac{33\ nC}{14.4\ V} \approx 2.3\ nF \quad (2)$$

Once C_g is estimated, C_{BOOT} should be sized to be at least 10 times larger than C_g.

$$C_{BOOT} \geq 10 \times C_g \geq 23\ nF \quad (3)$$

For this design example a 100nF capacitor was chosen for the bootstrap capacitor.

$$C_{BOOT} = 100\ nF \quad (4)$$

7.2.2.3 Selecting VDD Bypass Capacitor (C_{VDD})

The VDD capacitor (C_{VDD}) should be chosen to be at least 10 times larger than C_{BOOT} so there is minimal voltage drop on the VDD capacitor when charging the boot capacitor . For this design example a 1µF capacitor was selected.

$$C_{VDD} \geq 10 \times C_{BOOT} = 1\ \mu F \quad (5)$$

7.2.2.4 Selecting Bootstrap Resistor (R_{BOOT})

The optional resistor R_{BOOT} is selected to limit the current in D_{BOOT} and limit the ramp up slew rate of voltage of $V_{HB–HS}$. For this design, we selected a current limiting resistor of 2.2Ω. The bootstrap diode current ($I_{BOOT(pk)}$) was limited to roughly 6.5A.

$$R_{BOOT} = 2.2\ \Omega \quad (6)$$

$$I_{BOOT(pk)} = \frac{V_{DD} - V_{BOOT}}{R_{BOOT}} = \frac{15\ V - 0.6\ V}{2.2\ \Omega} \approx 6.5\ A \quad (7)$$

The power dissipation capability of the bootstrap resistor is important. The bootstrap resistor must be able to withstand the short period of high power dissipation during the initial charging sequence of the bootstrap capacitor. This energy is equivalent to 1/2 × C_{BOOT} × V^2. This energy is dissipated during the charging time of the bootstrap capacitor (~3 × R_{BOOT} × C_{BOOT}). Special attention must be paid to use a larger size R_{BOOT} when a larger value of C_{BOOT} is chosen.

7.2.2.5 Selecting Gate Resistor R_{ON}/R_{OFF}

The Gate resistors R_{ON} and R_{OFF} are sized to reduce ringing caused by parasitic inductances and capacitances and also to limit the current coming out of the gate driver. For this design 3Ω R_{ON} and 1Ω R_{OFF} resistors were selected.

- R_{ON}/R_{OFF}: External gate resistors
- V_{BOOT}: Forward voltage drop of external bootstrap diode
- V_{GDF}: Forward voltage drop of external antiparallel diode
- R_{OL}/R_{OH}: Gate driver pulldown/pullup resistance from datasheet
- R_{NMOS}: Effective resistance of pullup NMOS in hybrid structure
- R_{G_int}: Power transistor internal gate resistance, found in power transistor datasheet

Maximum HO Drive Current ($I_{HO(src)}$):

$$I_{HO(src)} = \min\left(3.5A, \frac{V_{DD} - V_{BOOT}}{(R_{NMOS} \parallel R_{OH}) + R_{ON} + R_{G\_int}}\right) = \frac{15\ V - 0.6\ V}{(3.1\ \Omega \parallel 12.6\ \Omega) + 3\ \Omega + 3.3\ \Omega} \approx 1.6\ A \quad (8)$$

Maximum HO Sink Current ($I_{HO(sk)}$):

$$I_{HO(sk)} = \min\left(4A, \frac{V_{DD} - V_{BOOT} - V_{GDF}}{R_{OL} + (R_{ON} \parallel R_{OFF}) + R_{G\_int}}\right) = \frac{15\ V - 0.6\ V - 0.6\ V}{1\ \Omega + (3\ \Omega \parallel 1\ \Omega) + 3.3\ \Omega} \approx 2.7\ A \quad (9)$$

Maximum LO Drive Current ($I_{LO(src)}$):

$$I_{LO(src)} = \min\left(3.5A, \frac{V_{DD}}{(R_{NMOS} \parallel R_{OH}) + R_{ON} + R_{G\_int}}\right) = \frac{15\ V}{(3.1\ \Omega \parallel 12.6\ \Omega) + 3\ \Omega + 3.3\ \Omega} \approx 1.7\ A \quad (10)$$

Maximum LO Sink Current ($I_{LO(sk)}$):

$$I_{LO(sk)} = \min\left(4A, \frac{V_{DD} - V_{GDF}}{R_{OL} + (R_{ON} \parallel R_{OFF}) + R_{G\_int}}\right) = \frac{15\ V - 0.6\ V}{1\ \Omega + (3\ \Omega \parallel 1\ \Omega) + 3.3\ \Omega} \approx 2.9\ A \quad (11)$$

The external gate driver resistors, R_{ON} and R_{OFF}, are used to:

1. Limit ringing caused by parasitic inductances/capacitances in the gate drive loop.
2. Limit ringing caused by high voltage/current switching dV/dt, dI/dt, and body-diode reverse recovery.
3. Fine-tune gate drive strength, for example peak sink and source current to optimize the switching loss.
4. Reduce electromagnetic interference (EMI) related to switching.

7.2.2.6 Selecting Bootstrap Diode

A fast recovery diode should be chosen to avoid reverse recovery losses from discharging the bootstrap capacitor. Thus, a fast reverse recovery time t_{RR}, low forward voltage V_F and low junction capacitance is recommended.

7.2.2.7 Estimate the UCC278X4-Q1 Power Losses

The power losses of the UCC278X4-Q1 ($P_{UCC278X4-Q1}$) are estimated by calculating losses from several components.The combined power losses due to quiescent current (I_{QDD}, I_{QBS}) and no-load switching are calculated below:

$$P_{QC} = V_{DD} \times \left(I_{VDD(100\ kHz)} + I_{VHB(100\ kHz)}\right) = 15\ V \times (330\ \mu A + 275\ \mu A) \approx 9\ mW \quad (12)$$

Refer to Figure 5-16 to find I_{VDD} and I_{VHB}.

Dynamic losses incurred due to the gate charge while driving the FETs Q1 and Q2 are calculated below. Please note that this component typically dominates over the dynamic losses related to the internal VDD and VHB switching logic circuitry in the UCC278X4-Q1.

$$P_{QG1,\,QG2} = 2 \times V_{DD} \times Q_G \times f_{SW} = 2 \times 15\ V \times 33\ nC \times 100\ kHz \approx 99\ mW \quad (13)$$

The dynamic losses are shared between the internal pullup and pulldown resistance of the gate driver IC, the external gate resistance, and the internal gate resistance of the switching device. The pullup resistance changes dynamically during switching, so using R_{OH} provides for an overestimate of the gate driver power dissipation, which provides for design margin.

$$P_{GD} = \frac{P_{QG1,\,QG2}}{2} \times \left(\frac{R_{OH}}{R_{OH} + R_{ON} + R_{G\_int}} + \frac{R_{OL}}{R_{OL} + (R_{ON} \parallel R_{OFF}) + R_{G\_int}} \right) \quad (14)$$

$$P_{GD} = \frac{99\ mW}{2} \times \left(\frac{12.6\ \Omega}{12.6\ \Omega + 3\ \Omega + 3.3\ \Omega} + \frac{1\ \Omega}{1\ \Omega + (3\ \Omega \parallel 1\ \Omega) + 3.3\ \Omega} \right) \approx 43\ mW \quad (15)$$

The total power losses in the gate driver IC for this example are calculated below:

$$P_{Total\_GD} \approx P_{QC} + P_{GD} = 9\ mW + 43\ mW \approx 0.052\ W \quad (16)$$

7.2.3 Application Curves

Figure 7-2 and Figure 7-3 show the measured LI to LO turn-on and turn-off delay of one UCC278X4-Q1 device. Channel 3 depicts LI and Channel 2 depicts LO.

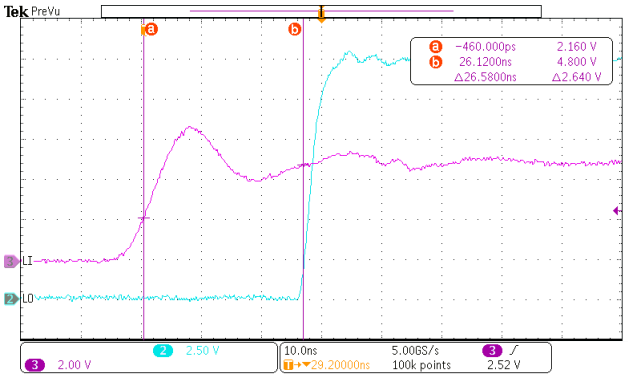


Figure 7-2. LI to LO Turn-On Propagation Delay

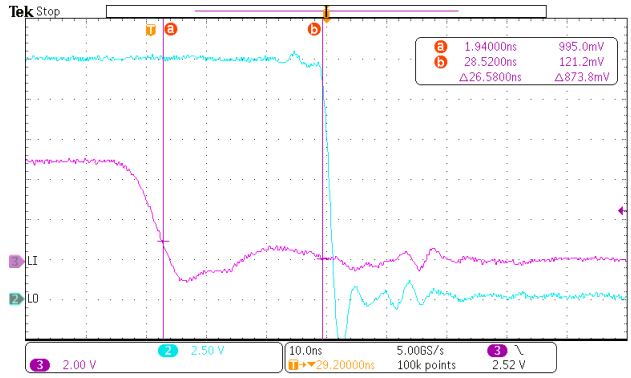


Figure 7-3. LI to LO Turn-Off Propagation Delay

Figure 7-4 and Figure 7-5 show the measured HI to HO turn-on and turn-off delay of one UCC278X4-Q1 device. Channel 3 depicts HI and Channel 2 depicts HO.

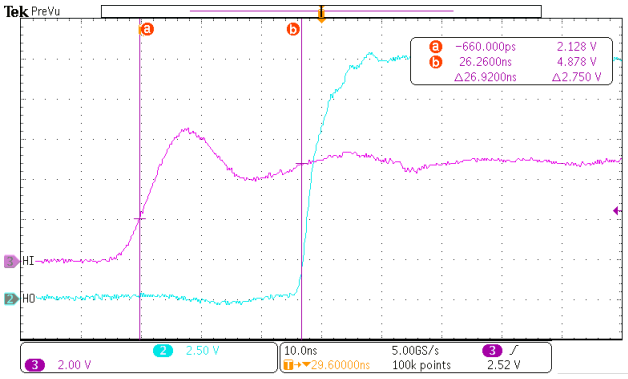


Figure 7-4. HI to HO Turn-On Propagation Delay

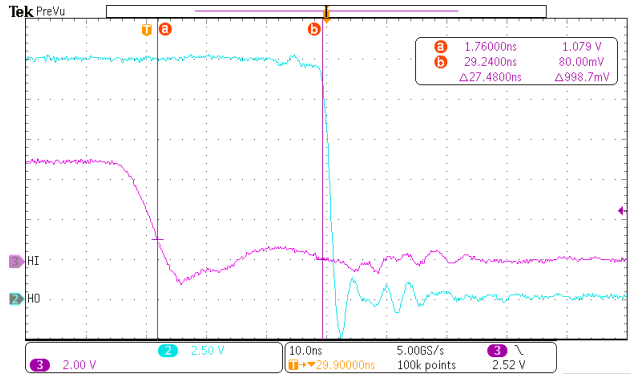


Figure 7-5. HI to HO Turn-Off Propagation Delay

7.3 Power Supply Recommendations

Because the UCC278X4-Q1 is a 3.5A, peak-current driver, it requires the placement of low-esr noise-decoupling capacitance as close as possible from the VDD terminal to the VSS terminal to ensure a stable supply during switching. Ceramic capacitors with stable dielectric characteristics over temperature are recommended, such as X7R or better. Additionally, a larger electrolytic capacitor may also be added in parallel to act as an energy storage capacitor, especially in systems with large gate charge.

The recommended electrolytic capacitor is a 22µF, 50V capacitor. The recommended decoupling capacitors are a 1µF 0805-sized 50V X7R capacitor, ideally with (but not essential) a second smaller parallel 100nF 0603-sized 50V X7R capacitor.

Similarly, a low-esr X7R capacitance is recommended for the HB-HS power terminals which must be placed as close as possible to device pins.

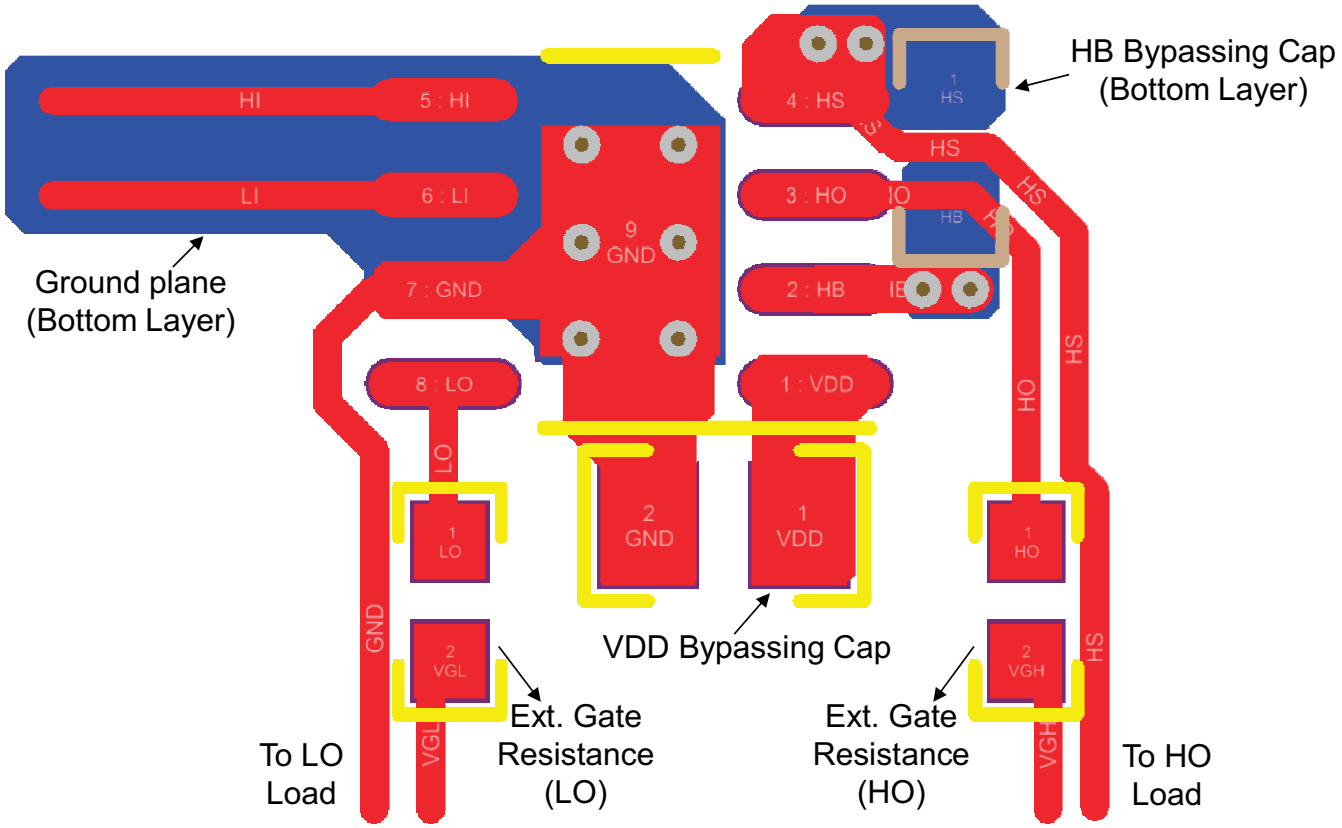
7.4 Layout

7.4.1 Layout Guidelines

- Locate the UCC278X4-Q1 as close as possible to the MOSFETs in order to minimize the length of high-current traces between the HO/LO and the Gates of MOSFETs, as well as the return current path to the driver HS and VSS from the Source/Emitter of the MOSFETs.
- Locate the VDD capacitor (C_{VDD}) and VHB capacitor (C_{BOOT}) as close as possible to the pins of the UCC278X4-Q1.
- A 2Ω to 5Ω resistor in series with the bootstrap diode is recommended to limit bootstrap current.
- An RC filter with 1Ω to 51Ω resistance and 10pF to 390pF capacitance for HI/LI is recommended.
- Avoid LI and HI (driver input) traces placed close to the HS node or any other high dV/dt traces that can induce significant noise into the relatively high impedance leads.
- Separate power traces and signal traces, such as output and input signals.
- Ensure there is not high switching current flowing in the control ground (input signal reference) from the power train ground.

7.4.2 Layout Example

Figure 7-6. UCC278X4-Q1 Layout Example



8 Device and Documentation Support

8.1 Device Support

8.1.1 Third-Party Products Disclaimer

TI'S PUBLICATION OF INFORMATION REGARDING THIRD-PARTY PRODUCTS OR SERVICES DOES NOT CONSTITUTE AN ENDORSEMENT REGARDING THE SUITABILITY OF SUCH PRODUCTS OR SERVICES OR A WARRANTY, REPRESENTATION OR ENDORSEMENT OF SUCH PRODUCTS OR SERVICES, EITHER ALONE OR IN COMBINATION WITH ANY TI PRODUCT OR SERVICE.

8.2 Documentation Support

8.2.1 Related Documentation

Using the UCC27288EVM

8.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

8.5 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

8.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.7 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
September 2025	*	Initial Release

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
UCC27834QDRQ1	Active	Production	SOIC (D) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 150	U7834Q

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

OTHER QUALIFIED VERSIONS OF UCC27834-Q1 :

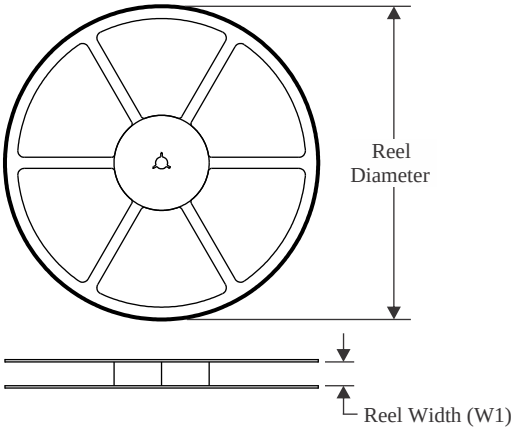
- Catalog : UCC27834

NOTE: Qualified Version Definitions:

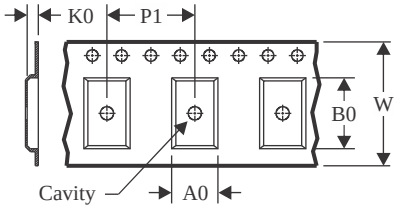
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

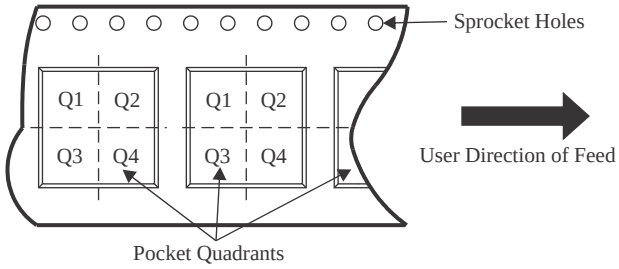


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

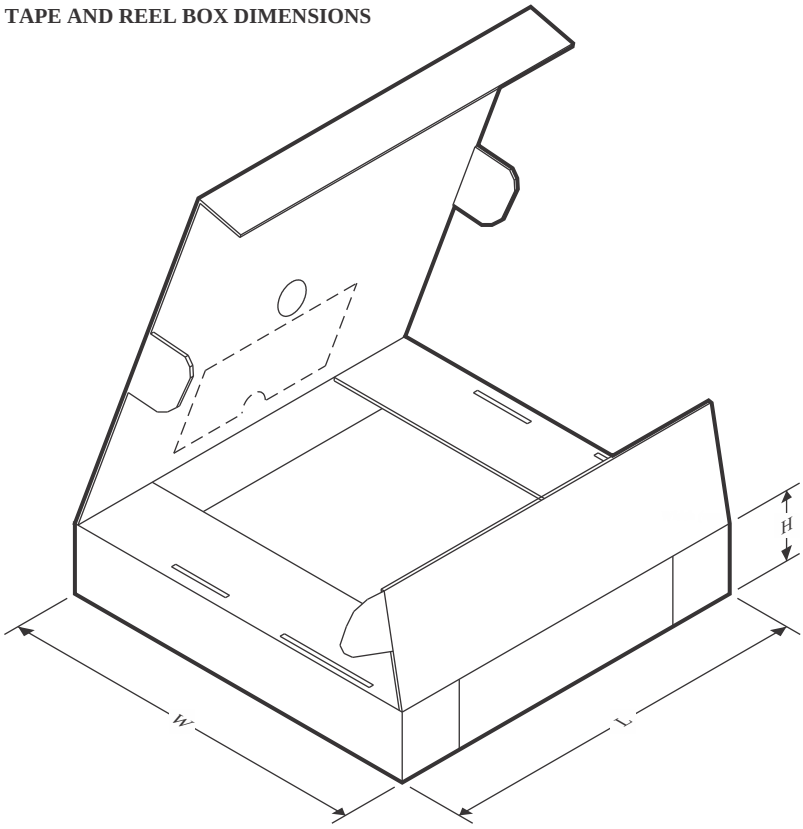
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

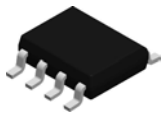
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UCC27834QDRQ1	SOIC	D	8	3000	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UCC27834QDRQ1	SOIC	D	8	3000	353.0	353.0	32.0

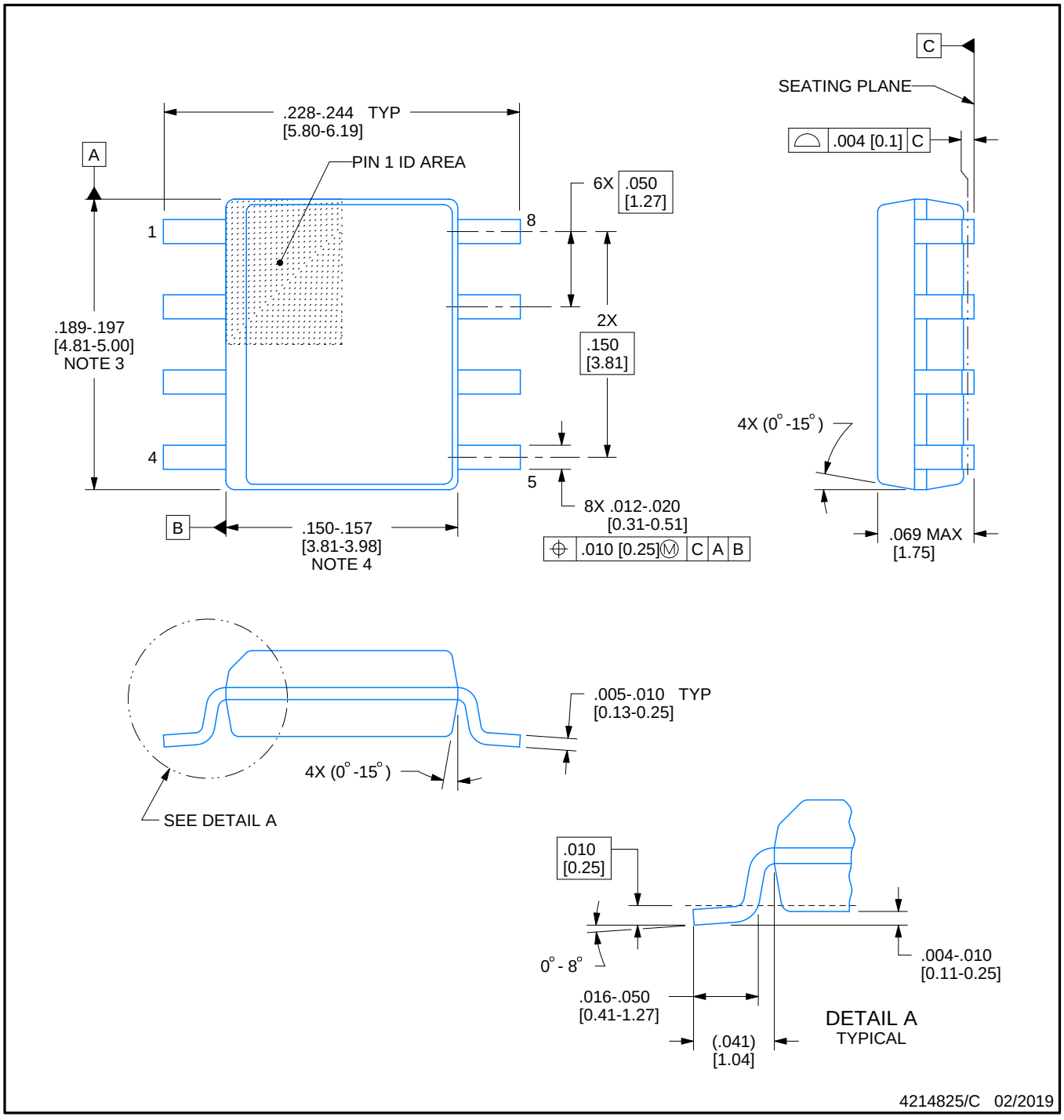


PACKAGE OUTLINE

D0008A

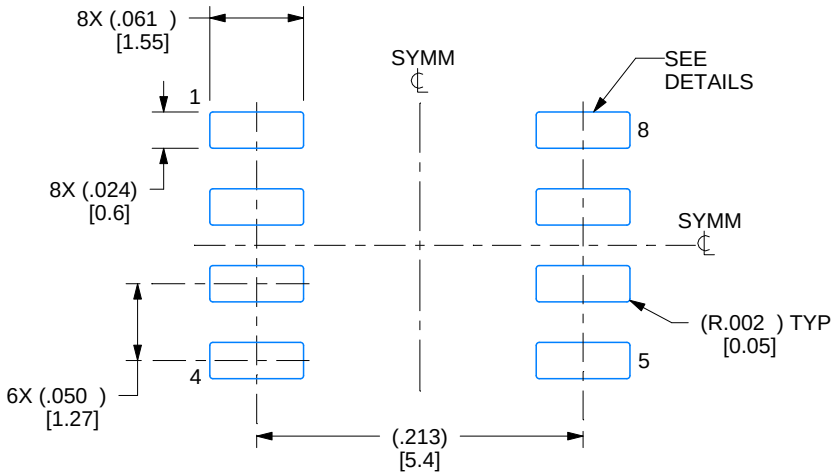
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

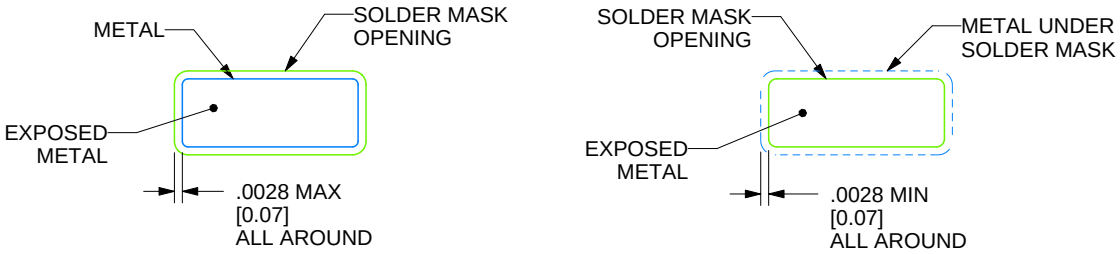


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

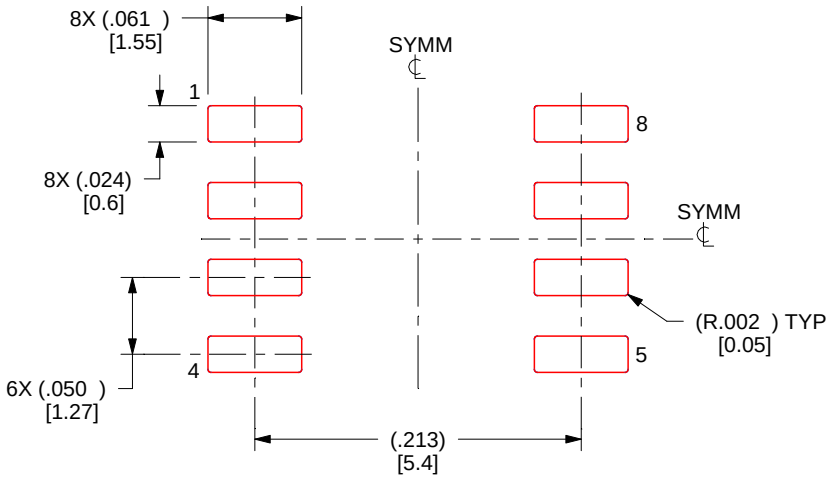
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265