



UCC2751xA-Q1 Single-Channel High-Speed Low-Side Gate Driver With Negative Input Voltage Capability

1 Features

- Qualified for Automotive Applications
- AEC-Q100 Qualified With the Following Results:
 - Device Automotive Qualified Grade 1: -40°C to $+125^{\circ}\text{C}$ Ambient Operating Temperature Range
 - Device HBM ESD Classification Level 2
 - Device CDM ESD Classification Level C6
- Low-Cost Gate-Driver Device Offering Superior Replacement of NPN and PNP Discrete Solutions
- Pin-to-Pin Compatible With TI's [TPSS2828-Q1](#) and the [TPS2829-Q1](#)
- 4-A Peak Source and 4-A Peak Sink Symmetrical Drive
- Fast Propagation Delays (17-ns typical)
- Fast Rise and Fall Times (8-ns and 7-ns typical)
- 4.5-V to 18-V Single Supply Range
- Outputs Held Low During VDD UVLO (Ensures Glitch-Free Operation at Power-Up and Power-Down)
- CMOS Input Logic Threshold (Function of Supply Voltage With Hysteresis)
- Hysteretic Logic Thresholds for High Noise Immunity
- EN Pin for Enable Function (Allowed to be no Connect)
- Ability to Support Negative Voltages (-5 V) at Input and Enable pins
- Output Held Low when Input Pins are Floating
- Input Pin Absolute Maximum Voltage Levels Not Restricted by VDD Pin Bias Supply Voltage
- Operating Temperature Range of -40°C to 140°C
- 5-Pin DBV Package (SOT-23)

2 Applications

- Automotive
- Switch-Mode Power Supplies
- DC-to-DC Converters
- Companion Gate Driver Devices for Digital Power Controllers
- Solar Power, Motor Control, UPS
- Gate Driver for Emerging Wide Band-Gap Power Devices (such as GaN)

3 Description

The UCC2751xA-Q1 single-channel high-speed low-side gate driver devices effectively drive MOSFET and IGBT power switches. With a design that inherently minimizes shoot-through current, the UCC2751xA-Q1 family of devices sources and sinks high, peak-current pulses into capacitive loads offering rail-to-rail drive capability and extremely small propagation delay typically 17 ns.

The UCC2751xA-Q1 family of devices provides 4-A source, 4-A sink (symmetrical drive) peak-drive current capability at $V_{DD} = 12\text{ V}$.

The UCC2751xA-Q1 family of devices operates over a wide VDD range of 4.5 V to 18 V and wide temperature range of -40°C to 140°C . Internal undervoltage lockout (UVLO) circuitry on VDD pin holds output low outside VDD operating range. The ability to operate at low voltage levels such as below 5 V, along with best in class switching characteristics, is especially suited for driving emerging wide band-gap power switching devices such as GaN power-semiconductor devices.

The input pin threshold of the UCC2751xA-Q1 family of devices is based on CMOS logic where the threshold voltage is a function of the VDD supply voltage. Typically, the input high threshold (V_{IN-H}) is 55% V_{DD} and the input low threshold (V_{IN-L}) is 39% V_{DD} . Wide hysteresis (16% V_{DD} typically) between the high and low thresholds offers excellent noise immunity and allows users to introduce delays using RC circuits between the input PWM signal and the INx pin of the device.

Device Information⁽¹⁾

PART NUMBER	PACKAGE	BODY SIZE (NOM)
UCC27518A-Q1	SOT-23 (5)	2.90 mm x 1.60 mm
UCC27519A-Q1		

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Typical Application Diagram

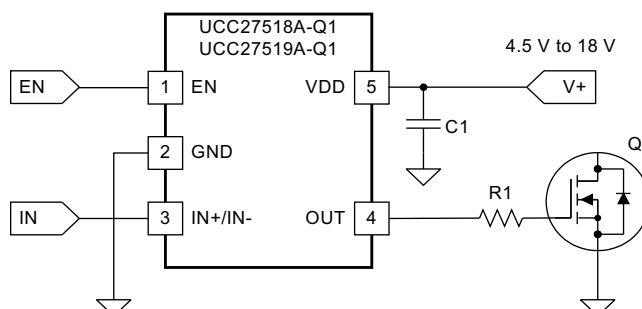


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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (September 2013) to Revision B	Page
• Added <i>ESD Ratings</i> table, <i>Feature Description</i> section, <i>Device Functional Modes</i> , <i>Application and Implementation</i> section, <i>Power Supply Recommendations</i> section, <i>Layout</i> section, <i>Device and Documentation Support</i> section, and <i>Mechanical, Packaging, and Orderable Information</i> section	1
• Changed the OUT (OUTA, OUTB) voltage parameter to show values for DC and repetitive pulse in the <i>Absolute Maximum Ratings</i> table	5
• Changed the minimum value of IN+, IN–, and EN pins from –0.3 V to –6 V in the <i>Absolute Maximum Ratings</i> table	5
• Updated the startup current parameter for the bias current in the <i>Electrical Characteristics</i> table	6
• Moved timing and switching parameters into new <i>Switching Characteristics</i> table	7

Changes from Original (August 2013) to Revision A	Page
• Changed document status from <i>Product Preview</i> to <i>Production Data</i>	1

5 Description (continued)

The UCC2751xA-Q1 family of devices also features a floatable enable function on the EN pin. The EN pin can be left in a no-connect condition, which allows pin-to-pin compatibility between the UCC2751xA-Q1 family of devices and the TPS2828-Q1 or TPS2829-Q1 device, respectively. The enable pin threshold is a fixed voltage threshold and does not vary based on V_{DD} pin bias voltage. Typically, the enable high threshold (V_{EN-H}) is 2.1 V and the enable low threshold (V_{EN-L}) is 1.25 V.

6 Device Comparison Table

The UCC2751x family of gate-driver products ([Table 1](#)) represent Texas Instruments' latest generation of single-channel, low-side high-speed gate driver devices featuring high-source and sink current capability, industry best-in-class switching characteristics, and a host of other features ([Table 2](#)) all of which combine to ensure efficient, robust, and reliable operation in high-frequency switching power circuits.

Table 1. UCC2751x Product Family Summary

PART NUMBER ⁽¹⁾	PACKAGE	PEAK CURRENT (SOURCE, SINK)	INPUT THRESHOLD LOGIC
UCC27511DBV UCC27511ADBQ1	SOT-23, 6 pin	4 A, 8 A (Asymmetrical Drive)	CMOS and TTL-Compatible (low voltage, independent of VDD bias voltage)
UCC27512DRS	3-mm × 3-mm WSON, 6 pin		
UCC27516DRS	3-mm × 3-mm WSON, 6 pin		
UCC27517DBV UCC27517ADBQ1 UCC27517ADBQ1	SOT-23, 5 pin	4 A, 4 A (Symmetrical Drive)	CMOS (follows VDD bias voltage)
UCC27518DBV UCC27518ADBQ1	SOT-23, 5 pin		
UCC27519DBV UCC27519ADBQ1	SOT-23, 5 pin		

(1) Visit www.ti.com for the latest product datasheet.

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7 Pin Configuration and Functions



Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	EN	I	Enable input. When the EN pin is biased LOW, the output is disabled regardless of input state. When the EN pin is biased high or left floating, the output is enabled. The EN pin is allowed to float because it is pin-to-pin compatible with the NC pin of the TPS282x device.
2	GND	—	Ground. All signals are referenced to this pin.
3	IN– (UCC27518A-Q1)	I	Input. This pin is the inverting input in the UCC27518A-Q1 device. The output is held LOW if the IN– pin is unbiased or floating.
	IN+ (UCC27519A-Q1)	I	Input. This pin is the noninverting input in the UCC27519A-Q1 device. The output is held LOW if the IN+ pin is unbiased or floating.
4	OUT	O	Sourcing and sinking current output of driver.
5	VDD	I	Supply input.

8 Specifications

8.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾⁽²⁾⁽³⁾

		MIN	MAX	UNIT
Supply voltage	VDD	−0.3	20	V
OUTA, OUTB voltage	DC	−0.3	VDD + 0.3	V
	Repetitive pulse < 200 ns ⁽⁴⁾	−2	VDD + 0.3	
Output continuous current	I _{OUT_DC} (source/sink)		0.3	A
Output pulsed current (0.5 μs)	I _{OUT_pulsed} (source/sink)		4	A
IN+, IN−, EN ⁽⁵⁾		−6	20	V
Operating virtual junction temperature, T _J		−40	150	°C
Lead temperature	Soldering, 10 s		300	°C
	Reflow		260	
Storage temperature, T _{stg}		−65	150	°C

- (1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltages are with respect to GND unless otherwise noted. Currents are positive into, negative out of the specified terminal. See Packaging Section of the datasheet for thermal limitations and considerations of packages.
- (3) These devices are sensitive to electrostatic discharge; follow proper device handling procedures.
- (4) Values are verified by characterization on bench
- (5) Maximum voltage on input pins is not restricted by the voltage on the VDD pin.

8.2 ESD Ratings

		VALUE	UNIT
V _(ESD) Electrostatic discharge	Human-body model (HBM), per AEC Q100-002 ⁽¹⁾	±2500	V
	Charged-device model (CDM), per AEC Q100-011	±1500	

- (1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

8.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	NOM	MAX	UNIT
Supply voltage, VDD	4.5	12	18	V
Input voltage, (IN+ and IN−) and enable (EN)	0		18	V
Operating ambient temperature	−40		140	°C

8.4 Thermal Information

THERMAL METRIC ⁽¹⁾		UCC27518A-Q1 UCC27519A-Q1	UNIT
		DBV (SOT-23)	
		5 PINS	
R _{θJA}	Junction-to-ambient thermal resistance	215.5	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	136.1	°C/W
R _{θJB}	Junction-to-board thermal resistance	43.2	°C/W
ψ _{JT}	Junction-to-top characterization parameter	20.3	°C/W
ψ _{JB}	Junction-to-board characterization parameter	42.3	°C/W

- (1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, [SPRA953](#).

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8.5 Electrical Characteristics

VDD = 12 V, TA = –40°C to 140°C, 1-μF capacitor from VDD to GND. Currents are positive into, negative out of the specified terminal.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT	
BIAS CURRENTS							
I _{DD(off)}	Startup current	VDD = 3.4 V	IN+ = VDD (UC27519A-Q1) IN– = GND (UCC27518A-Q1)	51	85	123	μA
			IN– = VDD (UCC27518A-Q1)	51	70	103	
			IN+ = GND (UC27519A-Q1)	51	70	110	
UNDERVOLTAGE LOCKOUT (UVLO)							
V _{ON}	Supply start threshold	T _A = 25°C	3.85	4.2	4.57	V	
		T _A = –40°C to 140°C	3.8	4.2	4.67		
V _{OFF}	Minimum operating voltage after supply start		3.45	3.9	4.35	V	
V _{DD_H}	Supply voltage hysteresis		0.19	0.3	0.45	V	
INPUTS (IN+, IN–)							
V _{IN_H}	Input signal high threshold	VDD = 4.5 V		55	62	%VDD	
V _{IN_L}	Input signal low threshold		31	39			
V _{IN_HYS}	Input signal hysteresis			16			
V _{IN_H}	Input signal high threshold	VDD = 12 V		55	59	%VDD	
V _{IN_L}	Input signal low threshold		31	39			
V _{IN_HYS}	Input signal hysteresis			16			
V _{IN_H}	Input signal high threshold	VDD = 18 V		55	58	%VDD	
V _{IN_L}	Input signal low threshold		35	38			
V _{IN_HYS}	Input signal hysteresis			17			
ENABLE (EN)							
V _{EN_H}	Enable signal high threshold	VDD = 12 V		2.1	2.3	V	
V _{EN_L}	Enable signal low threshold		1	1.25			
V _{EN_HYS}	Enable hysteresis			0.86			
SOURCE AND SINK CURRENT							
I _{SRC/SNK}	Source/sink peak current ⁽¹⁾	C _{LOAD} = 0.22 μF, F _{SW} = 1 kHz		±4		A	
OUTPUTS (OUT)							
V _{DD} –V _{OH}	High output voltage	VDD = 12 V I _{OUT} = –10 mA		50	90	mV	
		VDD = 4.5 V I _{OUT} = –10 mA		60	130		
V _{OL}	Low output voltage	VDD = 12 I _{OUT} = 10 mA		5	11	mV	
		VDD = 4.5 V I _{OUT} = 10 mA		6	12		
R _{OH}	Output pullup resistance ⁽²⁾	VDD = 12 V I _{OUT} = –10 mA		5	7.5	Ω	
		VDD = 4.5 V I _{OUT} = –10 mA		5.0	11		

(1) Ensured by design.

(2) ROH represents on-resistance of P-channel MOSFET in pullup structure of the output stage of the UCC27518A-Q1 and UCC27519A-Q1 device.

Electrical Characteristics (continued)

VDD = 12 V, T_A = –40°C to 140°C, 1-μF capacitor from VDD to GND. Currents are positive into, negative out of the specified terminal.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
R _{OL}	Output pulldown resistance	VDD = 12 V I _{OUT} = 10 mA		0.5	1	Ω
		VDD = 4.5 V I _{OUT} = 10 mA		0.6	1.2	

8.6 Switching Characteristics

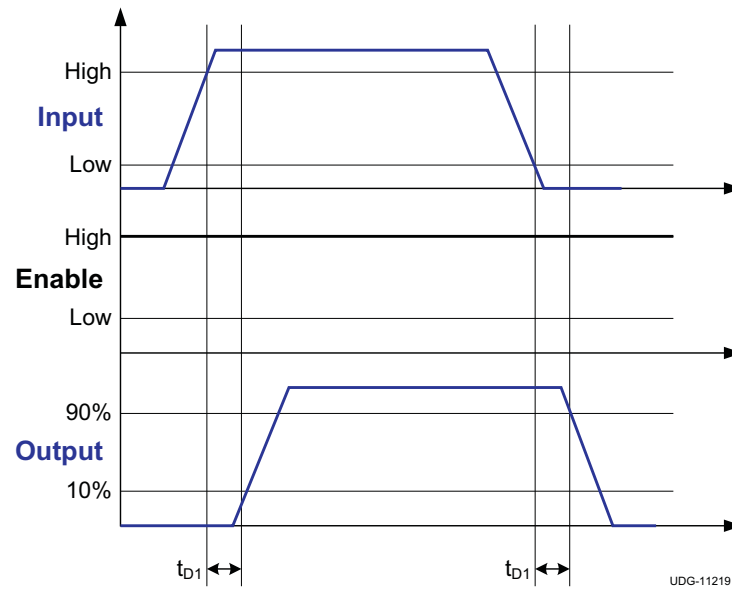
VDD = 12 V, T_A = –40°C to 140°C, 1-μF capacitor from VDD to GND. Currents are positive into, negative out of the specified terminal. Over operating free-air temperature range (unless otherwise noted). See the timing diagrams in [Figure 1](#), [Figure 2](#), [Figure 3](#), and [Figure 4](#).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t _R	Rise time	C _{LOAD} = 1.8 nF		8	12	ns
t _F	Fall time	C _{LOAD} = 1.8 nF		7	11	ns
t _{D1}	IN+ to output propagation delay	VDD = 10 V 7-V input pulse, C _{LOAD} = 1.8 nF	6	17	25	ns
t _{D2}	IN– to output propagation delay	VDD = 10 V 7-V input pulse, C _{LOAD} = 1.8 nF	6	17	24	ns
t _{D3}	EN to output high propagation delay	C _{LOAD} = 1.8 nF, 5-V enable pulse	4	12	16	ns
t _{D4}	EN to output low propagation delay	C _{LOAD} = 1.8 nF, 5-V enable pulse	4	12	19	ns

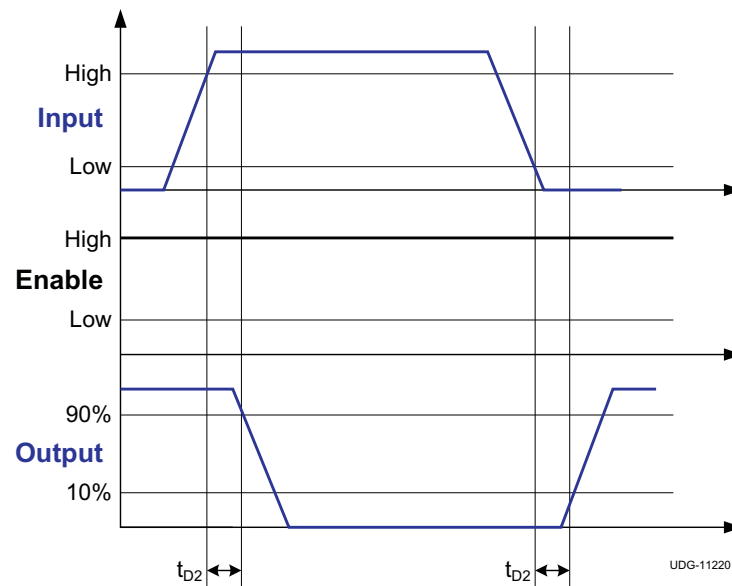
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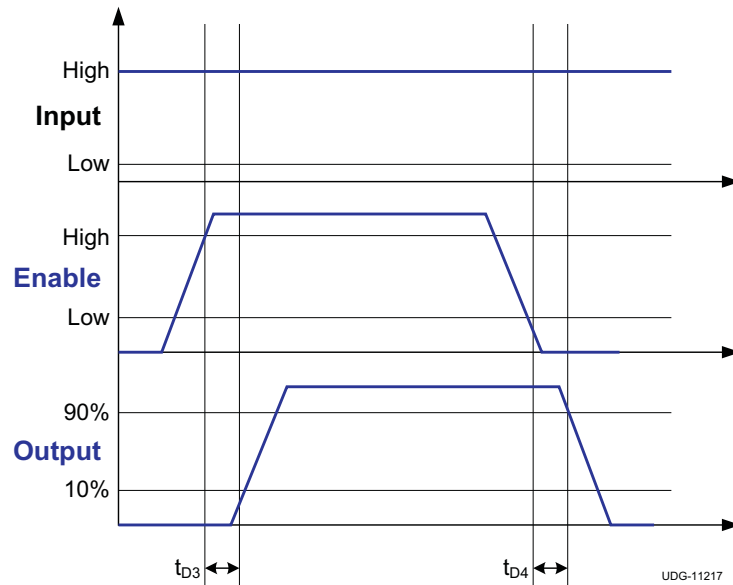
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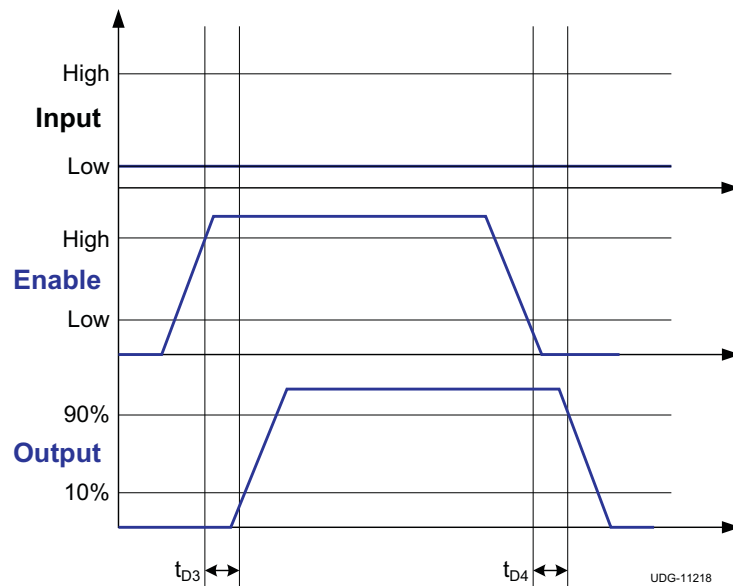
**Figure 1. Noninverting Configuration
(IN+ Pin, UCC27519A-Q1)**



**Figure 2. Inverting Configuration
(IN- Pin, UCC27518A-Q1)**



**Figure 3. Enable and Disable Function
(Noninverting Configuration, UCC27519A-Q1)**



**Figure 4. Enable and Disable Function
(Inverting Configuration, UCC27518A-Q1)**

8.7 Typical Characteristics

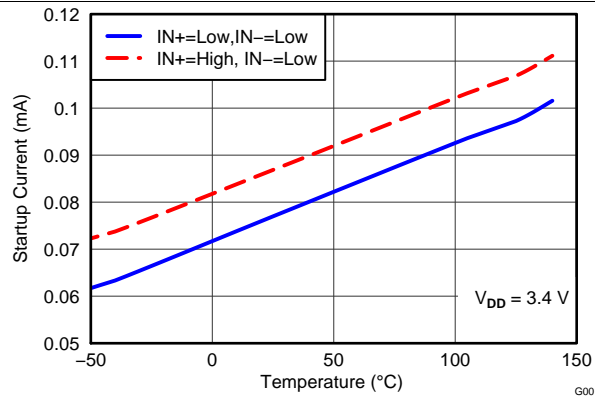


Figure 5. Start-Up Current vs Temperature

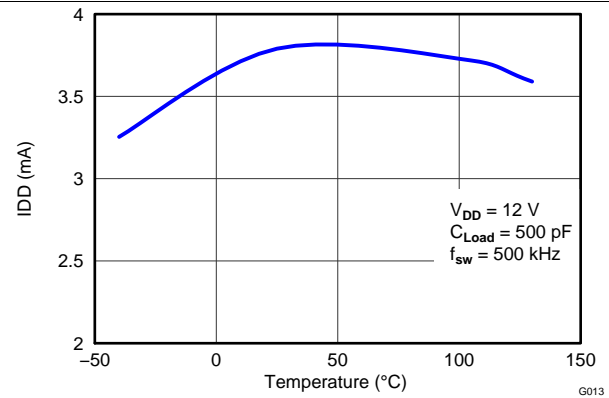


Figure 6. Operating Supply Current vs Temperature (Output Switching)

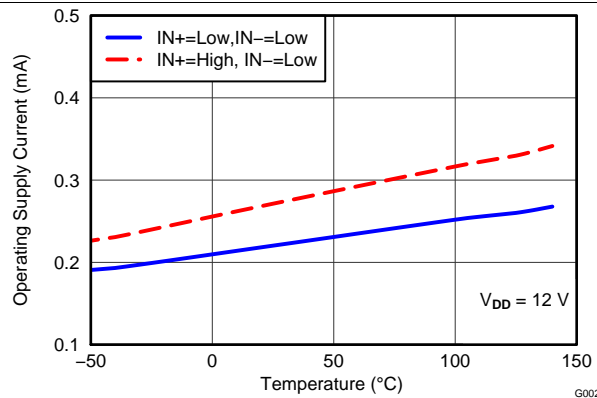


Figure 7. Supply Current vs Temperature (Output in DC On/Off condition)

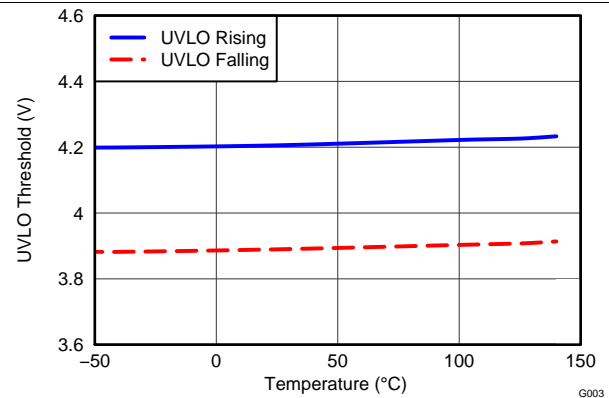


Figure 8. UVLO Threshold Voltage vs Temperature

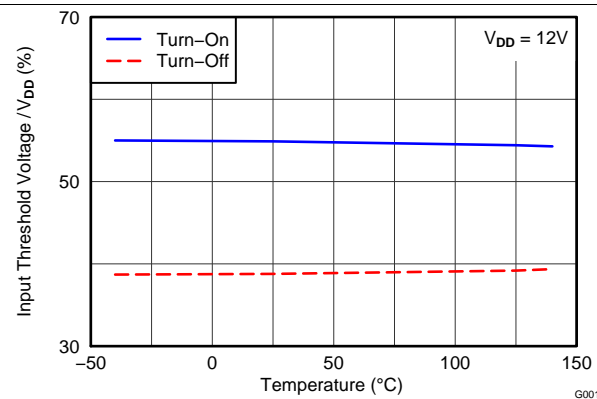


Figure 9. Input Threshold vs Temperature

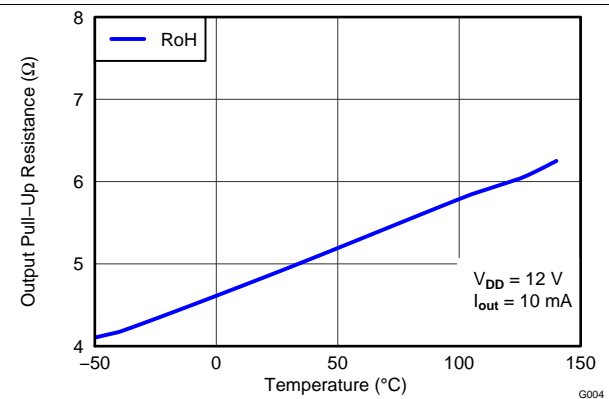


Figure 10. Output Pullup Resistance vs Temperature

Typical Characteristics (continued)

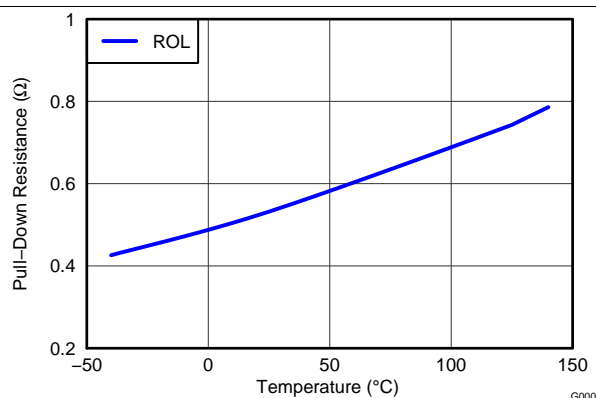


Figure 11. Output Pulldown Resistance vs Temperature

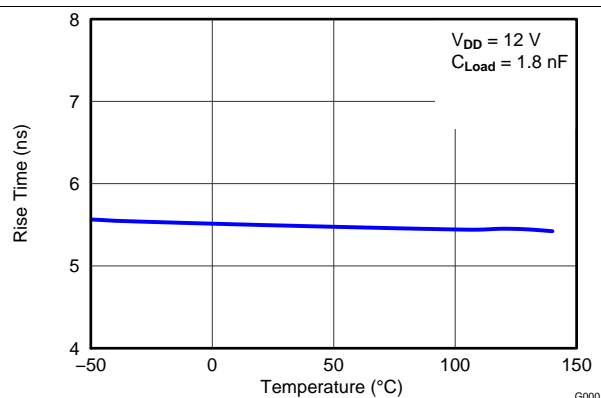


Figure 12. Rise Time vs Temperature

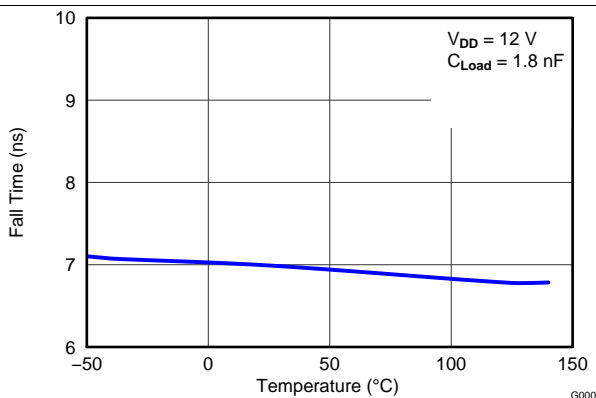


Figure 13. Fall Time vs Temperature

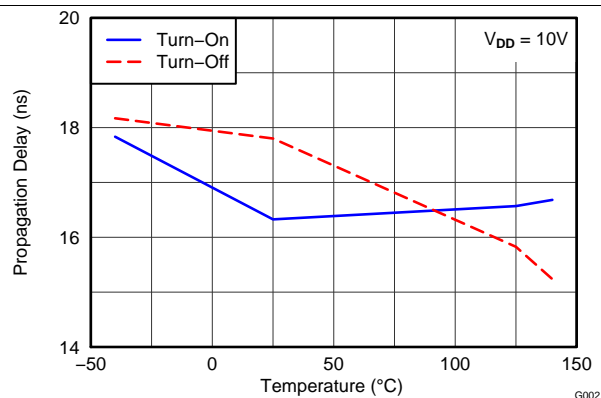


Figure 14. Input To Output Propagation Delay vs Temperature

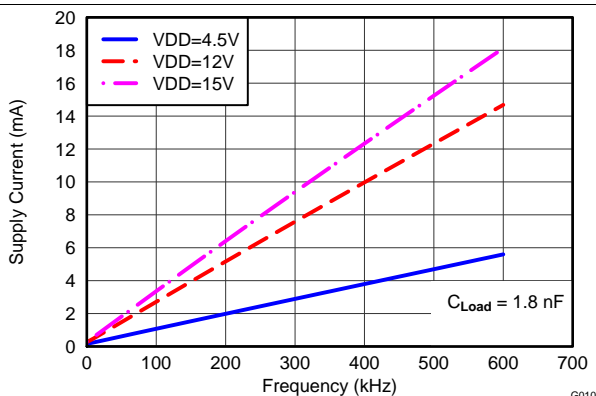


Figure 15. Operating Supply Current vs Frequency

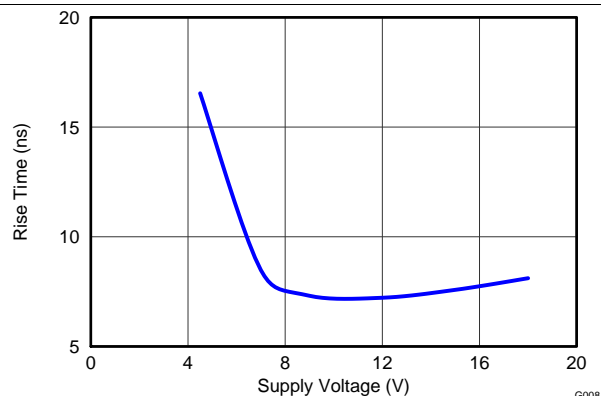


Figure 16. Rise Time vs Supply Voltage

Typical Characteristics (continued)

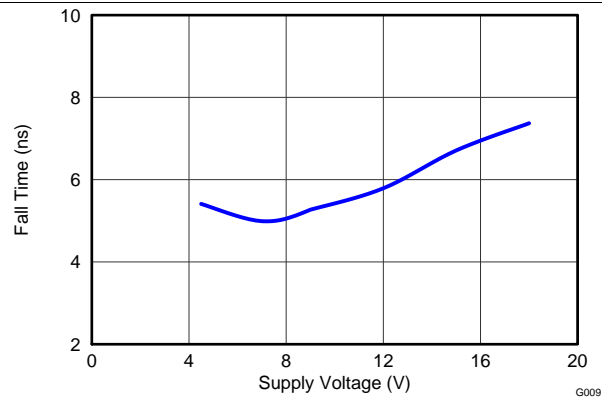


Figure 17. Fall Time vs Supply Voltage

9 Detailed Description

9.1 Overview

The UCC2751xA-Q1 single-channel, high-speed, low-side gate-driver device is capable of effectively driving MOSFET and IGBT power switches. Using a design that inherently minimizes shoot-through current, the UCC2751x device is capable of sourcing and sinking high peak-current pulses into capacitive loads offering rail-to-rail drive capability and extremely small propagation delay of 13 ns (typical).

The UCC2751xA-Q1 family of devices provides 4-A source, 4-A sink (symmetrical drive) peak-drive current capability. The device is designed to operate over a wide V_{DD} range of 4.5 to 18 V, and a wide temperature range of -40°C to $+140^{\circ}\text{C}$. Internal undervoltage lockout (UVLO) circuitry on the VDD pin holds the output low outside V_{DD} operating range. The capability to operate at low voltage levels, such as below 5 V, along with best-in-class switching characteristics, is especially suited for driving emerging wide bandgap power-switching devices such as GaN power-semiconductor devices.

The UCC27518A-Q1 device follows an inverting logic between the input and output, while the UCC27519A-Q1 device follows noninverting logic. The input pins of the devices are based on CMOS input-threshold logic. In CMOS input logic, the threshold voltage level is a function of the bias voltage on the V_{DD} pin of the device. This feature offers the benefits of higher noise immunity due to the higher threshold voltage (compared to logic level input thresholds), as well as the ability to accept slow dV/dt input signals for manipulating the propagation delay between the PWM controller signal and the gate driver output. For system robustness, internal pullup and pulldown resistors on the input pins ensure that outputs are held low when the input pins are in floating condition.

Table 2. UCC2751x Family of Features and Benefits

FEATURE	BENEFIT
High Source, Sink Current Capability 4 A, 4 A (Symmetrical)	High current capability offers flexibility in employing UCC2751x family of devices to drive a variety of power switching devices at varying speeds
Best-in-class 13-ns (typ) Propagation delay	Extremely low pulse transmission distortion
Expanded VDD Operating range of 4.5 V to 18 V	Flexibility in system design
Expanded Operating Temperature range of -40°C to 140°C (See Electrical Characteristics table)	Low VDD operation ensures compatibility with emerging wide bandgap power devices such as GaN
VDD UVLO Protection	Outputs are held low in UVLO condition, which ensures predictable, glitch-free operation at power-up and power-down
Outputs held low when input pins (INx) in floating condition	Protection feature, especially useful in passing abnormal condition tests during certification
Ability of input pins (and enable pin in UCC27518A-Q1 and UCC27519A-Q1) to handle voltage levels not restricted by VDD pin bias voltage	System simplification, especially related to auxiliary bias supply architecture
Negative voltage handling capability on input pins of UCC2751xA and UCC2751x-A-Q1 devices	Enhanced robustness when long traces are present between PWM controller and the gate driver
CMOS input threshold logic in UCC27518A-Q1 and UCC27519A-Q1 ($V_{IN_H} - 70\% V_{DD}$, $V_{IN_L} - 30\% V_{DD}$)	Well suited for slow input voltage signals, with flexibility to program delay circuits (RCD)

9.2 Functional Block Diagram

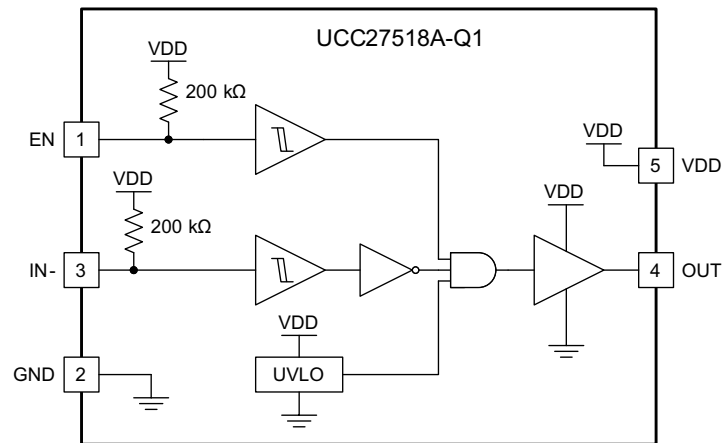


Figure 18. UCC27518A-Q1 Functional Block Diagram

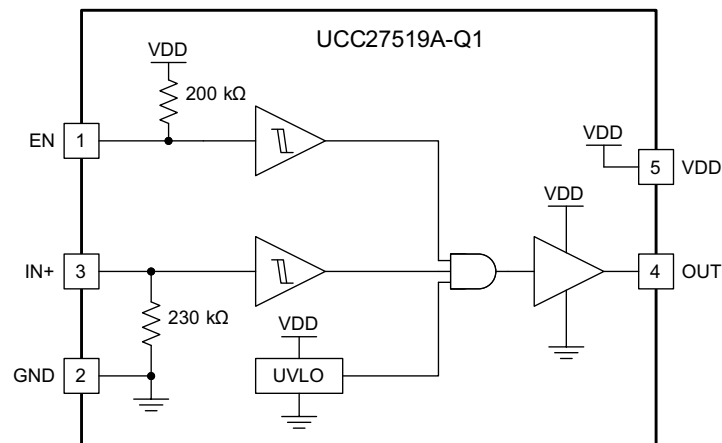


Figure 19. UCC27519A-Q1 Functional Block Diagram

9.3 Feature Description

9.3.1 VDD and Undervoltage Lockout

The UCC2751x family of devices has internal undervoltage lockout (UVLO) protection feature on the V_{DD} pin supply-circuit blocks. Whenever the driver is in UVLO condition (such as when V_{DD} voltage less than V_{ON} during power up and when V_{DD} voltage is less than V_{OFF} during power down), this circuit holds all outputs LOW, regardless of the status of the inputs. The UVLO is typically 4.2 V with 300-mV typical hysteresis. This hysteresis helps prevent chatter when low V_{DD} supply voltages have noise from the power supply and also when droops in the V_{DD} bias voltage occur when the system commences switching and when a sudden increase in I_{DD} occurs. The capability to operate at low voltage levels such as below 5 V, along with best-in-class switching characteristics, is especially suited for driving emerging GaN wide bandgap power semiconductor devices.

For example, at power up, the UCC2751x driver output remains LOW until the V_{DD} voltage reaches the UVLO threshold. The magnitude of the OUT signal rises with V_{DD} until steady-state V_{DD} is reached. In the noninverting device (PWM signal applied to IN+ pin) shown in Figure 20, the output remains LOW until the UVLO threshold is reached, and then the output is in-phase with the input. In the inverting device (PWM signal applied to IN- pin) shown in Figure 21, the output remains LOW until the UVLO threshold is reached, and then the output is out-phase with the input.

Feature Description (continued)

Because the driver draws current from the VDD pin to bias all internal circuits, for the best high-speed circuit performance, two VDD bypass capacitors are recommended to prevent noise problems. The use of surface mount components is highly recommended. A 0.1- μF ceramic capacitor should be located as close as possible to the VDD to GND pins of the gate driver. In addition, a larger capacitor (such as 1 μF) with relatively low ESR should be connected in parallel and close proximity, to help deliver the high-current peaks required by the load. The parallel combination of capacitors should present a low impedance characteristic for the expected current levels and switching frequencies in the application.

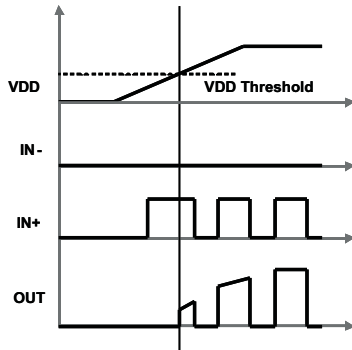


Figure 20. Power-Up (Noninverting Drive)

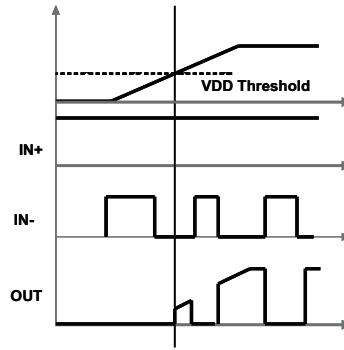


Figure 21. Power-Up (Inverting Drive)

9.3.2 Operating Supply Current

The UCC2751xA-Q1 family of devices features very-low quiescent I_{DD} currents. The typical operating supply current in undervoltage lockout (UVLO) state and fully-on state (under static and switching conditions) are summarized in [Figure 5](#), [Figure 6](#) and [Figure 7](#). The I_{DD} current when the device is fully on and outputs are in a static state (DC high or DC low, refer [Figure 7](#)) represents lowest quiescent I_{DD} current when all the internal logic circuits of the device are fully operational. The total supply current is the sum of the quiescent I_{DD} current, the average I_{OUT} current because of switching and finally any current related to pullup resistors on the unused input pin. For example when the inverting input pin is pulled low additional current is drawn from VDD supply through the pullup resistors (see the [Functional Block Diagram](#) section for the device block diagram). Knowing the operating frequency (f_{SW}) and the MOSFET gate (Q_G) charge at the drive voltage being used, the average I_{OUT} current can be calculated as product of Q_G and f_{SW} .

A complete characterization of the I_{DD} current as a function of switching frequency at different VDD bias voltages under 1.8-nF switching load is provided in [Figure 15](#). The strikingly linear variation and close correlation with theoretical value of average I_{OUT} indicates negligible shoot-through inside the gate-driver device attesting to its high-speed characteristics.

9.3.3 Input Stage

The input pins of UCC2751xA-Q1 family of devices are based on CMOS input logic where the threshold voltage level is a function of the bias voltage applied on the VDD pin. Typically, the Input high threshold (V_{INH}) is 55% VDD and input low threshold (V_{INL}) is 39% VDD. Hysteresis (typically 19% VDD), which is available on the input threshold, offers noise immunity. With high VDD voltages resulting in wide hysteresis, slow dV/dt input signals are acceptable in the INx pins and RC circuits can be inserted between the input PWM signal and the INx pins of UCC2751xA-Q1 family of devices, to program a delay between the input signal and output transition.

The input pins have the ability to sustain negative voltages below the GND pin. This ability offers higher robustness and makes the design simpler when long traces are present between the PWM controller output and input of gate driver. An example of such a situation is when the controller is mounted on a daughter card and the gate driver is on the power stage board, close to the power switches.

Feature Description (continued)

9.3.4 Enable Function

The enable pin is based on a noninverting configuration (active high operation). When the EN pin is driven high the output is enabled and when the EN pin is driven low the output is disabled. Unlike input pin, the enable pin threshold is based on a TTL/CMOS-compatible input threshold logic that does not vary with the supply voltage. Typically, the enable high threshold (V_{ENH}) is 2.1 V and enable low threshold (V_{ENL}) is 1.25 V. Thus the EN pin can be effectively controlled using logic signals from 3.3-V and 5-V microcontrollers. The EN pin is internally pulled up to VDD using pullup resistor as a result of which the output of the device is enabled in the default state. Hence the EN pin can be left floating or not connected (NC) for standard operation, when enable feature is not needed. Essentially, this allows the UCC2751xA-Q1 family devices to be pin-to-pin compatible with TI's previous generation drivers, the TPS2828-Q1 and TPS2829-Q1 device respectively, where pin number 1 is an NC pin. The enable pin also has the ability to sustain negative voltages below the GND pin.

9.3.5 Output Stage

The UCC2751xA-Q1 family of devices is capable of delivering 4-A source, 4-A sink (symmetrical drive) at VDD = 12 V. The output stage of the UCC2751xA-Q1 family of devices are shown in Figure 22. The UCC2751xA-Q1 family of devices features a unique architecture on the output stage which delivers the highest peak source current when it is most needed during the Miller plateau region of the power switch turn-on transition (when the power switch drain or collector voltage experiences dV/dt). The device output stage features a hybrid pullup structure using a parallel arrangement of N-channel and P-channel MOSFET devices. By turning on the N-channel MOSFET during a narrow instant when the output changes state from low to high, the gate-driver device is able to deliver a brief boost in the peak-sourcing current enabling fast turn on.

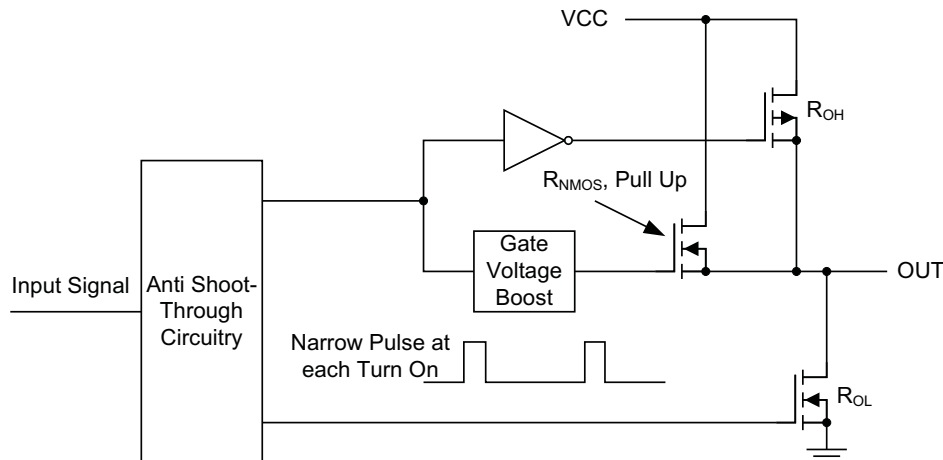


Figure 22. UCC2751xA-Q1 Gate Driver Output Structure

The R_{OH} parameter (see the [Electrical Characteristics](#) table) is a DC measurement and is representative of the on-resistance of the P-channel device only, because the N-channel device is turned on only during output change of state from low to high. Thus the effective resistance of the hybrid pullup stage is much lower than what is represented by R_{OH} parameter. The pulldown structure is composed of a N-channel MOSFET only. The R_{OL} parameter (see the [Electrical Characteristics](#) table), which is also a DC measurement, is representative of true impedance of the pulldown stage in the device. In the UCC2751xA-Q1 family of devices, the effective resistance of the hybrid pullup structure is approximately $1.4 \times R_{\text{OL}}$.

The driver output voltage swings between VDD and GND providing rail-to-rail operation, thanks to the MOS output stage which delivers very low dropout. The presence of the MOSFET body diodes also offers low impedance to switching overshoots and undershoots. This means that in many cases, external Schottky diode clamps may be eliminated. The outputs of these drivers are designed to withstand 500-mA reverse current without either damage to the device or logic malfunction.

Feature Description (continued)

9.3.6 Low Propagation Delays

The UCC2751xA-Q1 driver device features best-in-class input-to-output propagation delay of 17 ns (typical) at VDD = 12 V. This promises the lowest level of pulse transmission distortion available from industry standard gate driver devices for high-frequency switching applications. As shown in [Figure 14](#), there is very little variation of the propagation delay with temperature and supply voltage as well, offering typically less than 20-ns propagation delays across the entire range of application conditions.

9.4 Device Functional Modes

[Table 3](#) lists the device logic for each device.

Table 3. Device Logic Table

EN	UCC27518A-Q1		UCC27519A-Q1	
	IN– PIN	OUT PIN	IN+ PIN	OUT PIN
H	L	H	L	L
H	H	L	H	H
L	Any	L	Any	L
Any	x ⁽¹⁾	L	x ⁽¹⁾	L
x ⁽¹⁾	L	H	L	L
x ⁽¹⁾	H	L	H	H

(1) x = floating condition

10 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

High-current gate-driver devices are required in switching power applications for a variety of reasons. To effect fast switching of power devices and reduce associated switching power losses, a powerful gate driver is employed between the PWM output of controllers and the gates of the power semiconductor devices. Gate drivers provide other uses such as minimizing the effect of high-frequency switching noise by locating the high-current driver physically close to the power switch, driving gate-drive transformers and controlling floating power-device gates, and reducing power dissipation and thermal stress in controllers by moving gate charge power losses into itself. Finally, emerging wide-bandgap power device technologies, such as GaN-based switches, which are capable of supporting very high switching frequency operation, are driving very special requirements in terms of gate drive capability. These requirements include operation at low VDD voltages (5 V or lower), low propagation delays, and availability in compact, low-inductance packages with good thermal capability. In summary gate-driver devices are extremely important components in switching power combining benefits of high-performance, low cost, component count and board space reduction, and simplified system design.

10.2 Typical Application

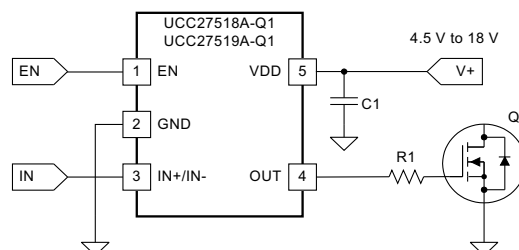


Figure 23. Typical Application Diagram

10.2.1 Design Requirements

When selecting the proper gate-driver device for an end application, some design considerations must be evaluated first to make the most appropriate selection. [Table 4](#) lists these design considerations and example values.

Table 4. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input-to-output logic	Noninverting
Input threshold type	CMOS type
VDD bias supply voltage	10 V (minimum), 13 V (nominal), 15 V (peak)
Peak source and sink currents	Minimum 3-A source, minimum 3-A sink
Enable and disable function	Yes, required
Propagation delay	Maximum 40 ns or less

10.2.2 Detailed Design Procedure

10.2.2.1 Input-to-Output Logic

The design must specify which type of input-to-output configuration should be used. If turning on the power MOSFET or IGBT when the input signal is in high state is preferred, then the noninverting configuration must be selected. If turning off the power MOSFET or IGBT when the input signal is in high state is preferred, the inverting configuration must be selected. The UCC2751xA-Q1 family of devices follow inverting and noninverting logic, respectively.

10.2.2.2 Input Threshold Type

The type of input voltage threshold determines the type of controller used with the gate driver device. The UCC2751xA-Q1 family of devices feature CMOS input-threshold logic with wide hysteresis. In CMOS input-threshold logic, the threshold voltage level is a function of the bias voltage on the V_{DD} pin of the device. The typical high threshold is 55% of the V_{DD} supply voltage, and the typical low threshold is 39% of the V_{DD} supply voltage at V_{DD} = 12 V. Built-in hysteresis is included which is typically 16% of V_{DD} supply voltage. See the table for the specified input-threshold voltage levels and hysteresis specifications for the UCC2751xA-Q1 family of devices at different V_{DD} bias levels.

In most applications, the absolute value of the threshold voltage offered by the CMOS logic is higher (for example, V_{INH} = 5.5 V if V_{DD} = 10 V) than what is offered by logic-level threshold devices. This higher threshold voltage offers the following benefits:

- Better noise immunity because of the higher threshold level desirable in high power systems.
- Ability to accept slow dV/dt input signals, which allows designers to use RCD circuits on the input pin to program propagation delays in the application, as shown in Figure 24.

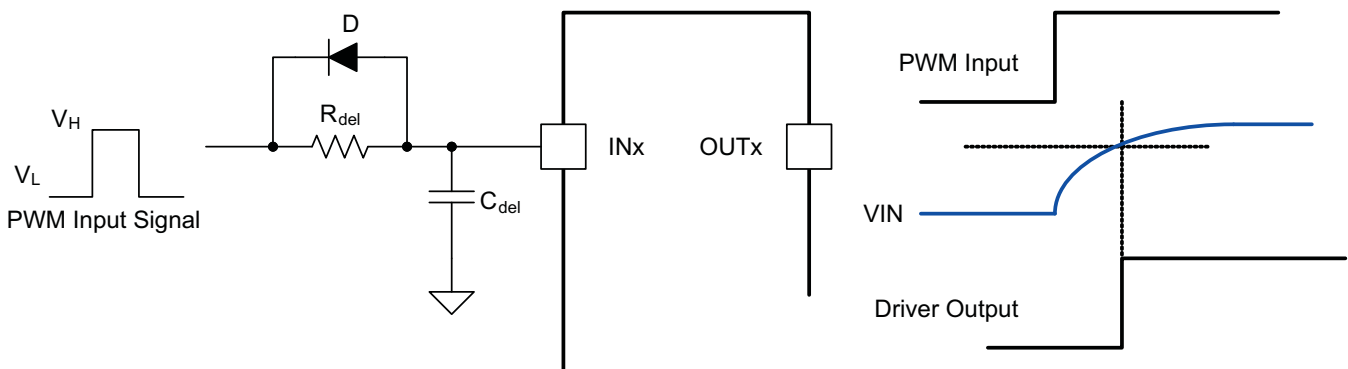


Figure 24. Using RCD Circuits

$$t_{del} = -R_{del}C_{del} \times \ln \left(\frac{V_L - V_{IN-H}}{V_H - V_L} + 1 \right) \quad (1)$$

As a result of the CMOS input logic, the UCC2751xA-Q1 family of devices cannot be driven directly by logic-level control signals from microcontrollers, digital power controllers, or DSPs. The UCC2751xA-Q1 family of devices is ideally suited for being driven by analog controllers driven by the same V_{DD} voltage as the gate driver devices.

10.2.2.3 V_{DD} Bias Supply Voltage

The bias supply voltage to be applied to the V_{DD} pin of the device should never exceed the values listed in the table. However, different power switches demand different voltage levels to be applied at the gate terminals for effective turn on and turnoff. With certain power switches, a positive gate voltage may be required for turn on, and a negative gate voltage may be required for turnoff, in which case the V_{DD} bias supply equals the voltage differential. With a wide operating range from 4.5 V to 18 V, the UCC2751xA-Q1 family of devices can be used to drive a variety of power switches, such as Si MOSFETs (for example, V_{GS} = 4.5 V, 10 V, 12 V), IGBTs (V_{GE} = 15 V, 18 V), and wide-bandgap power semiconductors (such as GaN, certain types of which allow no higher than 6 V to be applied to the gate terminals).

10.2.2.4 Peak Source and Sink Currents

Generally, the switching speed of the power switch during turnon and turnoff should be as fast as possible to minimize switching power losses. The gate driver device must be able to provide the required peak current for achieving the targeted switching speeds for the targeted power MOSFET. Using the example of a power MOSFET, the system requirement for the switching speed is typically described in terms of the slew rate of the drain-to-source voltage of the power MOSFET (such as dV_{DS}/dt).

For example, the system requirement might state that a SPP20N60C3 power MOSFET must be turned-on with a dV_{DS}/dt of 20 V/ns or higher under a DC bus voltage of 400 V in a continuous-conduction-mode (CCM) boost PFC-converter application. This type of application is an inductive, hard-switching application, and reducing switching power losses is critical. This requirement means that the entire drain-to-source voltage swing during power MOSFET turnon event (from 400 V in the OFF state to $V_{DS(on)}$ in on state) must be completed in approximately 20 ns or less.

When the drain-to-source voltage swing occurs, the Miller charge of the power MOSFET (QGD parameter in SPP20N60C3 power MOSFET data sheet = 33 nC typical) is supplied by the peak current of gate driver. According to the power MOSFET inductive switching mechanism, the gate-to-source voltage of the power MOSFET at this time is the Miller plateau voltage, which is typically a few volts higher than the threshold voltage of the power MOSFET, $V_{GS(TH)}$. To achieve the targeted dV_{DS}/dt , the gate driver must be capable of providing the QGD charge in 20 ns or less. In other words, a peak current of 1.65 A ($= 33 \text{ nC} / 20 \text{ ns}$) or higher must be provided by the gate driver. The UCC2751xA-Q1 gate driver is capable of providing 4-A peak sourcing current, which exceeds the design requirement and has the capability to meet the necessary switching speed.

The 2.4x overdrive capability provides an extra margin against part-to-part variations in the QGD parameter of the power MOSFET, along with additional flexibility to insert external gate resistors and fine tune the switching speed for efficiency versus EMI optimizations. However, in practical designs the parasitic trace inductance in the gate drive circuit of the PCB will have a definitive role to play on the power MOSFET switching speed. The effect of this trace inductance is to limit the dI/dt of the output current pulse of the gate driver.

To illustrate this, consider the output current pulse waveform from the gate driver to be approximated to a triangular profile, where the area under the triangle ($\frac{1}{2} \times I_{PEAK} \times \text{time}$) would equal the total gate charge of the power MOSFET (QG parameter in SPP20N60C3 power MOSFET datasheet = 87 nC typical). If the parasitic trace inductance limits the dI/dt , the full peak current capability of the gate driver may not be fully achieved in the time required to deliver the QG required for the power MOSFET switching. In other words, the time parameter in the equation would dominate and the I_{PEAK} value of the current pulse would be much less than the true peak current capability of the device, while the required QG is still delivered. Because of this, the desired switching speed may not be realized, even when theoretical calculations indicate the gate driver is capable of achieving the targeted switching speed. Thus, place the gate driver device very close to the power MOSFET and design a tight gate drive-loop with minimal PCB trace inductance to realize the full peak-current capability of the gate driver.

10.2.2.5 Enable and Disable Function

Certain applications demand independent control of the output state of the driver without involving the input signal. The UCC2751xA-Q1 family of devices include the enable pin (EN), which achieves this.

10.2.2.6 Propagation Delay

The acceptable propagation delay from the gate driver is dependent on the switching frequency at which it is used, and the acceptable level of pulse distortion to the system. The UCC2751xA-Q1 family of devices feature industry best-in-class 17-ns (typical) propagation delays, which ensure very little pulse distortion and allow operation at very high-frequencies. See the table for the propagation and switching characteristics of the UCC2751xA-Q1 family of devices.

10.2.3 Application Curve

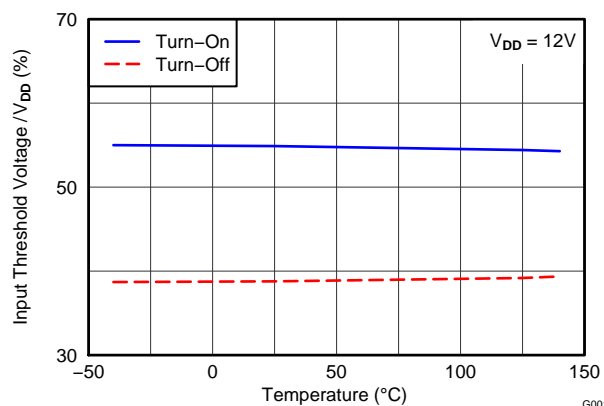


Figure 25. Input Threshold vs Temperature

11 Power Supply Recommendations

The bias supply voltage range for which the UCC2751xA-Q1 family of devices is rated to operate is from 4.5 V to 18 V. The lower end of this range is governed by the internal under voltage-lockout (UVLO) protection feature on the V_{DD} pin supply circuit blocks. Whenever the driver is in UVLO condition with the V_{DD} pin voltage below the V_(ON) supply start threshold, this feature holds the output low, regardless of the status of the inputs. The upper end of this range is driven by the 20-V absolute maximum voltage rating of the V_{DD} pin of the device (which is a stress rating). Maintaining a 2-V margin to allow for transient voltage spikes, the maximum recommended voltage for the V_{DD} pin is 18 V.

The UVLO protection feature also involves a hysteresis function. When the V_{DD} pin bias voltage has exceeded the threshold voltage and the device begins to operate, if the voltage drops, the device continues to deliver normal functionality unless the voltage drop exceeds the hysteresis specification V_{DD(hys)}. While operating at or near the 4.5 V range, ensure that the voltage ripple on the auxiliary power supply output is smaller than the hysteresis specification of the device to avoid triggering device shutdown.

During system shutdown, the device operation continues until the V_{DD} pin voltage has dropped below the V_(OFF) threshold, which must be accounted for while evaluating system shutdown timing design requirements. Likewise, at system startup the device does not begin operation until the VDD pin voltage has exceeded above the V_(ON) threshold. The quiescent current consumed by the internal circuit blocks of the device is supplied through the V_{DD} pin. The charge for source current pulses delivered by the OUT pin is also supplied through the same V_{DD} pin. As a result, every time a current is sourced out of the output pin (OUT), a corresponding current pulse is delivered into the device through the VDD pin. Therefore, ensure that local bypass capacitors are provided between the VDD and GND pins and located as close to the device as possible, for the purpose of decoupling. A low ESR, ceramic surface mount capacitor is necessary. TI recommends to have 2 capacitors; a 100-nF ceramic surface-mount capacitor which can be nudged very close to the pins of the device, and another surface-mount capacitor of few microfarads added in parallel.

12 Layout

12.1 Layout Guidelines

Proper PCB layout is extremely important in a high-current, fast-switching circuit to provide appropriate device operation and design robustness. The UCC2751xA-Q1 gate driver incorporates short-propagation delays and powerful output stages capable of delivering large current peaks with very fast rise and fall times at the gate of power switch to facilitate voltage transitions very quickly. At higher VDD voltages, the peak-current capability is even higher (4-A, 4-A peak current is at VDD = 12 V). Very high di/dt can cause unacceptable ringing if the trace lengths and impedances are not well controlled. The following circuit layout guidelines are strongly recommended when designing with these high-speed drivers.

- Locate the driver device as close as possible to power device to minimize the length of high-current traces between the output pins and the gate of the power device.
- Locate the VDD bypass capacitors between VDD and GND as close as possible to the driver with minimal trace length to improve the noise filtering. These capacitors support high-peak current being drawn from VDD during turnon of power MOSFET. The use of low inductance SMD components such as chip resistors and chip capacitors is highly recommended.
- The turn-on and turn-off current loop paths (driver device, power MOSFET and VDD bypass capacitor) should be minimized as much as possible to keep the stray inductance to a minimum. High di/dt is established in these loops at two instances—during turnon and turnoff transients, which will induce significant voltage transients on the output pin of the driver device and gate of the power switch.
- Wherever possible parallel the source and return traces, taking advantage of flux cancellation.
- Separate power traces and signal traces, such as output and input signals.
- Star-point grounding is a good way to minimize noise coupling from one current loop to another. The GND of the driver should be connected to the other circuit nodes such as source of power switch and ground of PWM controller at one point. The connected paths should be as short as possible to reduce inductance and be as wide as possible to reduce resistance.
- Use a ground plane to provide noise shielding. Fast rise and fall times at OUT may corrupt the input signals during transition. The ground plane must not be a conduction path for any current loop. Instead the ground plane must be connected to the star-point with one single trace to establish the ground potential. In addition to noise shielding, the ground plane can help in power dissipation as well.

12.2 Layout Example

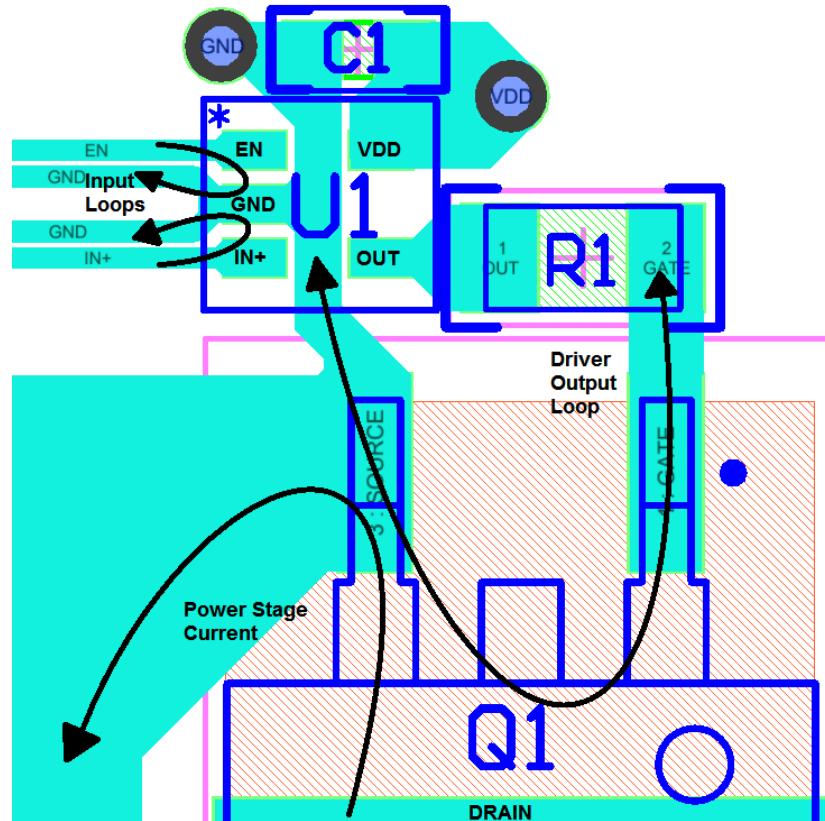


Figure 26. Layout Example

12.3 Thermal Consideration

The useful range of a driver is greatly affected by the drive power requirements of the load and the thermal characteristics of the package. For a gate driver to be useful over a particular temperature range the package must allow for the efficient removal of the heat produced while keeping the junction temperature within rated limits. The thermal metrics for the driver package are listed in the [Thermal Information](#) table. For detailed information regarding the thermal information table, please refer to the Application Note from Texas Instruments entitled *Semiconductor and IC Package Thermal Metrics* (SPRA953).

12.4 Power Dissipation

Power dissipation of the gate driver has two portions as shown in [Equation 2](#):

$$P_{DISS} = P_{DC} + P_{SW} \quad (2)$$

Use [Equation 3](#) to calculate the DC portion of the power dissipation.

$$P_{DC} = I_Q \times V_{DD}$$

where

- I_Q is the quiescent current for the driver (3)

The quiescent current is the current consumed by the device to bias all internal circuits such as input stage, reference voltage, logic circuits, protections, and also any current associated with switching of internal devices when the driver output changes state (such as charging and discharging of parasitic capacitances, parasitic shoot-through). The UCC2751xA-Q1 family of devices features very low quiescent currents (less than 1 mA, refer [Figure 7](#)) and contains internal logic to eliminate any shoot-through in the output driver stage. Thus the effect of the P_{DC} on the total power dissipation within the gate driver can be assumed to be negligible.

Power Dissipation (continued)

The power dissipated in the gate-driver package during switching (P_{SW}) depends on the following factors:

- Gate charge required of the power device (usually a function of the drive voltage V_G , which is very close to input bias supply voltage V_{DD} because of low V_{OH} drop-out).
- Switching frequency.
- Use of external gate resistors.

When a driver device is tested with a discrete, capacitive load it is a fairly simple matter to calculate the power that is required from the bias supply. The energy that must be transferred from the bias supply to charge the capacitor is given by [Equation 4](#).

$$E_G = \frac{1}{2} C_{LOAD} V_{DD}^2$$

where

- C_{LOAD} is load capacitor
 - V_{DD} is bias voltage feeding the driver
- (4)

There is an equal amount of energy dissipated when the capacitor is charged. This leads to a total power loss given by [Equation 5](#).

$$P_G = C_{LOAD} V_{DD}^2 f_{SW}$$

where

- f_{SW} is the switching frequency
- (5)

The switching load presented by a power MOSFET or IGBT can be converted to an equivalent capacitance by examining the gate charge required to switch the device. This gate charge includes the effects of the input capacitance plus the added charge needed to swing the drain voltage of the power device as it switches between the ON and OFF states. Most manufacturers provide specifications of typical and maximum gate charge, in nC, to switch the device under specified conditions. Using the gate charge Q_G , one can determine the power that must be dissipated when charging a capacitor. This is done by using the equation, $Q_G = C_{LOAD} \times V_{DD}$, to provide the following equation for power:

$$P_G = C_{LOAD} V_{DD}^2 f_{SW} = Q_G V_{DD} f_{SW}$$
(6)

This power P_G is dissipated in the resistive elements of the circuit when the MOSFET/IGBT is being turned on or off. Half of the total power is dissipated when the load capacitor is charged during turnon, and the other half is dissipated when the load capacitor is discharged during turnoff. When no external gate resistor is employed between the driver and MOSFET or IGBT, this power is completely dissipated inside the driver package. With the use of external gate-drive resistors, the power dissipation is shared between the internal resistance of driver and external gate resistor in accordance to the ratio of the resistances (more power dissipated in the higher resistance component). Based on this simplified analysis, the driver power dissipation during switching is calculated as follows:

$$P_{SW} = Q_G \times V_{DD} \times f_{SW} \times \left(\frac{R_{OFF}}{(R_{OFF} + R_{GATE})} + \frac{R_{ON}}{(R_{ON} + R_{GATE})} \right)$$

where

- $R_{OFF} = R_{OL}$
 - R_{ON} (effective resistance of pullup structure) = $1.4 \times R_{OL}$
- (7)

13 Device and Documentation Support

13.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 5. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
UCC27518A-Q1	Click here	Click here	Click here	Click here	Click here
UCC27519A-Q1	Click here	Click here	Click here	Click here	Click here

13.2 Community Resource

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

TI E2E™ Online Community *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

13.3 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

13.4 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

13.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
UCC27518AQDBVRQ1	Active	Production	SOT-23 (DBV) 5	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	EAFAQ
UCC27518AQDBVRQ1.A	Active	Production	SOT-23 (DBV) 5	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	EAFAQ
UCC27519AQDBVRQ1	Active	Production	SOT-23 (DBV) 5	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	519Q
UCC27519AQDBVRQ1.A	Active	Production	SOT-23 (DBV) 5	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	519Q

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "-" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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TAPE AND REEL INFORMATION


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UCC27518AQDBVRQ1	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
UCC27519AQDBVRQ1	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UCC27518AQDBVRQ1	SOT-23	DBV	5	3000	180.0	180.0	18.0
UCC27519AQDBVRQ1	SOT-23	DBV	5	3000	180.0	180.0	18.0



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.

EXAMPLE BOARD LAYOUT

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

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NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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