UCC25661x-Q1 Family 750kHz Wide V_{IN}/V_{OUT} Range LLC Controller Optimized for Light-Load Efficiency

1 Features

- Full-load switching frequency: 50kHz to 750kHz
- IPPC control enables wide input and output LLC (WLLC) operation
- Enhanced light load management:
  - High-frequency pulse skip for improved light load efficiency
  - Low-frequency burst for low standby power
  - Audible frequency range skip for reduced audible noise
  - Integrated PFC on/off control signal to help further reduce standby power (UCC256614-Q1)
- Internal resonant-capacitor voltage synthesizer for enhanced signal reliability and high start-up frequency support
- Zero current switching (ZCS) avoidance to eliminate capacitive region operation
- Adaptive soft start with minimized inrush current
- Integrated high-voltage start-up (UCC256612-Q1 and UCC256614-Q1)
- Integrated gate driver: +0.6A and –1.2A
- Complete protections
  - Overcurrent protection (OCP): 50ns, cycle-by-cycle current limit
  - Overvoltage protection (OVP), internal and external overtemperature protection (OTP)
  - Input and VCCP UVLO with internal 19V VCCP Clamp
  - Independently configured OCP and overload protection (OLP) (UCC256612-Q1, UCC256613-Q1, and UCC256614-Q1)
- SOIC-14 package with removed pins for high-voltage clearance

2 Applications

- Cell monitor unit and battery junction box
- HEV/EV OBC and DC/DC converter
- EV charging infrastructure
- HEV/EV inverter and motor control
- Zone and body domain controller

3 Description

The UCC25661x-Q1 family is a high-frequency LLC controller that implements a input-power proportional control (IPPC) scheme, along with enhanced light-load management and multiple protection features.

IPPC widens the control range of the LLC converter and simplifies the design of wide input applications, such as high voltage to low voltage (HV-LV) redundant auxiliary, key-off, and bias isolated power supplies. IPPC simplifies the design of wide output applications, such as light electric vehicle battery chargers (scooters, mopeds, golf carts, and fork lifts).

The UCC25661x-Q1 family has enhanced light-load management that improves efficiency and minimizes audible noise. To minimize standby power in charger applications, the UCC25661x-Q1 family directly disables the PFC controller when operating in burst mode.

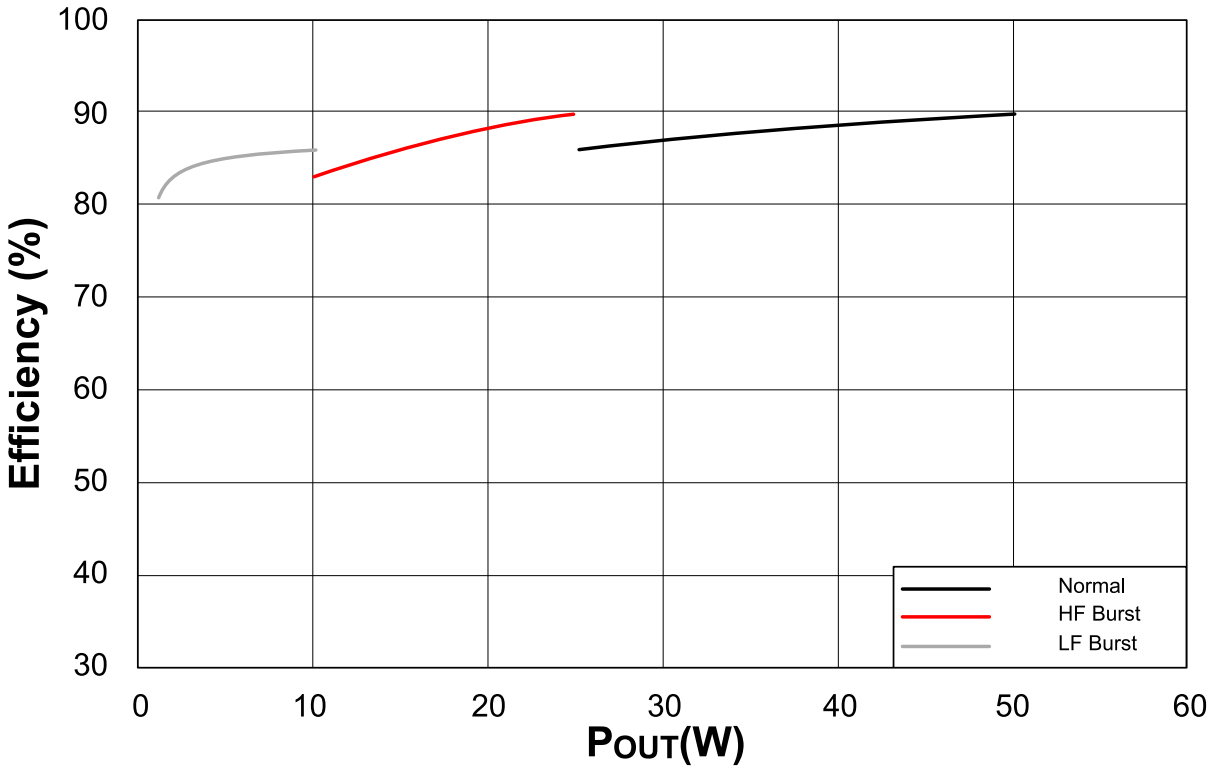
The automatic capacitive region avoidance scheme, along with the adaptive soft start with a reverse recovery avoidance scheme, establishes that the device never works in a mode where there is a potential to damage the FETs. Because of the automatic capacitive region avoidance scheme, the controller works best with a prebiased load.

The UCC25661x-Q1 family comes with robust protection for designing a reliable power supply. The UCC25661x-Q1 family has options supporting various features, see details in the Device Comparison table.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
UCC25661x-Q1 family	DDB (SOIC, 16)	9.9mm × 3.9mm

(1) For all available packages, see Section 11.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Typical Efficiency Curve

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4 Device Comparison Table

Orderable Part Number	UCC256612-Q1	UCC256613-Q1	UCC256614-Q1	UCC256615-Q1
Integrated High Voltage Startup	●		●	●
Integrated X-Capacitor Discharge				
Extended Gain Range (EGR)			●	●
OCP/OLP Decoupling	●	●	●	
PFC On/Off during LF Burst			●	
IPPC Enable	●	●	●	●
OPP fault Enable	●	●	●	
ZCS fault Enable	●	●	●	●

5 Pin Configuration and Functions

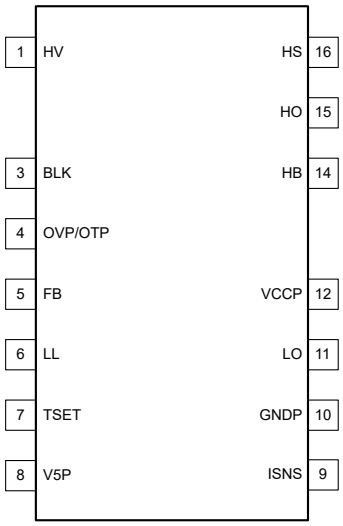


Figure 5-1. DDB Package, 16-Pin SOIC; Pins 2 and 13 Removed (Top View)

Table 5-1. Pin Functions

PIN[1]		I/O	DESCRIPTION
NAME	NO.		
HV	1	I	High-voltage (HV) start-up. This pin is used to perform HV start-up. After start-up is completed, the HV pin is used for AC presence detection. This pin is connected to the rectified AC line (for UCC256614-Q1) or input bulk capacitor (for UCC256612-Q1, UCC256614-Q1, and UCC256615-Q1).
	2	-	Missing. HV spacer for creepage between high voltage and low voltage pins
BLK	3	I	Bulk DC voltage sensing and input for feedforward control. Connect BLK through a resistor divider between positive terminal of bulk capacitor and GNDP to set the LLC converter start and stop voltage thresholds. See Section 7.3.5.1 for more details.
OVP/OTP	4	I	Overvoltage protection and external overtemperature protection input. Connect OVP/OTP to GNDP through an NTC resistor and to VCCP through zener diode. See Section 7.3.5.2 for more details.
FB	5	I	Feedback control input. Connect FB to the collector pin of an optocoupler in the isolated feedback network. See Section 7.3.3 for more details.
LL	6	I	Light load operation and burst mode threshold setting input. Connect LL to the center node of resistor divider between V5P an GNDP. The impedance and voltage at LL pin is used to select the thresholds for high frequency and low frequency burst mode operation. See Section 7.5.3 for more details.
TSET	7	I/O	VCR Synthesizer Time Constants Setting Input and PFC on/off output (UCC256614-Q1). Connect TSET to the center node of resistor divider between V5P and GNDP to program the internal resonant integrator (VCR synthesizer) time constants, maximum dead time and minimum switching frequency down to which IPPC is maintained. After programming phase ends during controller power up, TSET pin provides PFC on/off signal in UCC256614-Q1 variant.
V5P	8	P	5V Internal regulator output. Connect a decoupling capacitor (recommended value between 1µF and 4.7µF) from V5P to GNDP. Place this capacitor close to the V5P pin.

Table 5-1. Pin Functions (continued)

PIN[1]		I/O	DESCRIPTION
NAME	NO.		
ISNS	9	I	Resonant circuit current sense input. Connect ISNS pin to resonant capacitor through a series differentiator capacitor and a current sense resistor to GNDP. This pin senses the differentiated resonant capacitor voltage. This signal is internally used to: • Generate the control signal • OCP and cycle-by-cycle current limiting • Capacitive region avoidance See Section 8.2.2.17 for more details.
GNDP	10	P	Ground reference pin. Connect GNDP to primary-side bulk capacitor negative terminal.
LO	11	O	Low-side switch gate driver output. Connect to low-side switch gate terminal with a minimal gate drive circuit loop area.
VCCP	12	P	IC supply voltage pin. Connect a low-ESR ceramic decoupling capacitor between VCCP and GNDP. For applications including an auxiliary bias winding on the LLC transformer, the VCCP pin is connected through a diode to the bias winding. For applications where HV start-up is disabled, VCCP is supplied by an auxiliary bias supply. VCCP pin internally clamps to 19V.
	13	N/A	Missing pin. High-voltage spacer for creepage between high-voltage and low-voltage pins.
HB	14	P	High-side gate driver bias input. Connect a capacitor (minimum of 0.1µF) between HB and HS pins. See Section 8.3.2 for more details.
HO	15	O	High-side switch gate driver output. Connect to high-side switch gate terminal with a minimal gate drive circuit loop area.
HS	16	P	High-side gate driver return path and switching node connection input. Connect to the switching node of the half-bridge structure of the LLC converter. The voltage at this pin used to determine the adaptive dead time. See Section 7.3.4 for more details.

(1) Refer to Section 8.2 for more details.

6 Specifications

6.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted), all voltages are with respect to GND, currents are positive into and negative out of the specified terminal.(1)

		MIN	MAX	UNIT
Input voltage	HV, HB	-0.3	700	V
	ISNS	-6.5	6.5	V
	BLK, LL, TSET	-0.55	5.5	V
	HB - HS	-0.3	25	V
	VCCP	-0.55	30	V
	OVP/OTP	-0.55	5.5	V
5V	DC	-0.55	5.5	V
HO output voltage	DC	HS – 0.3	HB + 0.3	V
	Transient, less than 100ns	HS – 2	HB + 0.3	
LO output voltage	DC	-0.3	VCCP+ 0.3	V
	Transient, less than 100ns	-2	VCCP + 0.3	
Floating ground slew rate	dV_{HS}/dt	-200	200	V/ns
HO, LO pulsed current	I_{OUT_PULSED}	-0.6	1.2	A
Junction temperature range	T_J	-40	150	°C
Storage temperature range, T_{stg}	T_{stg}	-65	150	
Lead temperature	Soldering, 10 seconds		300	
	Reflow		260	

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, HV, HO, HS, HB pins(1)	±1000	V
		Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all other pins(1)	±2000	
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±500	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

All voltages are with respect to GND, -40°C < T_J = T_A < 125°C, currents are positive into and negative out of the specified terminal, unless otherwise noted.

		MIN	NOM	MAX	UNIT
HV, HS	Input voltage			640	V
V_{VCCP}	Supply voltage		15	18.5	V
HB - HS	Driver bootstrap voltage	10	14	17.5	V
C_B	Ceramic bypass capacitor from HB to HS	0.1		5	µF
C_{VCCP}	VCCP pin decoupling capacitor	33		470	µF
$I_{VCCPMAX}$	Maximum input current of VCCP			100	mA
T_A	Operating ambient temperature	-40		125	°C

6.4 Thermal Information

THERMAL METRIC(1)		UCC25661x D (SOIC) 14 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	74.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	30.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	31.8	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	4.4	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	31.4	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application note.

6.5 Electrical Characteristics

All voltages are with respect to GND, −40°C < T_J < 125°C, VCC = 15V, currents are positive into and negative out of the specified terminal, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY VOLTAGE						
VCC_{Short}	Below this threshold, use reduced start up current		0.6	1	1.4	V
$VCC_{ReStartJfet}$	Below this threshold, re-enable JFET			10.2		V
$VCC_{ReStart}$	HV start-up is re-enabled when VCC is below this level during start-up phase		12.5	13	13.5	V
$VCC_{StartSelf}$	Start-up when VCC is above this level		13.5	14	14.5	V
$VCC_{StartExt}$	Start-up when VCC is above this level		10.5	10.9	11.3	V
$VCC_{StopSwitching}$	Switching Stopped below this threshold		9	9.5		V
VCC_{UVLOr}	VCC under voltage lockout voltage (rising)		7.25	7.5	7.82	V
VCC_{UVLOf}	VCC under voltage lockout voltage hysteresis		6.5	6.8	7.1	V
VCC_{Hold_r}	Jfet stop voltage during start-up programming phase		7.9	8.2	8.5	V
VCC_{Hold_f}	Jfet start voltage during start-up programming phase		7.65	7.9	8.15	V
VCC_{Shunt}	VCC internal clamp voltage			19		V
$IVCC_{Clamp}$	VCC internal clamp current			15		mA
VCC_OV	VCC OVP threshold			20.5		V

6.5 Electrical Characteristics (continued)

All voltages are with respect to GND, −40°C < T_J < 125°C, VCC = 15V, currents are positive into and negative out of the specified terminal, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENT						
$I_{CCSleep}$	Current drawn from VCC rail during burst off period			800		µA
I_{CCRun}	Current drawn from VCC pin while gate is switching, excluding Gate Current	Dead time = 1µs maximum dead time		8		mA
REGULATED SUPPLY						
V5P	Regulated supply voltage (1)	No load	4.75	5	5.25	V
	Regulated supply voltage	10mA load	4.75	5	5.25	V
$V5P_{UVLO}$	V5P under voltage lock out voltage (1)			4		V
$I_{V5Pstart-upCurrLimit}$	Max current that can be drawn on the pin when VCCP < $VCC_{StartSelf}$ (1)	VCCP = 15V		6		mA
$I_{V5PCurrLimit}$	V5P at IV5P = 15mA	VCCP = 15V	10.2			mA
HIGH VOLTAGE START-UP						
$I_{VCC\_Charge\_Low}$	Reduced VCCP charge current from HV Pin	V_{HV} = 20V, VCC = 0V (UCC256612−Q1, UCC256614−Q1)	0.23	0.44	0.65	mA
$I_{VCC\_Charge\_High}$	Full VCCP charge current	V_{HV} = 20V, VCC = 4V, (UCC256612−Q1, UCC256614−Q1)	7.5	10	13.8	mA
BULK VOLTAGE SENSE						
$V_{BLKStartHys}$	BLK voltage comparator hysteresis (1)	For UCC256614−Q1	0.04	0.05	0.06	V
$V_{BLKStartHys}$	BLK voltage comparator hysteresis (1)	For UCC256612−Q1, UCC256613−Q1	0.09	0.1	0.11	V
$V_{BLKStop}$	BLK voltage that forces LLC operation to stop		0.98	1	1.02	V
I_{BLKHys}	BLK hysteresis current	For UCC256614−Q1		1		µA
I_{BLKHys}	BLK hysteresis current	For UCC256612−Q1, UCC256613−Q1		5		µA
FEEDBACK PIN						
$R_{FBInternal}$	Internal pull down resistor value	For UCC256614−Q1	85	100	115	kΩ
$R_{FBInternal}$	Internal pull down resistor value	For UCC256612−Q1, UCC256613−Q1	42.5	50	57.5	kΩ
I_{FB}	FB internal current source	For UCC256614−Q1	68	80	92	µA
I_{FB}	FB internal current source	For UCC256612−Q1, UCC256613−Q1	136	160	184	µA
V_{FB}	FB pin voltage when FB pin sink current is at (I_{FB} − 50µA)	Iopto = 0.37 × IFB	3.3	3.5	3.7	V
ΔV_{FB}	FB pin voltage variation when FB pin sink current ranges from (Iopto = 0.37 × IFB to Iopto = 0.94 × IFB)				0.6	V
ΔV_{clamp}	FB pin voltage variation when FB pin sink current ranges from (Iopto = 0.94 × IFB) to (Iopto = 1.06 × IFB)	(Iopto = 0.94 × IFB) to (Iopto = 1.06 × IFB)	0.3			V
$I_{FBclamp}$	Maximum FB internal current source when FB is clamped	For UCC256614−Q1	75	87.5	100	µA
$I_{FBclamp}$	Maximum FB internal current source when FB is clamped	For UCC256612−Q1, UCC256613−Q1	150	175	200	µA
$\Delta V_{FBclamp}$	FB pin voltage variation when FB pin sink current ranges from (Iopto = 1.06IFB) to (Iopto = IFB + 0.94 × IFBClamp)	(Iopto = 1.06IFB) to (Iopto = IFB + 0.94 × IFBClamp)			0.5	V
f_{-3dB}	Feedback chain −3dB cut off frequency (2)	VFBReplica from 4.5V to 0.5V	1			MHz

6.5 Electrical Characteristics (continued)

All voltages are with respect to GND, −40°C < T_J < 125°C, VCC = 15V, currents are positive into and negative out of the specified terminal, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{FBOLP}	OLP protection(1)			4.75		V
$TOLP_{Fault}$	OLP protection time (1)			100		ms
RESONANT CURRENT SENSE						
V_{ISNS_OCP}	OCP threshold during steady state	For TSET option >2.5V (1)	3.9	4	4.1	V
V_{ISNS_OCP}	OCP threshold during steady state	For TSET option <2.5V	3.4	3.5	3.6	V
$V_{ISNS\_OCP\_SS}$	OCP threshold during soft start		2.9	3	3.1	V
n_{OCP}	Number of OCP cycles before OCP fault is tripped (1)			7		
n_{OCP_SS}	Number of OCP cycles before OCP fault is tripped at start-up(2)			50		
$V_{IpolarityHyst}$	ISNS Polarity comparator hysteresis			40		mV
V_{ISNS_ZCS}	ZCS comparator +Ve threshold after Soft Start			150		mV
V_{ISNS_ZCSn}	ZCS comparator −Ve threshold, after Soft Start			−150		mV
$V_{ISNS\_MINCURR\_SS}$	+Ve ISNS threshold during Soft Start			50		mV
$V_{ISNS\_MINCURR\_SSn}$	−Ve ISNS threshold during Soft Start			−50		mV
t_{leb}	Leading edge blanking for ZCS and OCP comparators(1)			250		nS
$TZCS_{Fault}$	Fault detected when ZCS event persists for the indicated time(2)	ZCS Event persists		10		mS
GATE DRIVER						
V_{LOL}	LO output low voltage	I_{sink} = 20mA			0.12	V
$V_{RVCC} - V_{LOH}$	LO output high voltage	I_{source} = 20mA			0.3	V
$V_{HOL} - V_{HS}$	HO output low voltage	I_{sink} = 20mA			0.12	V
$V_{HB} - V_{HOH}$	HO output high voltage	I_{source} = 20mA			0.35	V
$V_{HB-HSUVLOFall}$	High side gate driver UVLO falling threshold		6.4	7.25	8	V
$V_{HB-HSUVLOHys}$	High side gate driver UVLO threshold hysteresis		0.78	0.9	1.05	V
$I_{source\_pk\_HO}$	HO peak source current (2)	At VCCP = 12V		−0.6		A
$I_{source\_pk\_LO}$	LO peak source current (2)	At VCCP = 12V		−0.6		A
$I_{sink\_pk\_HO}$	HO peak sink current (2)	At VCCP = 12V		1.2		A
$I_{sink\_pk\_LO}$	LO peak sink current (2)	At VCCP = 12V		1.2		A
BOOTSTRAP						
$I_{BOOT\_QUIESCENT}$	(HB − HS) quiescent current	HB − HS = 12V		60	70	µA
I_{BOOT_LEAK}	HB to GND leakage current	V_{HB} = 600V		0.045	20	µA
$t_{ChargeBoot}$	Length of charge boot state(1)		230	265	300	µs
SOFT START						
SSRamp	Soft Start Ramp time(1)			25		ms
OVP/OTP						
Vclamp_otp1	Clamp Voltage at 0mA(1)	At 0mA current flowing through the clamp	1.35	1.5	1.65	V

6.5 Electrical Characteristics (continued)

All voltages are with respect to GND, −40°C < T_J < 125°C, VCC = 15V, currents are positive into and negative out of the specified terminal, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Vclamp_otp2	Clamp Voltage at 1mA(1)	At 1mA current flowing through the clamp	2.9	3.5	4.1	V
I_{OTP}	Current source on the BW/OTP pin			100		uA
V_{OVPpos}	Output voltage OVP − Threshold rising			3.5		V
$VOTP_{Neg}$	OTP − Threshold falling			0.8		V
$OTP_{CompHys}$	OTP comparator hysteresis		60	90	130	mV
$OVP_{CompHys}$	OVP comparator hysteresis		60	100	145	mV
$OTPBlanking_{start-up}$	OTP blanking time at start-up			50		ms
$TOTP_{Fault}$	OTP Fault detection time			330		uS
$TOVP_{Fault}$	OVP Fault detection time(2)			40		uS
TSET						
$I_{TSETPrgm}$	TSET pin sourcing current for programming			10		uA
LL						
I_{LLPrgm}	LL pin sourcing current for Burst mode transition threshold programming(2)			10		uA
t_{LLPrgm}	Burst mode transition threshold programming time(2)			2		ms
ADAPTIVE DEADTIME						
dV_{HS}/dt	Detectable slew rate (falling slope) (2)		0.1		200	V/ns
FAULT RECOVERY						
$t_{PauseTimeOut}$	Paused timer (1)			1		s
THERMAL SHUTDOWN						
T_{J_r}	Thermal shutdown temperature (1)	Temperature rising	125	150		°C
T_{J_H}	Thermal shutdown hysteresis (1)			20		°C

(1) Not tested in production. Validated by characterization
(2) Not tested in production. Validated by design

6.6 Switching Characteristics

All voltages are with respect to GND, -40°C< T_J =T_A < 125°C, VCC =15V, currents are positive into and negative out of the specified terminal, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{r(LO)}$	Rise time	10% to 90%, 1nF load		30	60	ns
$t_{f(LO)}$	Fall time	10% to 90%, 1nF load		20	30	ns
$t_{r(HO)}$	Rise time	10% to 90%, 1nF load		30	60	ns
$t_{f(HO)}$	Fall time	10% to 90%, 1nF load		15	50	ns
$t_{DT(min)}$	Minimum dead time (1)			50		ns
$t_{DT(max)}$	Maximum dead time (dead time fault) (1)	ZCS event is not detected		1		µs
$t_{DT(max\_ZCS)}$	Maximum dead time (dead time fault) (1)	ZCS event is detected		1.1		µs
$t_{ON(min)}$	Minimum gate on time			250		ns
$t_{ON(max)}$	Maximum gate on time			10		µs

All voltages are with respect to GND, -40°C< T_J =T_A < 125°C, VCC =15V, currents are positive into and negative out of the specified terminal, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{Ipol(ZCS)}$	Blanking time after which the IPOL signal can be used to terminate DT	ZCS event is detected		500		ns

(1) Not tested in production. Verified by design

6.7 Typical Characteristics

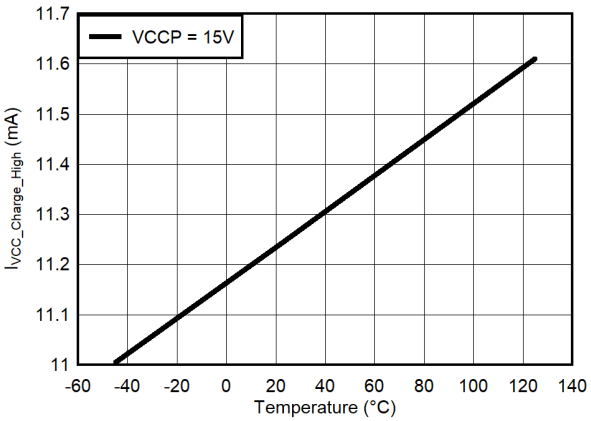


Figure 6-1. $I_{VCC\_Charge\_High}$ vs Temperature

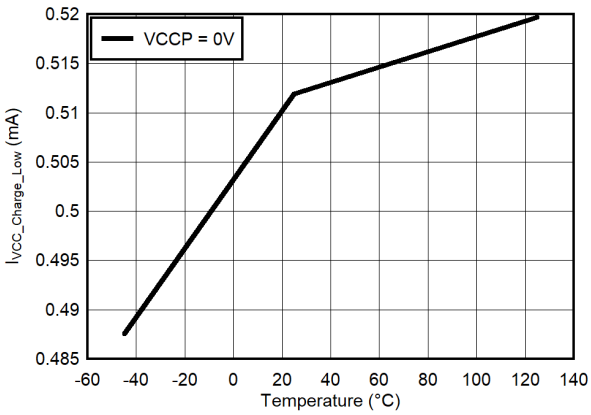


Figure 6-2. $I_{VCC\_Charge\_low}$ vs Temperature

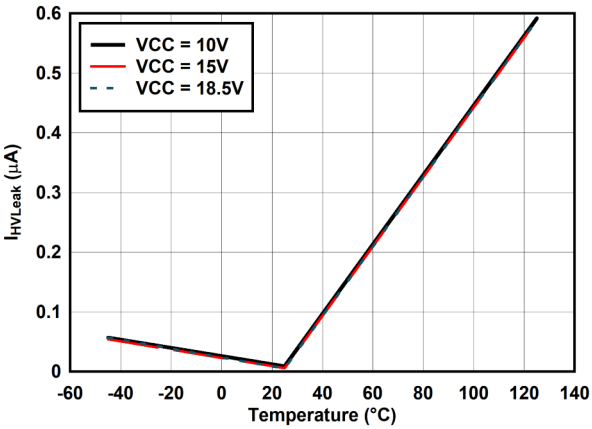


Figure 6-3. I_{HVLeak} vs Temperature

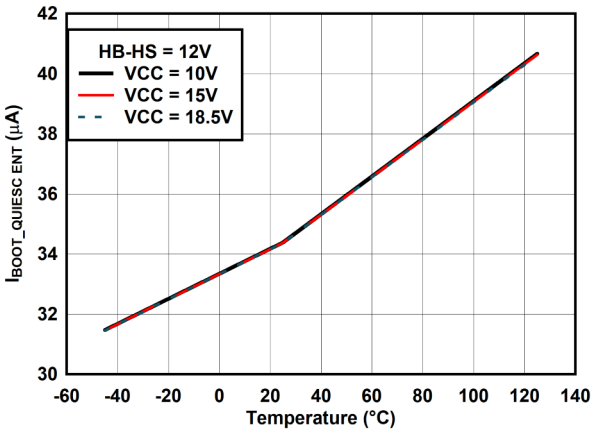


Figure 6-4. $I_{BOOT\_QUIESCENT}$ vs Temperature

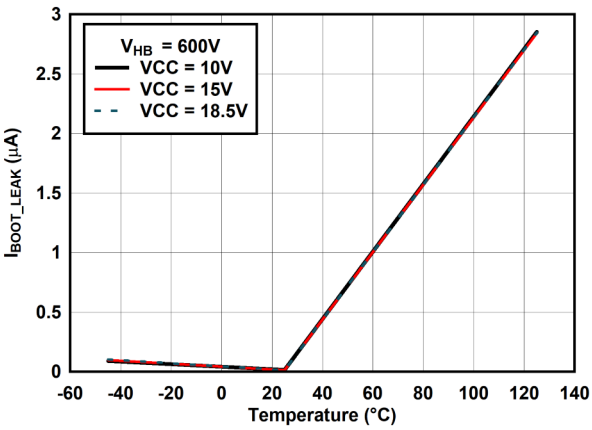


Figure 6-5. I_{BOOT_LEAK} vs Temperature

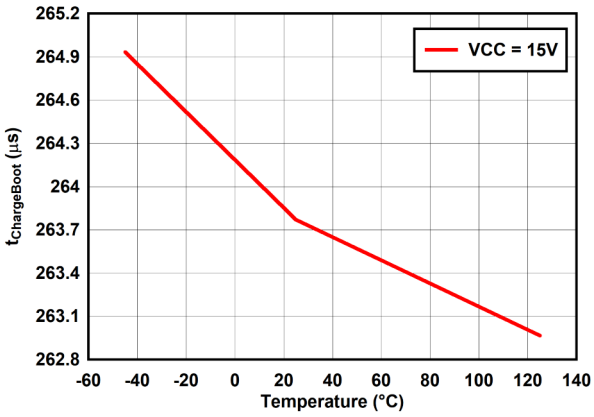


Figure 6-6. $t_{ChargeBoot}$ vs Temperature

6.7 Typical Characteristics (continued)

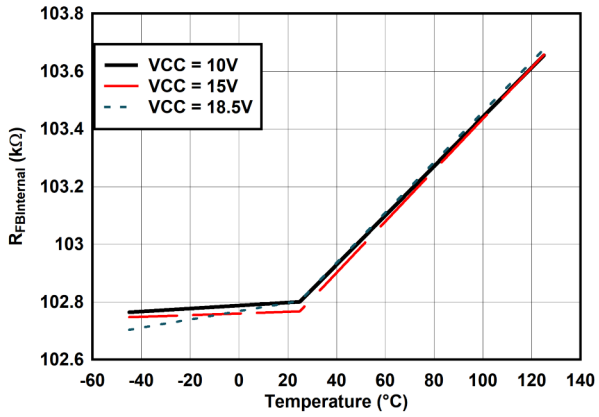


Figure 6-7. $R_{FBInternal}$ vs Temperature

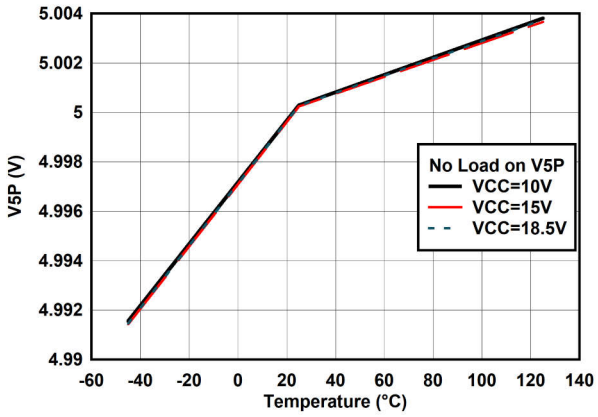


Figure 6-8. V5P (no load) vs Temperature

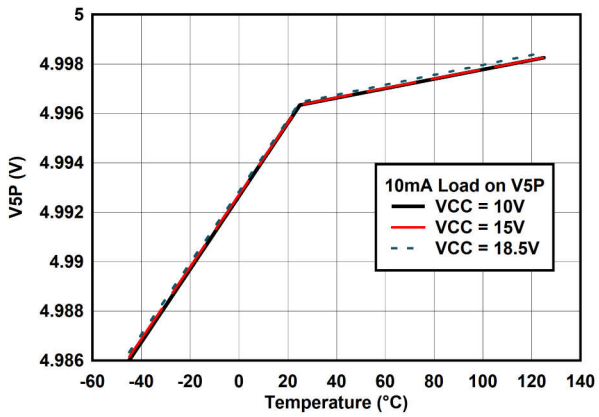


Figure 6-9. V5P (10mA Load)vs Temperature

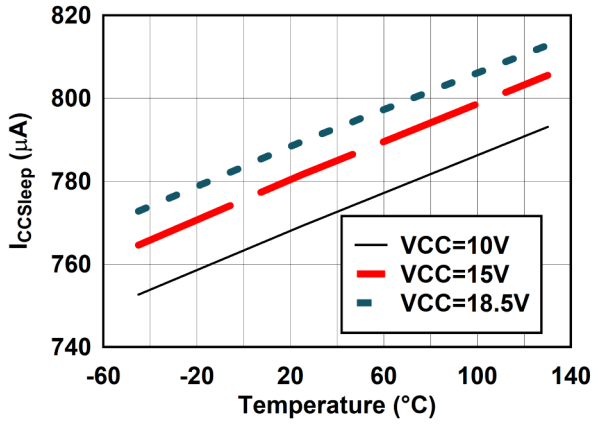


Figure 6-10. $I_{CCSleep}$ vs Temperature

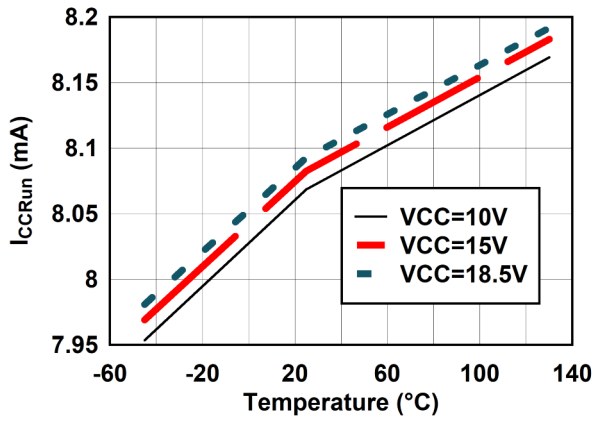


Figure 6-11. I_{CCRun} vs Temperature

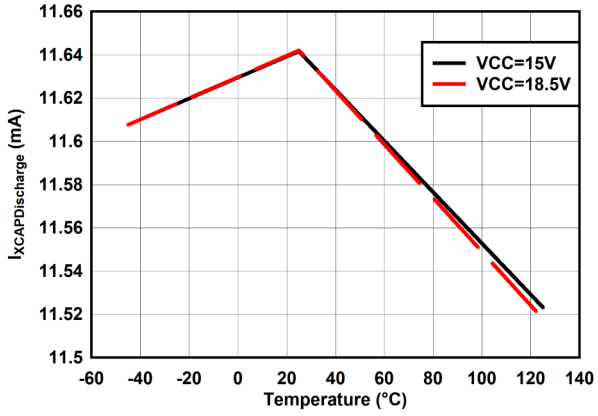


Figure 6-12. $I_{XCAPDischarge}$ vs Temperature

6.7 Typical Characteristics (continued)

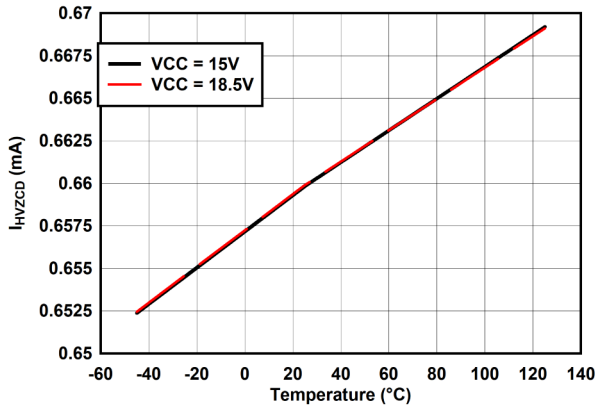


Figure 6-13. I_{HVZCD} vs Temperature

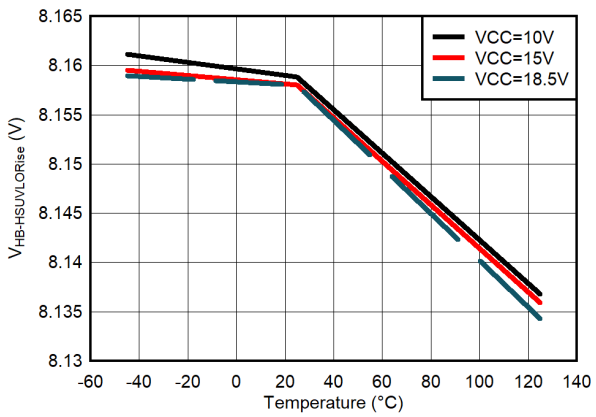


Figure 6-14. $V_{HB-HSUVLORise}$ vs Temperature

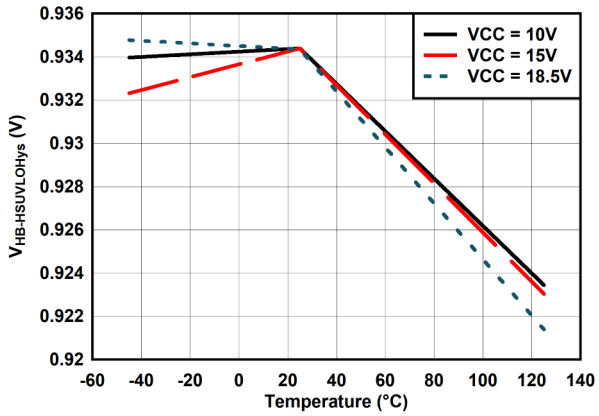


Figure 6-15. $I_{HB-HSUVLOHys}$ vs Temperature

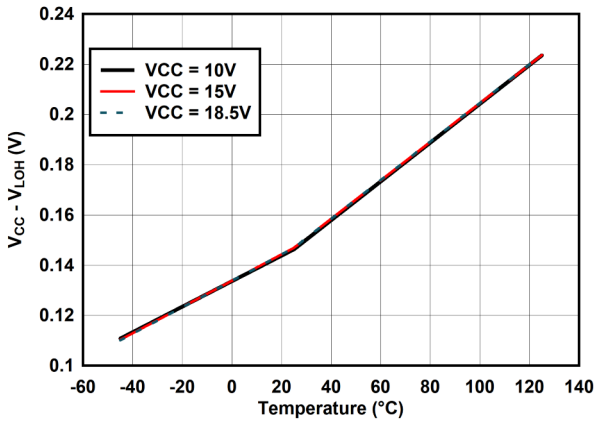


Figure 6-16. (V_{RVCC}- V_{LOH}) vs Temperature

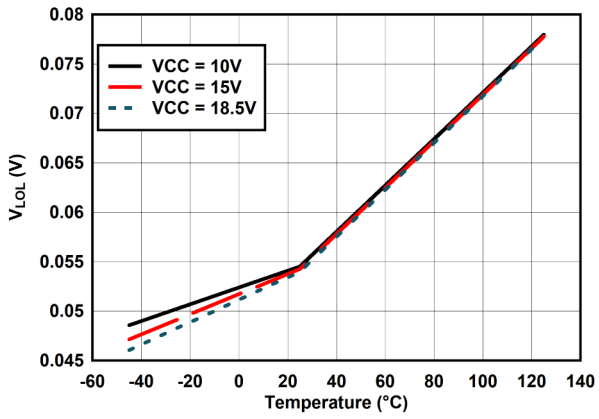


Figure 6-17. V_{LOL} vs Temperature

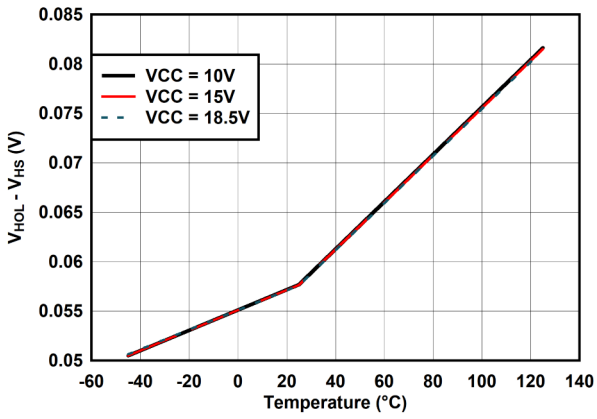


Figure 6-18. (V_{HOL}- V_{HS}) vs Temperature

6.7 Typical Characteristics (continued)

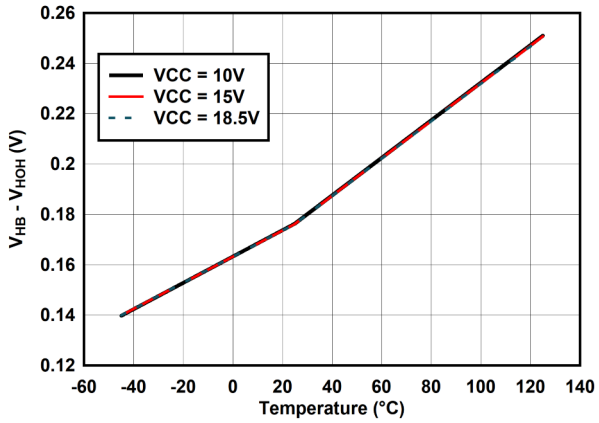


Figure 6-19. (V_{HB} - V_{HOH}) vs Temperature

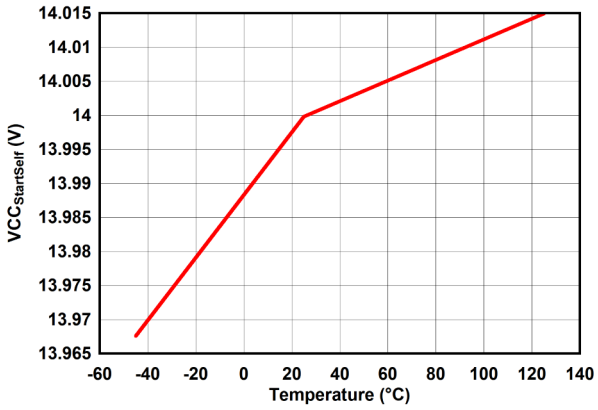


Figure 6-20. $VCC_{StartSelf}$ vs Temperature

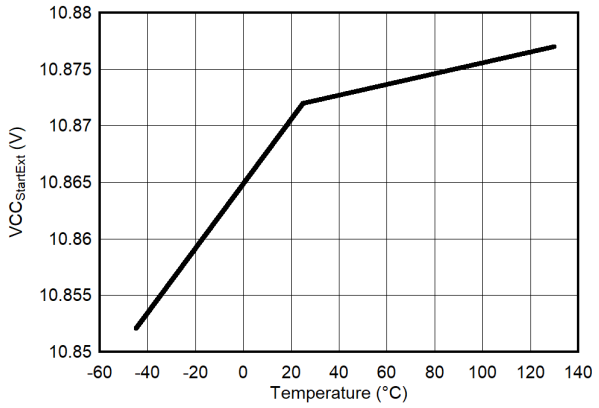


Figure 6-21. $VCC_{StartEXT}$ vs Temperature

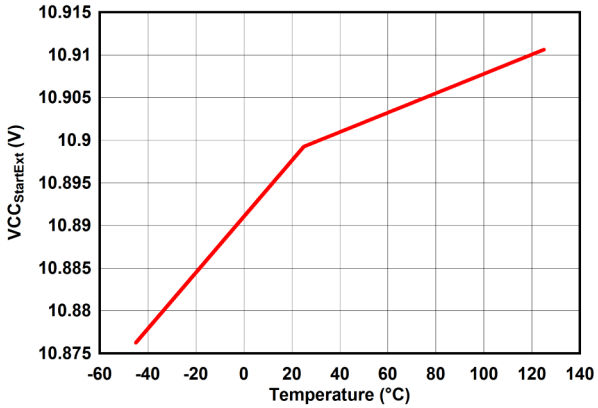


Figure 6-22. $VCC_{StartExt}$ vs Temperature

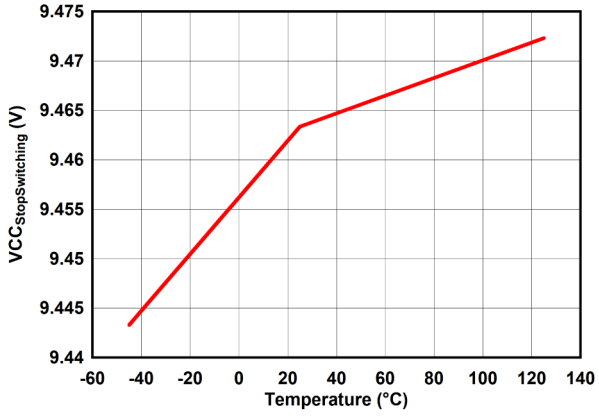


Figure 6-23. $VCC_{StopSwitching}$ vs Temperature

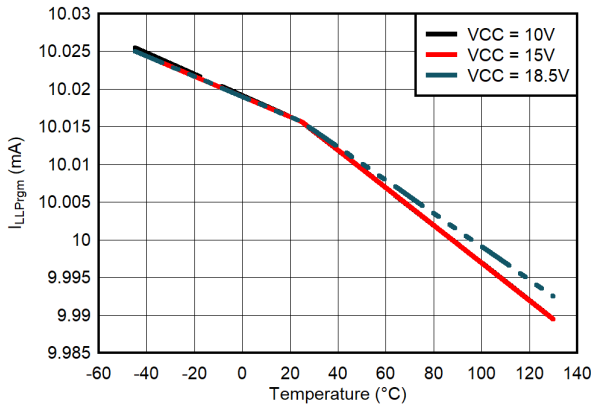


Figure 6-24. I_{LLPrgm} vs Temperature

7 Detailed Description

7.1 Overview

The UCC25661x-Q1 family is a fully featured LLC resonant controller for isolated power supplies. The UCC25661x-Q1 family incorporates high levels of integration and several design features to accommodate wide input and output voltage operation, high power density, and increased reliability of the LLC power stage.

The novel control scheme input power proportional control (IPPC) offers excellent transient performance inherent in the current mode controls, while enabling a linear relationship between input power and control signal across wide input and output voltage variation. The IPPC control enables consistent light load, burst mode performance operation across a wide input and output voltage variation.

Some of the new features in UCC25661x-Q1 family are specified below:

- IPPC enables better burst mode and dynamic response under wide input and output voltage operation
- New operation modes to increase light load efficiency while reducing audible noise
  - High-frequency (HF) pulse skip for improved light load efficiency
  - Low-frequency (LF) burst mode for reduced stand by power consumption
  - Programmable light-load and burst-mode thresholds
  - Adaptive burst-mode threshold adjustment to accommodate input voltage change
- Up to 750kHz full-load switching frequency enables high power density designs
- Combined resonant current sensing with internal control voltage generation, improves control robustness
- Input voltage feed forward
- Extended gain range (EGR), benefits include:
  - Enables better support for wider input and output voltage range applications, in addition to IPPC
  - Increases the availability of power from wide input voltage range when PFC is disabled
- Integrated protections include:
  - Fast 50ns cycle-by-cycle current limiting
  - OCP fault to protect under short circuit conditions
  - Over power protection (OPP) to limit peak input power, except UCC256615-Q1 OPP does not generate fault
  - Zero current switching (ZCS) avoidance scheme to eliminate capacitive region operation
  - Adaptive soft start for reduced inrush current and eliminating reverse recovery at start-up
  - External OVP/OTP protection
  - Input and bias supply (VCCP) UVLO
  - Input voltage feed forward
  - OCP/OLP decoupling allows protection thresholds to be set independently

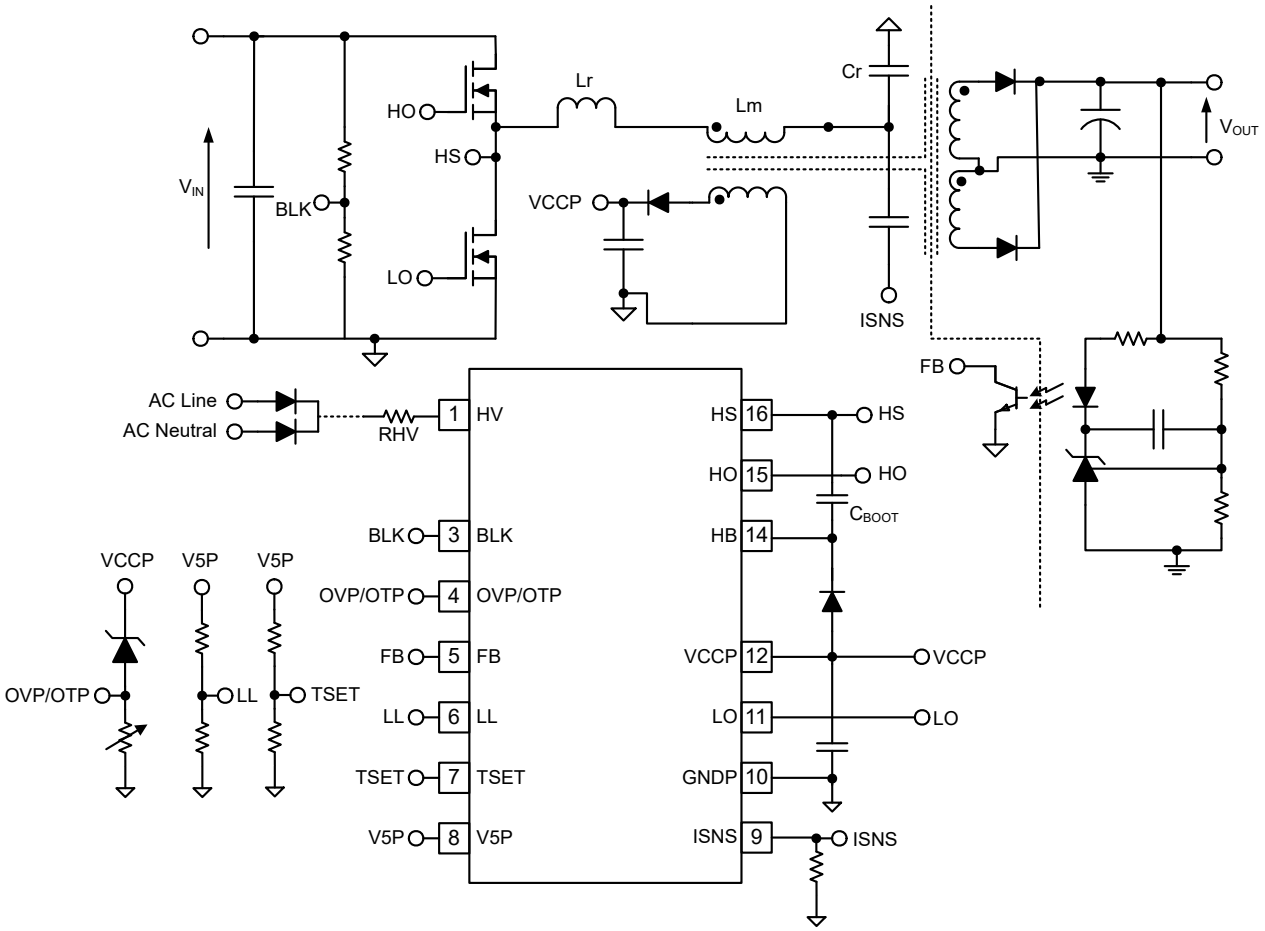
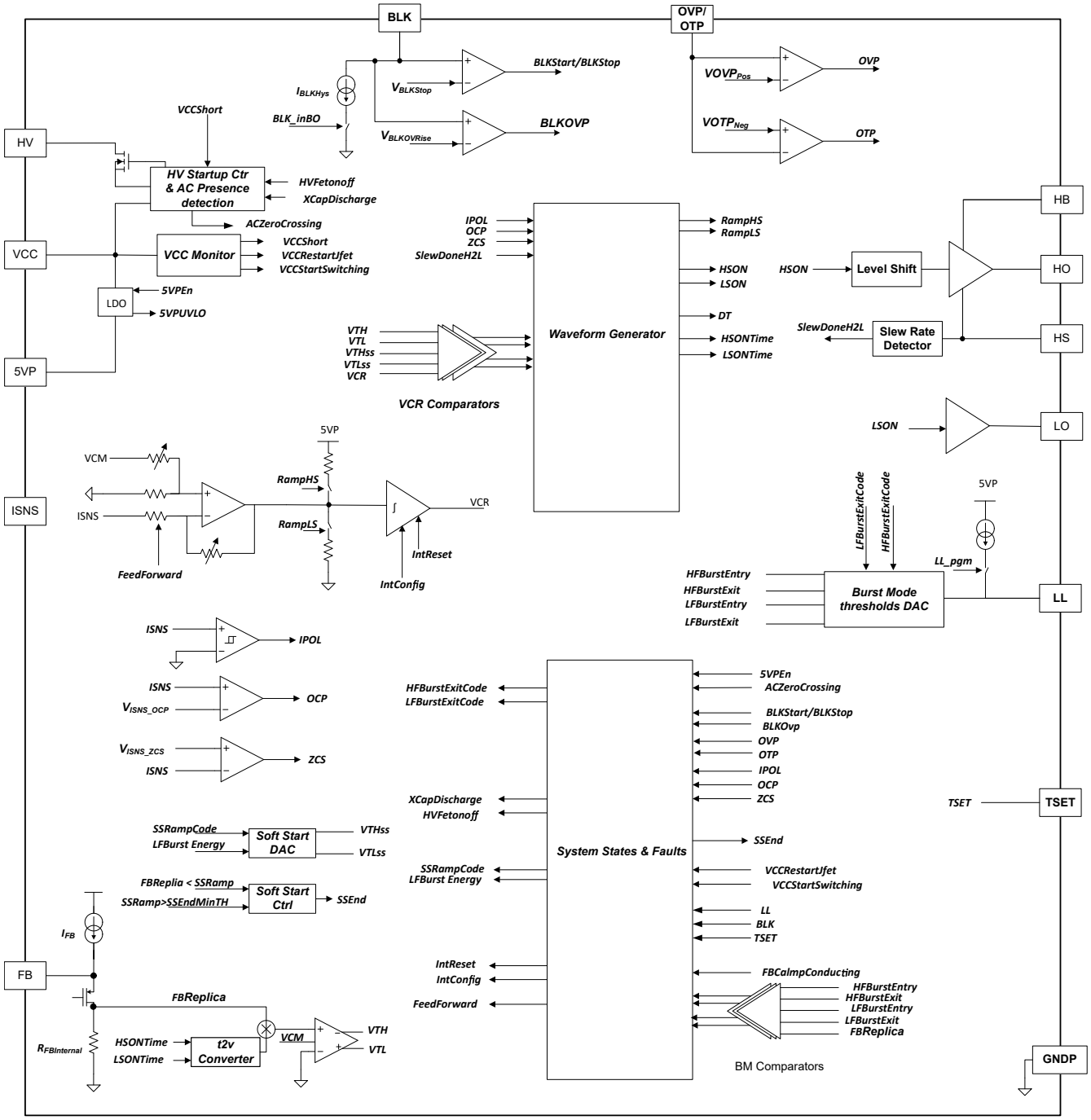


Figure 7-1. Simplified Application Schematic

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Input Power Proportional Control

The previous generation of TI LLC controllers use a version of charge control called hybrid hysteretic control (HHC). An improved version of HHC, called input power proportional control (IPPC) is used in the UCC25661x-Q1 family LLC controller. Compared to traditional direct frequency control, where the control signal is proportional to the switching frequency, traditional charge control methods deliver faster transient response while simplifying compensator design as the power stage transfer function becomes a first order system. In traditional charge control, both input current and switching frequency determine the control signal. IPPC significantly reduces the control signals dependency on switching frequency, thereby minimizing the impact of input and output voltage variations.

IPPC brings in the following advantages:

- Control signal is proportional to input power
- Consistent burst mode and over load performance in wide LLC (WLLC) operation application
- Retains faster load transient performance and improves line transient performance

The UCC25661x-Q1 family measures the resonant tank current on the ISNS pin through an external differentiator formed by capacitor C_{ISNS} and resistor R_{ISNS}. The voltage on the ISNS pin is integrated in the VCR synthesizer block to form an internal VCR signal *VCR_synth*.

The VCR Synthesizer block applies feed forward gain based on the BLK pin voltage, applies ramp compensation to generate the compensated internal VCR signal.

The compensated internal VCR signal is then compared with two sets of thresholds to control the high side switch turn-off (V_{TH}) and low side switch turn-off (V_{TL}). The thresholds V_{TH} and V_{TL} generate from the internal control signal FBReplica and the high-side and low-side switch on-time from the previous half switching cycle. During the soft start, the V_{TH} and V_{TL} thresholds generate based on the internal soft start ramp to minimize the resonant tank inrush current during start-up.

In Figure 7-2, the high-side and low-side switches are controlled based on the internal VCR signal and comparator thresholds V_{TH} and V_{TL}. When the VCR is higher than V_{TH}, the high-side switch is turned off. When VCR is lower than V_{TL}, the low-side switch is turned off.

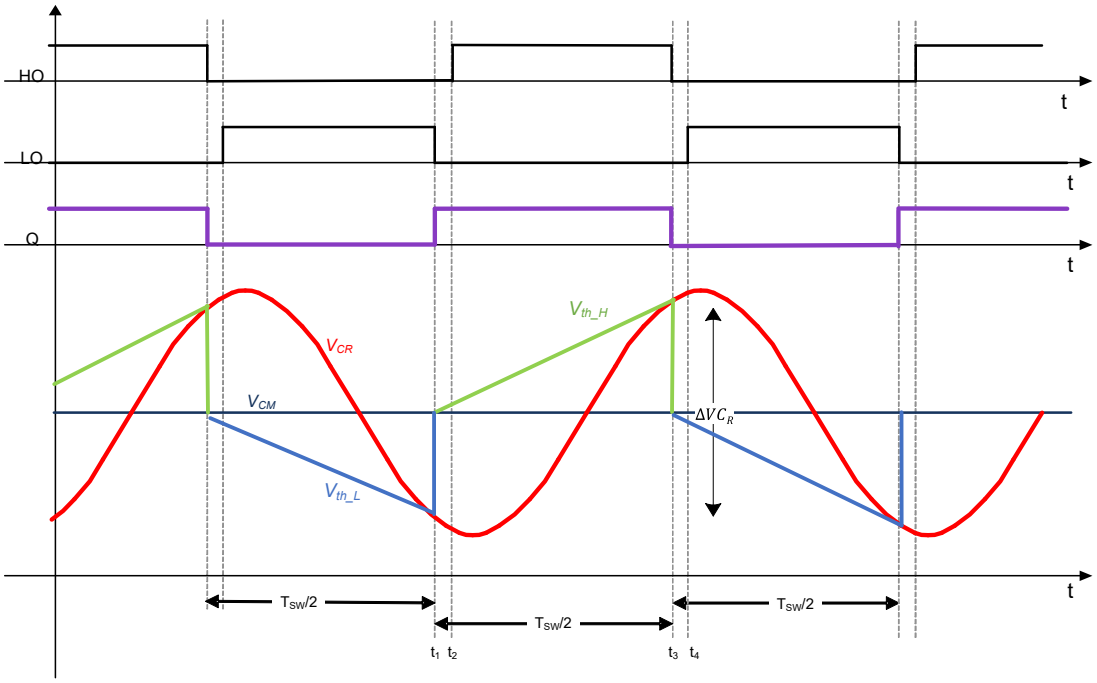


Figure 7-2. IPPC Basic waveforms

FBReplica is the internal voltage representation of the feedback pin (FB) current. Section 7.3.3 defines the feedback chain. Calculate the comparator thresholds V_{TH} and V_{TL} using the equations below.

$$V_{TH} = (V_{CM} + k \times FBReplica \times Tsw \div 2) \quad (1)$$

$$V_{TL} = (V_{CM} - k \times FBReplica \times Tsw \div 2) \quad (2)$$

$$V_{TH} - V_{TL} = \Delta V_{CR} = k \times FBReplica \times Tsw \quad (3)$$

7.3.1.1 Voltage Feedforward

By implementing input voltage feed forward, the control signal is proportional to the input power P_{inavg}.

Rewrite Equation 4 with input voltage feedforward applied where K_1 and K_2 are internal synthesizer gains.

$$FBReplica = \frac{2}{C_r} \times K_1 \times Pin_{avg} + K_2 \times I_{RAMP} \quad (4)$$

The BLK pin periodically senses the input voltage to the LLC power stage. A periodic average of the input voltage adjusts the feed forward gain to make the control signal proportional to input power. Section 7.3.2 contains more details.

7.3.2 VCR Synthesizer

The UCC25661x-Q1 family implements a VCR synthesizer which integrates the resonant tank current to form a internal representation of the resonant capacitor voltage. By implementing the VCR synthesizer internally, the UCC25661x-Q1 family provides the ability to support very high frequency start-up with controlled inrush currents and feed forward gain stage. The internal VCR synthesizer also makes the controller less susceptible to external noise picked up on the ISNS pin, making the controller more robust.

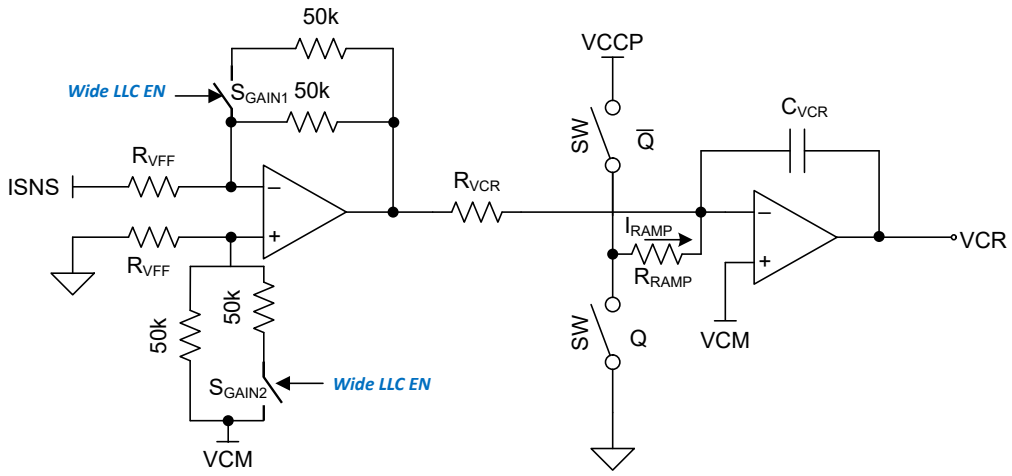


Figure 7-3. VCR Synthesizer Block Diagram

The first stage of the VCR synthesizer consists of a programmable gain stage, used to implement the input voltage feed forward function. The second stage consist of a programmable integrator with ramp compensation. The UCC256614-Q1 has extended gain range (EGR) enabled. EGR feature helps to reduce the FBReplica variation when input voltage of the LLC changed over a wide range (3:1) by reducing the gain of the programmable gain stage of the VCR synthesizer by factory programming the switches S_{GAIN1} *and* S_{GAIN2} to on. To accommodate a wide frequency range of LLC power stages, the time constant of the integrator is externally configurable at start-up to meet the needs of the design using the TSET pin.

During start-up, an external resistor divider connected between V5P and GNDP programs TSET. Connect the center node of the external divider to TSET pin. During the programming phase, a constant current $I_{TSETPrgm}$

feeds to the TSET pin and the resulting voltage is measured through a ADC (V_{TSETA}). After $I_{TSETPrgm}$ turns off, measure the voltage of the TSET resistor divider (V_{TSETB}).

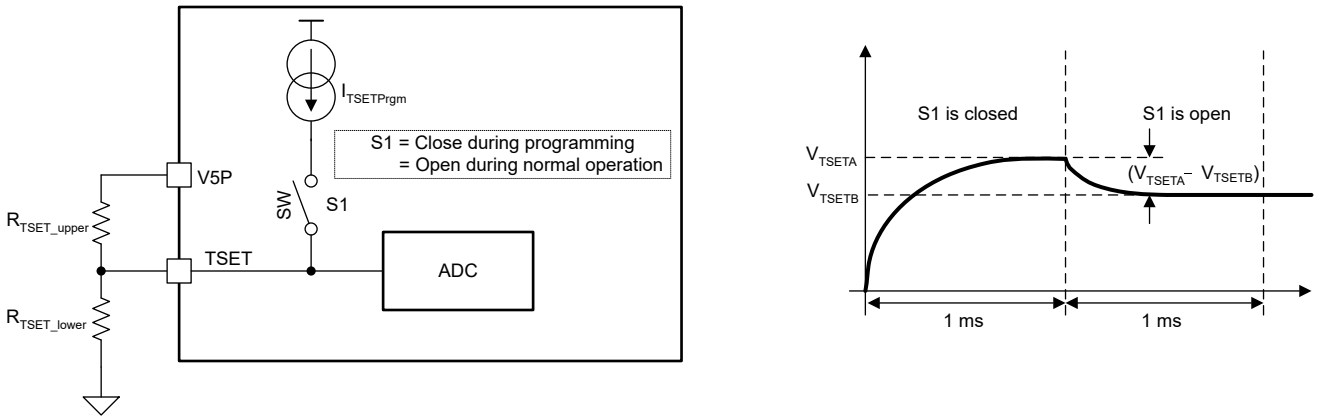


Figure 7-4. TSET Pin Programming

The voltage programmed for VTSETB voltage configures the minimum operating frequency for IPPC operation and the maximum dead time. The difference between VTSETA and VTSETB configures the integrator time constants to set the FBReplica magnitude for a given power output. The difference between VTSETA and VTSETB helps with independently setting the overload power (OLP) and over-current protection (OCP) thresholds.

7.3.2.1 TSET Programming

The V_{TSETB} voltage configures the minimum frequency for IPPC operation and the dead time. $V_{TSETA} – V_{TSETB}$ configures the integrator time constants and sets the FBReplica magnitude for a given power output and helps setting OLP and OCP thresholds independently. In the table value TSET voltage values indicated are nominal values. Maximum and minimum range used for each TSET setting are within ±48mV of the nominal value.

Table 7-1. TSET Programming Options Table

TSET Option Number	TSET Voltage (V) for 3.5V OCP	Minimum Frequency for IPPC Operation (kHz)	Integrator Time Constant (ns)	Maximum Dead-Time (µs)
17	2.295	698.6	68	0.5
16	2.168	591.6	80	0.5
15	2.041	501	93	0.5
14	1.914	424.3	112	0.5
13	1.787	359.3	132	1
12	1.66	304.3	156	1
11	1.533	256.7	184	1
10	1.416	218.2	214	1
9	1.299	184.8	257	1
8	1.182	156.5	304	1
7	1.074	132.5	359	1
6	0.967	112.2	424	1
5	0.850	95	490	1
4	0.742	80.5	588	1
3	0.644	68.1	694	1
2	0.547	57.7	820	1
1	0.450	48.9	968	1
X(1)	< 0.392	—	X	—

(1) Not recommended to use.

7.3.3 Feedback Chain (Control Input)

A voltage regulator circuit located on the secondary side of the isolation barrier provides control of the output voltage. The demand signal from the secondary-side regulator circuit transfers across the isolation barrier using an optocoupler. Use an opto-emulator, such as from ISOM81xx family, if adding external circuitry to provide bias current from the V5P pin. The tradeoff is higher standby power.

A constant current source I_{FB} is generated from VCCP voltage and connected to the FB pin. A resistor RFB connect to the current source with a PMOS in series. During normal operation, the PMOS is always on, and the FB pin voltage is equal to the Zener diode reference voltage plus the voltage drop on the PMOS source to gate.

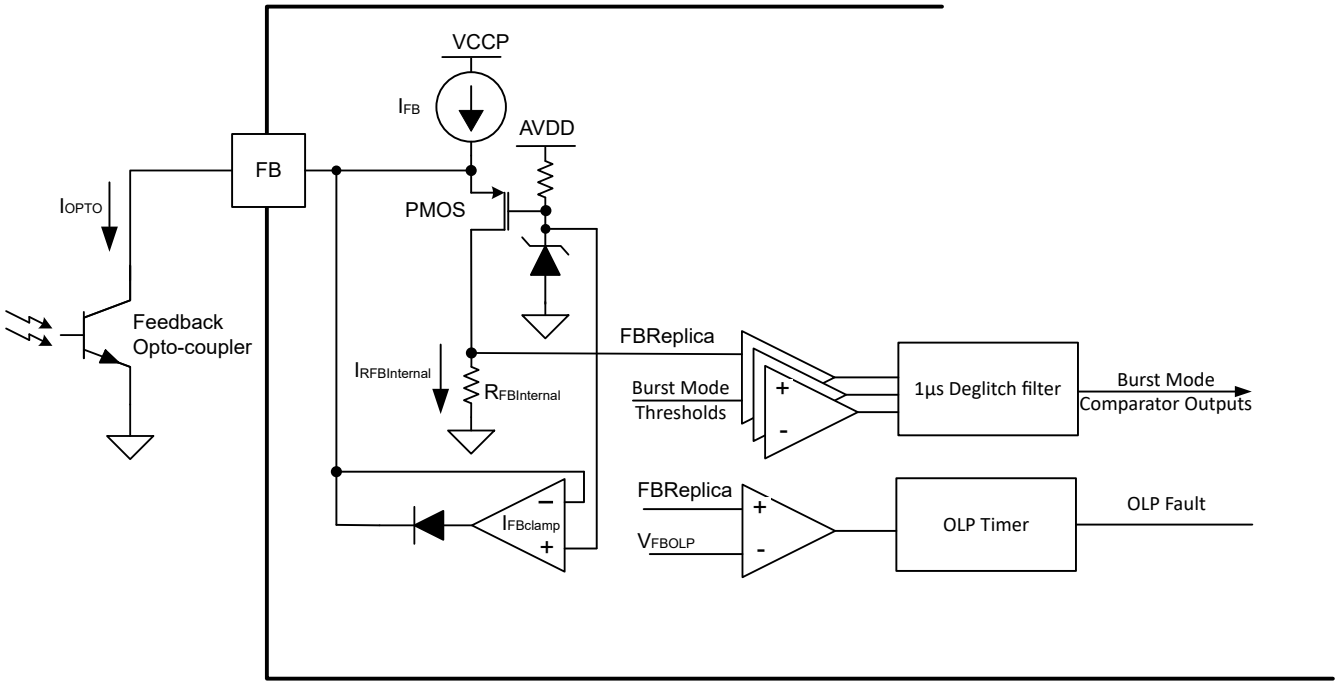


Figure 7-5. Feedback Chain Block Diagram

$$I_{R_{FBInternal}} = I_{FB} - I_{OPTO} \quad (5)$$

The control signal *FBReplica* is calculated using Equation 6.

$$FBReplica = I_{R_{FBInternal}} \times R_{FBInternal} \quad (6)$$

From this equation, when I_{OPTO} increases, $I_{RFBInternal}$ decreases, decreasing the *FBReplica*. As a result, the control signal is inverted. When I_{OPTO} continues to increase and reaches the value of I_{FB}, the FB pin voltage starts to drop because there is not enough current flow through the PMOS. FB pin pulled low impacts the system transient response, due to the extra delay introduced by charging the parasitic capacitor of the optocoupler to pull up the FB pin voltage. Use a FB pin voltage clamp circuit to prevent a power supply control issue. When FB pin voltage drops below the FB pin clamp voltage threshold, turn on an extra current source to clamp the FB voltage. The clamp strength is $I_{FBClamp}$. The FB pin clamp circuit improves the system transient performance from light load to heavy load. Figure 7-6 shows the FB pin clamp operation.

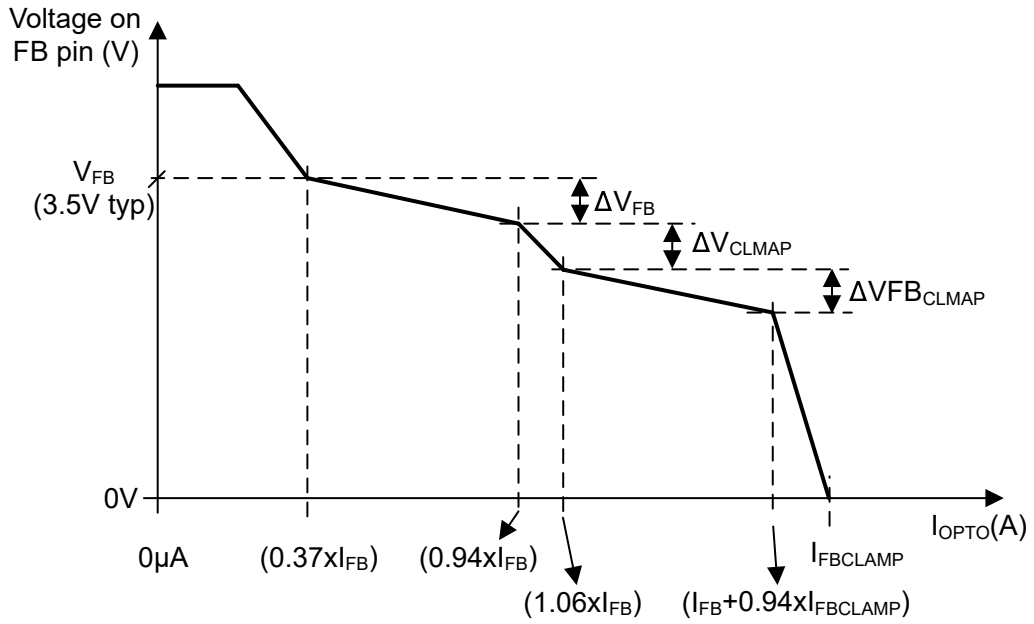


Figure 7-6. FB Pin Voltage versus FB Pin Current

7.3.4 Adaptive Dead Time

The UCC25661x-Q1 family implements a high-speed low latency slew-rate detection block to optimize the dead time between high-side and low-side pulses. The adaptive dead-time block adjusts the dead time to prevent shoot-through or excessive body-diode conduction.

At the core of the adaptive dead time block is the slew rate detector block, capable of detecting slew rates up to 200V/ns; UCC25661x-Q1 family is an excellent choice for use in high frequency resonant converters.

In burst mode, during a ZCS prevention operation or in power stages where the slew rate can be very slow, use the resonant tank current polarity signal (Ipolarity comparator output) to augment the slew-rate detector.

Because of the natural symmetric operation of LLC, only the dead time between high-side switch turn off and low-side switch turn on are determined by the slew rate detector. Dead time is copied and then applied to the dead time between low-side MOSFET turn off and high-side MOSFET turn on. There are a few exceptions where the dead time is not copied. The conditions are listed below.

- Missing slew rate detector signal in the previous high to low transition
- ZCS detection in the previous cycle

Under the above-mentioned conditions, use the Ipolarity comparator based on the ISNS signal to adjust the dead time during low to high transitions.

7.3.5 Input Voltage Sensing

The input voltage sensing through BLK pin is used to implement multiple functions listed below:

- Input voltage brownin and brownout
- Input feedforward (explained in Section 7.3.1)
- Input voltage OVP

7.3.5.1 Brownin and Brownout Thresholds and Options

UCC25661x-Q1 family provides programmable brownin and brownout thresholds. When the voltage on the BLK pin falls below $V_{BLKStop}$, the controller enters brownout state and stops switching. In the brownout state, an additional current sink is turned on to draw I_{BLKHys} form the BLK pin. By changing the equivalent resistance connected to the pin externally, program the actual brownin voltage.

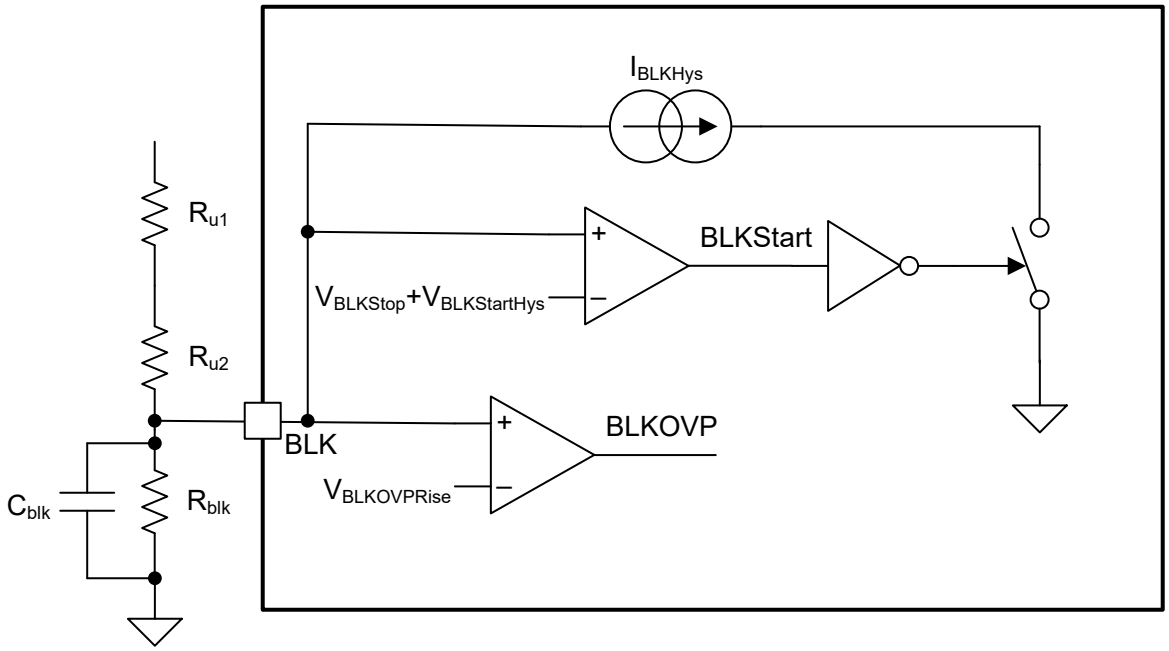


Figure 7-7. BLK Pin Input Voltage Sensing Architecture

When brownout is detected, the controller stops switching. If BLK voltage rises above the brownin voltage, the controller immediately begins soft-start and does not wait for fault idle time.

7.3.5.2 Output OVP and External OTP

UCC25661x-Q1 family uses a multifunction pin (OVP/OTP) that monitors for output overvoltage and external over-temperature conditions. Output voltage is monitored through reflected voltage on bias winding and supply voltage VCCP.

A Zener diode is connected between VCCP and the OVP/OTP pin. Under normal operating conditions, the Zener does not conduct and the OVP/OTP pin voltage is the result of the NTC resistance and I_{OTP} source current. If VCCP rises high enough to exceed the Zener breakdown voltage, the voltage on the OVP/OTP pin is pulled high because of the Zener current. If the voltage on OVP/OTP exceeds the $VOVP_{pos}$ threshold for 40us, the controller detects a fault and stops switching.

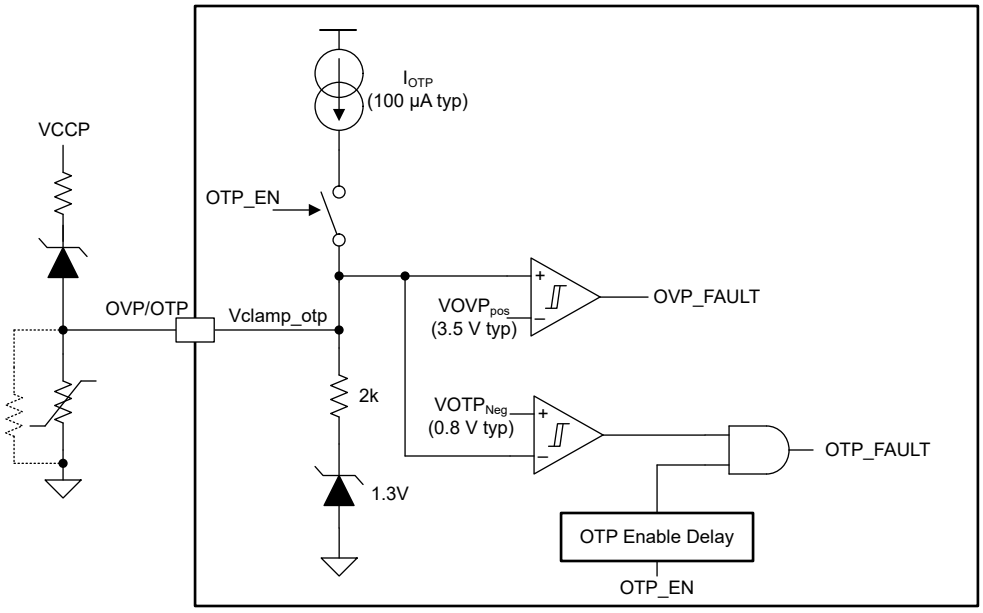


Figure 7-8. OVP/OTP Protection Architecture

An NTC connects OVP/OTP to GNDP. An internal current source, I_{OTP}, flows out of the OVP/OTP pin and into the NTC resistor. Based on the temperature of the NTC, the resulting voltage on the pin compares to $VOTP_{Neg}$ to determine if an external over-temperature fault occurs. Upon detection of external over-temperature protection, UCC25661x-Q1 family moves to the fault state. After the 1s wait period, UCC25661x-Q1 family checks the OVP/OTP pin voltage. If the OVP/OTP pin voltage is higher than $VOVP_{Pos}$, the UCC25661x-Q1 family attempts to restart, or continues to wait in a fault-idle state. During burst mode, the over-temperature protection disables to minimize quiescent current. When transitioning from burst mode to normal switching, the OTP function re-enables.

7.3.6 Resonant Tank Current Sensing

The ISNS pin senses the resonant tank current through a differentiator. Besides serving as over current protection pin, the ISNS pin is also an essential part of the control functions.

The ISNS pin has the following functions.

- Input to the integrator that develops the control voltage, used for IPPC control
- OCP (cycle-by-cycle) protection
- Resonant current polarity detection
- ZCS prevention and dead-time management
- Reverse recovery avoidance at start-up

7.4 Protections

7.4.1 Zero Current Switching (ZCS) Protection

ZCS protection is a necessary function for LLC converters to avoid crossing over into the capacitive region of operation. In the capacitive region, the reverse recovery of the body diode allows both switches to briefly conduct simultaneously, damaging the MOSFETs. In addition, the gain versus frequency relationship inverts in the capacitive region and can cause the converter to completely lose regulation of the power stage.

The goal of the ZCS protection is to confirm that the MOSFET can be turned off before the current inverts, eliminating possibility of a hard reverse recovery of the MOSFET body diode, increasing the reliability of the power stage. The minimum turn off current is set at a threshold which can increase the chances of achieving ZVS, or close to ZVS switching for switches under this condition.

Coupled with the dead time engine which looks at both the slew done signal and the IPOL signal, verify that the opposite MOSFET turns on at the valley point of the V_{DS} voltage, minimizing turn-on losses.

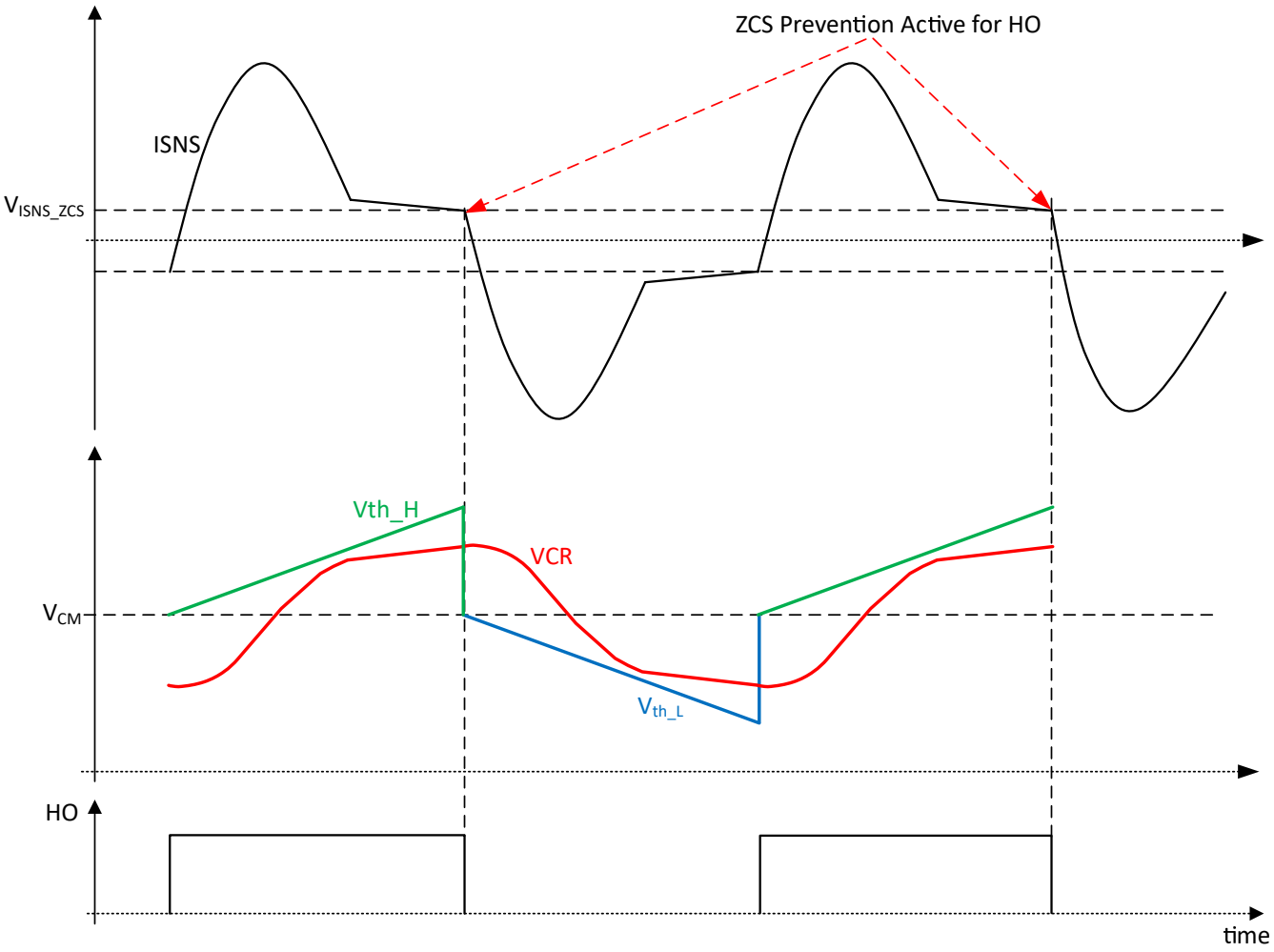


Figure 7-9. ZCS Protection

When operation nears the inductive and capacitive boundary, the resonant current decreases before the gate is turned off. If the ISNS waveform is less than the V_{ISNS_ZCS} threshold, the gate pulse HO is terminated early, instead of waiting for the VCR waveform to cross the VTH boundary. The early gate termination scheme is capable of leaving enough resonant current at the gate turn-off edge to drive the ZVS transition during the dead-time. Similar explanation holds good for the LO gate pulse.

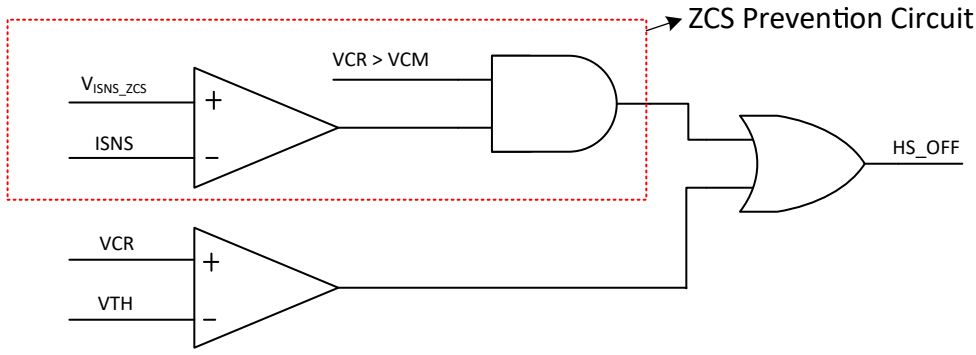


Figure 7-10. ZCS Prevention Scheme When the High-Side MOSFET is On

The shape of the resonant current located below the resonant frequency poses a challenge when detecting the correct falling edge of the resonant current waveform. The UCC25661x-Q1 implements additional logic to check that the correct falling edge of the ISNS signal is detected to avoid false tripping.

To improve robustness against noise, the ISNS ZCS comparators are blanked at the rising edge of HO or LO gate. The same blanking time t_{leb} is used for both the VCR comparators and the ISNS ZCS comparators.

When a ZCS event is detected, the internal soft start ramp voltage slowly reduces. When the internal soft start ramps down, the switching frequency is forced to increase, forcing the converter out of the capacitive region.

In the event of a persistent ZCS condition for a period of $TZCS_{Fault}$, the UCC25661x-Q1 controller ceases switching and move to the fault state.

7.4.2 Minimum Current Turn-off During Soft Start

During start-up, the first few switching cycles on the MOSFET on the primary side undergo body diode reverse recovery and hard switching. This is mainly due to the fact that at start up, the resonant capacitor can have a DC bias voltage which is off from the steady state operating voltage of Vin/2. This leads to a asymmetry in the resonant tank current at start-up. In the first few cycles, asymmetry can be high enough that the current at the point of switch turn-off is in the wrong polarity.

For example, refer to the figure below.

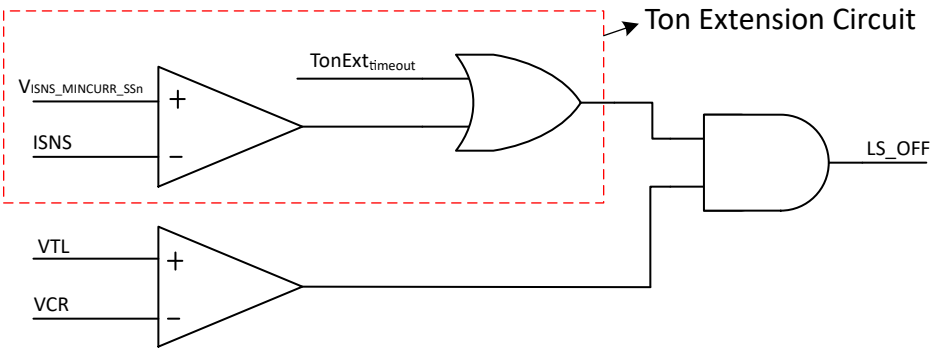


Figure 7-11. Ton Extension Scheme

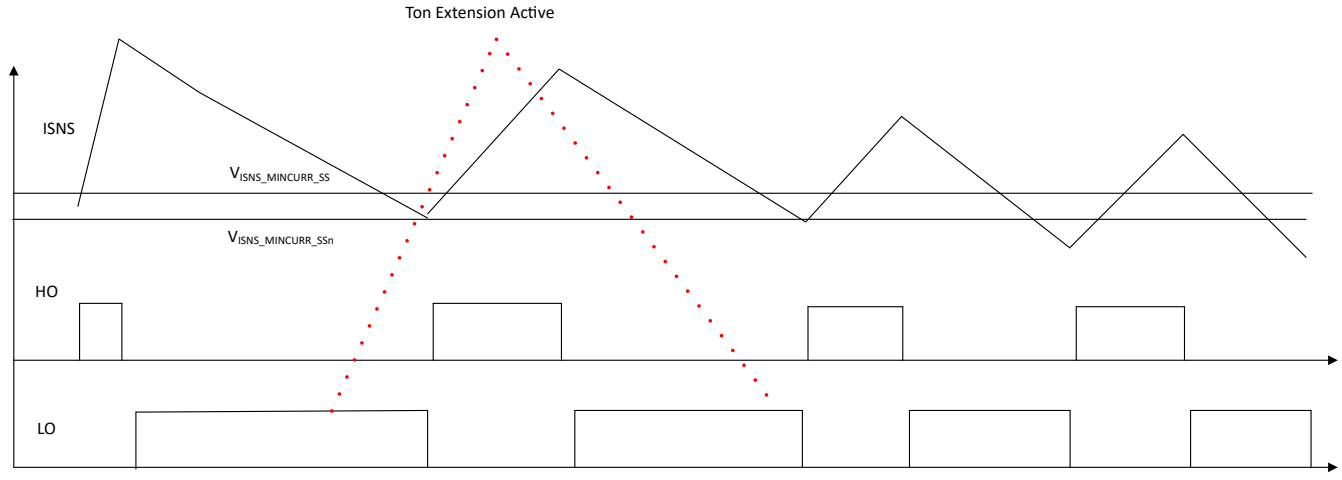


Figure 7-12. ZCS Prevention During Startup

7.4.3 Cycle-by-Cycle Current Limit and Short Circuit Protection

The OCP and cycle-by-cycle current limiting feature in UCC25661x-Q1 family provides a fast (<50ns) response to short circuit.

The cycle-by-cycle protection helps to limit the peak stress in the power stage. When the ISNS voltage is greater than the V_{ISNS_OCP}, the present HO gate pulse is terminated. Correspondingly, during the second half cycle, the present LO pulse is terminated when the corresponding overcurrent limit is detected. If OCP is detected in n_{OCP} (7) consecutive switching cycles during, the device moves to the fault state. During start-up, if OCP condition is detected in n_{OCP_SS}(50) consecutive switching cycles, the devices moves to fault state. The n_{OCP} and n_{OCP_SS} are factory configurable parameters.

7.4.4 Overload Protection (OLP)

Using IPPC with feed forward enables us to get a close correlation between Pout Vs internal control signal FBReplica.

When the FBReplica goes above the V_{FBOLP} (for example, the I_{opto} is reduced to 0µA), the system starts to limit the input power and the OLP timer count increases. If the FBReplica stays above V_{FBOLP} for >(T_{OLP}), the OLP fault is detected and the system enters into a fault restart sequence.

7.4.5 VCC OVP Protection

An internal current limited clamp on the VCCP pin protects the VCCP pin and clamps the gate drive output voltage when the voltage applied to the VCCP pin exceeds the recommended maximum voltage. The clamp has a maximum sink current $IVCC_{Clamp}$. If the current going through the VCC_{Shunt} exceeds $IVCC_{Clamp}$, there is a further increase in the VCCP pin voltage above VCC_OV and UCC25661x-Q1 moves to fault condition and retry after the 1s fault idle time.

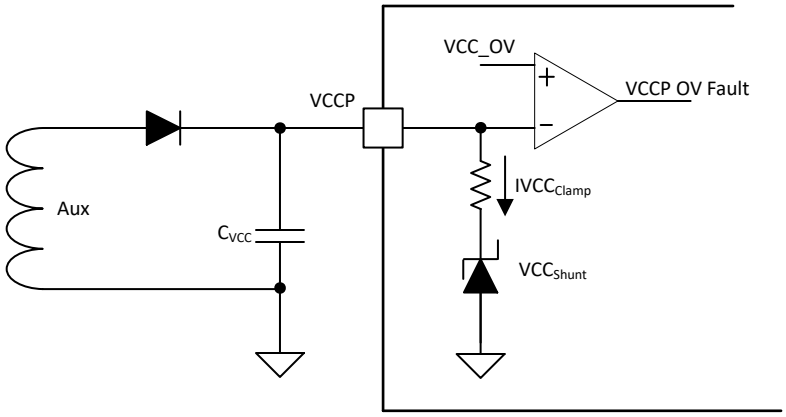


Figure 7-13. VCC Clamp

7.5 Device Functional Modes

7.5.1 Startup

7.5.1.1 With HV Startup

First time start-up sequence

1. When AC is plugged in, voltage is applied on HV pin. If VCCP voltage is below VCC_{Short}, VCCP pin is charged with $I_{VCC\_Charge\_Low}$. If VCCP voltage is higher than VCC_{Short}, VCCP pin is charged with $I_{VCC\_Charge\_High}$.
2. When VCCP voltage is higher than VCC_{UVLOr}, an internal LDO regulates the V5P voltage until the device initialization is complete.
3. V5P is established. LL pin and TSET pin are used for burst mode and internal VCR Synthesizer programming.
4. If the HV start-up option is enabled, the TSET pin outputs high (means PFC OFF) to prevent PFC from turning on before VCCP is full established.
5. When VCCP is higher than $VCC_{StartSelf}$, HV charge current stops. LLC start-up process begins. TSET voltage is kept lower than 1V, allowing PFC to start up.

6. If during stages 3 and 4, VCCP voltage drops below $VCC_{ReStartJfet}$, HV charge current enables again and VCCP gets charged with $I_{VCC\_Charge\_High}$
7. Once LLC finishes start-up, HV charge current is disabled until VCCP drops below $VCC_{ReStartJfet}$.
8. During normal operation if the VCCP voltage falls below $VCC_{StopSwitching}$, a fault occurs and UCC25661x-Q1 family shuts down. Follow normal restart sequence.

Restart sequence

1. After a fault is detected, UCC25661x-Q1 family shuts down. For fault retry mode, after 1s idle time, UCC25661x-Q1 family retries. TSET outputs high when VCCP remains higher than VCC_{UVLOf}.
2. If VCCP voltage is below VCC_{Short}, the VCCP pin is charged with $I_{VCC\_Charge\_Low}$. If VCCP voltage is higher than VCC_{Short}, the VCCP pin is charged with $I_{VCC\_Charge\_High}$. If the VCCP pin voltage is higher than $VCC_{StartSelf}$, HV start-up is not enabled, Phase I is skipped. V5P is established and LL pin is released for burst mode programming.

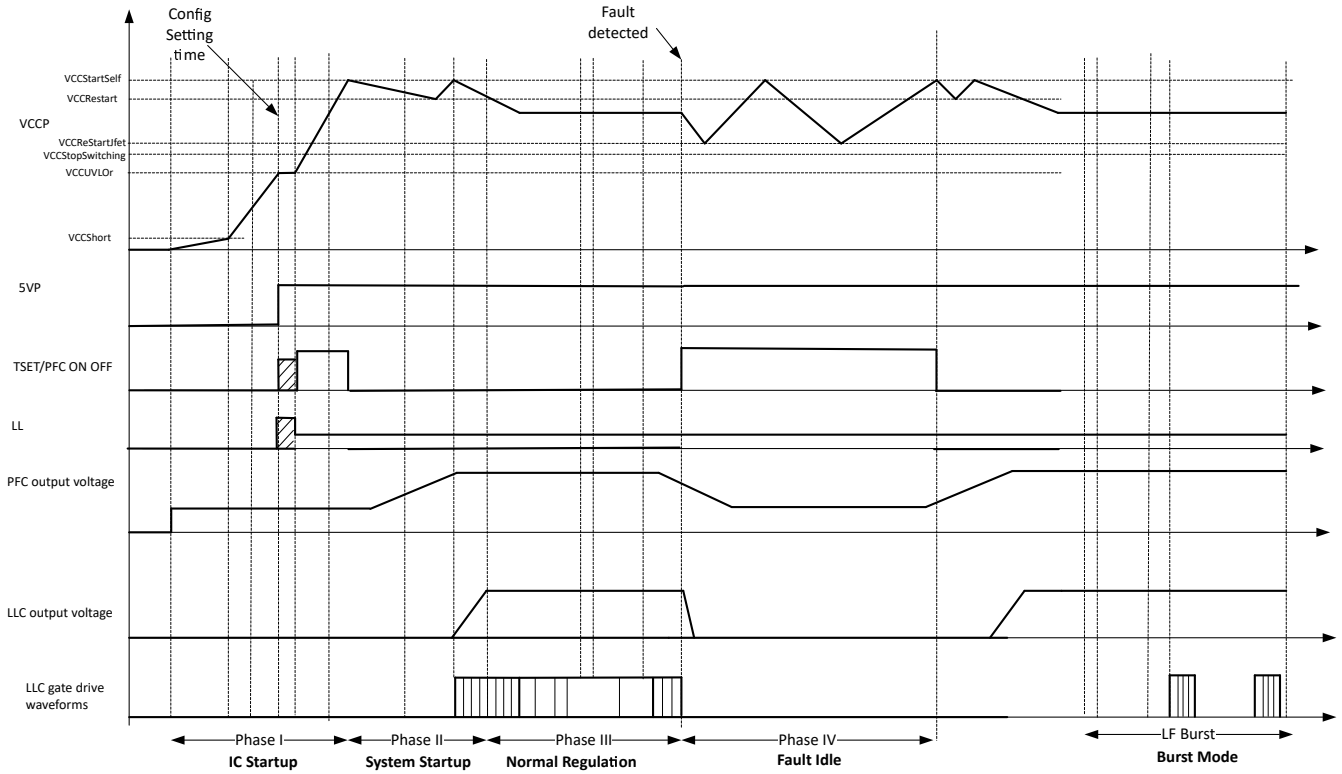


Figure 7-14. Startup Sequence for *HV Startup* Feature Enabled

7.5.1.2 Without HV Startup

When HV start-up is disabled, the PFC on and off signal is also disabled. The start-up sequence is as follows:

1. When VCCP voltage is higher than VCC_{UVLOr}, V5P is established
2. LL pin and TSET pin are used for burst mode and internal VCR integrator programming.
3. When VCC drops below VCC_{UVLOf}, the V5P turns off and system shuts down.

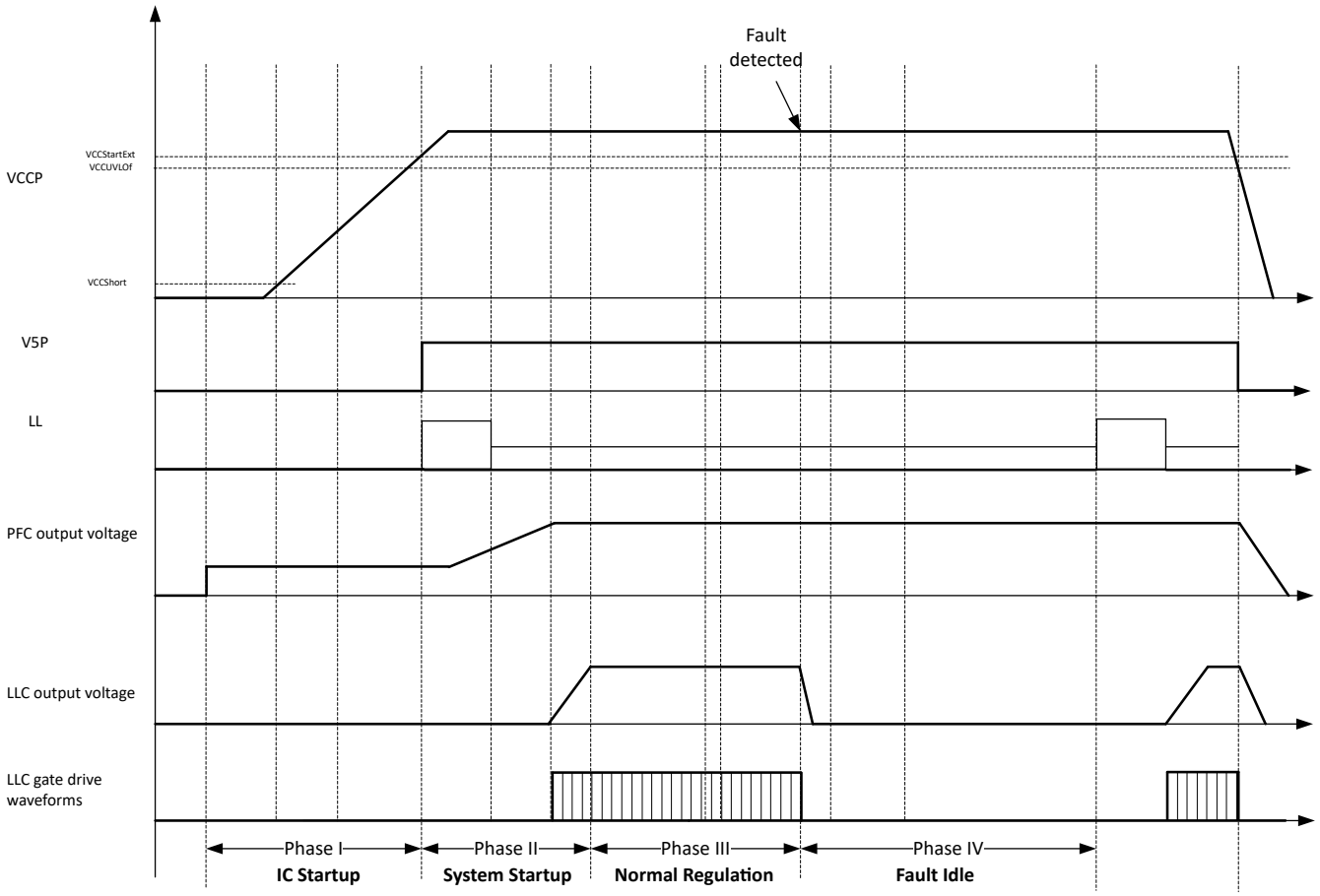


Figure 7-15. Startup Sequence for *HV Startup* Feature Disabled

7.5.2 Soft Start Ramp

The soft start ramp is internally generated in the UCC25661x-Q1 family. A fixed maximum soft start time of 25ms is internally generated to reduce inrush current at start-up while allowing a fast output voltage during ramp-up.

7.5.2.1 Startup Transition to Regulation

In UCC25661x-Q1 family, a new soft start is implemented to control the inrush current at start up. The new scheme avoids premature soft start termination and provides smooth transition between soft start and closed loop regulation.

At start up, internal Soft start voltage (*SSRamp*) ramps up using a defined slope and the *FBReplica* is as high as the output voltage is, below the regulation voltage. The lower of the two signals determines the turn-off control of the power stage switches.

The soft start is exited only after the *SSRamp* is above a minimum threshold, avoiding any premature soft start exit.

7.5.3 Light Load Management

7.5.3.1 Operating Modes (Burst Pattern)

UCC25661x-Q1 family burst mode algorithm minimizes audible noise, while improving light load efficiency. This balance is accomplished by maintaining the burst packet frequency to either be above the audible range (>25kHz) or to maintain the burst packet frequency to be at the very low end of the audible region (<400Hz). UCC25661x-Q1 family employs two burst mode patterns: high-frequency (HF) pulse skip and low-frequency (LF) burst.

HF burst packet includes a fixed number of LO and HO pulses. The purpose of HF burst is to maintain the burst frequency higher than the audible frequency range. In Figure 7-16, the low-side gate is enabled on the second valley of the switch node to begin delivery of the next HF burst packet.

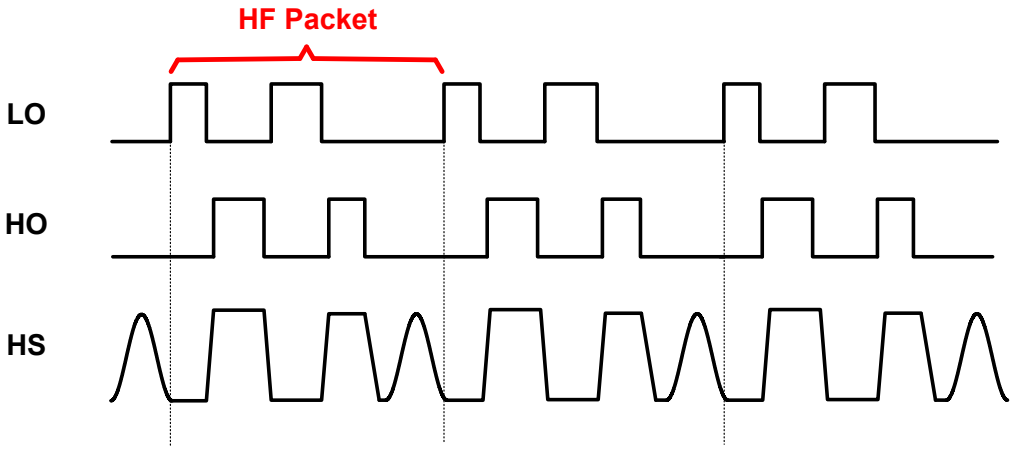


Figure 7-16. High Frequency Pulse Skip Packet

LF burst includes a number of HF burst packets and a LF burst off period.

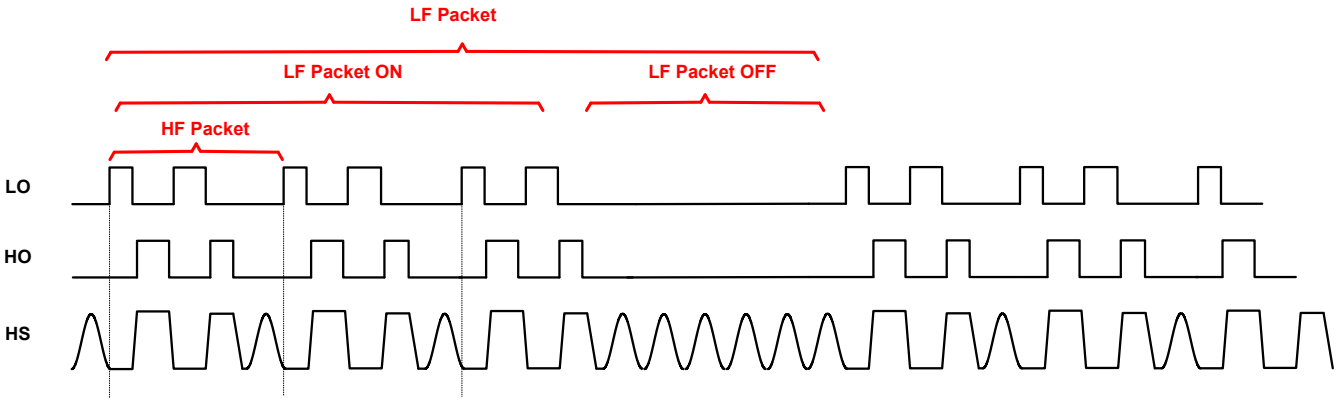


Figure 7-17. Low Frequency Burst Packet

The number of HF burst packet is calculated to maintain the LF burst frequency within a frequency range. A set of target frequency range is internally provided, the default option is to regulate the LF burst at approximately 200Hz.

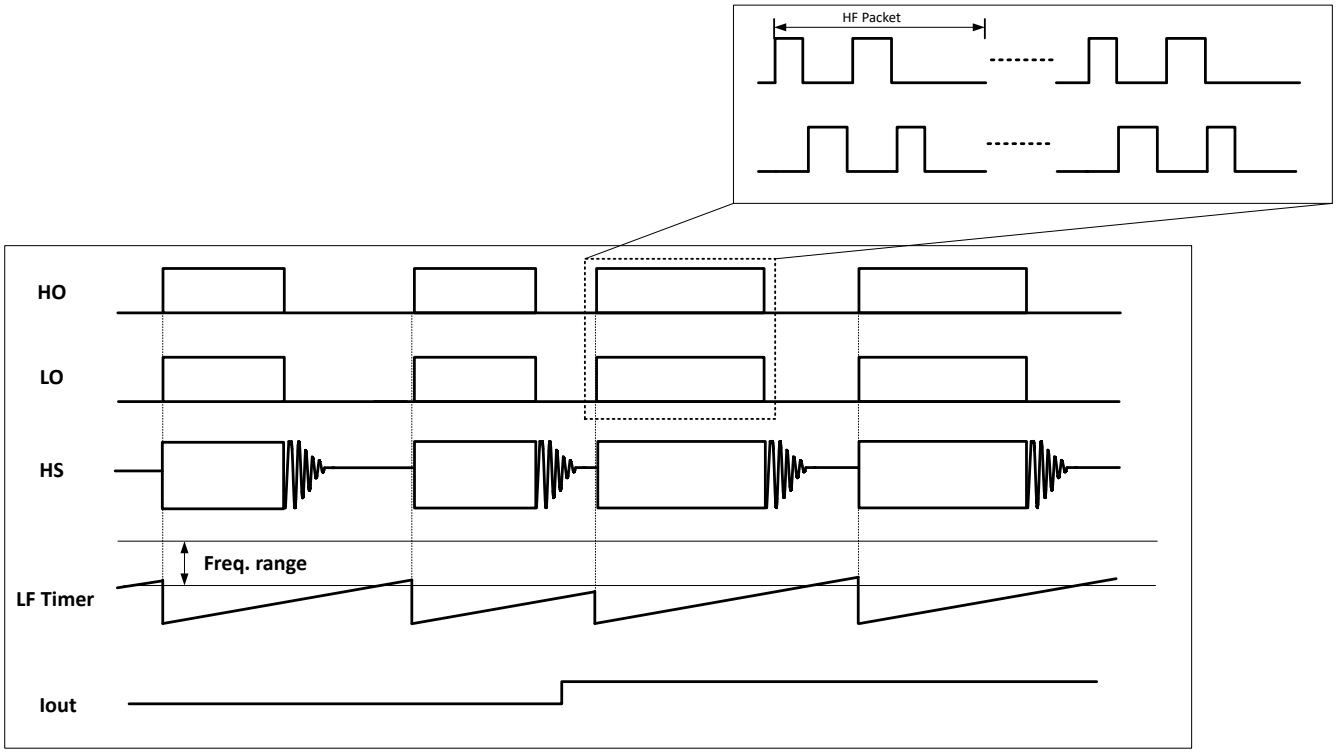


Figure 7-18. Packet Size Regulation Inside LF Burst

7.5.3.2 Mode Transition Management

Using the LL pin, the user configures the power level at which the UCC25661x-Q1 family enters the HF pulse skip and LF Burst mode. The two thresholds that can be set are the *HFBurstEntry* and *LFBursttEntry*. Section 7.5.3.3 provides more information regarding the configuration process.

Figure 7-19 describes the entry and exit behavior of UCC25661x-Q1 in burst mode.

- The *HFBurstEntry* corresponds to the *FBReplica* voltage at desired power level where the system enters HF Pulse skip.
- The *LFBurstEntry* corresponds to a modified *FBReplica* voltage at which the system enters LF Burst.
- When *FBreplica* is higher than HFBurstEntry, UCC25661x-Q1 family operates in normal switching.
- When *FBreplica* is less than *HFBurstEntry* but greater than *LFBurstEntry*, UCC25661x-Q1 family operates in HF pulse skip mode. In the HF pulse skip mode, the energy in each packet is still controlled by the control signal *FBReplica*.
- When *FBreplica* is less than *LFBurstEntry*, UCC25661x-Q1 operates in LF burst mode. In the LF Burst mode, the energy in each packet is fixed at *LFBurstEntry* threshold.
- While operating in LF Burst mode, a new LF Burst segment is started when the *FBReplica* rises above the *LFBurstEntry* threshold. The segment is terminated when the desired number of packets are delivered and the *FBReplica* is below the *PacketStop* threshold.
- The desired number of packets in a LF Burst segment is computed to regulate the LF Burst operating frequency within 200Hz to 400Hz.
- In case of a sudden load drop, the LF Burst segment is immediately terminated to avoid output over voltage condition.

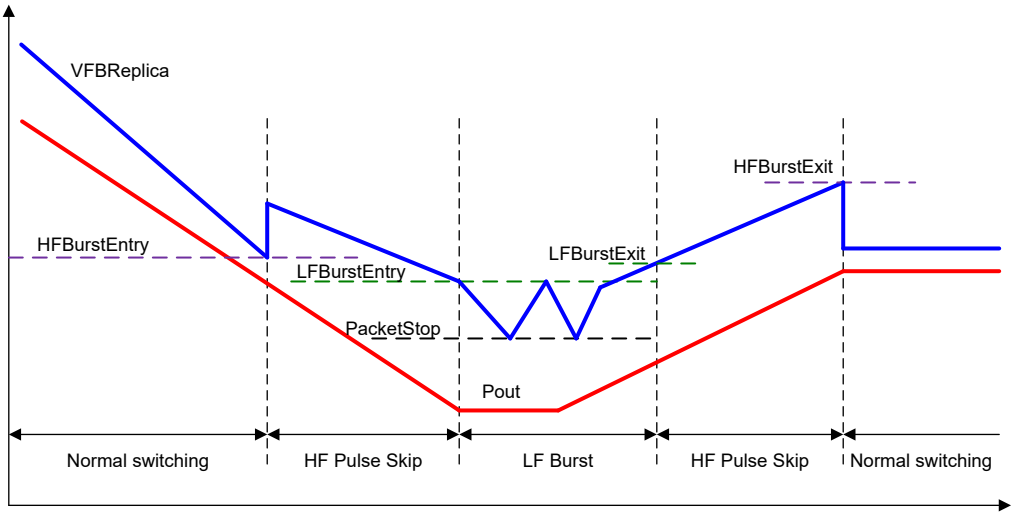


Figure 7-19. Burst Mode Determination from *FBReplica* Comparators

7.5.3.3 Burst Mode Thresholds Programming

Burst mode threshold programming is done by an external resistor divider connected between V5P and GNDP. Connect the center node of the external divider to LL pin. During the programming phase, a constant current I_{LLPrgm} is fed to the LL pin. The resulting voltage is measured with an ADC (V_{LLA}) at time T_{LLPrgm}. After T_{Prgm}, I_{LLPrgm} is turned off and the voltage of the LL resistor divider is measured (V_{LLB}).

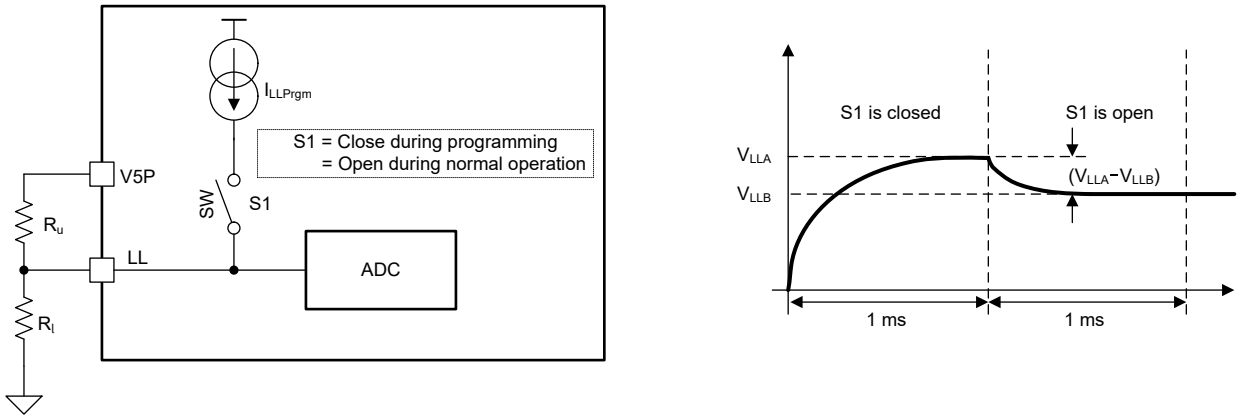


Figure 7-20. LL pin Programming

The voltage on the LL pin after switch S1 is off (V_{LLB}) is directly used to set the input power at which the system stops the LF Burst segment (*PacketStop* = V_{LLB}).

Based on the measured V_{LLB} voltage and the difference in voltage between V_{LLA} and V_{LLB}, determine the *FBReplica* voltage at which the controller enters HF Burst.

The equation to calculate V_{LLA} - V_{LLB} is given below.

$$V_{LLA} - V_{LLB} = (R_u \parallel R_I) \times I_{LLprgm} \quad (7)$$

$$\text{HFBurstEntry} = \text{PacketStop} \div a \quad (8)$$

Constant *a* is user programmable as provided in the below table.

$$R_u \parallel R_I = Rth \quad (9)$$

Equation 10 shows the *FBReplica* at which the controllers starts the LF Burst segment.

$$\text{LFBurstEntry} = \text{PacketStop} \div 0.6 \quad (10)$$

HFBurstexit and *LFBurstexit* thresholds have hysteresis from *HFBurstentry* and *LFBurstentry* respectively. The two hystereses are not user defined parameters. These two hystereses are dynamically estimated internally, based on the operating point of the converter.

Burst mode feature can be disabled by programming the (V_{LLA} - V_{LLB}).

Table 7-2. Burst Mode Externally Programmable Settings

(VLLA- VLLB) (V)	a = (PacketStop ÷ HFBurstEntry) ratio	Comment
>2.41	NA	Burst disable
2.185	0.45	LF frequency range 200Hz to 400Hz
1.754	0.50	LF frequency range 200Hz to 400Hz
1.391	0.55	LF frequency range 200Hz to 400Hz
1.087	0.60	LF frequency range 200Hz to 400Hz
0.833	0.65	LF frequency range 200Hz to 400Hz
0.617	0.70	LF frequency range 200Hz to 400Hz
0.441	0.75	LF frequency range 200Hz to 400Hz
0.176	0.80	LF frequency range 200Hz to 400Hz

The ability to directly set the input power at which the system goes into various low power modes disables the burst mode and enables an extra degree of freedom in the system design.

7.5.3.4 PFC On/Off

In UCC256614-Q1, use the TSET pin as PFC on/off logic. After the initial programming phase, TSET becomes a logic output pin expected to drive a small signal MOSFET (for example, 2N7002). When UCC256614-Q1 operates in LF Burst mode, the PFC on/off signal is high. TSET pin voltage is low when the controller exits LF Burst mode.

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

Use UCC25661-Q1 in a wide range of applications in which LLC topology is implemented. To make the part easier to use, TI has prepared a list of materials to demonstrate the features of the device:

- Full featured EVM hardware
- An excel design calculator
- Reference designs

The following sections show a typical design example.

8.2 Typical Application

Figure 8-1 below shows a typical half bridge LLC application using UCC25661-Q1 as the controller. For designers that would prefer to avoid optocoupler based feedback due to lifetime reliability concerns, see PMP31342 and use ISOM8110-Q1 opto-emulator, note that opto-emulator has relatively higher standby power relative to optocoupler.

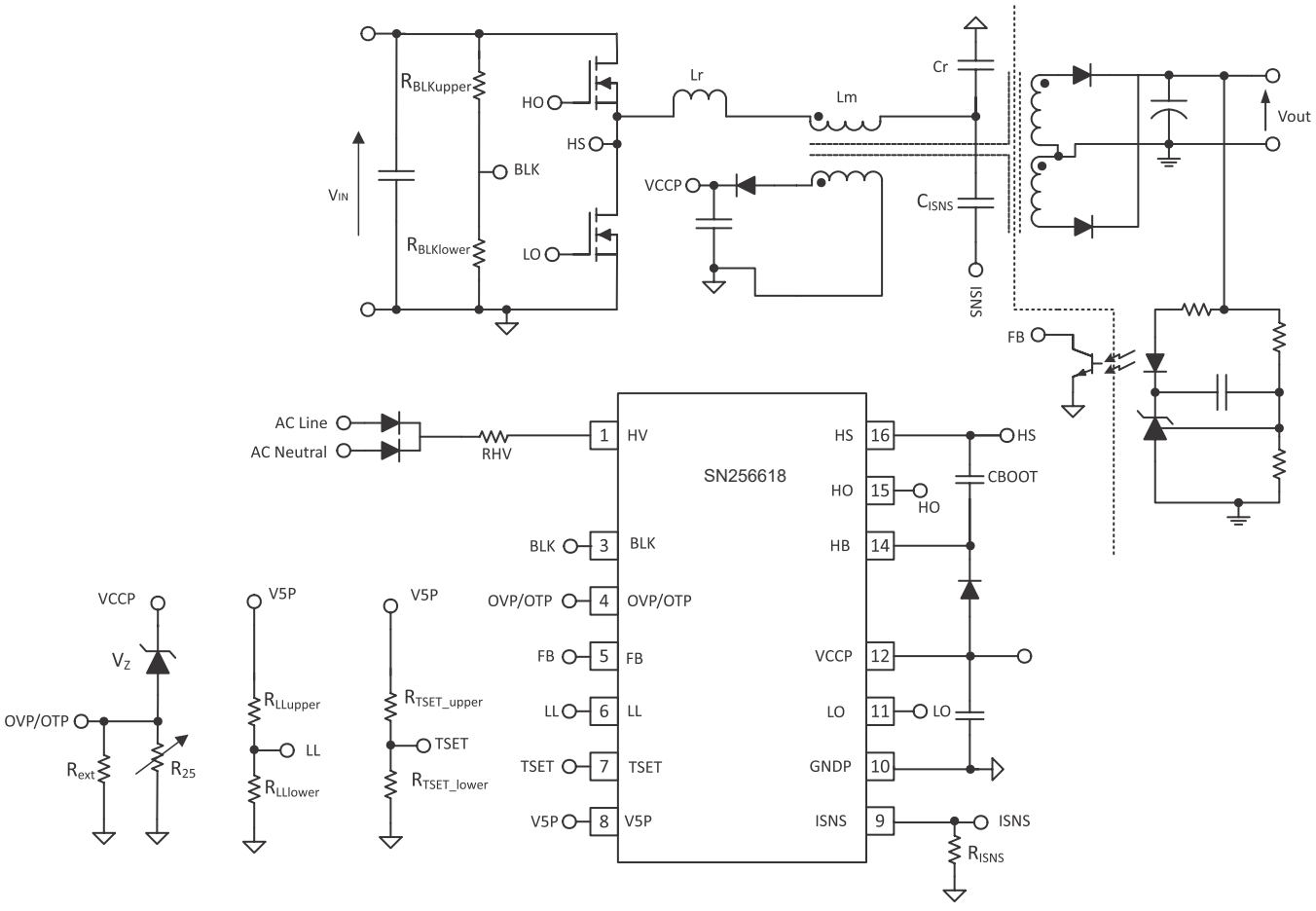


Figure 8-1. HV-LV DC/DC converter based on UCC25661

8.2.1 Design Requirements

The design specifications are summarized in Table 8-1.

Table 8-1. System Design Specifications

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
INPUT CHARACTERISTICS					
DC voltage range		365	390	410	VDC
AC voltage range		85		264	VAC
AC voltage frequency		47		63	Hz
Input DC UVLO on			365		VDC
Input DC UVLO off			315		VDC
OUTPUT CHARACTERISTICS					
Output voltage, VOUT	No load to full load		12		VDC
Output load current, IOUT	360VDC to 410VDC			15	A
Output voltage ripple	390VDC and full load = 15A		120		mVpp
SYSTEMS CHARACTERISTICS					
Resonant frequency			100		kHz
Peak efficiency	390VDC		92		
Operating temperature	Natural convection		25		°C

8.2.2 Detailed Design Procedure

8.2.2.1 LLC Power Stage Requirements

To begin designing, determine the LLC power stage component values. The LLC power stage design procedure is outlined here in the TI application note *Designing an LLC Resonant Half-Bridge Power Converters*. The application note contains a full explanation of the origin of each of the equations used. The equations below are based on the First Harmonic Approximation (FHA) method that is commonly used to analyze the LLC topology. The FHA method is a good starting point for any design. A final design requires an iterative approach combining the FHA results, circuit simulation, and hardware testing. For detailed explanations of the tradeoffs in selecting power stage components and parameters, see the *Designing an LLC resonant half-bridge power converter* video or *Survey of resonant converter topologies* video series. The application note *LLC Design for UCC29950* shows a different design approach.

8.2.2.2 LLC Gain Range

First, determine the transformer turns ratio by the nominal input and output voltages.

$$N_{PS} = \frac{V_{IN(nom)} \div 2}{V_{OUT(nom)}} = \frac{390 \div 2}{12} = 16.25 \Rightarrow 16.5 \quad (11)$$

Then determine the LLC gain range $M_{G(min)}$ and $M_{G(max)}$. Assume there is a 0.5V drop in the rectifier diodes (V_f) and an additional 0.5V due to other losses (V_{loss}). If using synchronous rectification like in reference design PMP23454, exclude the V_f term from below equation.

$$M_{G(min)} = N_{PS}\frac{V_{OUT(min)} + V_f}{V_{IN(min)} \div 2} = 16.5\frac{12 + 0.5}{410 \div 2} = 1.006 \quad (12)$$

$$M_{G(max)} = N_{PS}\frac{V_{OUT(max)} + V_f + V_{loss}}{V_{IN(min)} \div 2} = 16.5\frac{12 + 0.5 + 0.5}{365 \div 2} = 1.175 \quad (13)$$

8.2.2.3 Select L_n and Q_e

L_N is the ratio between the magnetizing inductance and the resonant inductance. Typically, a higher L_N enables integrating the resonant inductance into the LLC transformer as the leakage inductance, thus simplifying the bill of materials. Increasing L_N implies that the line and load voltage regulation range is reduced, which can violate design requirements. Finally, decreasing L_N introduces higher magnetizing current which can help ZVS but increases conduction losses.

$$L_N = \frac{L_M}{L_R} \tag{14}$$

Q_E is the quality factor of the resonant tank. Decreasing Q_E implies a wider switching frequency range, but increasing Q_E can decrease gain. It is possible that the end application is not designed for either the increase or decrease option.

$$Q_E = \frac{\sqrt{L_R \div C_R}}{R_E} \tag{15}$$

In this equation, R_E is the equivalent load resistance.

Selecting L_N and Q_E values results in an LLC gain curve that intersects with $M_{G(min)}$ and $M_{G(max)}$ traces. The peak gain of the resulting curve is larger than $M_{G(max)}$. L_N and Q_E selection criteria are located in the Design Calculator.

In this case, the selected L_N and Q_E values are:

$$L_N = 6 \tag{16}$$

$$Q_E = 0.3 \tag{17}$$

8.2.2.4 Determine Equivalent Load Resistance

Determine the equivalent load resistance by Equation 18.

$$R_E = \frac{8 \times {N_{PS}}^2}{\pi^2} \times \frac{V_{OUT(nom)}}{I_{OUT(nom)}} = \frac{8 \times {16.5}^2}{\pi^2} \times \frac{12}{15} = 176.5\Omega \tag{18}$$

8.2.2.5 Determine Component Parameters for LLC Resonant Circuit

Before finalizing the resonant tank component parameters, select a nominal switching frequency (resonant frequency). In the UCC25661EVM-128 180W design, 100kHz is the resonant frequency. Higher resonant frequency shrink passive components. Some designers limit the maximum resonant frequency, avoiding the AM band to meet CISPR 25 standards for EMC.

$$f_0 = 100\text{kHz} \tag{19}$$

Calculate the resonant tank parameters using Equation 20, Equation 21, and Equation 22.

$$C_R = \frac{1}{2\pi \times Q_E \times f_0 \times R_E} = \frac{1}{2\pi \times 0.3 \times 100\text{kHz} \times 176.5\Omega} = 30.0\text{nF} \tag{20}$$

$$L_R = \frac{1}{(2\pi \times f_0)^2 C_R} = \frac{1}{(2\pi \times 100\text{kHz})^2 \times 30.0\text{nF}} = 84.4\mu\text{H} \tag{21}$$

$$L_M = L_N \times L_R = 6 \times 84.4\mu\text{H} = 506.4\mu\text{H} \tag{22}$$

After selecting the preliminary parameters, find the closest actual component value that is available, and reassess the gain curve. Verify the circuit operation by running a time domain simulation in SIMPLIS or another

modeling tool. Running simulations allows testing many unique combinations and iterations of resonant tank parameters without purchasing components and waiting for delivery.

The following resonant tank parameters are:

$$C_R = 30nF \quad (23)$$

$$L_R = 85\mu H \quad (24)$$

$$L_M = 510\mu H \quad (25)$$

Based on the final resonant tank parameters, confirm the desired resonant frequency is calculated from the following equation:

$$f_0 = \frac{1}{2\pi\sqrt{L_R C_R}} = \frac{1}{2\pi\sqrt{30nF \times 85\mu H}} = 99.7kHz \quad (26)$$

Based on the new LLC gain curve, the normalized switching frequency at maximum and minimum gain are given by:

$$f_{N(Mgmax)} = 0.7 \quad (27)$$

$$f_{N(Mgmin)} = 1.0 \quad (28)$$

The maximum and minimum switching frequencies are a product of the normalized switching frequency and the corresponding gain:

$$f_{SW(Mgmax)} = 69.8kHz \quad (29)$$

$$f_{SW(Mgmin)} = 99.7kHz \quad (30)$$

8.2.2.6 LLC Primary-Side Currents

The primary-side currents are calculated to understand the sizing and ratings necessary during component selection purposes. The currents are calculated based on a 110% overload condition.

The primary side RMS load current is calculated by:

$$I_{OE} = \frac{\pi}{2\sqrt{2}} \times \frac{I_O}{n} = \frac{\pi}{2\sqrt{2}} \times \frac{1.1 \times 15A}{16.5} = 1.111A \quad (31)$$

Where I_o is the maximum load current times the allowable overload condition, for UCC25661EVM-128 10% was chosen as the allowable output current overload condition.

The RMS magnetizing current at minimum switching frequency is calculated using:

$$I_M = \frac{\pi}{2\sqrt{2}} \times \frac{N_{PS} V_{OUT}}{\omega L_M} = \frac{\pi}{2\sqrt{2}} \times \frac{16.5 \times 12}{2\pi \times 64.8kHz \times 510\mu H} = 0.797A \quad (32)$$

The total current in resonant tank is calculated using Equation 33.

$$I_R = \sqrt{{I_M}^2 + {I_{OE}}^2} = \sqrt{(1.111A)^2 + (0.797A)^2} = 1.367A \quad (33)$$

8.2.2.7 LLC Secondary-Side Currents

The total secondary side RMS load current is the current referred from the primary side current (I_{OE}) to the secondary side.

$$I_{OES} = N_{PS} \times I_{OE} = 16.5 \times 1.111A = 18.327A \quad (34)$$

In this design and many other TI reference designs based on analog LLC, the secondary side of the transformer is in a center-tapped configuration. The secondary side configuration affects the voltage gain and the number rectifier diodes. The current of each secondary transformer winding is calculated by:

$$I_{WS} = \frac{\sqrt{2} \times I_{OES}}{2} = \frac{\sqrt{2} \times 18.327A}{2} = 12.959A \quad (35)$$

The corresponding half-wave average current is:

$$I_{SAV} = \frac{\sqrt{2} \times I_{OES}}{\pi} = \frac{\sqrt{2} \times 18.327A}{\pi} = 8.250A \quad (36)$$

8.2.2.8 LLC Transformer

To maximize efficiency, a bias winding is required to use the high-voltage start-up function. Design the bias winding so that the VCCP voltage is greater than 12V. The > 12V VCCP voltage is not required for the UCC256613 where an external auxiliary bias supply is expected to power VCCP.

Build or purchase the transformer according to these specifications:

- Turns ratio: Primary:Secondary:Bias = 33:2:3
- Primary terminal voltage: 450V_{pk}
- Primary magnetizing inductance: L_M = 510µH
- Primary side winding rated current: I_R = 1.367A
- Secondary terminal voltage: 36V_{pk}
- Secondary winding rated current: I_{WS} = 12.959A
- Minimum switching frequency: 69.8kHz
- Maximum switching frequency: 99.7kHz
- Insulation between primary and secondary sides: IEC60950 reinforced insulation

For some applications that operate as a wide input LLC where the PFC can shut off in standby mode, the operating frequency can be much lower during heavy load shutdown. The LLC operates at just above the ZCS boundary, which is a lower frequency. Rate the magnetic components in the resonant circuit, transformer, and resonant inductor, to operate at a lower frequency.

The bias voltage is obtained as 18V, as per the turns ratio. To reduce the controller voltage to 15V, use a voltage regulator circuit in the EVM before supplying to the VCCP of the controller.

8.2.2.9 LLC Resonant Inductor

The AC voltage across the resonant inductor is calculated using the AC voltage across the resonant inductor impedance multiplied by the current:

$$V_{CR} = \frac{I_R}{\omega C_R} = \frac{1.367A}{2\pi \times 69.8kHz \times 30nF} = 104.0V \quad (37)$$

Build or purchase the inductor according to the following specifications:

- Inductance: L_R = 85µH
- Rated current: I_R = 1.367A
- Terminal AC voltage: 50.946V
- Frequency range: 69.8kHz to 99.7kHz

Some designs use the leakage inductance of the transformer as the resonant inductance and do not require an external resonant inductor which can save cost and space. However, consult a magnetics vendor to determine if the design required an external resonant inductor.

8.2.2.10 LLC Resonant Capacitor

The LLC resonant capacitor carries the full-primary current at the switching frequency. Select a capacitor with a low dissipation factor and minimal parasitic series resistance to prevent overheating. The AC voltage across the resonant capacitor is calculated by the impedance of the AC voltage across the resonant capacitor multiplied by the current.

$$V_{CR} = \frac{I_R}{\omega C_R} = \frac{1.367A}{2\pi \times 69.8kHz \times 30nF} = 104.0V \quad (38)$$

$$V_{CR(RMS)} = \sqrt{\left(\frac{V_{IN[max]}}{2}\right)^2 + {V_{CR}}^2} = \sqrt{\left(\frac{410}{2}\right)^2 + {104.0}^2} = 229.9V \quad (39)$$

Peak voltage:

$$V_{CR(peak)} = \frac{V_{IN(max)}}{2} + \sqrt{2}V_{CR} = \frac{410}{2} + \sqrt{2} \times 104.0 = 352.0V \quad (40)$$

Valley voltage:

$$V_{CR(valley)} = \frac{V_{IN(max)}}{2} - \sqrt{2}V_{CR} = \frac{410}{2} - \sqrt{2} \times 104.0 = 58.0V \quad (41)$$

Rated current:

$$I_R = 1.367A \quad (42)$$

8.2.2.11 LLC Primary-Side MOSFETs

Each MOSFET sees the input voltage as the maximum applied voltage. As a general recommendation, select the MOSFET voltage rating as ×1.5 of the maximum bulk voltage to establish sufficient margin without oversizing:

$$V_{QLLC(peak)} = 1.5 \times V_{IN(max)} = 615V \quad (43)$$

Select the MOSFET current rating as ×1.2 of the maximum primary side RMS current to provide a sufficient margin. Some applications require a lower margin:

8.2.2.12 Design Considerations for Adaptive Dead-Time

After designing the resonant tank and selecting the primary side MOSFET, check the ZVS operation of the converter. ZVS is achieved when enough energy remains in the resonant inductor at the gate turn-off edge to discharge the switch node capacitance. ZVS is also achieved when the inductive energy is larger than the effective capacitive energy, where the effective capacitance is the Coss of the two switches in the power stage. UCC256614-Q1 implements adaptive dead-time based on the slewing of the switch node. The slew detection circuit has a detection range of 0.1V/ns to 200V/ns.

To check the ZVS operation, the controller conducts a series of time domain simulations, and the resonant current at the gate turn off edges are captured. An example plot is shown below:

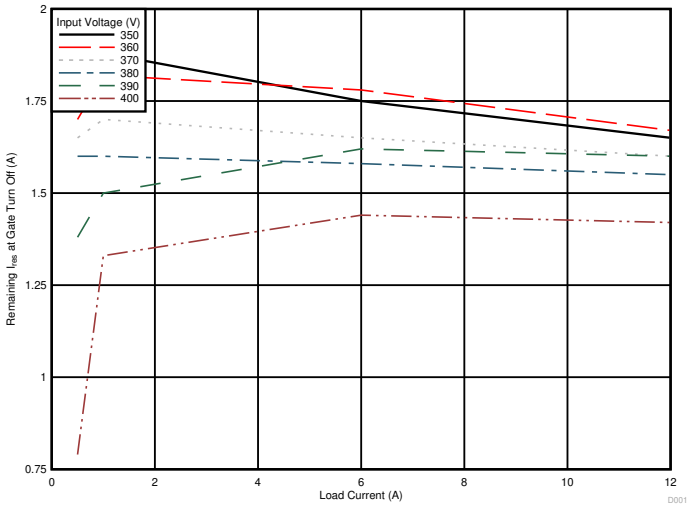


Figure 8-2. Adaptive Dead-Time

Figure 8-2 assumes that the maximum switching frequency occurs at 5% load and system starts to burst at 5% load.

From Figure 8-2, the minimum resonant current remaining in the tank is I_{min} = 0.8A, in the operation range of interest. The parasitic capacitance of the primary-side switch node is required to calculate the slew rate. Estimate the slew rate from the value of Coss given in the MOSFET data sheet. In this case, $C_{switchnode}$ = 400pF as the Coss for each MOSFET is 200pF. The minimum slew rate is calculated using:

$$\frac{I_{MIN}}{C_{switchnode}} = \frac{0.8A}{400pF} = 2V/ns \tag{44}$$

The minimum slow rate is larger than the 0.1V/ns minimum detectable slew rate which helps in establishing ZVS maintenance.

8.2.2.13 LLC Rectifier Diodes

Using SR controllers such as UCC24612 and MOSFETs can boost efficiency at full load by 2-3% by minimizing losses from rectification diodes such as forward voltage and switching. Assuming that diodes are used for rectification, the voltage rating of the output diodes is calculated using:

$$V_{DD} = 1.2 \times \frac{V_{IN(max)}}{N_{PS}} = 1.2 \times \frac{410}{16.5} = 29.82V \tag{45}$$

The current rating of the output diodes is given by:

$$V_{DB} = 1.2 \times \frac{V_{IN(max)}}{N_{PS}} = 1.2 \times \frac{410}{16.5} = 29.82V \tag{46}$$

In general, select rectification diodes so that the 20% margin is maintained for both current and voltage. Typically, fast recovery diodes are used to minimize reverse recovery losses.

8.2.2.14 LLC Output Capacitors

The LLC converter topology does not require an output filter. Use a small second stage filter inductor to reduce peak-to-peak output ripple. Assuming that the output capacitors carry the full wave output current of the rectifier, the capacitor ripple current rating is:

$$I_{RECT} = \frac{\pi}{2\sqrt{2}} I_{OUT} = \frac{\pi}{2\sqrt{2}} \times 15 = 16.66A \tag{47}$$

In this design, capacitors with 20V rating are used for 12V output voltage:

$$V_{LLCcap} = 20V \quad (48)$$

The capacitor RMS current rating is:

$$I_{C(out)} = \sqrt{\left(\frac{\pi}{2\sqrt{2}} I_{OUT}\right)^2 - {I_{OUT}}^2} = \sqrt{\left(\frac{\pi}{2\sqrt{2}} \times 15\right)^2 - 15^2} = 7.251A \quad (49)$$

Solid aluminum capacitors with conductive polymer technology have high ripple-current ratings and are a good choice, especially if the design is required to operate at colder temperatures. Connect multiple capacitors in parallel if the ripple-current rating for a single capacitor is not sufficient.

The ripple voltage at the output of the LLC stage is a function of the amount of AC current that flows in the capacitors. To estimate the ripple voltage, assume that all the current, including the DC current in the load, flows in the filter capacitors.

$$ESR_{max} = \frac{V_{OUT(pk-pk)}}{I_{RECT(pk)}} = \frac{0.12v}{2\frac{\pi}{4} \times 15A} = 5.1m\Omega \quad (50)$$

The capacitor specifications are:

- Voltage rating: 20V
- Ripple current rating: 7.251A
- Effective ESR: < 5.1mΩ

8.2.2.15 HV Pin Series Resistors

Multiple resistors are connected in series with HV pin to limit the voltage rating, size, and power dissipation of each resistor. Select the series resistors to limit the maximum current into the HV pin. The UCC25661 evaluation module uses a 5kΩ resistor, but recalculate series resistors values for other input voltages (like 800V) or in system where LLC delivers power during low line operation and the PFC is disabled (standby mode of battery charger).

8.2.2.16 BLK Pin Voltage Divider

BLK pin senses the LLC DC input voltage and determines when to turn on and off the LLC converter. Also, BLK pin voltage is used for feedforward compensation. Size the resistor divider so that the current in the divider is larger than the leakage into the BLK pin (Iblksink). The maximum desired power consumption of the BLK pin resistor divider is P_{BLKsns} = 15mW. The BLK sense resistor total value is given by:

$$R_{BLKsns} = R_{BLKupper} + R_{BLKlower} = \frac{V_{IN(nom)}^2}{P_{BLKsns}} = \frac{390^2}{0.015} = 10M\Omega \quad (51)$$

Select 365V as the LLC start-up voltage. Relate $V_{BLKStart}$ to $V_{BLKStop}$, $V_{BLKStartHys}$, $I_{BLKSink}$ as below:

$$V_{BLKStart} = 365\left(\frac{R_{BLKlower}}{R_{BLKupper} + R_{BLKlower}}\right) = V_{BLKStop} + V_{BLKStartHys} + I_{BLKsink}\left(\frac{R_{BLKupper}R_{BLKlower}}{R_{BLKupper} + R_{BLKlower}}\right) \quad (52)$$

For $V_{BLKStop}$ = 1V, $V_{BLKStartHys}$ = 0.1V, $I_{BLKSink}$ = 5µA, $R_{BLKupper}$, and $R_{BLKlower}$ are obtained as 10MΩ and 35.4kΩ respectively.

A standard value of 35.4kΩ is selected for $R_{BLKlower}$ and a standard value of ×3 3.3MΩ in series is selected for $R_{BLKupper}$.

The actual start-up voltage is calculated using:

$$V_{BLKStart}\left(\frac{R_{BLKupper}+R_{BLKlower}}{R_{BLKlower}}\right)=\left(\begin{matrix}V_{BLKStop}+V_{BLKStartHys}+\\ I_{BLKSink}\left[\frac{R_{BLKupper}R_{BLKlower}}{R_{BLKupper}+R_{BLKlower}}\right]\end{matrix}\right)\times\left(\frac{R_{BLKupper}+R_{BLKlower}}{R_{BLKlower}}\right)=358V \quad (53)$$

The power consumption in BLK resistors is calculated using:

$$P_{BLKsns}=\frac{V_{IN(nom)}{}^2}{\left(R_{BLKupper}+R_{BLKlower}\right)}=\frac{390^2}{(10M\Omega+35.4k\Omega)}=15.3mW \quad (54)$$

The LLC turn off voltage is calculated using:

$$V_{BLKStop}\left(\frac{R_{BLKupper}+R_{BLKlower}}{R_{BLKlower}}\right)=280.6V \quad (55)$$

8.2.2.17 ISNS Pin Differentiator

The ISNS pin senses the resonant current through a differentiator. The ISNS pin and TSET and BLK pin resistors set the overload protection level. The typical threshold voltage of overload protection (V_{FBOLP}) is 4.75V. The ISNS pin sets the over current protection level (OCP1). The threshold value of OCP1 is either 3.5V or 4V, depending on the TSET pin resistors and the variant in use. For the EVM, UCC256611 is in use. So, for this variant, OCP1 threshold value is 3.5V.

The peak resonant inductor current at full load:

$$I_{R\_PEAK}=\sqrt{2}I_R=\sqrt{2}\times1.367=1.933A \quad (56)$$

Select a current sense capacitor first, as there are less high voltage capacitor choices than resistors:

$$C_{ISNS}=150pF \quad (57)$$

For UCC25661EVM-128 and all UCC25661x-Q1 orderable part numbers, the OCP1 threshold value is 3.5V.

$$OCP1\_Threshold=3.5V \quad (58)$$

Calculate the required ISNS resistor value:

$$R_{ISNS}<\frac{OCP1\_Threshold\times C_r}{I_{R\_PEAK}\times C_{ISNS}}=\frac{3.5V\times30nF}{1.933A\times150pF}=329\Omega \quad (59)$$

$$R_{ISNS}=226\Omega \quad (60)$$

is selected.

The peak resonant current at OCP1 level is calculated using:

$$I_{R\_PEAK\_OCP1}=\frac{OCP1\_Threshold\times C_r}{R_{ISNS}\times C_{ISNS}}=\frac{3.5\times30nF}{226\times150pF}=3.097A \quad (61)$$

8.2.2.18 TSET Pin

The TSET pin resistors are used to set the VCR integrator time constants. The VCR integrator time constants include

- Timer gain
  - k_s
  - R_{VCR}
  - R_{RAMP}
  - C_{VCR}

- Minimum switching frequency in IPPC mode

The TSET pin resistors also determine the $V_{FBreplica}$ voltage for a given output power.

Choose the V_{TSETB} voltage based on $f_{SW(Mgmin)}$ and the full load operating frequency at the minimum input voltage and maximum output power. For this design, option four is selected in the design calculator as the observed full load operating frequency is 89kHz at the minimum input voltage of 365V and at the rated output power. For option four, establish that V_{TSETB} voltage is between 0.742V ± 48mV, as TSET Programming Options Table shows.

Choose the (V_{TSETA}-V_{TSETB}) voltage to set the FBReplica magnitude for a select power output. Choose the (V_{TSETA}-V_{TSETB}) voltage difference so that at rated power, the FBReplica magnitude is below V_{FBOLP}, as shown in Figure 8-3 with the required margin at worst case. For UCC25661EVM-128, option five is selected for this difference TSET voltage so that VCR integrator time constants and the select ISNS and BLK resistors makes the FBReplica magnitude close to 4V at the maximum input power. So, for option number 5, establish that (V_{TSETA}-V_{TSETB}) voltage is between 0.850V ± 48mV, as TSET Programming Options Table shows.

$$V_{TSETB} = \frac{R_{TSET\_lower} \times V5P}{R_{TSET\_lower} + R_{TSET\_upper}} \quad (62)$$

$$V_{TSETA} = V_{TSETB} + \frac{R_{TSET\_lower} \times R_{TSET\_upper}}{R_{TSET\_lower} + R_{TSET\_upper}} \times I_{TSETPrgm} \quad (63)$$

Equation 62 outputs as R_{TSET_upper} equals 572.78kΩ. Equation 63 outputs as R_{TSET_lower} equals 99.81kΩ.

Finally, R_{TSET_upper} = 576kΩ and R_{TSET_lower} = 100kΩ are chosen.

Calculate V_{TSETB} and (V_{TSETA}-V_{TSETB}) using Equation 64 and Equation 65.

$$V_{TSETB} = \frac{100k \times 5V}{100k + 576k} = 0.74V \quad (64)$$

$$\left(V_{TSETA} - V_{TSETB}\right) = \frac{100k \times 576k}{100k + 576k} \times 10\mu A = 0.852V \quad (65)$$

Figure 8-3 shows the FBReplica voltage with respect to the input power of the LLC.

To calculate P_{in}, 92% efficiency is used in the following expression:

$$P_{in} = \frac{P_{out}}{\eta} \quad (66)$$

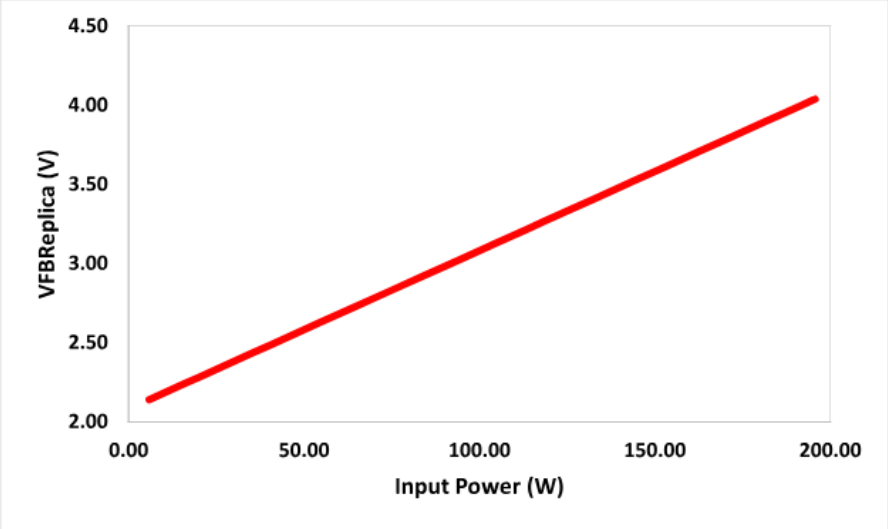


Figure 8-3. FBReplica versus P_{in}

The FBReplica voltage is measured by inserting a 10kΩ resistor between the feedback optocoupler emitter and the ground. Assume the voltage measured on the 10kΩ resistor is V_{10k}. Calculated then FBReplica voltage using:

$$\mathrm{FBReplica} = \left(I_{FB} - \frac{V_{10k\Omega}}{10k\Omega}\right) \times R_{FBInternal} \quad (67)$$

8.2.2.19 OVP/OTP Pin

The OVP/OTP protects the power stage from over voltage. The OVP/OTP pin is also used for over-temperature protection using a negative temperature coefficient (NTC) thermistor. As the bias winding voltage is the mirror image of the output voltage through the turns ratio of the transformer, pulling up the OVP/OTP pin with a Zener diode is a convenient approach to set the OVP on the primary side. In this design, the nominal output voltage is 12V. To maintain the voltage on VCCP above the UVLO threshold, the bias winding to the secondary side winding turns ratio is 1.5, in other words greater than 12V. Assuming there is a 0.5V drop in the rectifier diodes (Vf) and a further 0.5V drop due to other losses (Vloss), the nominal voltage of the bias winding is calculated using:

$$V_{BiasWindingNom} = \left(12 + 0.5 + 0.5\right) \times \frac{N_{aux}}{N_2} = \left(12 + 0.5 + 0.5\right) \times \frac{3}{2} = 19.5V \quad (68)$$

The desired OVP threshold in this design is 140% of the nominal value. The OVP threshold level (V_{OVPpos}) in UC25661 device is 3.5V.

The required voltage rating of the Zener diode is calculated using:

$$V_z = \left(1.4 \times V_{out} + V_{drop}\right) \times \frac{N_{aux}}{N_2} - V_{OVPpos} = \left(1.4 \times 12 + 0.5 + 0.5\right) \times \frac{3}{2} - 3.5 = 23.2V \quad (69)$$

Assuming actual voltage rating of zener used is 23V, the actual output voltage at which OVP is triggered is

$$V_{out\_ovp} = \left(V_z + V_{OVPpos}\right) \times \frac{N_2}{N_{aux}} - V_{drop} = \left(23 + 3.5\right) \times \frac{2}{3} - 1 = 16.67V = 139\% \times V_{out} \quad (70)$$

During normal operation, the voltage of the OVP/OTP pin is within the working window from 0.8V to 3.5V. For over temperature protection, pull down the OVP/OTP pin below the OTP threshold of 0.8V.

At room temperature, the OVP/OTP pin voltage is considered as 1.4V. So, at room temperature, the effective resistance value at the OVP/OTP pin is

$$R_{OVP/OTP\_25} = \frac{1.4V}{I_{OVP\_OTP}} = \frac{1.4V}{100 \times 10^{-6}A} = 14k\Omega \quad (71)$$

$$R_{OVP/OTP\_25} = \frac{R_{ext} \times R_{NTC\_25}}{R_{ext} + R_{NTC\_25}} = 14k\Omega \quad (72)$$

where R_{ext} is external resistor that is in parallel with the thermistor. R_{NTC_25} is the resistance value of the thermistor at room temperature.

For UCC25661EVM-128, over temperature protection is set at the 110°C. Based on the availability and temperature coefficient of the NTCs, choose Equation 73. Refer to the B57371V2474J060 data sheet for more information. R_{NTC_110} is the resistance of the thermistor at the 110°C.

$$\frac{R_{NTC\_110}}{R_{NTC\_25}} = 0.035263 \quad (73)$$

For OTP trigger, set the OVP/OTP pin voltage below 0.8V.

$$R_{OVP/OTP\_110} = \frac{0.8V}{I_{OVP\_OTP}} = \frac{0.8V}{100 \times 10^{-6}A} = 8k\Omega \quad (74)$$

$$R_{OVP/OTP\_110} = \frac{R_{ext} \times R_{NTC\_110}}{R_{ext} + R_{NTC\_110}} = 8k\Omega \quad (75)$$

From Equation 72, Equation 73, Equation 75, R_{NTC_25} is 510kΩ and R_{ext} is 14.4kΩ. As a result, R_{NTC_25} = 470kΩ and R_{ext}=15kΩ. The manufacturer part number for R_{NTC_25} = 470kΩ is B57371V2474J060.

At room temperature and with new chosen resistors, the OVP/OTP voltage is calculated as:

$$R_{OVP/OTP\_25} \times I_{OVP\_OTP} = \left(\frac{15k \times 470k}{15k + 470k}\right) \times 100 \times 10^{-6} = 1.454V \quad (76)$$

At 110^{0}C, the OVP/OTP voltage is calculated as:

$$R_{OVP/OTP\_110} \times I_{OVP\_OTP} = \left(\frac{15k \times [470k \times 0.035263]}{15k + [470k \times 0.035263]}\right) \times 100 \times 10^{-6} = 0.78V \quad (77)$$

8.2.2.20 Burst Mode Programming

The LL pin voltage (VLLB) and the resistor divider that connect to the LL pin allow the user to set the HFBurstEntry and LFBurstEntry thresholds:

$$VLLB = \frac{R_{LL\_lower} \times V5P}{R_{LL\_upper} + R_{LL\_lower}} \quad (78)$$

$$VLLA = VLLB + \frac{R_{LL\_lower} R_{LL\_upper}}{R_{LL\_upper} + R_{LL\_lower}} \times I_{LLPrgm} \quad (79)$$

As shown in Table 7-1, (V_{LLA} – V_{LLB}) voltage determines the V_{LLB} / HFBurstEntry ratio (a).

For UCC25661EVM-128, (V_{LLB}/HFBurstEntry) = 0.55 is considered. Verify that the (V_{LLA} – V_{LLB}) value is between 1.087V and 1.391V.

Then HFBurstEntry is related to LL pin voltage as Equation 80 calculates.

$$HFBurstEntry = \frac{VLLB}{0.55} = 1.818 \times VLLB \quad (80)$$

The LFBurstEntry is related to LL pin voltage as Equation 81 calculates.

$$LFBurstEntry = \frac{VLLB}{0.6} = 1.667 \times VLLB \quad (81)$$

Based on FBReplica vs Pin curve and hardware testing, optimize V_{LLB} and (V_{LLA}-V_{LLB}) to meet the desired performance.

For UCC25661EVM-128, VLLB = 1.2V and VLLA = (max voltage of [VLLA – VLLB]) – 0.1V are considered. By substituting these values in Equation 78, Equation 79, $R_{LLupper}$ is calculated as 538k and $R_{LLlower}$ is calculated as 170k.

Finally $R_{LLupper}$ = 536kΩ and $R_{LLlower}$ = 169kΩ are chosen for UCC25661EVM-128.

The final burst entries are calculated with the following equations.

$$VLLB = \frac{169k \times 5}{169k + 536k} = 1.199V \quad (82)$$

$$VLLA = 1.199V + \frac{169k \times 536k}{169k + 536k} \times 10\mu A = 2.483V \quad (83)$$

$$VLLA - VLLB = 1.285V \quad (84)$$

$$\text{HFBurstEntry} = 1.818 \times 1.199 = 2.179\text{V} \quad (85)$$

$$\text{LFBurstEntry} = 1.667 \times 1.199 = 1.998\text{V} \quad (86)$$

8.2.2.21 Application Curves

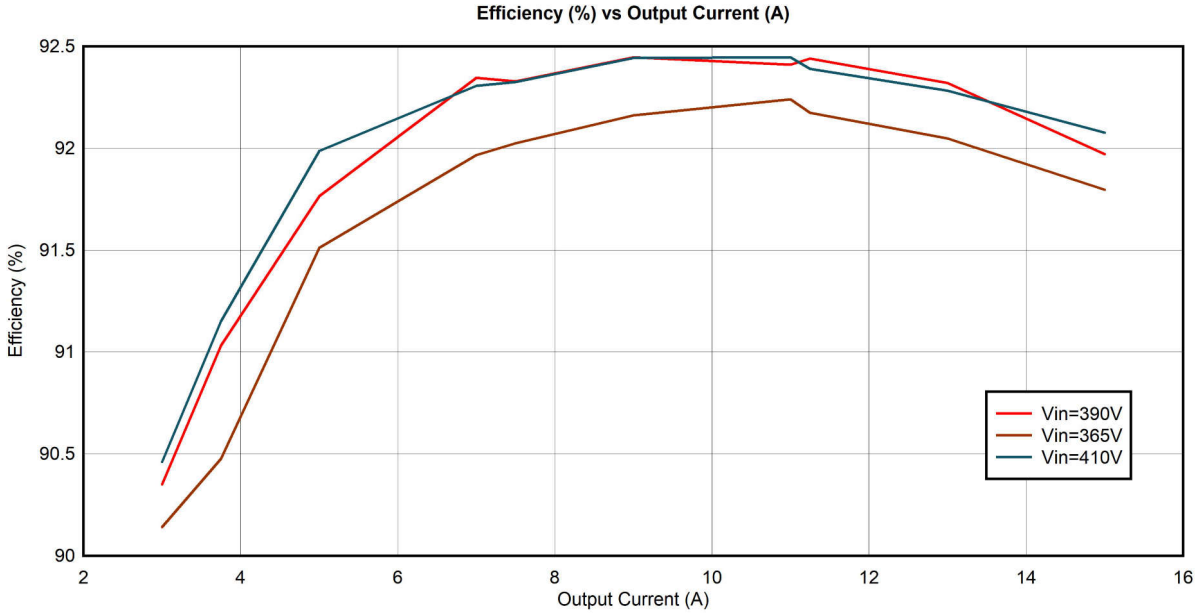


Figure 8-4. Efficiency

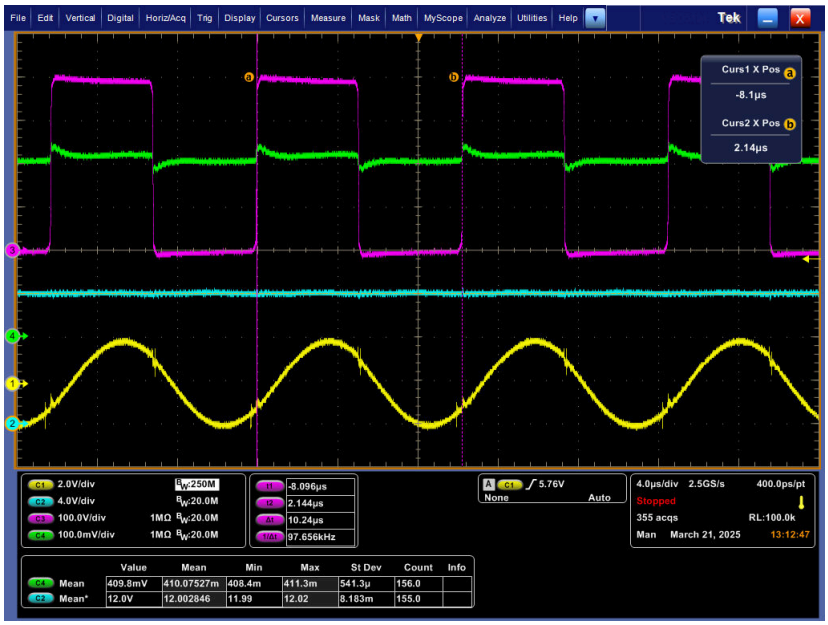


Figure 8-5. Steady State Waveforms at 15A Load and 390V Input

A. Ch1= ISNS, Ch2 = Vout, Ch3 = SW, Ch4 = I_OPT

8.3 Power Supply Recommendations

8.3.1 VCCP Pin Capacitor

Verify that the selected VCCP capacitor has value high enough to establish that during the LF Burst operation, VCCP does not fall below the $VCC_{StopSwitching}$ level.

Select a capacitor, or a combination of capacitors, that provide at least 100µF capacitance. The capacitors on VCCP pin support the quiescent current during LF burst operation as well as low impedance path for high frequency currents on VCCP. Consider derating the ceramic capacitors with DC-bias voltage using the manufacturer data sheet while selecting the capacitors.

8.3.2 Boot Capacitor

During LF burst off period, power consumed by the high-side gate driver from the HB pin from the C_{BOOT} and causes the bootstrap capacitor voltage to decay. At the start of the next burst period establish sufficient voltage remaining on C_{BOOT} to power the high-side gate driver (HO) until the conduction period of the low-side gate driver (LO) allows it to replenish from the C_{VCCP}. The power consumed by the high-side driver during this burst off period directly impacts the size and cost of capacitors that connect to HB and VCCP.

Assume the system has a maximum burst off period of 150ms and the bootstrap diode has a forward voltage drop of 1V. Target a minimum bootstrap voltage of 8V to avoid UVLO fault. The maximum allowable voltage drop on the boot capacitor is:

$$V_{bootmaxdrop} = V_{VCCP} - V_{bootforwarddrop} - 8V = 12V - 1V - 8V = 3V \quad (87)$$

Size the boot capacitor using Equation 88:

$$C_B = \frac{I_{BOOT\_QUIESCENT}}{V_{bootmaxdrop}} = \frac{60\mu A \times 150ms}{3V} = 3uF \quad (88)$$

Choose a low leakage, low-ESR ceramic capacitor. Consider derating of ceramic capacitors with DC-bias voltage using the manufacturer data sheet while selecting the capacitors.

8.3.3 V5P Pin Capacitor

Externally connect the V5P pin capacitor to a decoupling capacitor to GND. Because the load on the V5P pin capacitor is very small, a decoupling capacitor of 4.7µF is recommended.

8.4 Layout

8.4.1 Layout Guidelines

- Connect a 2.2µF ceramic capacitor on VCCP pin, in addition to the energy storage electrolytic capacitor. Place the 2.2µF ceramic capacitor as close as possible to the VCCP pin.
- The minimum recommended boot capacitor (C_B) is 0.1µF. Determine the minimum value of the boot capacitor by the minimum burst frequency. Establish that the boot capacitor is large enough to hold the bootstrap voltage during the lowest burst frequency. Refer to the I_{BOOT_LEAK} (boot leakage current) in the electrical table.
- Connect signal ground and power ground at the single-point. Power ground is recommended to connect to the negative terminal of the LLC converter input bulk capacitor.
- Place the filter capacitors for ISNS (100pF), BLK (10nF), LL (330pF), TSET (220pF), OVP/OTP (100pF) as close as possible to the respective pins.
- Keep the FB trace as short as possible and route the FB trace away from high dv/dt traces.
- Use film capacitors or C0G, NP0 ceramic capacitors for low distortion of the ISNS capacitor.
- Add necessary filtering capacitors on the VCCP pin to filter out the high spikes on the bias winding waveform.
- Keep necessary high voltage clearance and creepage.
- If 2kV HBM ESD rating is needed on the HV pin, place a 100pF capacitor from the HV pin to ground to pass up to 2kV HBM ESD.

8.4.2 Layout Example

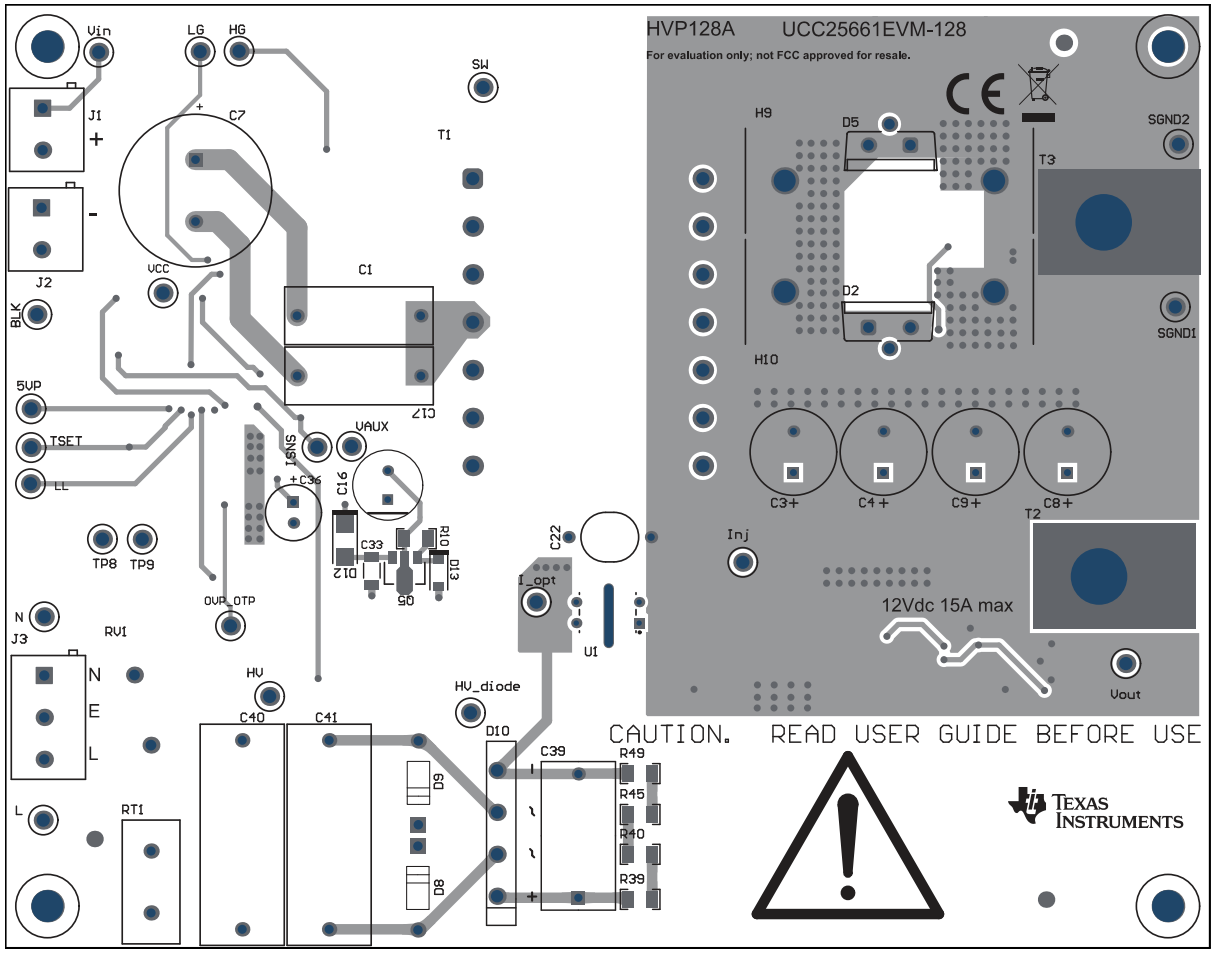


Figure 8-6. UCC25661EVM-128 (Top View)

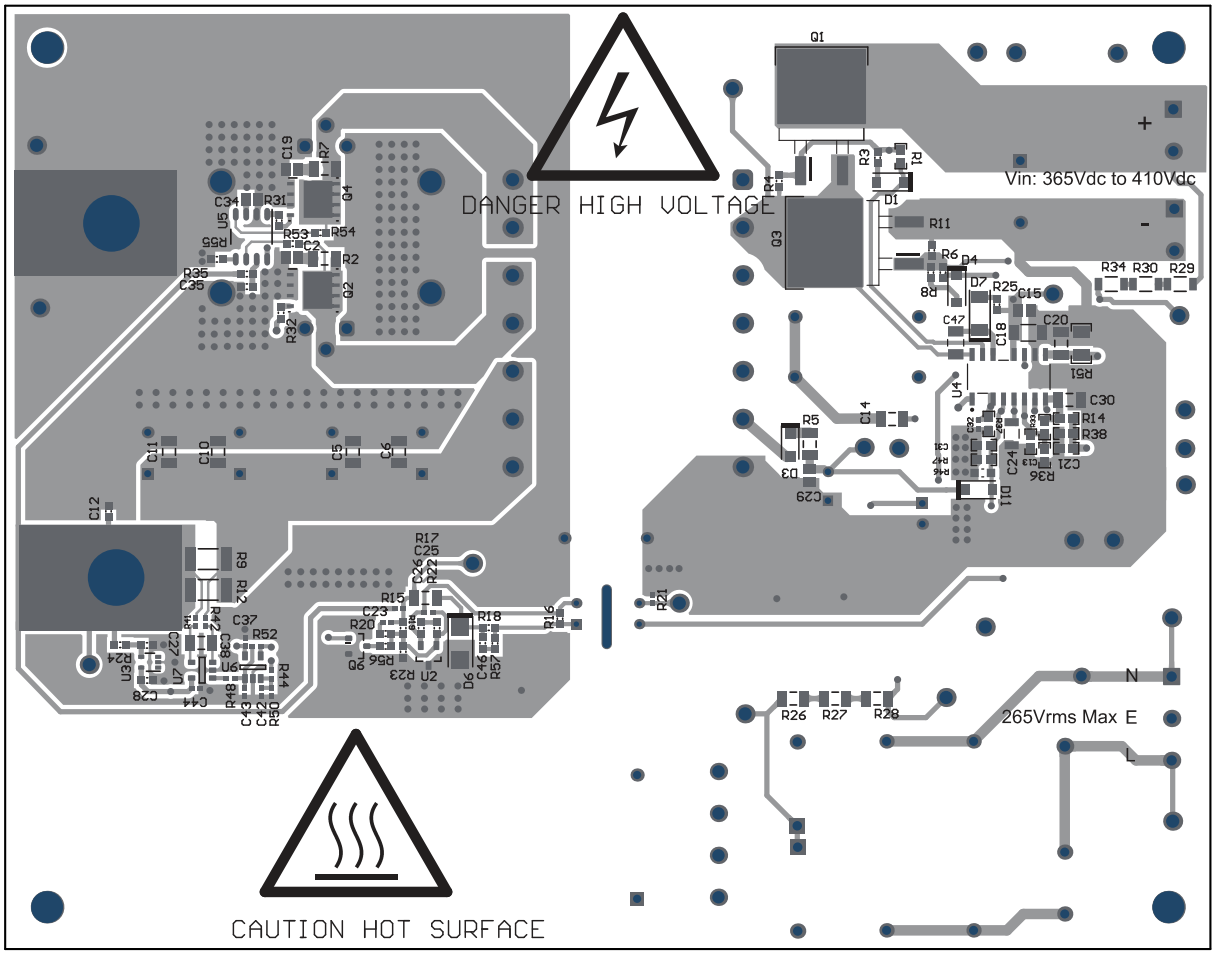


Figure 8-7. UCC25661EVM-128 (Bottom View)

9 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

9.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

9.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.
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9.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.5 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

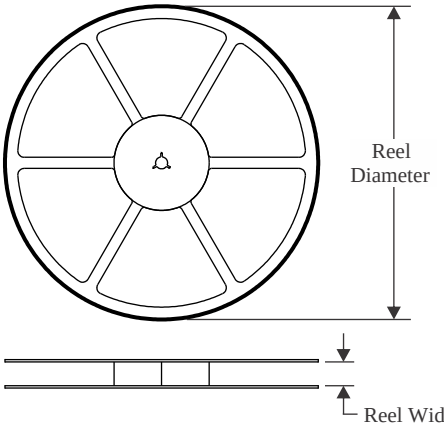
Changes from Revision * (May 2025) to Revision A (September 2025)	Page
• Updated from *Advance Information* to *Production Data*	1

11 Mechanical, Packaging, and Orderable Information

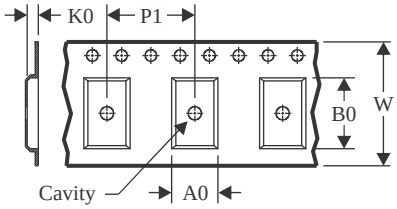
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

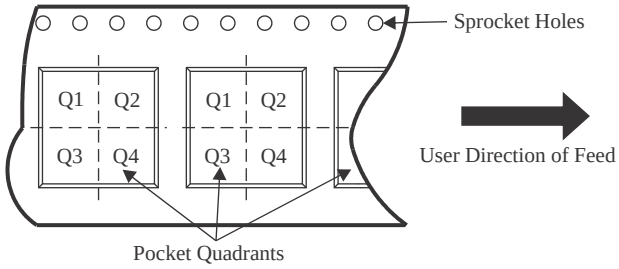


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

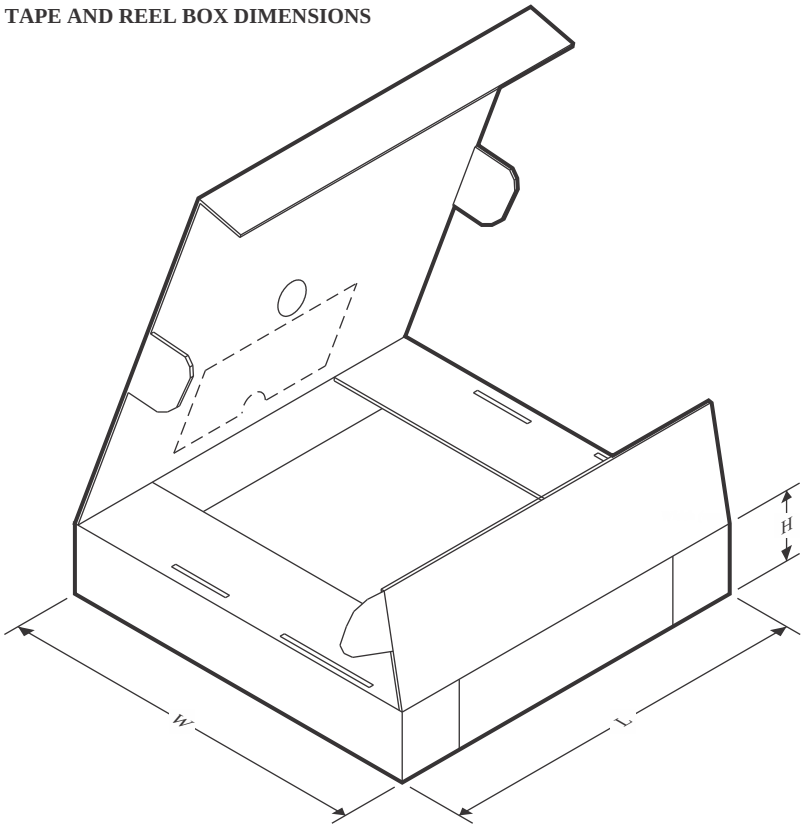
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UCC256612QDDBRQ1	SOIC	DDB	14	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
UCC256613QDDBRQ1	SOIC	DDB	14	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
UCC256614QDDBRQ1	SOIC	DDB	14	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
UCC256615QDDBRQ1	SOIC	DDB	14	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

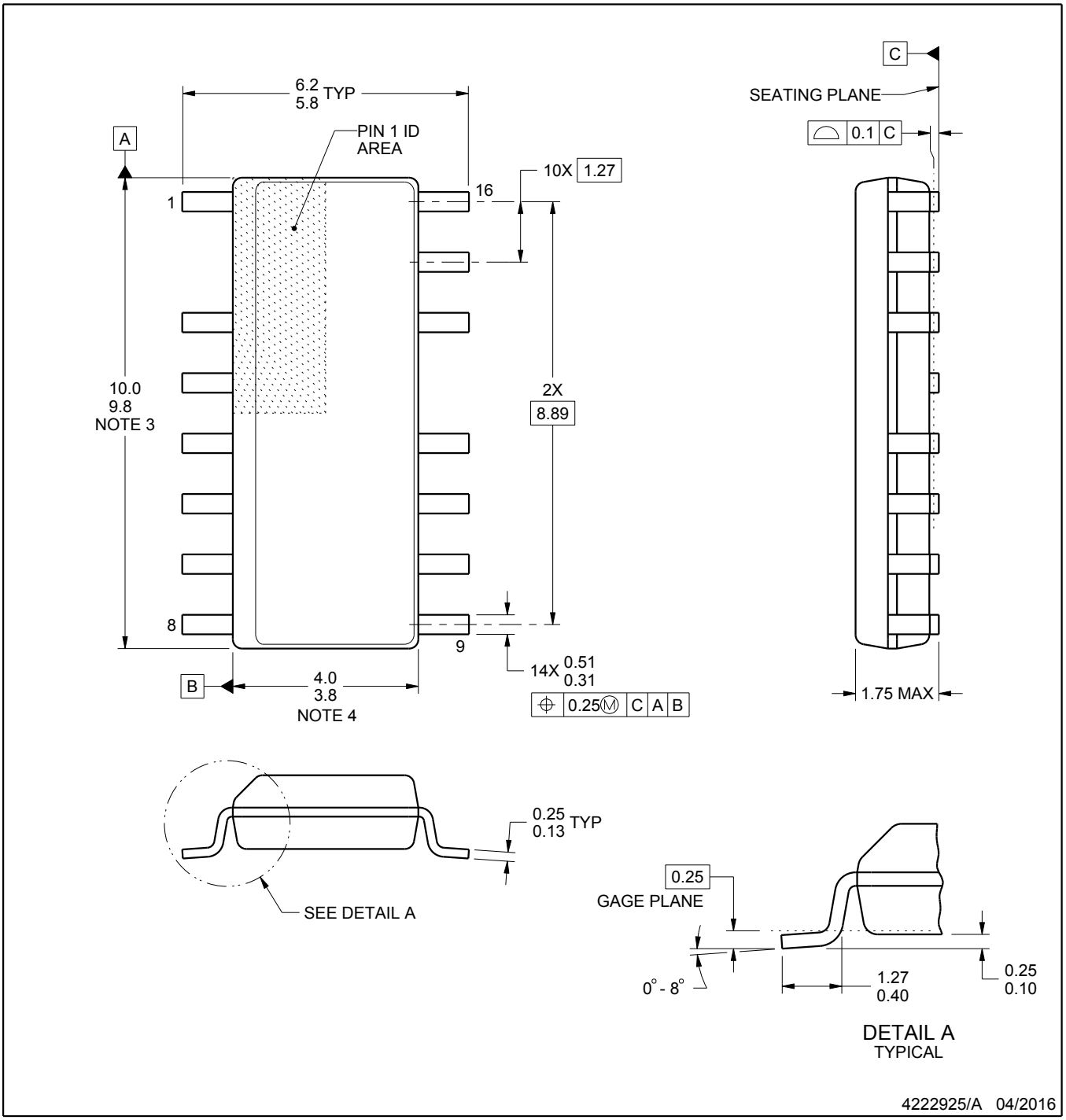
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UCC256612QDDBRQ1	SOIC	DDB	14	2500	353.0	353.0	32.0
UCC256613QDDBRQ1	SOIC	DDB	14	2500	353.0	353.0	32.0
UCC256614QDDBRQ1	SOIC	DDB	14	2500	353.0	353.0	32.0
UCC256615QDDBRQ1	SOIC	DDB	14	2500	353.0	353.0	32.0

PACKAGE OUTLINE

DDB0014A

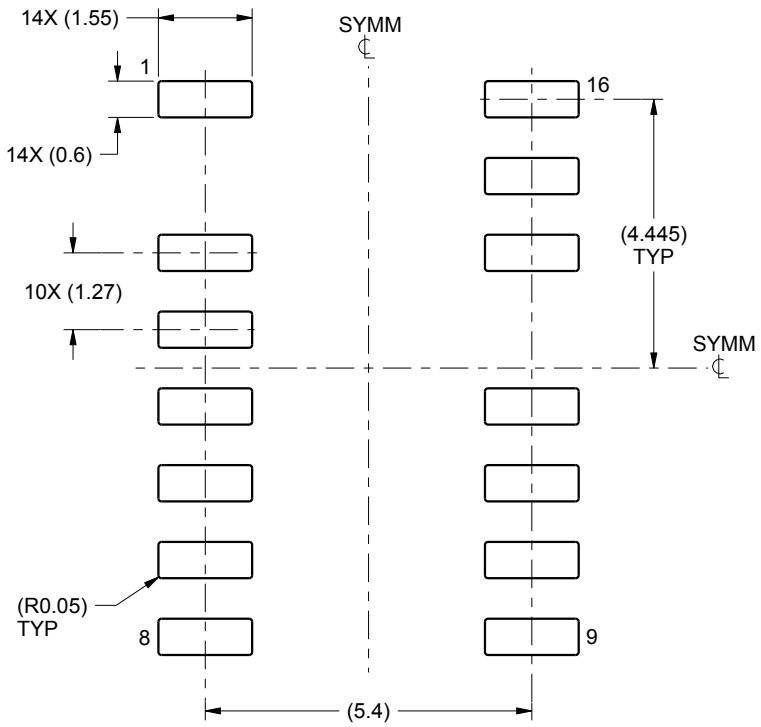
SOIC - 1.75 mm max height

SOIC

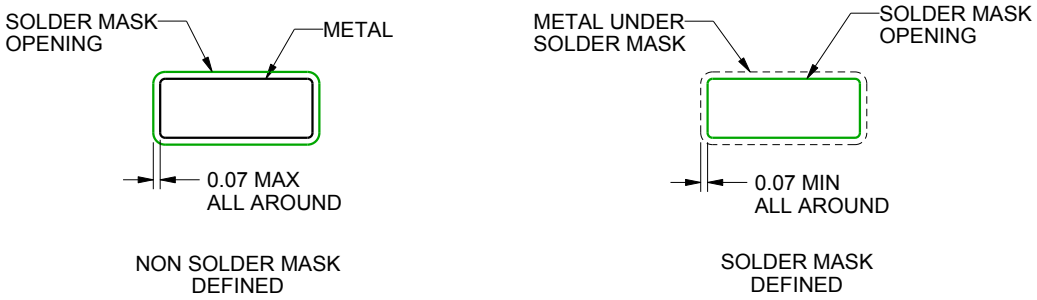


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-012, variation AC.



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

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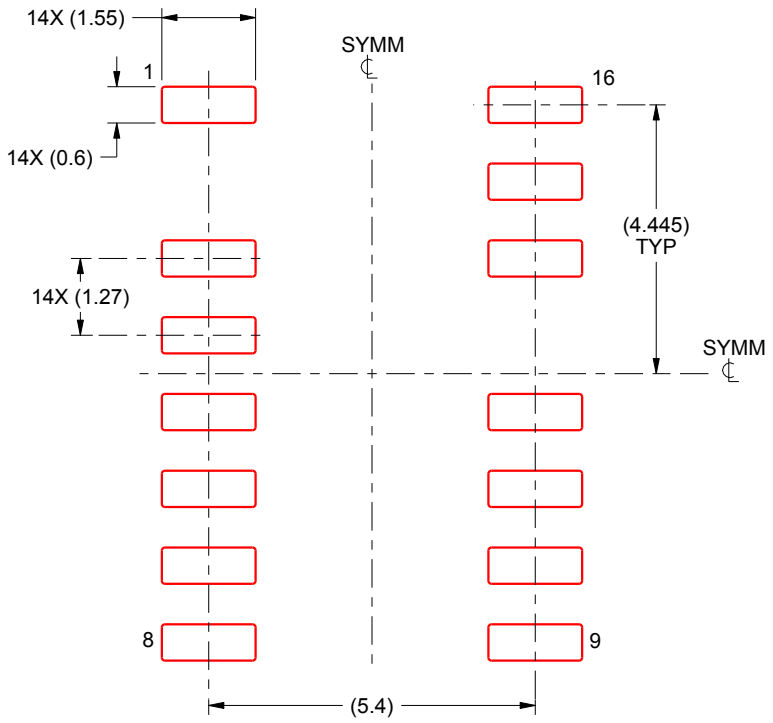
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4222925/A 04/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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