UCC218915-Q1 Single Channel Isolated Pre-Driver for SiC/IGBT with Active Protection for Automotive Applications

1 Features

- 5kV$_{RMS}$ single-channel isolated pre-driver
- AEC-Q100 qualified for automotive applications
  - Device temperature grade 1: -40°C to +125°C ambient operating temperature range
- SiC MOSFETs and IGBTs up to 1500V$_{pk}$
- 36V maximum output drive voltage (VDD-VEE)
- 2.8A outputs for directly driving external buffer PMOS/NMOS pair.
- 200V/ns minimum CMTI
- 200ns response time fast DESAT protection with 9V threshold
- External active Miller clamp
- Dedicated Soft Shut Down (SSD) pin with 1A sinking capability. Shut down current is controllable by an external resistor.
- ASC input on isolated side to turn on power switch during system fault. ASC status reported through ASC_FB on low-voltage side.
- Overcurrent reporting on $\overline{FLT}$ and reset from $\overline{RST}$/EN
- Fast enable/disable response on $\overline{RST}$/EN
- 12V VDD UVLO with power good on RDY
- Overtemperature protection with power good on RDY
- 100ns (maximum) propagation delay
- 28-DFP wide body package with creepage and clearance distance > 8mm
- Operating junction temperature –40°C to 150°C

2 Applications

- Traction inverter for EVs
- On-board charger and charging pile
- DC-DC converter for HEV/EVs

3 Description

The UCC218915-Q1 is a galvanically isolated single channel pre-driver designed for SiC MOSFETs and IGBTs up to 1500V DC operating voltage with advanced protection features, best-in-class dynamic performance, and robustness. The UCC218915-Q1 has dual 2.8A outputs for directly driving an external buffer NMOS/PMOS pair.

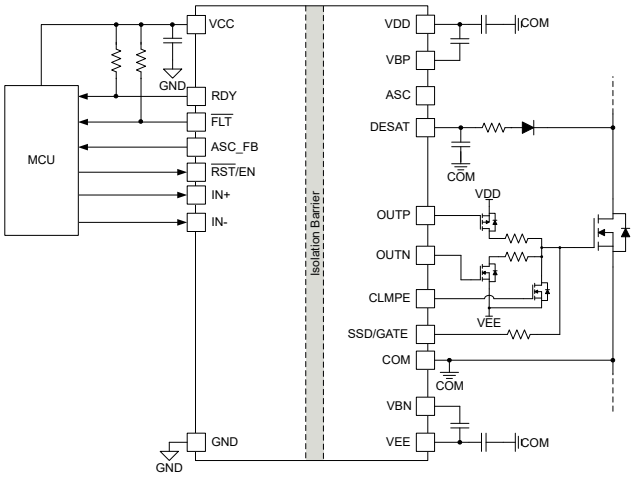
The input side is isolated from the output side with SiO_2 isolation technology, supporting up to 1.06kV$_{RMS}$ working voltage, 10kV$_{PK}$ surge immunity with longer than 40-years isolation barrier life, as well as providing low part-to-part skew, and >200V/ns common mode noise immunity (CMTI).

The UCC218915-Q1 includes state-of-art protection features, such as fast overcurrent and short circuit detection, controlled soft shutdown after a fault, fault reporting, active Miller clamp, active short circuit input on the high-voltage side and input and output side power supply UVLO to optimize SiC and IGBT switching behavior and robustness.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)	BODY SIZE (NOM)
UCC218915-Q1(3)	DFP (SSOP 28)	7.6mm × 10.3mm	7.6mm × 7.5mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.
(3) Advance Information



Simplified Application Schematic

ADVANCE INFORMATION

ADVANCE INFORMATION

Table of Contents

4 Pin Configuration and Functions

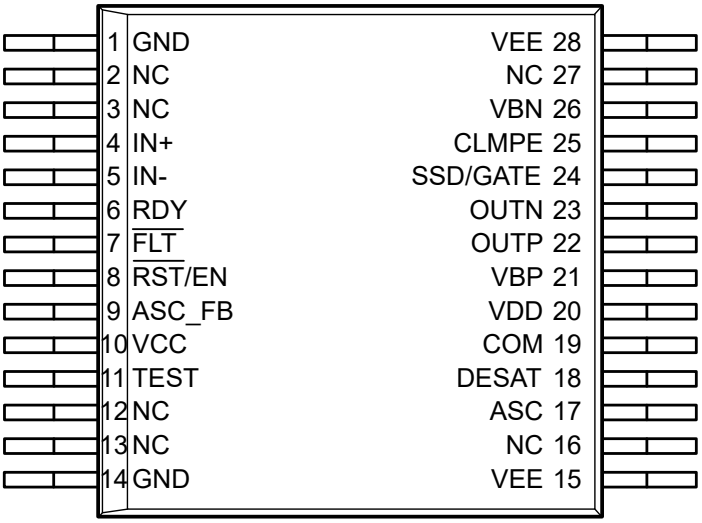


Figure 4-1. UCC218915-Q1 28-Pin DFP SSOP Package Top View

Pin Functions

PIN		I/O[1]	DESCRIPTION
NAME	NO.		
GND	1, 14	G	Input power supply and logic ground reference.
NC	2, 3, 12, 13, 16, 27	—	No connection
IN+	4	I	Non-inverting gate driver control input. Tie to VCC if unused.
IN-	5	I	Inverting gate driver control input. Tie to GND if unused.
RDY	6	O	Power good for VCC-GND, VDD-COM, and overtemperature. RDY is an open-drain output and can be paralleled with other RDY signals.
$\overline{\text{FLT}}$	7	O	Active low fault alarm output upon overcurrent or short circuit. $\overline{\text{FLT}}$ is an open drain output and can be paralleled with other faults.
$\overline{\text{RST}}$/EN	8	I	The $\overline{\text{RST}}$/EN serves two purposes: 1) Enables or shuts down the output side. The FET is turned off by a regular turn-off if EN is set to low; 2) Resets the DESAT condition signaled on the $\overline{\text{FLT}}$ pin if $\overline{\text{RST}}$/EN is set to low for more than 800ns. A reset of $\overline{\text{FLT}}$ is asserted at the rising edge of $\overline{\text{RST}}$/EN.
ASC_FB	9	O	ASC feedback output. This pin outputs high when ASC is active and the output stage is on. Leave floating if unused.
VCC	10	P	Input power supply from 3V to 5.5V. Bypass with a >1µF capacitor to GND. Place decoupling capacitor close to the pin.
TEST	11	I	Test mode input. Tie to GND or leave floating if unused.
VEE	15, 28	P	Negative supply rail for gate drive voltage. This is the OUTN low-level output voltage. Bypass with a >1µF capacitor to COM. Place decoupling capacitor close to the pin.
ASC	17	I	Active high to enable active short circuit function to force output on during system failure events. Tie to COM if unused.
DESAT	18	I	Desaturation current protection input. Tie to COM if unused.
COM	19	P	Common ground reference. Connect to emitter pin for IGBTs and source pin for MOSFETs.
VDD	20	P	Positive supply rail for gate drive voltage. This is the OUTP high-level output voltage. Bypass with a >1µF capacitor to COM. Place decoupling capacitor close to the pin.
VBP	21	P	Bias supply for the OUTP low voltage. A capacitor to VDD may be used to stabilize this supply.
OUTP	22	O	Pre-driver output for driving external buffer PMOS in a push-pull configuration.
OUTN	23	O	Pre-driver output for driving external buffer NMOS in a push-pull configuration.

ADVANCE INFORMATION

Pin Functions (continued)

PIN		I/O[1]	DESCRIPTION
NAME	NO.		
SSD/ GATE	24	O	Soft shutdown pull down for turning off after a DESAT fault. Connect a resistor from this pin to the gate of an IGBT or MOSFET to adjust the shutdown current. This pin is also used to monitor the gate voltage for the external Miller clamp.
CLMPE	25	O	External active Miller clamp control. Connect this pin to the gate of the external Miller clamp MOSFET. Leave floating if unused.
VBN	26	P	Bias supply for the OUTN high voltage. A capacitor to VEE may be used to stabilize this supply.

(1) P = Power, G = Ground, I = Input, O = Output

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
VCC	VCC - GND	–0.3	6	V
VDD	VDD - COM	–0.3	36	V
VEE	VEE - COM	–17.5	0.3	V
V_{MAX}	VDD - VEE	–0.3	36	V
IN+, IN-, $\overline{RST}$/EN	DC	GND–0.3	VCC+0.3	V
$\overline{FLT}$, RDY, ASC_FB	Voltage on primary-side output pins	GND–0.3	VCC	V
VBP, OUTP	Voltage on VBP, OUTP	VDD-20	VDD+0.3	V
VBN, OUTN	Voltage on VBN, OUTN	VEE-0.3	VEE+20	V
SSD/GATE	DC	VEE-0.3	VDD+0.3	V
	Transient, less than 100ns(2)	VEE-5.0	VDD+5.0	V
CLMPE	Voltage on CLMPE, reference to VEE	–0.3	20	V
DESAT	Voltage on DESAT, reference to COM	-0.3	VDD+0.3	V
ASC	Voltage on ASC, reference to COM	-0.3	6	V
$I_{\overline{FLT}}$, I_{RDY}	$\overline{FLT}$ and RDY pin input current		20	mA
T_J	Junction temperature	–40	150	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Values are verified by characterization on bench.

5.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002(1)		±2000	V
		Charged device model (CDM), per AEC Q100-011	Corner pins (GND and VEE)	±750	
			Other pins	±500	V

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
VCC	VCC-GND	3	5.5	V
VDD	VDD-COM	13	30	V
VEE	VEE-COM	-16	0	V
V_{MAX}	VDD-VEE		30	V
IN+, IN-, $\overline{RST}$/EN	Reference to GND, high level input voltage	0.7xVCC	VCC	V
	Reference to GND, low level input voltage	0	0.3xVCC	V
t_{PWM_MIN}	Minimum input pulse width (IN+ and IN-)	50		ns
$t_{\overline{RST}/EN}$	Minimum pulse width that resets the fault	800		ns
ASC	Reference to COM	0	5	V
T_A	Ambient temperature	–40	125	°C

ADVANCE INFORMATION

5.3 Recommended Operating Conditions (continued)

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
T_J	Junction temperature	–40	150	°C

5.4 Thermal Information

THERMAL METRIC(1)		UCC218915 DFP (TSSOP) 28 Pins	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	81.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	39.4	V
$R_{\theta JB}$	Junction-to-board thermal resistance	48.7	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	20.1	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	47.6	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

5.5 Power Ratings

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
P_D	Maximum power dissipation (both sides)	VCC = 5V, VDD-COM = 20V, COM-VEE = 5V, IN+/- = 5V, 140 kHz, 5% Duty Cycle for 10nF load, Ta = 25℃		TBD		mW
P_{D1}	Maximum power dissipation by transmitter side	VCC = 5V, VDD-COM = 20V, COM-VEE = 5V, IN+/- = 5V, 140 kHz, 5% Duty Cycle for 10nF load, Ta = 25℃		TBD		mW
P_{D2}	Maximum power dissipation by receiver side	VCC = 5V, VDD-COM = 20V, COM-VEE = 5V, IN+/- = 5V, 140 kHz, 5% Duty Cycle for 10nF load, Ta = 25℃		TBD		mW

5.6 Insulation Specifications

PARAMETER		TEST CONDITIONS	VALUE	UNIT
GENERAL				
CLR	External clearance(1)	Shortest terminal-to-terminal distance through air	> 8	mm
CPG	External Creepage(1)	Shortest terminal-to-terminal distance across the package surface	> 8	mm
DTI	Distance through the insulation	Minimum internal gap (internal clearance)	> 17	µm
CTI	Comparative tracking index	DIN EN 60112 (VDE 0303-11); IEC 60112	> 600	V
	Material Group	According to IEC 60664–1	I	
	Overvoltage Category per IEC 60664–1	Rated mains voltage ≤ 300 V_{RMS}	I-IV	
		Rated mains voltage ≤ 600 V_{RMS}	I-III	
		Rated mains voltage ≤ 1000 V_{RMS}	I-II	
DIN EN IEC 60747-17 (VDE 0884-17)(2)				
V_{IORM}	Maximum repetitive peak isolation voltage	AC voltage (bipolar)	1500	V_{PK}
V_{IOWM}	Maximum isolation working voltage	AC voltage (sine wave); time-dependent dielectric breakdown (TDDB) test	1063	V_{RMS}
		DC voltage	1500	V_{DC}

ADVANCE INFORMATION

5.6 Insulation Specifications (continued)

PARAMETER		TEST CONDITIONS	VALUE	UNIT
V_{IOTM}	Maximum transient isolation voltage	$V_{TEST} = V_{IOTM}$, t = 60 s (qualification test) V_{TEST}= 1.2 × V_{IOTM}, t = 1 s (100% production test)	7071	V_{PK}
V_{IMP}	Maximum impulse voltage(3)	Tested in air, 1.2/50-µs waveform per IEC 62368-1	7692	V_{PK}
V_{IOSM}	Maximum surge isolation voltage(4)	Tested in oil (qualification test), 1.2/50-µs waveform per IEC 62368-1	10000	V_{PK}
q_{pd}	Apparent charge(5)	Method a: After I/O safety test subgroup 2/3, V_{ini} =V_{IOTM}, t_{ini} = 60 s; $V_{pd(m)}$ = 1.2 × V_{IORM}, t_m = 10 s	≤ 5	pC
		Method a: After environmental tests subgroup 1, V_{ini} = V_{IOTM}, t_{ini} = 60 s; $V_{pd(m)}$ = 1.6 × V_{IORM}, t_m = 10 s	≤ 5	
		Method b: At routine test (100% production); V_{ini} = 1.2 x V_{IOTM}, t_{ini} = 1 s; $V_{pd(m)}$ = 1.875 × V_{IORM}, t_m = 1 s (method b1) or $V_{pd(m)}$= V_{ini}, t_m = t_{ini} (method b2)	≤ 5	
C_{IO}	Barrier capacitance, input to output(6)	V_{IO} = 0.5 × sin (2πft), f = 1 MHz	~1.2	pF
R_{IO}	Insulation resistance, input to output(6)	V_{IO} = 500 V, T_A = 25°C	≥ 10^{12}	Ω
		V_{IO} = 500 V, 100°C ≤ T_A ≤ 125°C	≥ 10^{11}	
		V_{IO} = 500 V at T_S = 150°C	≥ 10^9	
	Pollution degree		2	
	Climatic category		40/125/21	
UL 1577				
V_{ISO}	Withstand isolation voltage	$V_{TEST} = V_{ISO}$ = 5000 V_{RMS}, t = 60 s (qualification), V_{TEST} = 1.2 × V_{ISO}, t = 1 s (100% production)	5000	V_{RMS}

(1) Apply creepage and clearance requirements according to the specific equipment isolation standards of an application. Care must be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed circuit board (PCB) do not reduce this distance. Creepage and clearance on a PCB become equal in certain cases. Techniques such as inserting grooves and ribs on the PCB are used to help increase these specifications.
(2) This coupler is suitable for *safe electrical insulation* only within the safety ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.
(3) Testing is carried out in air to determine the surge immunity of the package
(4) Testing is carried out in oil to determine the intrinsic surge immunity of the isolation barrier.
(5) Apparent charge is electrical discharge caused by a partial discharge (pd).
(6) All pins on each side of the barrier tied together creating a two-pin device.

5.7 Electrical Characteristics

VCC = 3.3 V or 5.0 V, 1-µF capacitor from VCC to GND, VDD - COM and COM - VEE over recommended operating conditions unless otherwise noted, no external capacitor on VBN or VBP, C_L = 100 pF, -40°C < T_J < 150°C (unless otherwise noted)(1) (2).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLY QUIESCENT CURRENT						
I_{VCCQ}	VCC quiescent current	IN+ = GND, IN- = GND, f_s = 0 Hz	1	2	3	mA
		IN+ = VCC, IN- = GND, f_s = 0 Hz	3	4	5.5	mA
I_{VDDQ}	VDD quiescent current	IN+ = GND, IN- = GND, f_s = 0 Hz	3	5	7	mA
		IN+ = VCC, IN- = GND, f_s = 0 Hz	4	7	10	mA
I_{VEEQ}	VEE quiescent current	IN+ = GND, IN- = GND, f_s = 0 Hz, VEE = -5 V	-5	-3.5	-2	mA
		IN+ = VCC, IN- = GND, f_s = 0 Hz, VEE = -5 V	-5	-3.5	-2	mA
POWER SUPPLY PROTECTION						
V_{VCC_ON}	VCC UVLO rising threshold		2.5	2.6	2.75	V
V_{VCC_OFF}	VCC UVLO falling threshold		2.4	2.5	2.65	V
V_{VCC_HYST}	VCC UVLO hysteresis			100		mV

ADVANCE INFORMATION

5.7 Electrical Characteristics (continued)

VCC = 3.3 V or 5.0 V, 1-µF capacitor from VCC to GND, VDD - COM and COM - VEE over recommended operating conditions unless otherwise noted, no external capacitor on VBN or VBP, C_L = 100 pF, -40℃ < T_J < 150℃ (unless otherwise noted)(1) (2).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{VCCFIL}	VCC UVLO deglitch time			5		µs
$t_{VCC+ to OUT}$	VCC UVLO on delay to OUTN low	IN+ = VCC, IN- = GND		tbd	15	µs
$t_{VCC- to OUT}$	VCC UVLO off delay to OUTP high				11	µs
$t_{VCC+ to RDY}$	VCC UVLO on delay to RDY high	$\overline{RST}$/EN = VCC		tbd	20	µs
$t_{VCC- to RDY}$	VCC UVLO off delay to RDY low				11	µs
$V_{VDD\_UVLO\_ON}$	VDD UVLO rising threshold		11.4	12	12.6	V
$V_{VDD\_UVLO\_OFF}$	VDD UVLO falling threshold		10.45	11	11.55	V
V_{VDD_HYST}	VDD UVLO hysteresis			1		V
t_{VDDFIL}	VDD UVLO deglitch time			5		µs
$t_{VDD+ to OUT}$	VDD UVLO on delay to OUTN low	IN+ = VCC, IN- = GND			10	µs
$t_{VDD- to OUT}$	VDD UVLO off delay to OUTP high				10	µs
$t_{VDD+ to RDY}$	VDD UVLO on delay to RDY high	$\overline{RST}$/EN = $\overline{FLT}$ = VCC			15	µs
$t_{VDD- to RDY}$	VDD UVLO off delay to RDY low				15	µs
LOW VOLTAGE SIDE LOGIC INPUTS (IN+, IN-, $\overline{RST}$/EN)						
V_{INH}	Input High Threshold			0.57xV_{CC}	0.7xV_{CC}	V
V_{INL}	Input low threshold		0.3xV_{CC}	0.42xV_{CC}		V
V_{INHYS}	Input threshold hysteresis			0.15xV_{CC}		V
I_{IH}	Input high level input leakage current	V_{IN} = VCC, VCC = 5 V		50		uA
I_{IL}	Input low level input leakage current	V_{IN} = GND, VCC = 5V		-50		uA
R_{IND}	Input pins pull down resistance			100		kΩ
R_{INU}	Input pins pull up resistance			100		kΩ
t_{INFIL}	IN+, IN– and $\overline{RST}$/EN deglitch (ON and OFF) filter time	f_S = 50kHz		25		ns
t_{RSTFIL}	Deglitch filter time to reset $\overline{FLT}$		400	650	800	ns
GATE DRIVER STAGE						
I_{OUTP}	Peak source and sink current for OUTP		1.5	2.8		A
I_{OUTN}	Peak source and sink current for OUTN		1.5	2.8		A
V_{OUTP_L}	OUTP low-level output voltage		VDD-13	VDD-11	VDD-9	V
V_{OUTN_H}	OUTN high-level output voltage, referenced to VEE		9	11	13	V
t_{OUTDT}	Deadtime between OUTP and OUTN transitions		25	50	85	ns
EXTERNAL MILLER CLAMP						
V_{CLMPTH}	Miller clamp threshold voltage	Reference to VEE	1.7	2.0	2.3	V
V_{CLMPE}	Output high voltage		9	11	13	V
I_{CLMPEH}	Peak source current	C_{CLMPE} = 10nF		0.5		A
I_{CLMPEL}	Peak sink current			0.5		A
t_{CLMPER}	CLMPE rise time (10% to 90%)(3)	C_{CLMPE} = 330pF		5	20	ns
t_{DCLMPE}	Miller clamp ON delay time			35	60	ns
DESAT PROTECTION						
I_{CHG}	Blanking capacitor charge current	V_{DESAT} = 2.0V		2000		µA
I_{DCHG}	Blanking capacitor discharge current	V_{DESAT} = 6.0V		50		mA

ADVANCE INFORMATION

5.7 Electrical Characteristics (continued)

VCC = 3.3 V or 5.0 V, 1-µF capacitor from VCC to GND, VDD - COM and COM - VEE over recommended operating conditions unless otherwise noted, no external capacitor on VBN or VBP, C_L = 100 pF, -40℃ < T_J < 150℃ (unless otherwise noted)(1) (2).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{DESATTH}$	Detection threshold		8.5	9	9.5	V
$t_{DESATLEB}$	Leading edge blank time			200		ns
$t_{DESATFIL}$	DESAT deglitch filter		80	125	170	ns
$t_{DESATOFF}$	DESAT propagation delay to OUTP high	V_{DESAT}>$V_{DESATTH}$	150	200	300	ns
$t_{DESATFLT}$	DESAT to $\overline{FLT}$ low delay				10	µs
SOFT SHUTDOWN (SSD)						
I_{SSD}	Soft shutdown sink current	V_{SSD}-COM = 8 V	0.5	1	1.65	A
t_{SSD}	Soft shutdown activation time		1.5	2	2.5	µs
R_{SSD}	Soft shutdown pull-down resistance	I_{SSD} = 0.1A		1.9		Ω
OVERTEMPERATURE PROTECTION						
T_{TSDTH}	Thermal shutdown rising threshold		155			℃
$T_{TSDHYST}$	Thermal shutdown hysteresis			20		℃
ACTIVE SHORT CIRCUIT (ASC)						
V_{ASCL}	ASC input low threshold referenced to COM		1.2	1.45	1.7	V
V_{ASCH}	ASC input high threshold referenced to COM		2.3	2.7	3.1	V
R_{ASCD}	ASC input pulldown resistance			100		kΩ
t_{ASCFIL}	ASC deglitch filter time		400		700	ns
t_{ASC_r}	ASC on delay to OUTN low				1	µs
t_{ASC_f}	ASC off delay to OUTP high				1	µs
t_{ASC_FB}	ASC to ASC_FB delay				10	µs
FAULT REPORTING ($\overline{FLT}$, RDY)						
t_{RDYHLD}	VDD UVLO RDY low minimum holding time				100	µs
$t_{FLTMUTE}$	Output mute time on overcurrent fault	Reset fault through $\overline{RST}$/EN			100	µs
R_{ODON}	Open drain output on resistance	I_{ODON} = 10mA			30	Ω
COMMON MODE TRANSIENT IMMUNITY						
CMTI	CMTI noise immunity	V_{CM} = 1500 V	200			V/ns

(1) Currents are positive into and negative out of the specified terminal.
(2) All voltages are referenced to COM unless otherwise noted
(3) Timing thresholds for OUTP, OUTN, and CLMPE are 0.9V and 8.1V (10% and 90% of min value)

5.8 Switching Characteristics

VCC = 3.3 V or 5.0 V, 1-µF capacitor from VCC to GND, VDD - COM and COM - VEE over recommended operating conditions unless otherwise noted, no external capacitor on VBN or VBP, C_L = 1 nF, -40℃ < T_J < 150℃ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PDON}	Turn-on propagation delay	(IN+ - IN-) high to OUTN low		65	100	ns
t_{PDOFF}	Turn-off propagation delay	(IN+ - IN-) low to OUTP high		65	100	ns
PWD	Pulse width distortion (t_{PDOFF}-t_{PDON})				30	ns
t_{Pr}	OUTP rise time	10% to 90%(1)		11		ns
t_{Pf}	OUTP fall time	90% to 10%(1)		10		ns

ADVANCE INFORMATION

5.8 Switching Characteristics (continued)

VCC = 3.3 V or 5.0 V, 1-µF capacitor from VCC to GND, VDD - COM and COM - VEE over recommended operating conditions unless otherwise noted, no external capacitor on VBN or VBP, C_L = 1 nF, -40℃ < T_J < 150℃ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{Nr}	OUTN rise time	10% to 90%(1)		9		ns
t_{Nf}	OUTN fall time	90% to 10%(1)		5		ns
f_{MAX}	Maximum switching frequency		100			kHz

(1) Timing thresholds for OUTP, OUTN, and CLMPE are 0.9V and 8.1V (10% and 90% of min value)

ADVANCE INFORMATION

6 Detailed Description

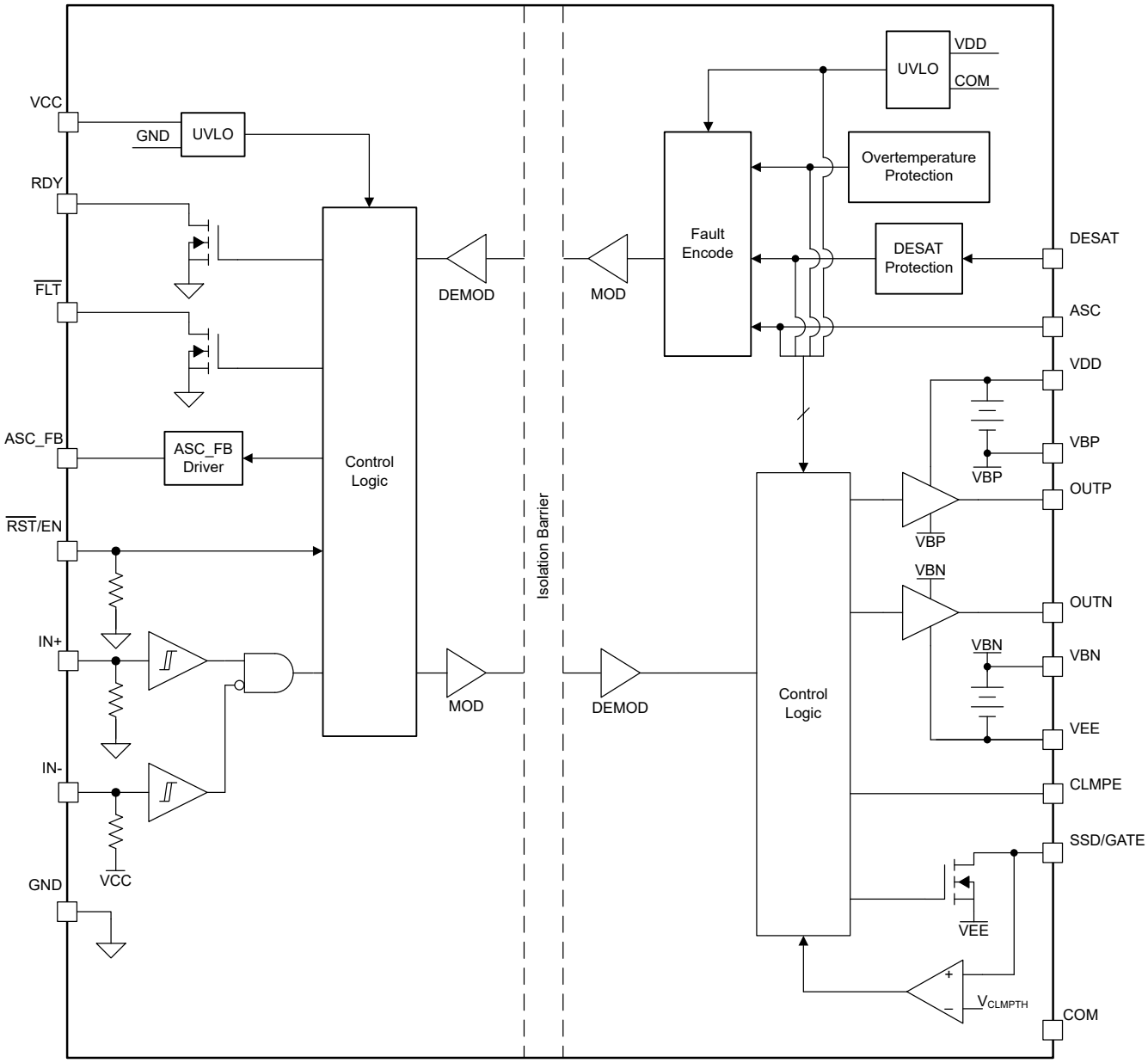
6.1 Overview

The UCC218915-Q1 is an advanced isolated pre-driver with state-of-art protection and sensing features for SiC MOSFETs and IGBTs. The device has dual 2.8A outputs for directly driving an external buffer NMOS/PMOS pair, allowing the device to be used with a wide range of power devices. The input side is isolated from the output side with a reinforced isolation barrier based on SiO_2 isolation technology, supporting up to 1.06kV_{RMS} working voltage and 8kV_{PK} surge immunity with longer than 40-years isolation barrier life. The isolation technology supports 200V/ns minimum CMTI to guarantee the reliability of the system with fast switching speeds. The small propagation delay and part-to-part skew can minimize the deadtime setting, so the conduction loss can be reduced.

The device includes extensive protection and monitoring features to increase the reliability and robustness of the SiC MOSFET and IGBT based systems. Primary and secondary-side supply UVLOs protect the system from operating when the supply voltage levels are too low. The active Miller clamp feature prevents the false turn on causing by Miller capacitance during fast switching. The device has state-of-art DESAT detection time, as well as fault reporting to the low voltage side DSP/MCU. Soft shut down is triggered when the DESAT fault is detected, minimizing the short circuit energy while reducing the overshoot voltage on the switches. The device also has an active-short circuit input on the high-voltage side to force the power switch on during certain fault conditions.

ADVANCE INFORMATION

6.2 Functional Block Diagram



6.3 Feature Description

6.3.1 Power Supplies

The input-side power supply VCC can support a wide voltage range from 3V to 5.5V to support both 3.3V and 5V controller signaling. VCC is monitored by an undervoltage comparator to ensure valid operation. See Section 6.3.2 for more information about the VCC undervoltage lockout protection.

The output-side power supply, VDD to VEE, can support a wide range up to 30V. The device can support either unipolar or bipolar supplies. The negative power supply, VEE, with respect to source or emitter, COM, is usually adopted to avoid false turn on when the other switch in the phase leg is turned on. Negative voltage is important for SiC MOSFETs due to their fast switching speeds, as well as for IGBTs when not using an active Miller clamp. VDD is monitored by an undervoltage comparator to enure valid operation. See Section 6.3.2 for more information about the VDD undervoltage lockout protection.

The OUTP and OUTN predriver outputs are driven to internally generated supply rails optimized for driving silicon buffer MOSFETs. VBP is 11V below VDD for controlling the buffer PMOS on and VBN is 11V above VEE for controlling the buffer NMOS on. Optional external capacitors can be placed from VDD to VBP and from VBN to VEE to minimize supply undershoot during switching transients.

6.3.2 VCC and VDD Undervoltage Lockout (UVLO)

The UCC218915-Q1 implements UVLO protection features for VCC and VDD. When the supply voltage is lower than the threshold voltage, the NMOS buffer FET driver output, OUTN, is held on so that the main power switch will be held off. The driver output will not turn on the PMOS buffer FET until all of the supplies are above the UVLO thresholds. The UVLO protection feature not only reduces the power consumption of the driver itself during low voltage power supply conditions, but also increases the efficiency of the power stage. For SiC MOSFETs and IGBTs, the on-resistance reduces while the gate-source voltage or gate-emitter voltage increases. If the power semiconductor is turned on with a low VDD value, the conduction loss increases significantly and can lead to a thermal issue and efficiency reduction of the power stage.

The UVLO protection blocks feature comparator thresholds with hysteresis and deglitch filters on the inputs to help improve noise immunity of the power supply. During the turn-on and turn-off switching transients, the driver sources and sinks a peak transient current from the power supply, which can result in sudden voltage drop of the power supply. With hysteresis and UVLO deglitch filters, the internal UVLO protection blocks will ignore small noises during the normal switching transients.

The RDY pin on the input side is used to indicate power good condition. The RDY pin is open drain. During UVLO conditions, the RDY pin is held low and connected to GND. Normally the pin is pulled up externally to VCC to indicate power is good.

Timing digrams of the UVLO protection feature of VCC and VDD are shown in Figure 6-1 and Figure 6-2.

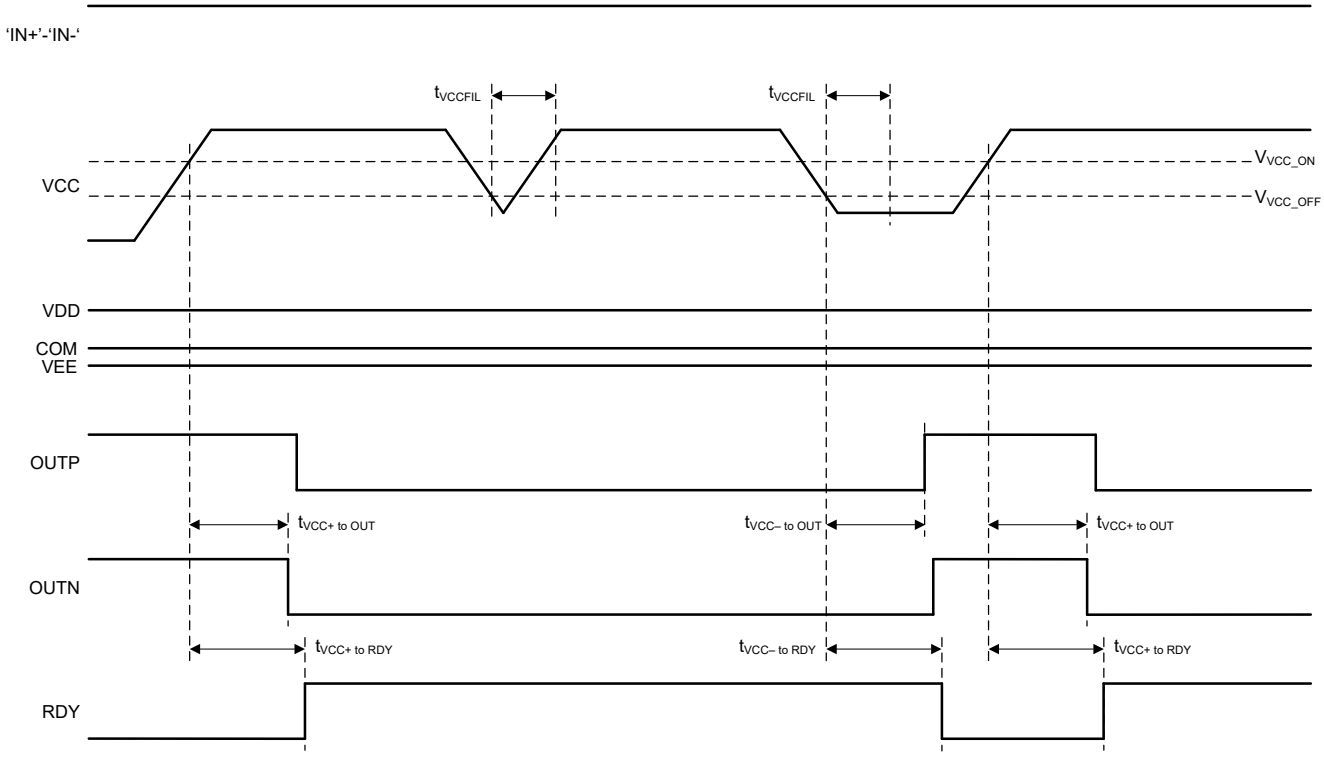


Figure 6-1. VCC Protection Timing Diagram

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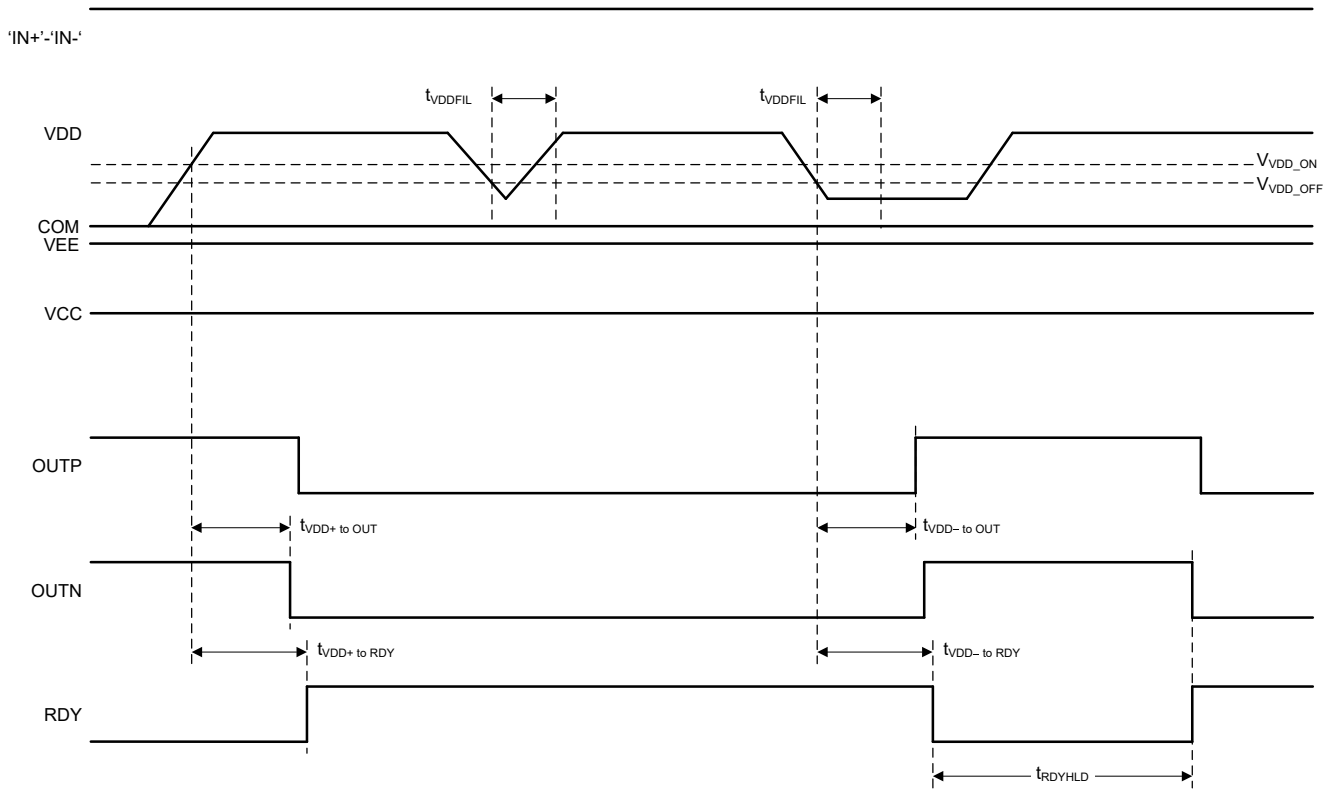

Figure 6-2. VDD Protection Timing Diagram

6.3.3 Input Filters for IN+, IN- and $\overline{\text{RST}}$/EN

The input pins to the UCC218915-Q1 are both 3.3V and 5V logic compatible. The IN+ and $\overline{\text{RST}}$/EN pins have internal pull-down resistors, and the IN- pin has an internal pull-up resistor. If any of these pins are left floating the driver will be disabled. The driver has both inverting and non-inverting PWM input pins. If only the non-inverting IN+ input is used, tie IN- to GND. If only the inverting IN- input is used, tie IN+ to VCC. Both IN+ and IN- can be used for PWM interlocking with the other driver in a half-bridge configuration to prevent phase leg shoot-through.

The device features 25ns typical internal deglitch filters on the IN+, IN-, and $\overline{\text{RST}}$/EN pins in order to protect against unintentional switching due to noise transients or narrow PWM pulses. Any signal less than 25ns will be filtered out and not passed through. For noisy systems, external low pass filters can be added externally to the input pins to further increase noise immunity. When choosing low pass filter components, both noise immunity and delay time should be considered according to system requirements. Figure 6-3 shows the impact of the deglitch filters with narrow pulses on IN+, IN-, and $\overline{\text{RST}}$/EN.

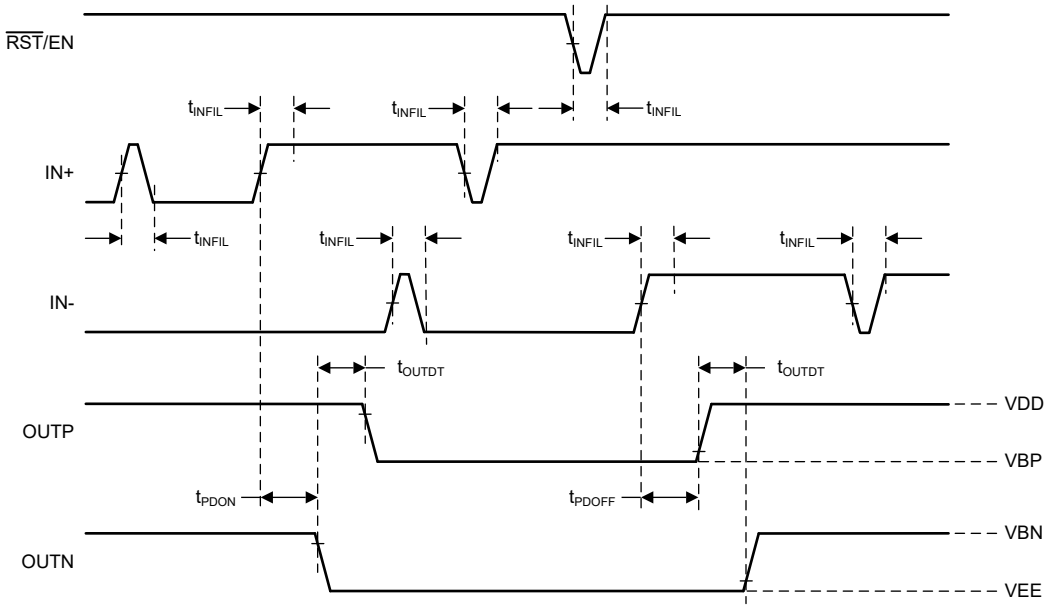

Figure 6-3. Impact of Deglitch Filters

6.3.4 Pre-Driver Outputs

The output stage of the is designed to drive a complimentary pair of external buffer MOSFETs in a push-pull configuration. The PMOS driver (OUTP) and the NMOS driver (OUTN) can each source and sink 2.8A making it suitable for driving a wide range of buffer MOSFETs to cover a wide range of power levels. OUTP and OUTN are driven complimentary with a deadtime, t_{OUTDT}, to prevent cross conduction. OUTP drives the gate of an external PMOS between VDD and VBP, which is an internally generated rail that is 11V below VDD. OUTN drives the gate of an external NMOS between VEE and VBN, which is an internally generated rail that is 11V above VEE. A simplified schematic of the pre-driver architecture is shown in Figure 6-4.

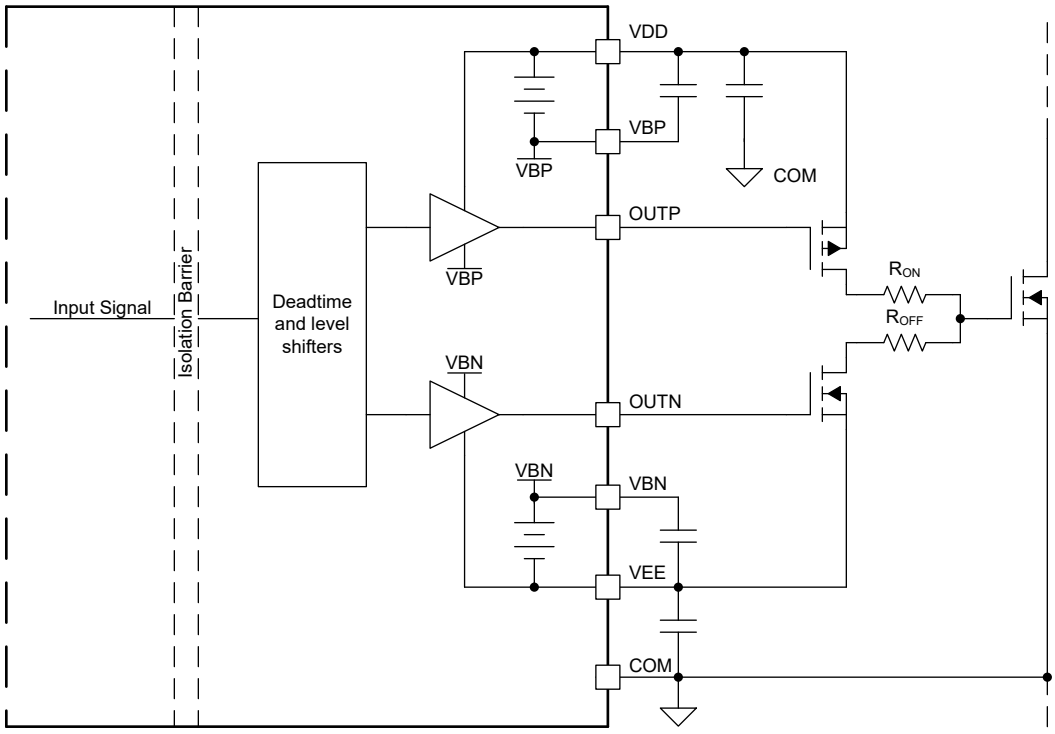

Figure 6-4. Pre-Driver Output Architecture

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Input-to-output states are given in Table 6-1 where ASC is not active and no system faults are present. A timing diagram showing the relationship betweein inputs and outputs is shown in Figure 6-5. Propagation delays from input-to-output, deadtime between OUTN and OUTP transitions, and rise and fall times of the output signals are shown.

Table 6-1. Input-to-Output States with ASC Not Active and No System Faults Present

$\overline{\text{RST}}$/EN	IN+	IN-	OUTP	OUTN	STATE OF EXTERNAL BUFFER FETS	STATE OF EXTERNAL POWER SWITCH
GND	x	x	VDD	VBN	NMOS On	Off
VCC	GND	x	VDD	VBN	NMOS On	Off
VCC	VCC	GND	VBP	VEE	PMOS On	On
VCC	VCC	VCC	VDD	VBN	NOMS On	Off

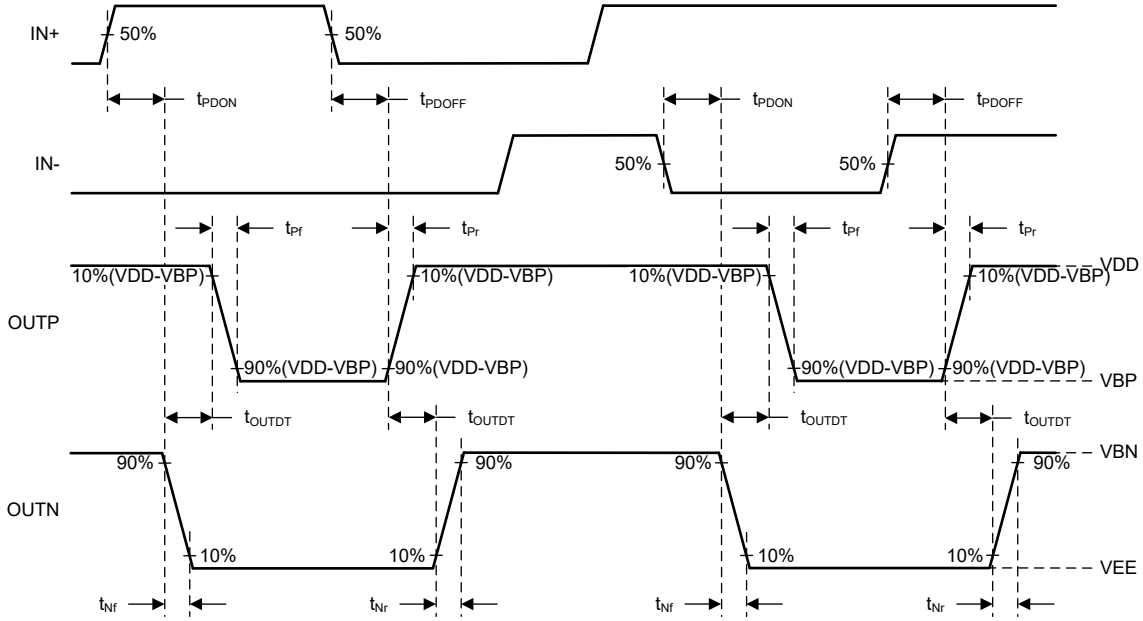

Figure 6-5. Input-to-Output Timing Diagram

6.3.5 External Active Miller Clamp

The UCC218915-Q1 has an active Miller clamp function to add an additional low impedance path to prevent unintentional turn-on while the driver is in the OFF state. In half-bridge applications it is possible for the body diode of the power semiconductor device to conduct while the driver is in the OFF state during deadtime. When this occurs, and the other power semiconductor device in the phase leg turns on, the drain-to-source or collector-to-emitter voltage will increase rapidly, causing high dV/dt across the Miller capacitance. This high dV/dt induces a current spike that can charge the gate capacitance and cause shoot-through if the main turn-off path isn't strong enough due to an external turn-off resistor, long PCB routing traces, or both.

The external active Miller clamp function provides a gate drive signal to drive an external Miller clamp FET. The FET is turned on when the power semiconductor device gate voltage is less than the Miller clamp threshold, V_{CLMPTH}. The gate voltage is sensed through the SSD/GATE pin. A simplified block diagram is shown in Figure 6-6 and a timing diagram is shown in Figure 6-7.

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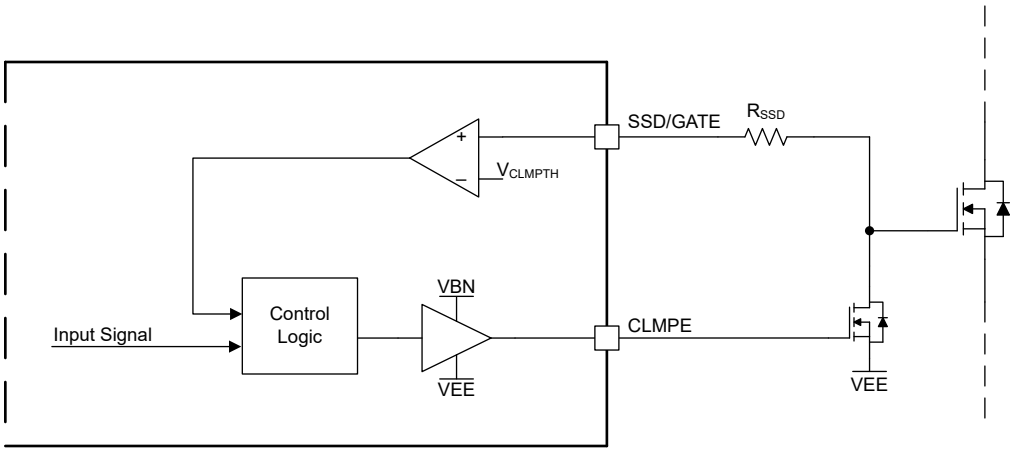

Figure 6-6. External Active Miller Clamp

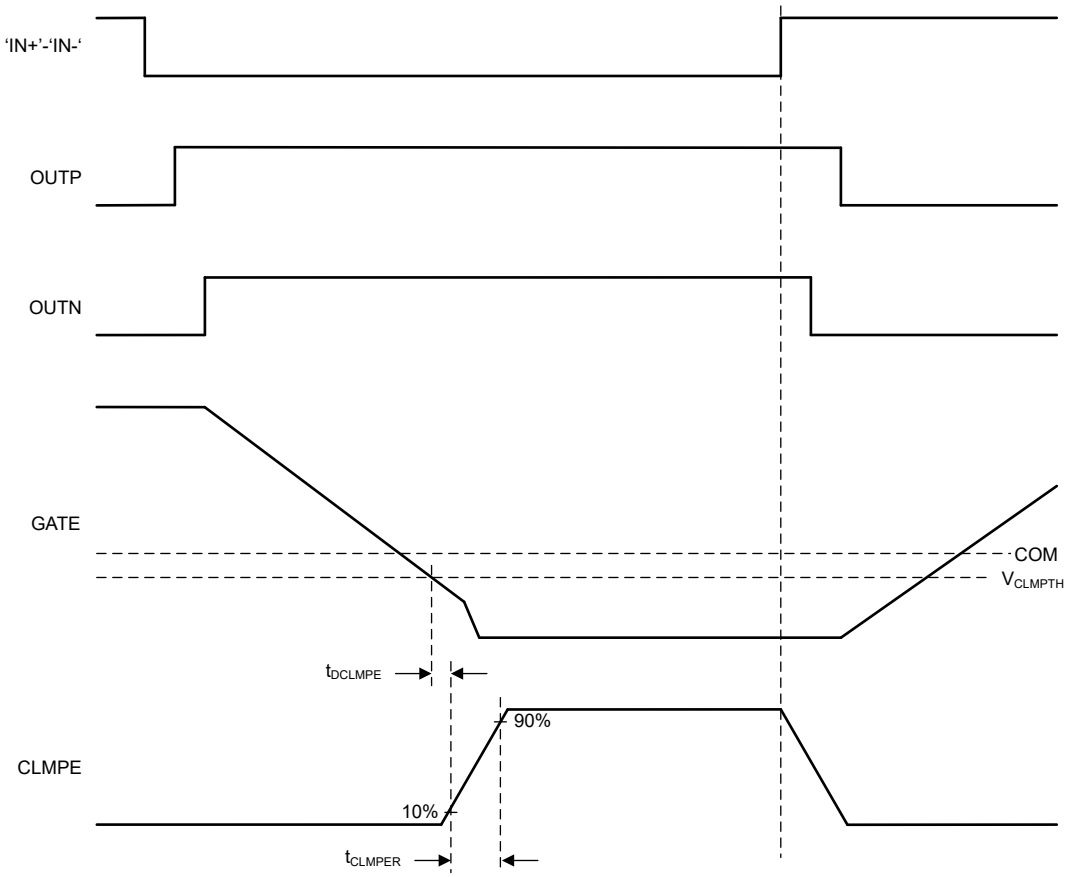

Figure 6-7. External Active Miller Clamp Timing Diagram

6.3.6 Desaturation (DESAT) Protection

The UCC218915-Q1 implements a fast overcurrent and short circuit protection feature to protect the power semiconductor device from catastrophic breakdown during a fault. The DESAT pin threshold, $V_{DESATTH}$, is with respect to COM, the source or emitter of the power semiconductor device. When the driver is in the off state, the DESAT pin is pulled down by an internal MOSFET to prevent DESAT from false triggering. When the driver is in the on state, an internal current source is activated to charge an external capacitor. The UCC218915-Q1 features an internal leading edge blanking time after OUTP switches the buffer PMOS on to avoid false triggers from noise during the switching transient. When the driver turns off, the internal pulldown MOSFET discharges

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the voltage of the DESAT pin. A simplified block diagram of the DESAT circuit is shown in Figure 6-8. Timing diagrams showing a DESAT fault, soft shutdown, fault reporting, and fault reset are shown in Figure 6-9.

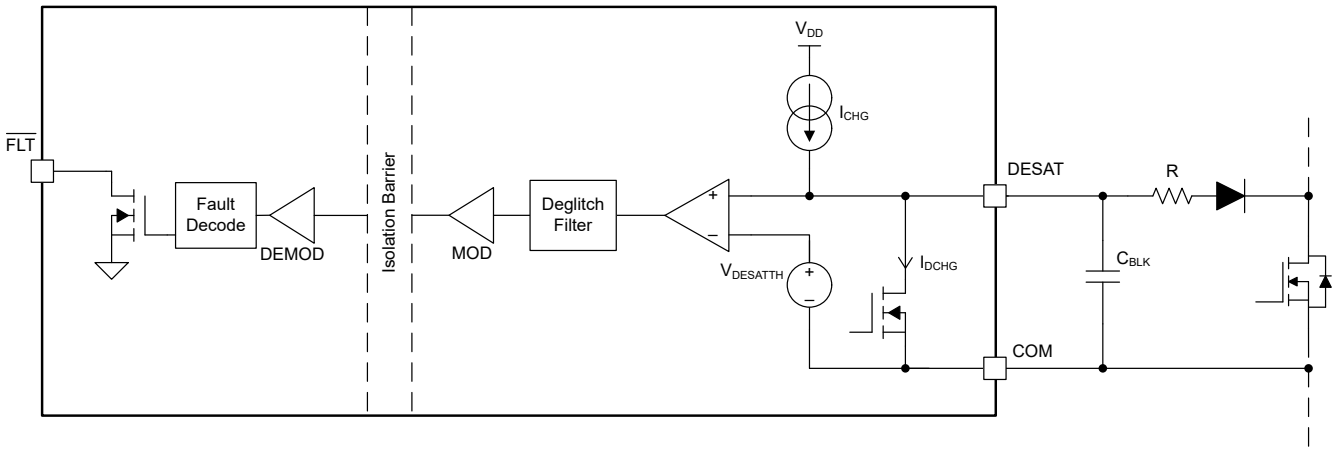

Figure 6-8. DESAT Protection

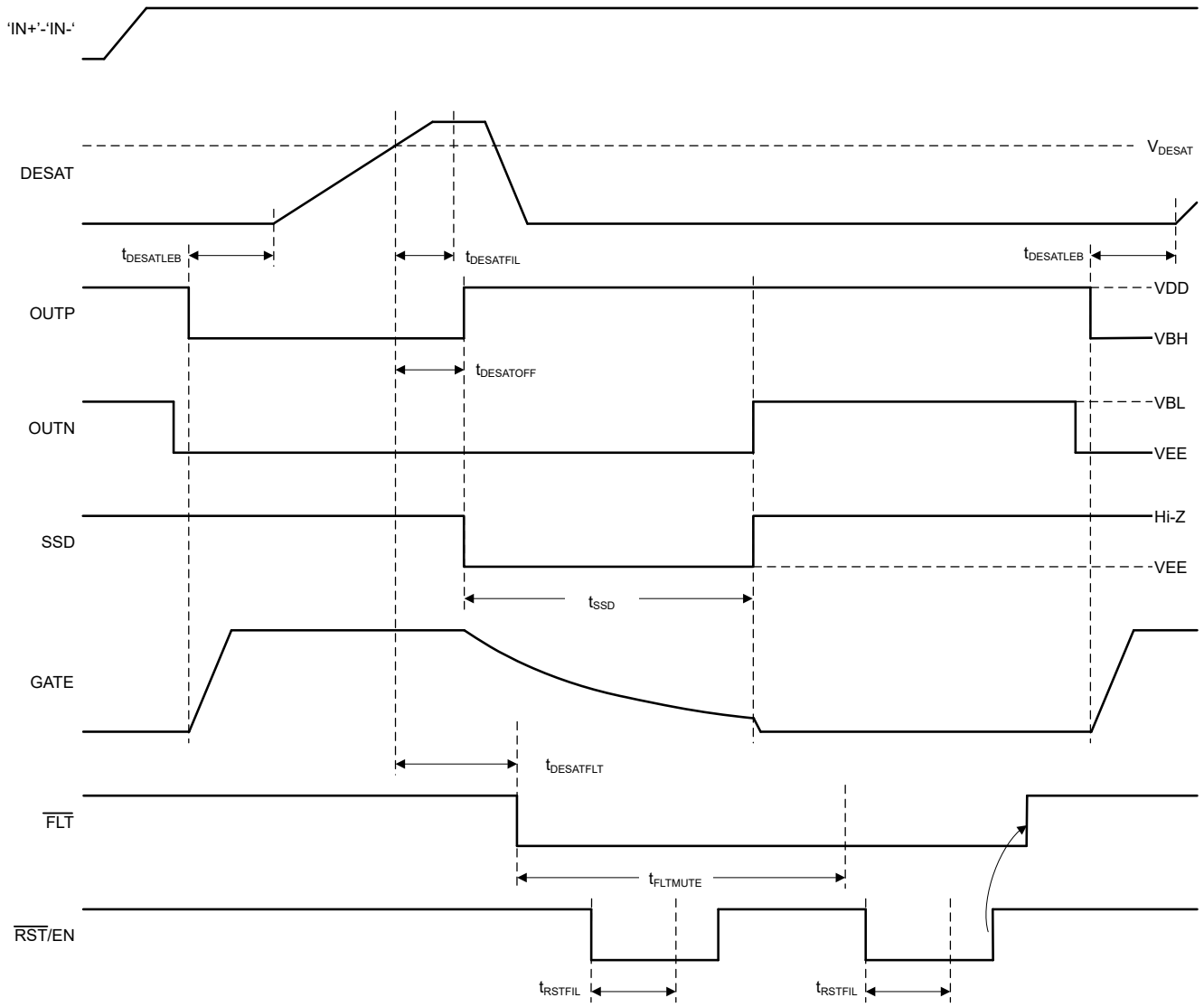

Figure 6-9. DESAT Protection Timing Diagram with Soft Shutdown

6.3.7 Soft Shutdown

When a DESAT fault is detected, the UCC218915-Q1 initiates a soft shutdown (SSD) to protect the power semiconductor device. When an overcurrent or short circuit event happens, the SSD feature slowly discharges the gate voltage to limit the overshoot voltage on the switching device created by high dI/dt due to the channel current. There is a tradeoff that needs to be made between the overshoot voltage and the short circuit energy. The turn-off speed must be slow enough to limit the overshoot voltage, but the shutdown time must not be too long that the large energy dissipation in the device can cause breakdown. The UCC218915-Q1 provides an internal pulldown FET that can be used with an external resistor to optimize the discharge current of the gate. When a DESAT fault is detected, OUTP is driven high and OUTN is driven low so that both the PMOS and NMOS buffer FETs are held off. The internal pulldown MOSFET on the SSD/GATE pin is turned on for a fixed time, t_{SSD}. After this time, OUTN is driven high to turn on the NMOS and hold the power semiconductor device off. A simplified block diagram is shown in Figure 6-10 and timing diagrams are shown in Figure 6-9.

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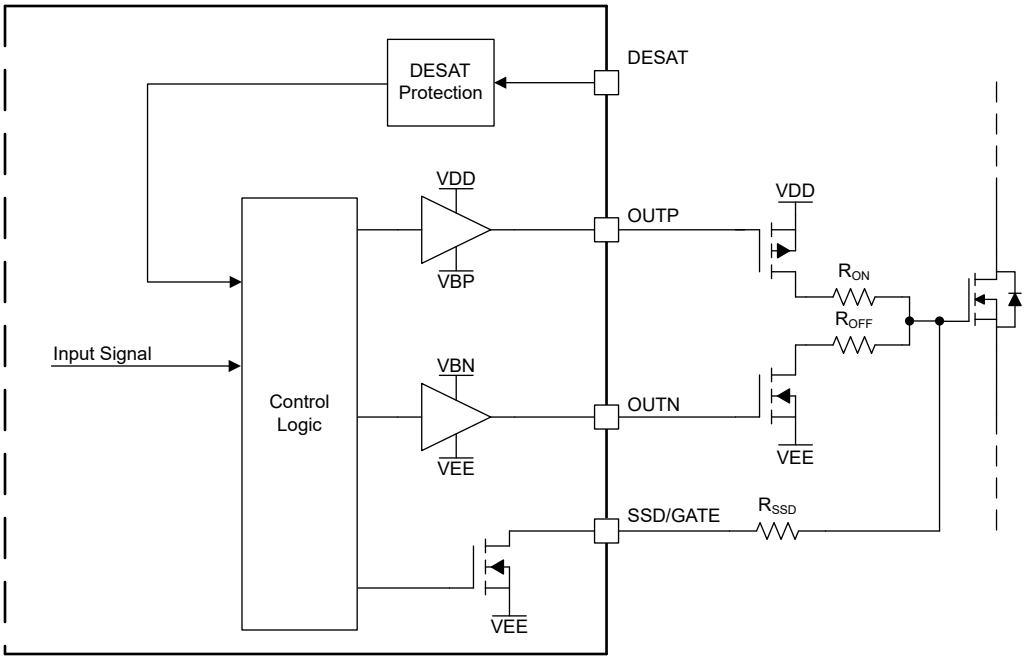

Figure 6-10. Soft Shutdown

6.3.8 Fault ($\overline{FLT}$), Reset and Enable ($\overline{RST}$/EN)

The $\overline{FLT}$ pin is open drain and can report a fault signal to the DSP/MCU when a fault is detected through the DESAT pin. The $\overline{FLT}$ pin is pulled down to GND after a fault is detected, and is held low until a reset signal is received from $\overline{RST}$/EN. The device has a fault mute time $t_{FLTMUTE}$, within which the device ignores any reset signal.

The $\overline{RST}$/EN pin is pulled down internally and is thus disabled by default when this pin is floating. It must be pulled up externally to enable the driver. The pin has two purposes:

- To enable and shut down the device. If the $\overline{RST}$/EN pin is pulled low for longer than t_{INFIL}, the driver is disabled and OUTN is driven high to activate the pull down NMOS to turn off the gate of the IGBT or SiC MOSFET.
- To reset the DESAT fault signaled on the $\overline{FLT}$ pin. If the $\overline{RST}$/EN pin is pulled low for more than t_{RSTFIL} after the mute time $t_{FLTMUTE}$, then the fault signal is reset and $\overline{FLT}$ returns to a high impedance state upon the next rising edge applied to the $\overline{RST}$/EN pin. A timing diagram is shown in Figure 6-9.

6.3.9 Active Short Circuit (ASC) Support and Feedback (ASC_FB)

When VCC loses power, or the MCU is malfunctioning, the motor can lose control and reversely charge the battery. Overvoltage of the battery can cause battery break down and can even be a fire hazard. For this scenario, the active short circuit (ASC) function can be used to protect the system by forcing the output on, turning on the power switch, and creating an active short circuit loop between the motor phases to bypass the battery.

When the ASC pin receives a logic high signal, the output is forced on regardless of the input side pin conditions. The ASC function has higher priority than the input signals and VCC UVLO. VDD UVLO, desaturation fault, and overtemperature protection have higher priority than ASC. The ASC_FB pin will output a logic high signal to indicate the ASC function is active when the ASC pin input voltage is high, the output is turned on due to the ASC input, and VCC is not in UVLO. Timing diagrams of ASC support with VCC UVLO, VDD UVLO and DESAT are shown in Figure 6-11, Figure 6-12 and Figure 6-13.

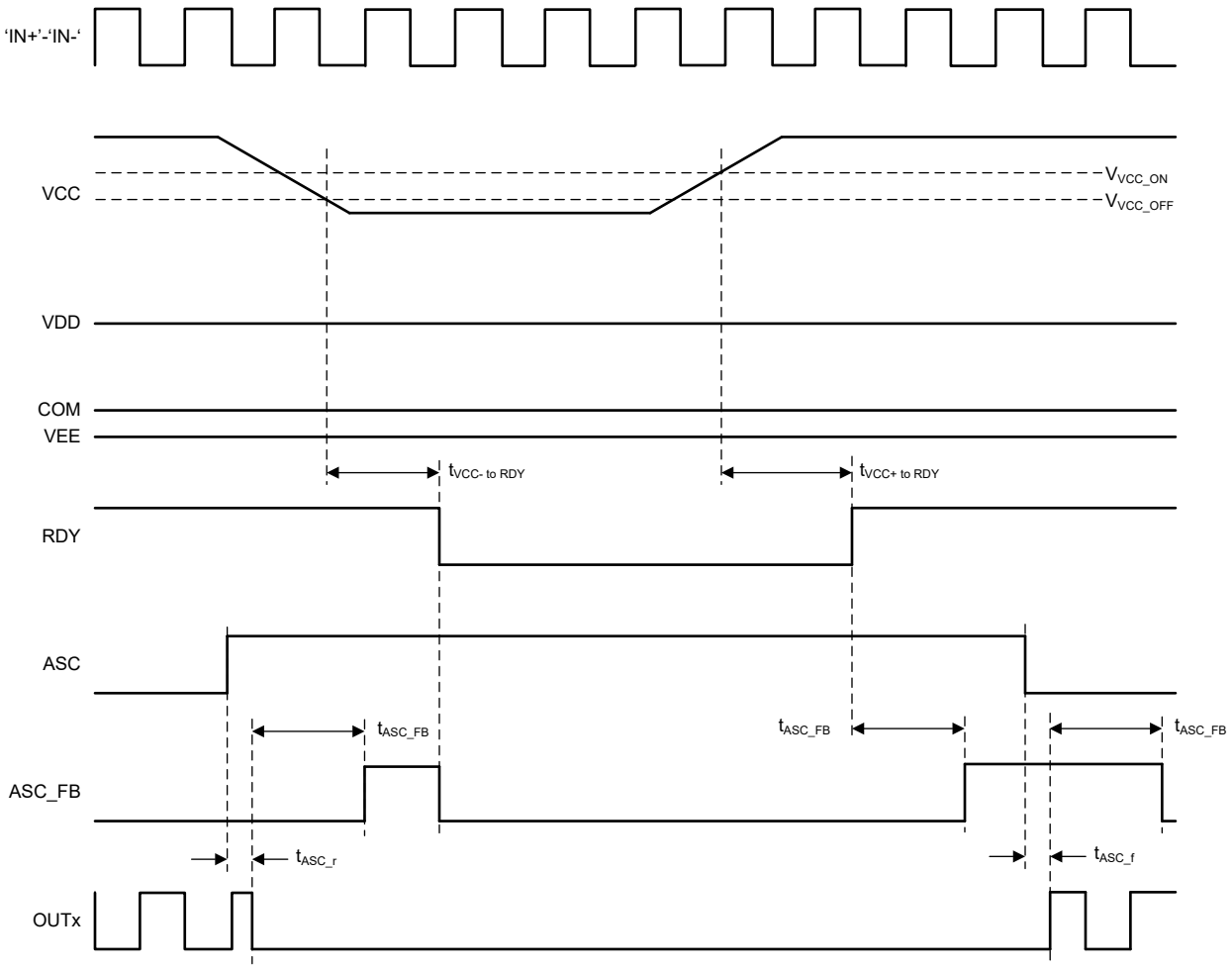

Figure 6-11. ASC Support with VCC UVLO

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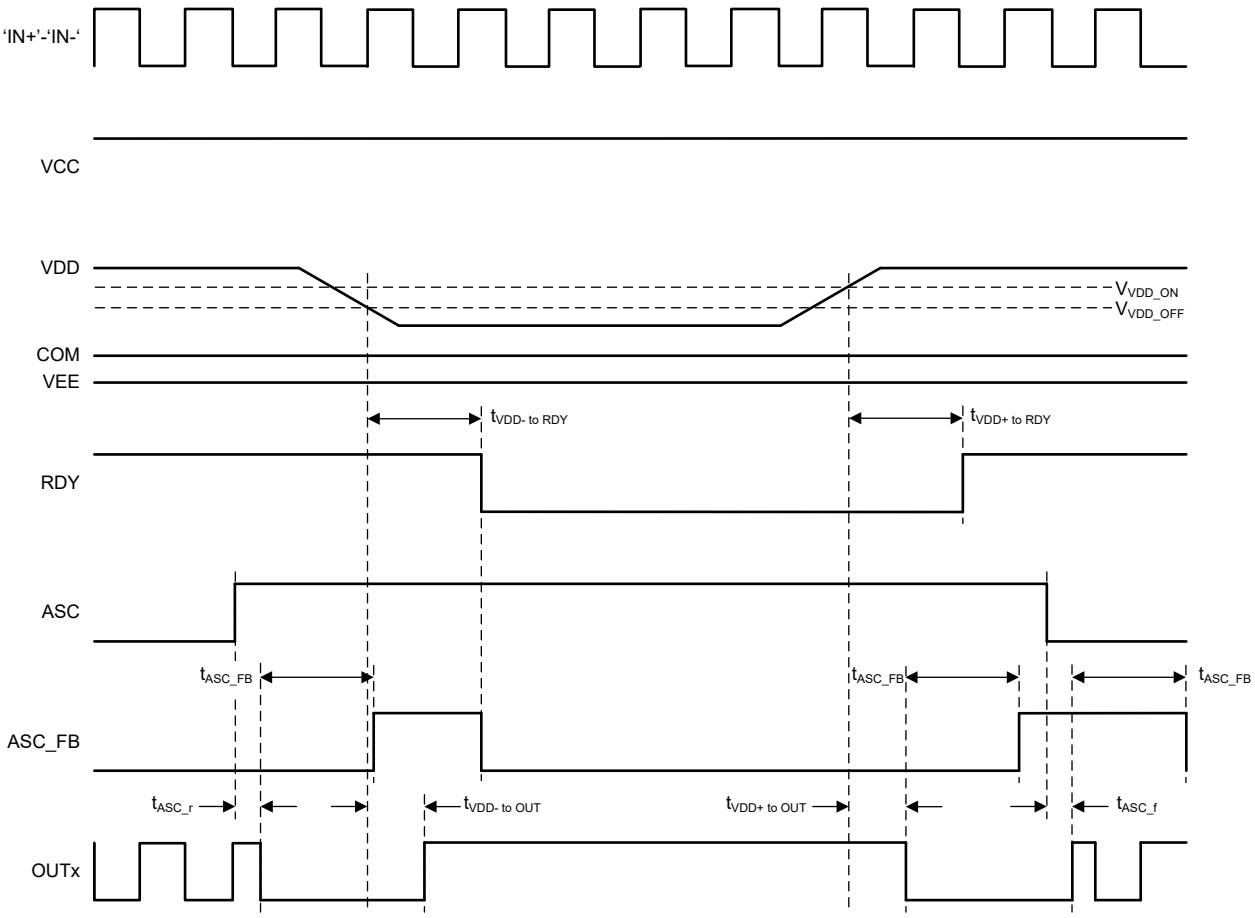

Figure 6-12. ASC Support with VDD UVLO

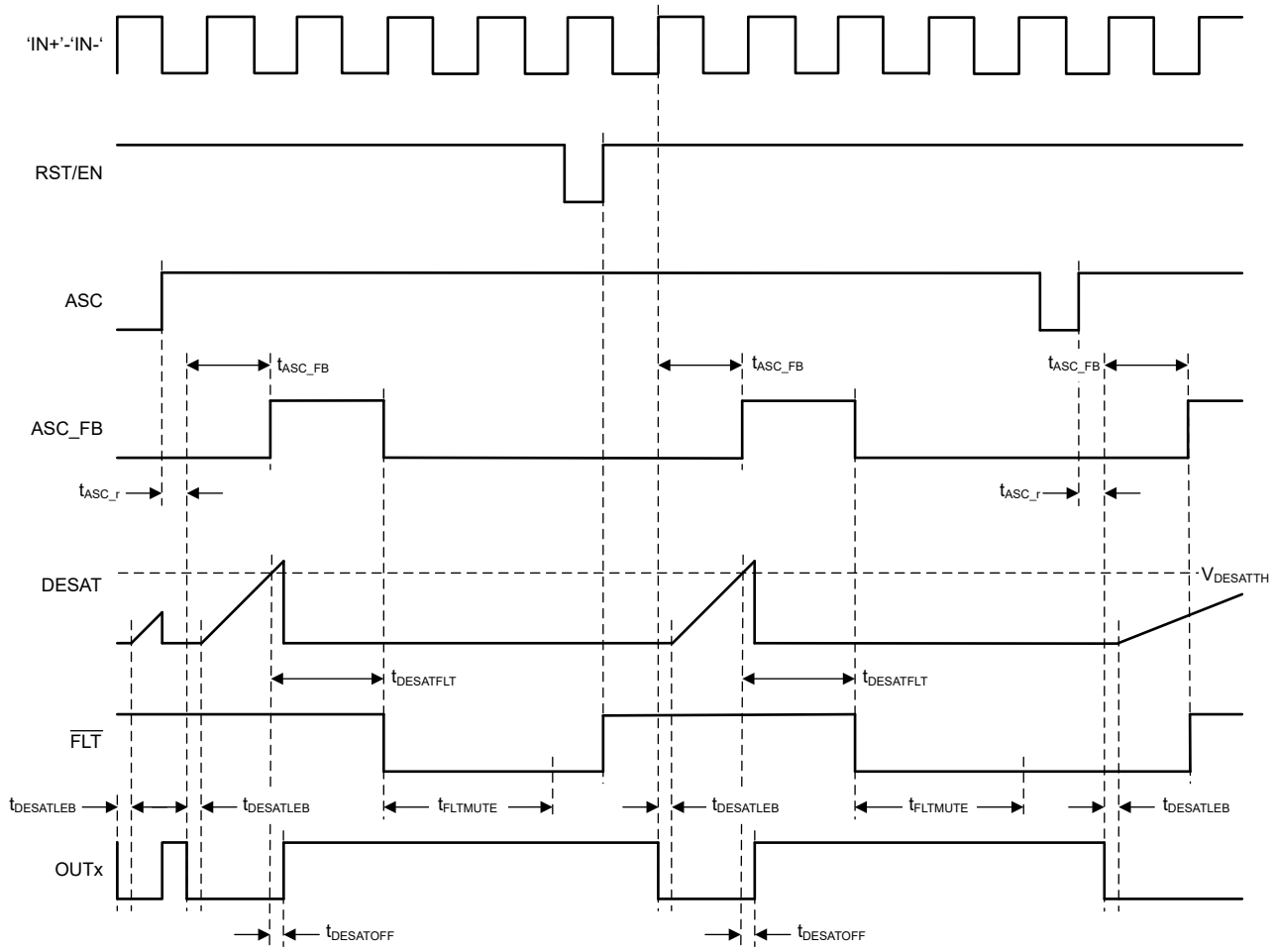

Figure 6-13. ASC Support with DESAT Fault

6.3.10 Overtemperature Protection

The silicon junction temperature is monitored to prevent the driver IC from damage during overheating conditions. When the device temperature exceeds it's 150°C maximum rating, the NMOS buffer FET driver output, OUTN, is held on so that the main power switch will be held off. The driver output will not turn on the PMOS buffer FET until the temperature recovers to 20°C below the thermal shutdown temperature, T_{TSDTH}. While the driver is in thermal shutdown, the RDY pin on the input side is held low and connected to GND.

6.4 Device Functional Modes

Table 6-2 lists the device function.

Table 6-2. Function Table

INPUT						OUTPUT			
VCC	VDD	IN+	IN-	$\overline{RST}$/EN	ASC	RDY	$\overline{FLT}$	OUTP/OUTN	CLMPE
X	PU	X	X	X	HI	X	Hi-Z	LO	LO
PD	PU	X	X	X	LO	LO	Hi-Z	HI	HI
PU	PD	X	X	X	X	LO	Hi-Z	LO	LO
PU	PU	X	X	LO	LO	HI	Hi-Z	HI	HI
PU	PU	LO	X	HI	LO	HI	Hi-Z	HI	HI
PU	PU	X	HI	HI	LO	HI	Hi-Z	HI	HI
PU	PU	HI	LO	HI	LO	HI	Hi-Z	LO	LO

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PU = Power Up (Supply greater than UVLO rising threshold); PD = Power Down (Supply less than UVLO falling threshold); X: Irrelevant; HI = Output High; LO = Output Low; Hi-Z = High Impedance

7 Applications and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Application Information

The device is very versatile because of the strong drive pre-driver output strength, wide range of output power supply, high isolation ratings, high CMTI and superior protection and sensing features. The 1.06kV$_{RMS}$ working voltage and 10kV$_{PK}$ surge immunity can support up both SiC MOSFET and IGBT modules with DC bus voltage up to 1500V. The device can be used in both low power and high power applications such as the traction inverter in HEV/EV, on-board charger and charging pile, motor driver, solar inverter, industrial power supplies and etc. The input side can support power supply and microcontroller signal from 3.3V to 5V, and the device level shifts the signal to output side through reinforced isolation barrier. The device has wide output power supply range up to 30V and support wide range of negative power supply. The UVLO benefits the power semiconductor with lower conduction loss and improves the system efficiency. As a reinforced isolated single channel driver, the device can be used to drive either a low-side or high-side driver.

The device features extensive protection and monitoring features, which can monitor, report and protect the system from various fault conditions.

- Fast detection and protection for the overcurrent and short circuit fault. The semiconductor is shutdown when the fault is detected and $\overline{\text{FLT}}$ pin is pulled down to indicate the fault detection. The device is latched unless reset signal is received from the $\overline{\text{RST}}$/EN pin.
- Soft shutdown feature (for certain OPNs) to protect the power semiconductor from catastrophic breakdown during overcurrent and short circuit fault. The shutdown energy can be controlled while the overshoot of the power semiconductor is limited.
- UVLO detection to protect the semiconductor from excessive conduction loss. Once the device is detected to be in UVLO mode, the output is pulled down and RDY pin indicates the power supply is lost. The device is back to normal operation mode once the power supply is out of the UVLO status. The power good status can be monitored from the RDY pin.
- The active Miller clamp feature protects the power semiconductor from false turn on.
- Enable and disable function through the $\overline{\text{RST}}$/EN pin
- Overtemperature protection
- Active short circuit functionality

7.2 Typical Application

Figure 7-1 shows the typical application of a half bridge using two UCC218915-Q1 isolated gate drivers. The half bridge is a basic element in various power electronics applications such as traction inverter in HEV/EV to convert the DC current of the electric vehicle's battery to the AC current to drive the electric motor in the propulsion system. The topology can also be used in motor drive applications to control the operating speed and torque of the AC motors.

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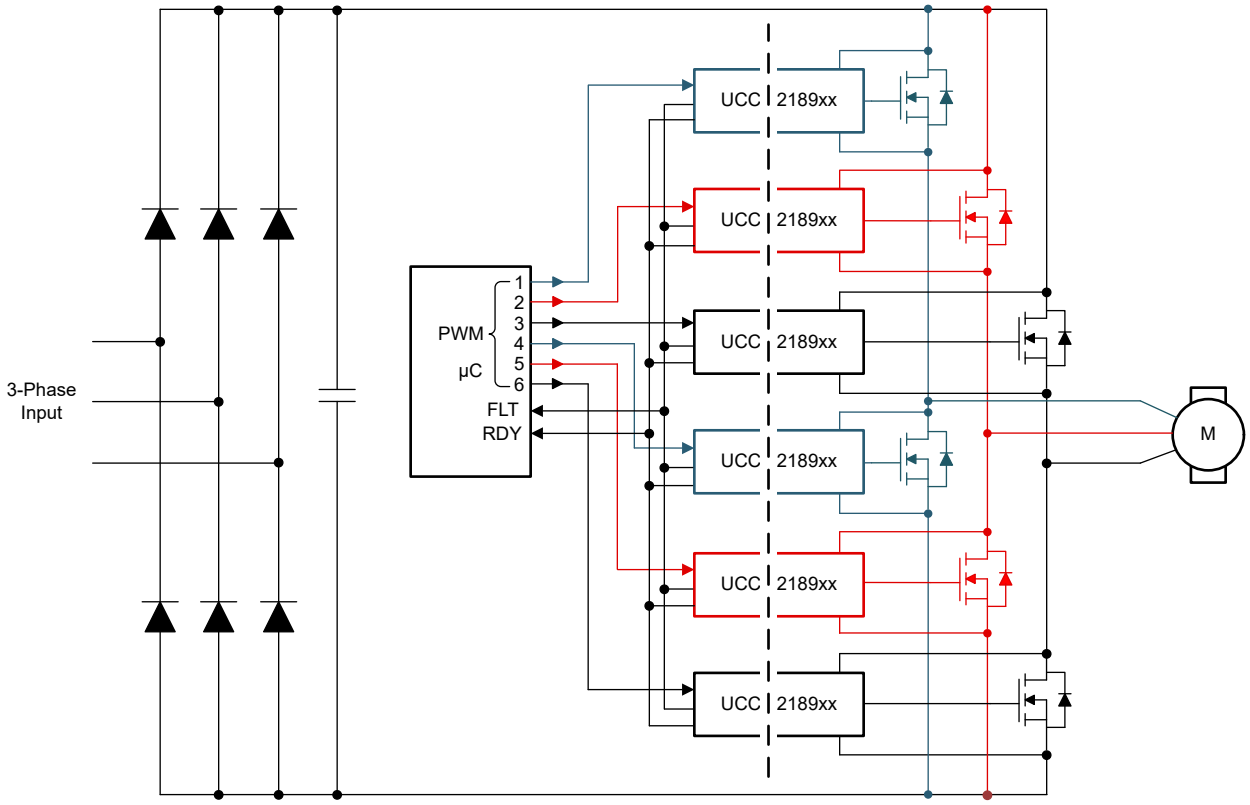

Figure 7-1. Typical Application Schematic

7.2.1 Design Requirements

The design of the power system for end equipment should consider some design requirements to ensure the reliable operation of the device through the load range. The design considerations include the peak source and sink current, power dissipation, overcurrent and short circuit protection, AIN-APWM function for analog signal sensing, etc.

A design example for a half bridge based on IGBT is given in this subsection. The design parameters are shown in Table 7-1.

Table 7-1. Design Parameters

PARAMETER	VALUE
Input Supply Voltage	5V
IN-OUT Configuration	Non-inverting
Positive Output Voltage VDD	15V
Negative Output Voltage VEE	-5V
DC Bus Voltage	800V
Peak Drain Current	300A
Switching Frequency	50kHz
Switch Type	IGBT Module

7.2.2 Detailed Design Procedure

7.2.2.1 Input Filters for IN+, IN- and $\overline{\text{RST}}$/EN

The input pins to the UCC218915-Q1 are both 3.3V and 5V logic compatible. The IN+ and $\overline{\text{RST}}$/EN pins have internal pull-down resistors, and the IN- pin has an internal pull-up resistor. If any of these pins are left floating the driver will be disabled. The driver has both inverting and non-inverting PWM input pins. If only the

non-inverting IN+ input is used, tie IN- to GND. If only the inverting IN- input is used, tie IN+ to VCC. Both IN+ and IN- can be used for PWM interlocking with the other driver in a half-bridge configuration to prevent phase leg shoot-through.

The device features 25ns typical internal deglitch filters on the IN+, IN-, and $\overline{\text{RST}}$/EN pins in order to protect against unintentional switching due to noise transients or narrow PWM pulses. Any signal less than 25ns will be filtered out and not passed through. For noisy systems, external low pass filters can be added externally to the input pins to further increase noise immunity. When choosing low pass filter components, both noise immunity and delay time should be considered according to system requirements. Figure 7-2 shows the impact of the deglitch filters with narrow pulses on IN+, IN-, and $\overline{\text{RST}}$/EN.

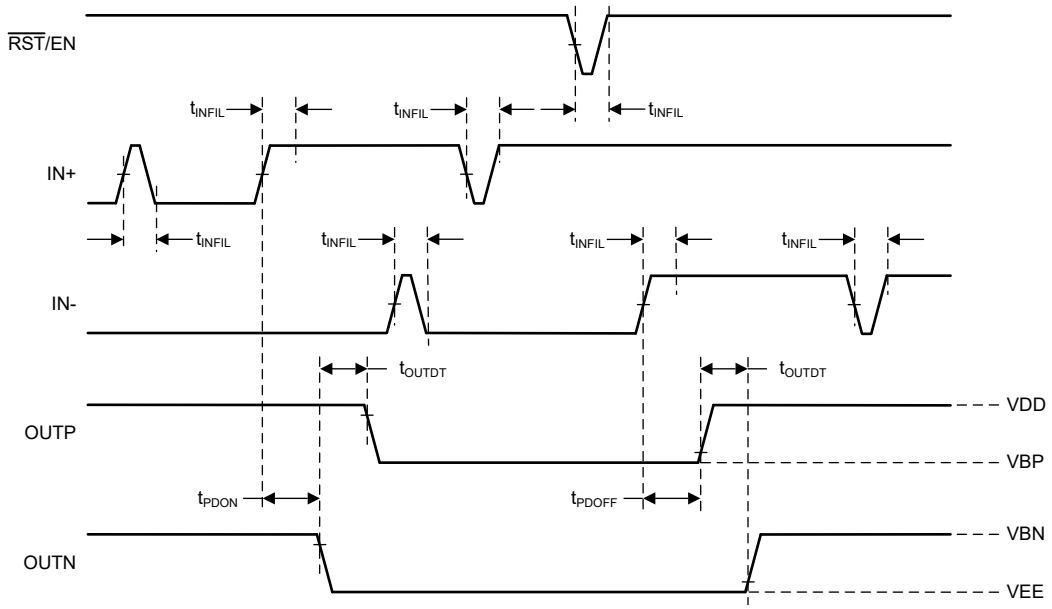

Figure 7-2. Impact of Deglitch Filters

7.2.2.2 PWM Interlock of IN+ and IN-

The device features the PWM interlock for IN+ and IN- pins, which can be used to prevent the phase leg shoot through issue. As shown in Table 6-2, the output is logic low while both IN+ and IN- are logic high. When only IN+ is used, IN- can be tied to GND. To utilize the PWM interlock function, the PWM signal of the other switch in the phase leg can be sent to the IN- pin. As shown in Figure 7-3, the PWM_T is the PWM signal to top side switch, the PWM_B is the PWM signal to bottom side switch. For the top side gate driver, the PWM_T signal is given to the IN+ pin, while the PWM_B signal is given to the IN- pin; for the bottom side gate driver, the PWM_B signal is given to the IN+ pin, while PWM_T signal is given to the IN- pin. When both PWM_T and PWM_B signals are high, the outputs of both gate drivers are logic low to prevent the shoot through condition.

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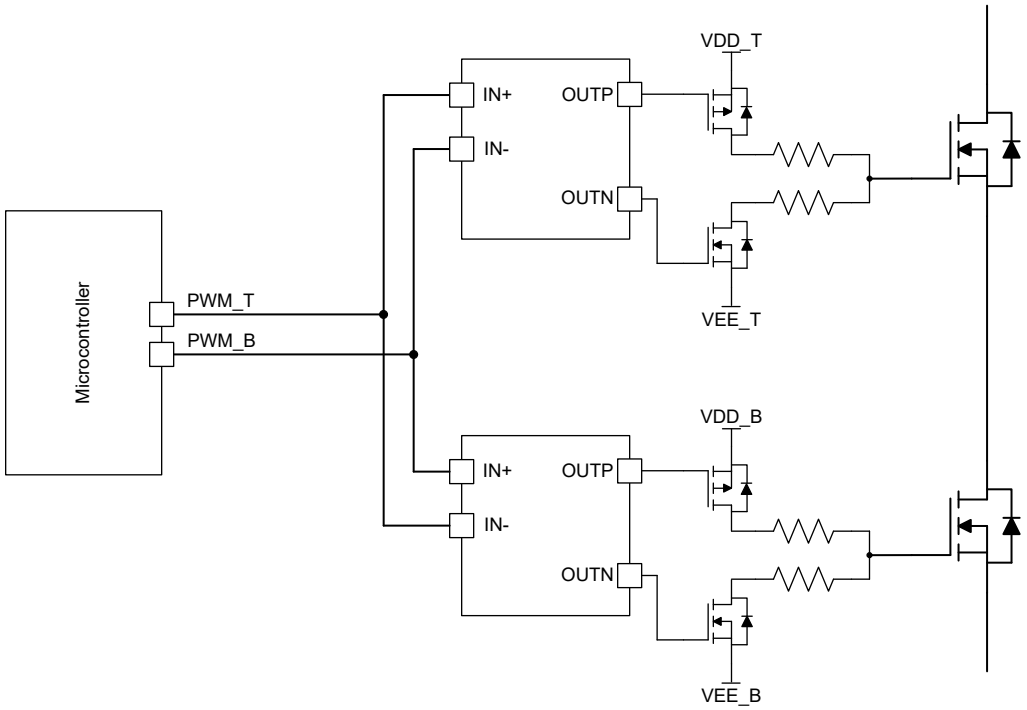

Figure 7-3. PWM Interlock for a Half Bridge

7.2.2.3 $\overline{\text{FLT}}$, RDY, and $\overline{\text{RST}}$/EN Pin Circuitry

Both $\overline{\text{FLT}}$ and RDY pin are open-drain output. The $\overline{\text{RST}}$/EN pin has 100kΩ internal pulldown resistor, so the driver is in OFF status if the $\overline{\text{RST}}$/EN pin is not pulled up externally. A 5kΩ resistor can be used as pullup resistor for the $\overline{\text{FLT}}$ and RDY pins.

To improve the noise immunity due to the parasitic coupling and common mode noise, low pass filters can be added between the $\overline{\text{FLT}}$, RDY, and $\overline{\text{RST}}$/EN pins and the microcontroller. A filter capacitor between 100pF to 300pF can be added.

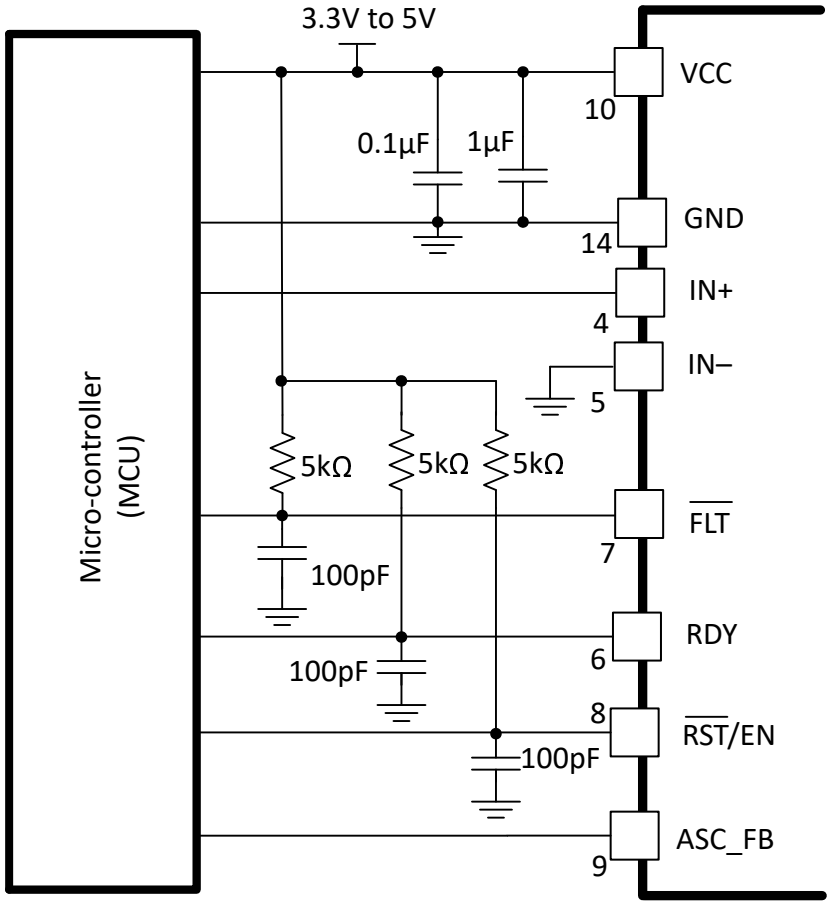

Figure 7-4. FLT, RDY and RST/EN Pins Circuitry

7.2.2.4 RST/EN Pin Control

RST/EN pin has two functions. It is used to enable or shutdown the outputs of the driver and to reset the fault signaled on the FLT pin after DESAT is detected. RST/EN pin needs to be pulled up to enable the device; when the pin is pulled down, the device is in disabled status. By default the driver is disabled with the internal 100kΩ pulldown resistor at this pin.

When the driver is latched after DESAT is detected, the FLT pin and output are latched low and need to be reset by the RST/EN pin. The microcontroller must send a signal to RST/EN pin after the fault to reset the driver. The driver will not respond until after the mute time $t_{FLTMUTE}$. The reset signal must be held low for at least t_{RSTFIL} after the mute time.

This pin can also be used to automatically reset the driver. The continuous input signal IN+ or IN- can be applied to RST/EN pin. There is no separate reset signal from the microcontroller when configuring the driver this way. If the PWM is applied to the non-inverting input IN+, then IN+ can also be tied to RST/EN pin. If the PWM is applied to the inverting input IN-, then a NOT logic is needed between the PWM signal from the microcontroller and the RST/EN pin. Using either configuration results in the driver being reset in every switching cycle without an extra control signal from microcontroller tied to RST/EN pin. One must ensure the PWM off-time is greater than t_{RSTFIL} in order to reset the driver in cause of a DESAT fault.

ADVANCE INFORMATION

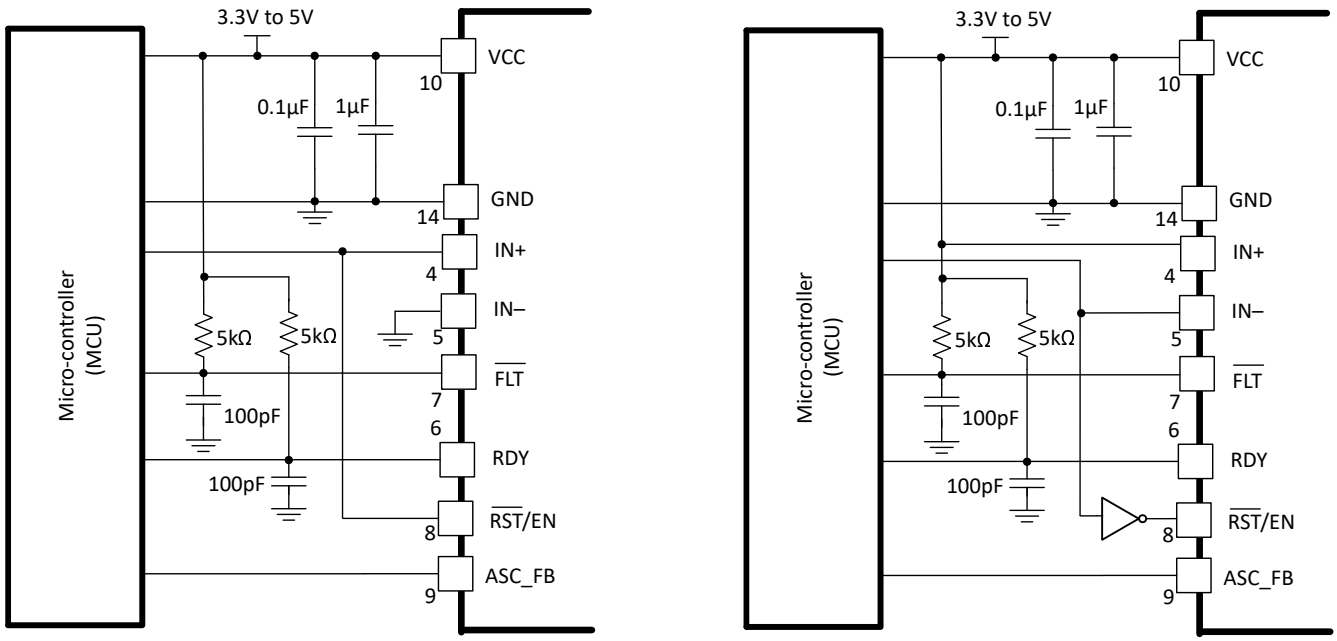

Figure 7-5. Automatic Reset Control

7.2.2.5 External Active Miller Clamp

External active Miller clamp feature allows the gate driver to stay at the low status when the gate voltage is detected below V_{CLMPTH}. When the other switch of the phase leg turns on, the dV/dt can cause a current through the parasitic Miller capacitance of the switch and sink in the gate driver. The sinking current causes a negative voltage drop on the turn off gate resistance, and bumps up the gate voltage to cause a false turn on. The external active Miller clamp features allows flexibility of board layout and active Miller clamp pulldown strength. Limited by the board layout, if the driver cannot be placed close enough to the switch, external active Miller clamp MOSFET can be placed close to the switch and the MOSFET can be chosen according to the peak current needed. Caution must be exercised when the driver is place far from the power semiconductor. Since the device has high peak sink and source current, the high dI/dt in the gate loop can cause a ground bounce on the board parasitics. The ground bounce can cause a positive voltage bump on CLMPE pin during the turn off transient, and results in the external active Miller clamp MOSFET to turn on shortly and add extra drive strength to the sink current. To reduce the ground bounce, a 2Ω resistance is recommended to the gate of the external active clamp MOSFET.

When the V_{OUTH} is detected to be lower than V_{CLMPTH} above VEE, the CLMPE pin outputs a 11V voltage with respect to VEE, the external clamp FET is in linear region and the pulldown current is determined by the peak drain current, unless the on-resistance of the external clamp FET is large.

$$I_{CLMPE\_PK} = \min(I_{D\_PK}, \frac{V_{DS}}{R_{DS\_ON}}) \quad (1)$$

Where

- I_{D_PK} is the peak drain current of the external clamp FET
- V_{DS} is the drain-to-source voltage of the clamp FET when the CLMPE is activated
- R_{DS_ON} is the on-resistance of the external clamp FET

The total delay time of the active Miller clamp circuit from the gate voltage detection threshold V_{CLMPTH} can be calculated as t_{DCLMPE}+t_{CLMPER}. t_{CLMPER} depends on the parameter of the external active Miller clamp MOSFET. As long as the total delay time is longer than the deadtime of high side and low side switches, the driver can effectively protect the switch from false turn on issue caused by Miller effect.

7.2.2.6 Overcurrent and Short Circuit Protection

A standard desaturation circuit can be applied to the DESAT pin. If the voltage of the DESAT pin is higher than the threshold V_{DESAT}, the soft turn-off is initiated. A fault will be reported to the input side to DSP/MCU. The output is held to LOW after the fault is detected, and can only be reset by the $\overline{RST}$/EN pin. The state-of-art overcurrent and short circuit detection time helps to ensure a short shutdown time for SiC MOSFET and IGBT.

If DESAT pin is not in use, it must be tied to COM to avoid overcurrent fault false triggering.

- Fast reverse recovery high voltage diode is recommended in the desaturation circuit. A resistor is recommended in series with the high voltage diode to limit the inrush current.
- A Schottky diode is recommended from COM to DESAT to prevent driver damage caused by negative voltage.
- A Zener diode is recommended from COM to DESAT to prevent driver damage caused by positive voltage.

7.3 Power Supply Recommendations

During the turn on and turn off switching transient, the peak source and sink current is provided by the VDD and VEE power supply through the buffer FETs. The large peak current is possible to drain the VDD and VEE voltage level and cause a voltage droop on the power supplies. To stabilize the power supply and ensure a reliable operation, a set of decoupling capacitors are recommended at the power supplies close to the gate driver VDD and VEE pins as well as close to the buffer FETs. A 10µF bypass cap is recommended between VDD and COM, VEE and COM as close to the buffer FETs as possible. A 1µF bypass cap is recommended between VDD and COM, VEE and COM, and VCC and GND close to the gate driver. A 0.1µF decoupling cap is also recommended for each power supply to filter out high frequency noise. The decoupling capacitors must be low ESR and ESL to avoid high frequency noise, and should be placed as close as possible to the VCC, VDD and VEE pins to prevent noise coupling from the system parasitics of PCB layout.

7.4 Layout

7.4.1 Layout Guidelines

Careful considerations must be taken in PCB design. Below are some key points:

- The decoupling capacitors of the input and output power supplies should be placed as close as possible to the gate driver power supply pins.
- Decoupling capacitors should also be placed as close as possible to the buffer FETs. The peak current generated at each switching transient can cause high dI/dt and voltage spike on the parasitic inductance of PCB traces.
- The buffer FETs should be placed as close as possible to the power semiconductor to reduce the parasitic inductance of the gate loop on the PCB traces.
- The driver COM pin should be connected to the Kelvin connection of SiC MOSFET source or IGBT emitter. If the power device does not have a split Kelvin source or emitter, the COM pin should be connected as close as possible to the source or emitter terminal of the power device package to separate the gate loop from the high power switching loop.
- Use a ground plane on the input side to shield the input signals. The input signals can be distorted by the high frequency noise generated by the output side switching transients. The ground plane provides a low-inductance filter for the return current flow.
- If the gate driver is used for the low side switch which the COM pin connected to the DC bus negative, use the ground plane on the output side to shield the output signals from the noise generated by the switch node; if the gate driver is used for the high side switch, which the COM pin is connected to the switch node, ground plane is not recommended.
- If ground plane is not used on the output side, separate the return path of the DESAT and ASC ground loop from the gate loop ground which has large peak source and sink current.
- No PCB trace or copper is allowed under the gate driver. A PCB cutout is recommended to avoid any noise coupling between the input and output side which can contaminate the isolation barrier.

7.4.2 Layout Example

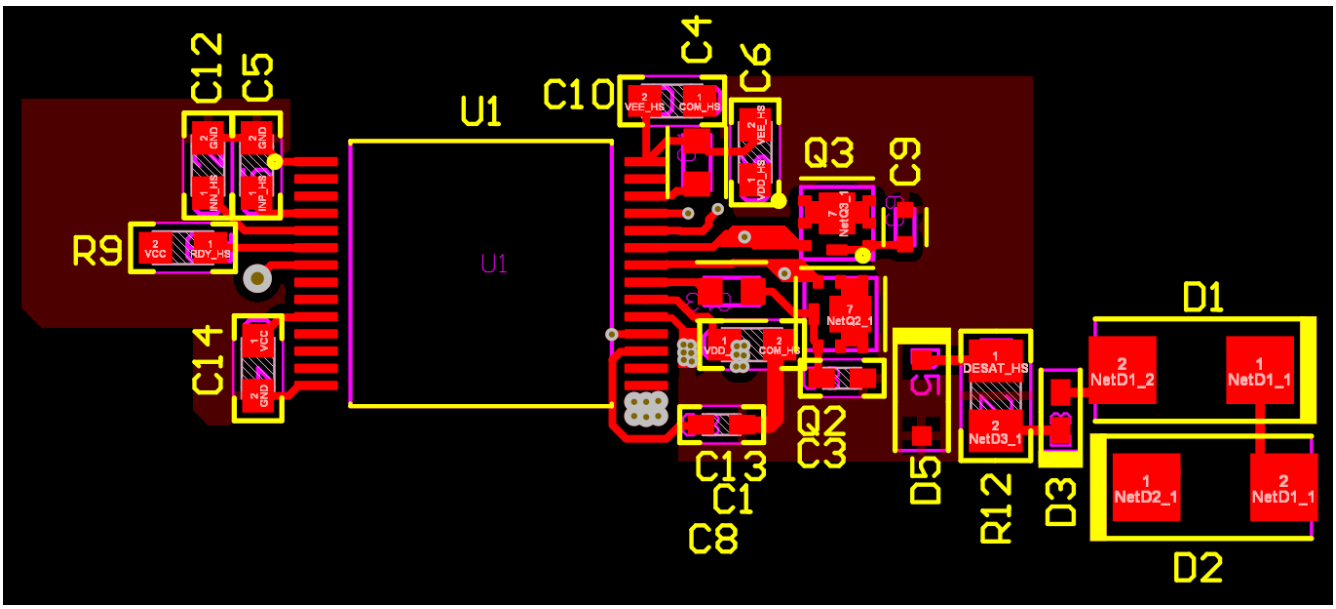

Figure 7-6. Layout Example - Top Layer

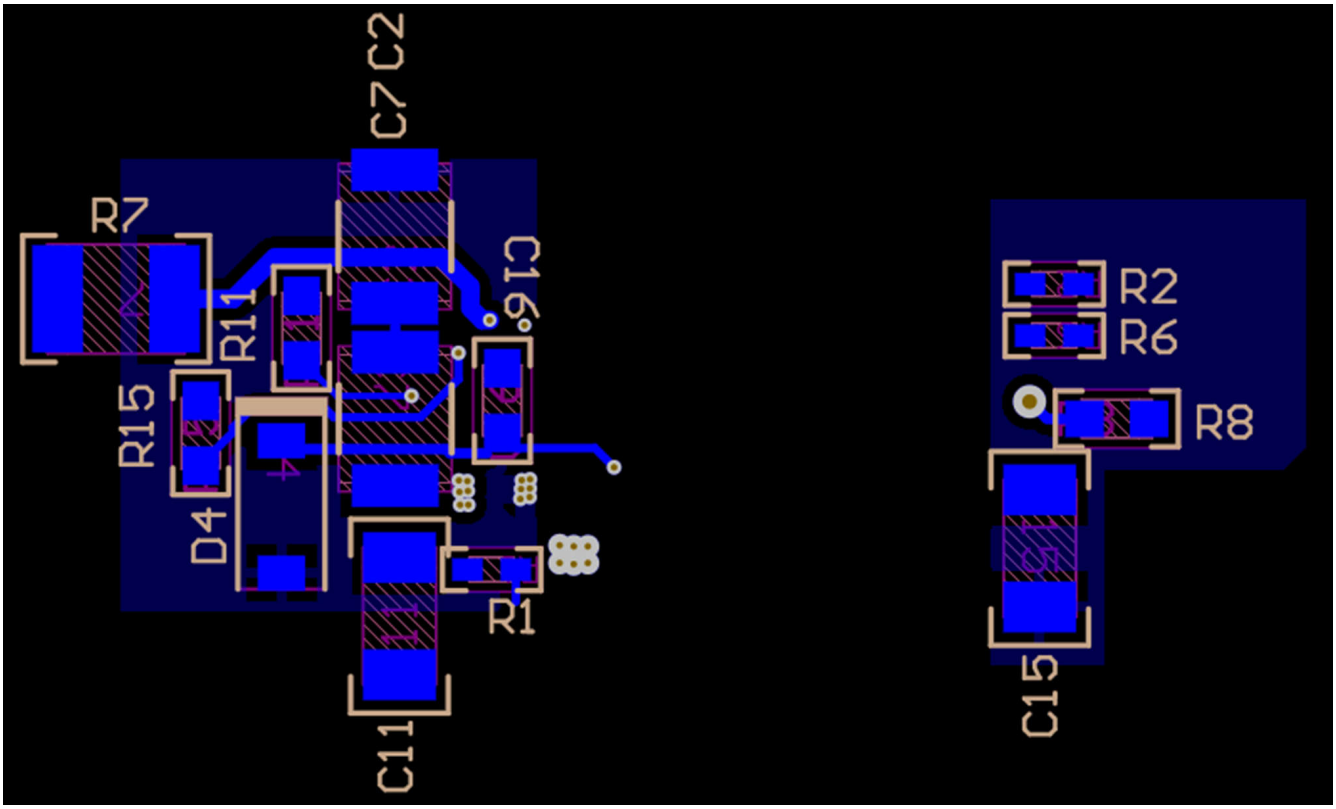

Figure 7-7. Layout Example - Bottom Layer

ADVANCE INFORMATION

8 Device and Documentation Support

8.1 Device Support

8.1.1 Third-Party Products Disclaimer

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8.2 Documentation Support

8.2.1 Related Documentation

For related documentation see the following:

- *Isolation Glossary*

8.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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8.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.7 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
September 2025	*	Initial Release

ADVANCE INFORMATION

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

10.1 Package Option Addendum

Packaging Information

Orderable Device	Status(1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan(2)	Lead/Ball Finish(6)	MSL Peak Temp(3)	Op Temp (°C)	Device Marking(4) (5)
PUCC218915AQDFPQ1	PREVIEW	TSSOP	DFP	28	53	RoHS & Green	NIPDAU	Level-3-260C -168 HR	–40 to 125	
UCC218915AQDFPRQ1	PRE_PROD	TSSOP	DFP	28	tbd	RoHS & Green	NIPDAU	Level-3-260C -168 HR	–40 to 125	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PRE_PROD Unannounced device, not in production, not available for mass market, nor on the web, samples not available.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material).

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

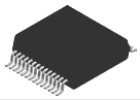
(5) Multiple Device markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

ADVANCE INFORMATION

10.2 Mechanical Data

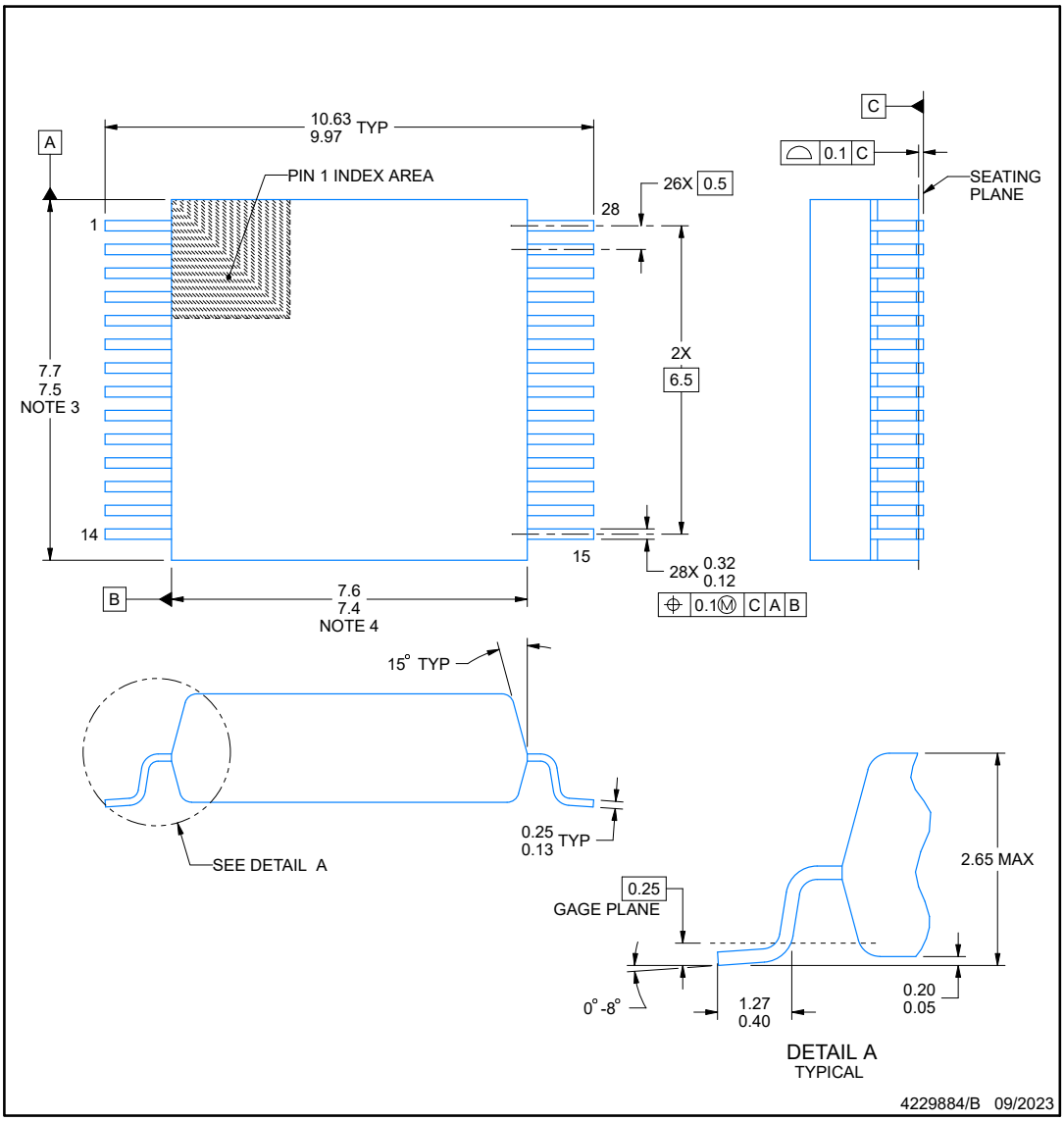
DFP0028A



PACKAGE OUTLINE

SSOP - 2.65 mm max height

SMALL OUTLINE PACKAGE



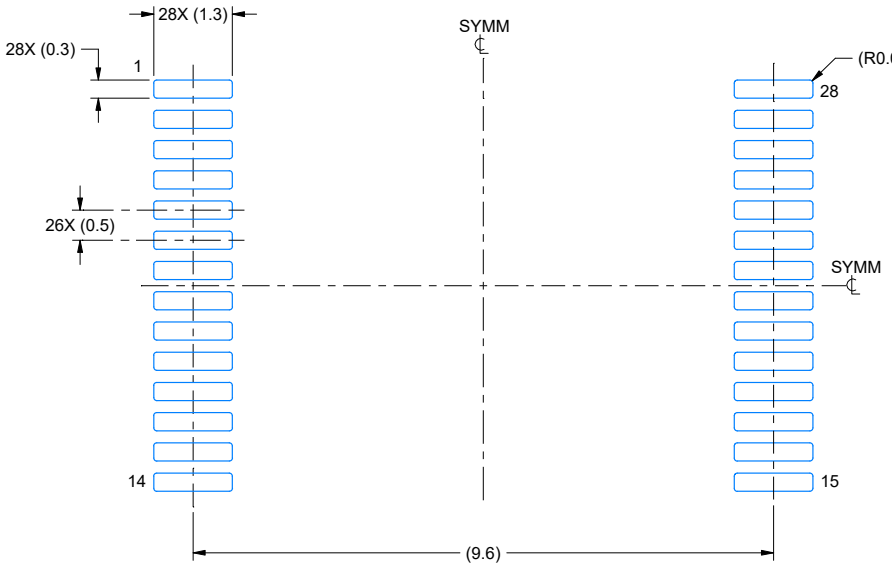
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.

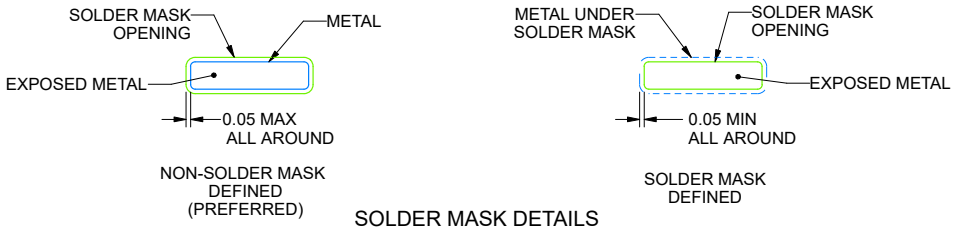
EXAMPLE BOARD LAYOUT

DFP0028A — **SSOP - 2.65 mm max height**

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

4229884/B 09/2023

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

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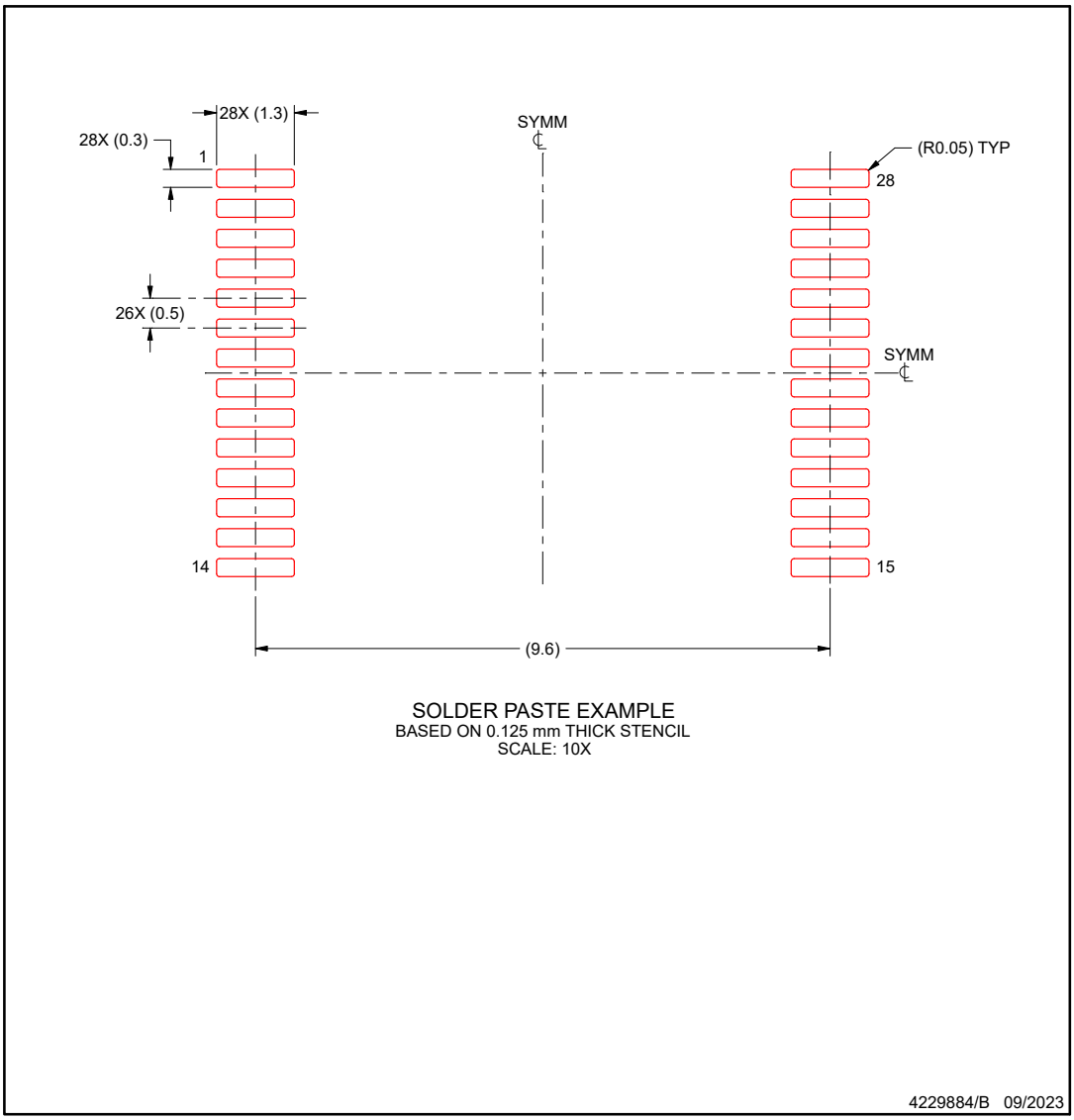
EXAMPLE STENCIL DESIGN

DFP0028A — **SSOP - 2.65 mm max height**

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4229884/B 09/2023

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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