UCC218200-Q1 15A Source/Sink Reinforced Isolated Single Channel Gate Driver for SiC/IGBT with Advanced Protection

1 Features

- 5kV$_{RMS}$ single channel isolated gate driver
- AEC-Q100 qualified for automotive applications
- SiC MOSFETs and IGBTs up to 1500V$_{pk}$
- 30V maximum output drive voltage (VDD-VEE)
- ±15A drive strength with split output
- 200-V/ns minimum CMTI
- 200ns response time fast DESAT protection with 9V threshold
- Dedicated Soft Shut Down (SSD) pin with 2.5A sinking capability. Shut down current is controllable by an external resistor.
- 4A internal active Miller clamp
- Overcurrent reporting on $\overline{FLT}$ and reset from $\overline{RST}$/EN
- Fast enable/disable response on $\overline{RST}$/EN
- 12V VDD UVLO and -3V VEE UVLO with power good on RDY
- Overtemperature protection with power good on RDY
- Output voltage gate monitor with real-time output state feedback on OUT_FB.
- Active short circuit (ASC) inputs on both primary and secondary sides to turn on power switch during system fault.
- Built-in self test diagnostics during power up for DESAT, UVLO, and output voltage gate monitor comparators.
- 20-Pin DFP wide body package with creepage and clearance distance > 8mm
- Operating junction temperature –40°C to 150°C

2 Applications

- Traction inverter for EVs
- On-board charger and chaging pile
- DC-DC converter for HEV/EVs

3 Description

The UCC218200-Q1 is a galvanically isolated single-channel gate driver designed for SiC MOSFETs and IGBTs up to 1500V DC operating voltage with advanced protection features, best-in-class dynamic performance, and robustness. The UCC218200-Q1 has up to ±15A peak source and sink current.

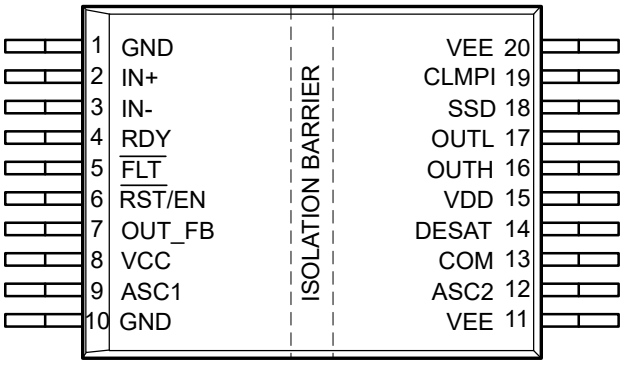
The input side is isolated from the output side with SiO_2 isolation technology, supporting up to 1.06kV$_{RMS}$ working voltage, 10kV$_{PK}$ surge immunity with longer than 40-years isolation barrier life, as well as providing low part-to-part skew, and >200V/ns common-mode noise immunity (CMTI).

The UCC218200-Q1 includes state-of-art protection features such as fast overcurrent and short circuit detection, controlled soft shutdown after a fault, fault reporting, active Miller clamp, input and output side power supply UVLO to optimize SiC and IGBT switching behavior and robustness, active short circuit inputs on both the primary and secondary sides, output voltage gate monitoring, and built-in self test during startup.

Package Information

PART NUMBER	PACKAGE(1)	BODY SIZE (NOM)
UCC218200B-Q1	DFP (SSOP 20)	5.6 mm × 7.5 mm

(1) For all available packages, see Section 6



Device Pin Configuration

ADVANCE INFORMATION

ADVANCE INFORMATION

4 Device and Documentation Support

4.1 Third-Party Products Disclaimer

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4.2 Documentation Support

4.2.1 Related Documentation

For related documentation see the following:

- *Isolation Glossary*

4.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

4.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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4.5 Trademarks

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4.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

4.7 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

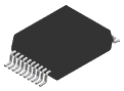
DATE	REVISION	NOTES
May 2025	*	Initial Release

6 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

6.1 Mechanical Data

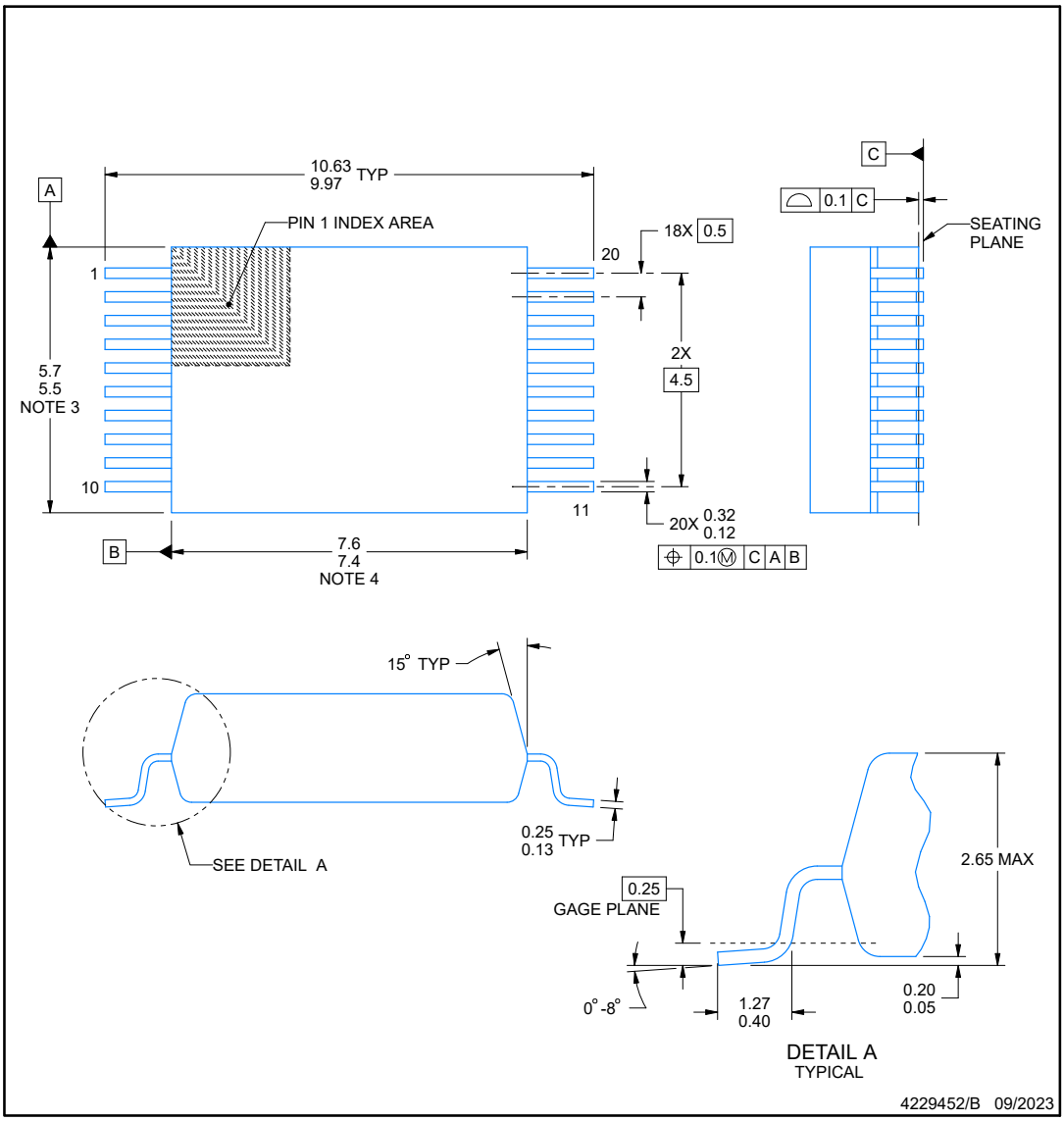
DFP0020A



PACKAGE OUTLINE

SSOP - 2.65 mm max height

SMALL OUTLINE PACKAGE



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.

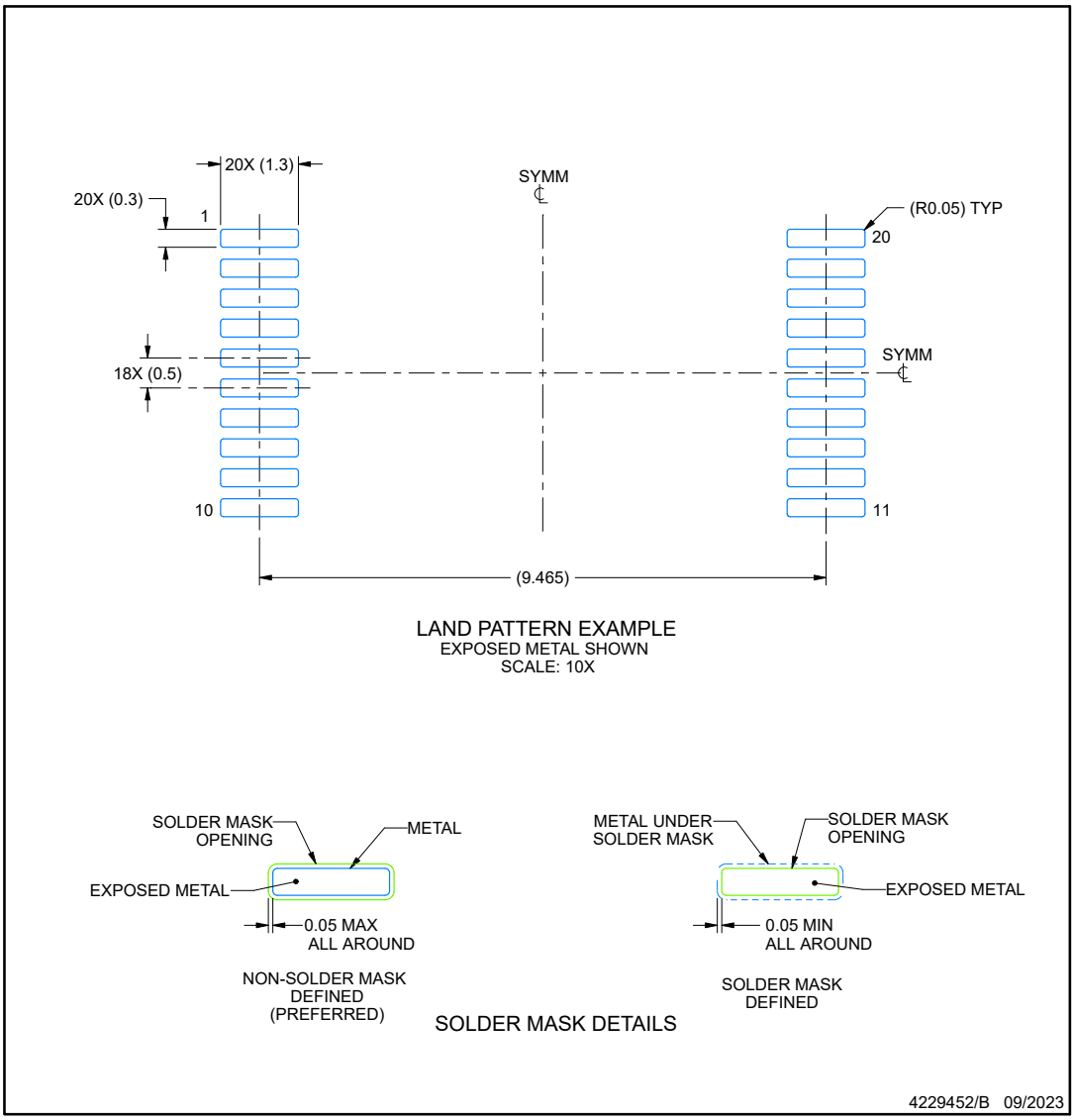
ADVANCE INFORMATION

ADVANCE INFORMATION

EXAMPLE BOARD LAYOUT

DFP0020A — **SSOP - 2.65 mm max height**

SMALL OUTLINE PACKAGE



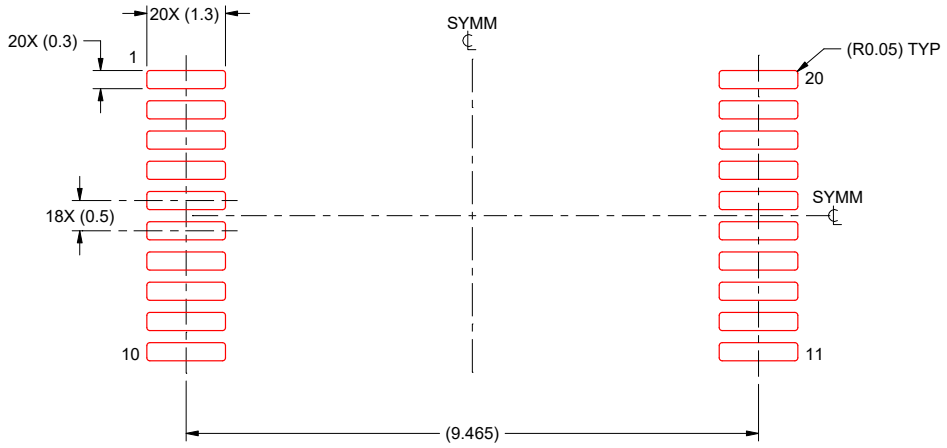
NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DFP0020A — **SSOP - 2.65 mm max height**

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4229452/B 09/2023

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
PUCC218200BQDFPRQ1	Active	Preproduction	SSOP (DFP) | 20	3000 | LARGE T&R	-	Call TI	Call TI	-40 to 150	

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265