UC284xL High-Performance Economy Current-Mode PWM Controller

1 Features

- Improved output driver and lower operating/startup current from UCx84x/UCx84xA/ UCx84xAQ/TLx84x/TLx84xB families
- Optimized for off-line and DC-DC converters
- Low start-up current (< 0.5mA)
- Trimmed oscillator discharge current
- Automatic feedforward compensation
- Pulse-by-pulse current limiting
- Enhanced load response characteristics
- Undervoltage lockout with hysteresis
- Double pulse suppression
- High-current totem pole output
- Internally-trimmed bandgap reference
- Up to 500kHz operation

2 Applications

- Switch mode power supplies (SMPS)
- DC-DC converters
- Power modules
- Industrial PSU
- Battery operated PSU

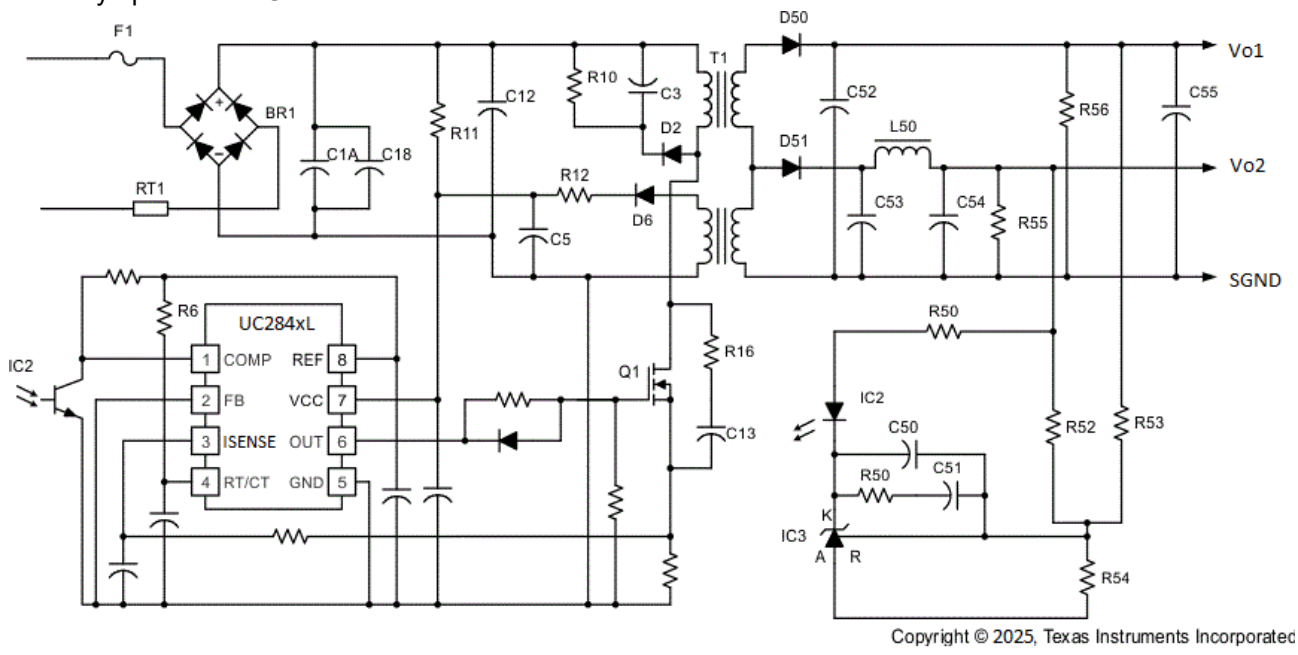
3 Description

The UC284xL control device is a pin-for-pin compatible improved version of the UC284x family. Providing the necessary features to control current-mode or switched-mode power supplies, this device provides improved features: higher V_{CC} range at 36V, lower start-up current at 0.25mA, tighter operating current tolerance at 15mA max, and faster response on cycle-by-cycle current protection at 100ns. Output driver of UC284xL is improved with shorter rise and fall time at 75ns max to reduce switching loss, and stronger driver capabilities with lower output low level farther from the FETs threshold voltage.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
UC284xL	D (SOIC, 8)	4.9mm × 6mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Typical Application Diagram

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4 Device Comparison

Table 4-1. Device Performance Improvements

PARAMETER	UC284x	UC284xL
V_{CC} max	30V	36V
CS-OUT delay	150ns	100ns
Rise/fall time max	150ns	75ns
OUT low level at 200mA	1.5V	0.5V
OUT high level at 200mA, V_{CC} = 15V	12V	13.1V
Startup current	0.3mA	0.25mA
Operating current max	17mA	15mA

5 Pin Configuration and Functions

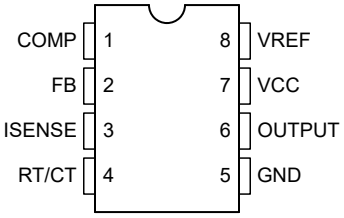


Figure 5-1. D Package, 8-Pin SOIC (Top View)

Table 5-1. Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
COMP	1	O	Outputs the low impedance 1MHz internal error amplifier that is also the input to the peak current limit or PWM comparator, with an open-loop gain (AVOL) of 80dB. This pin is capable of sinking a maximum of 6mA and is not internally current limited.
FB	2	I	Input to the error amplifier that can be used to control the power converter voltage-feedback loop for stability.
GND	5	—	This is the controller signal ground.
ISENSE	3	I	Input to the peak current limit, PWM comparator of the UC284xL controller. When used in conjunction with a current sense resistor, the error amplifier output voltage controls the power systems cycle-by-cycle peak current limit. The maximum peak current sense signal is internally clamped to 1V. See *Section 7.2*.
OUTPUT	6	O	Output of 1A totem pole gate driver. This pin can sink and source up to 1A of gate driver current. A gate driver resistor must be used to limit the gate driver current.
RT/CT	4	I	Input to the internal oscillator that is programmed with an external timing resistor (RT) and timing capacitor (CT). See *Section 7.3.5* for information on properly selecting these timing components. TI recommends using capacitance values from 470pF to 4.7nF. TI also recommends that the timing resistor values chosen be from 5kΩ to 100kΩ.
VCC	7	I	Bias input to the gate driver. This pin must have a biasing capacitor that is at least 10 times greater than the gate capacitance of the main switching FET used in the design.
VREF	8	O	Reference voltage output of the PWM controller. This pin must supply no more than 10mA under normal operation. This output is short-circuit protected at roughly 100mA. This reference is also used for internal comparators and needs a high frequency bypass capacitor of 1µF. The VCC capacitor also must be at least 10 times greater than the capacitor on the VREF pin.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
Supply voltage (2)	V_{CC} pin		V_{CC} Zener Voltage	V
Supply current, I_{CC}			25	mA
Output current, I_{OUT}			±1	A
Output energy (capacitive load)			5	µJ
Analog inputs		–0.3	6.3	V
Maximum negative voltage	All pins	–0.3		V
Error amplifier output sink current, I_{COMP}			10	mA
Power dissipation at $T_A \leq 25°C$			1	W
Lead temperature (soldering, 10s)			300	°C
Junction temperature, T_J		–55	150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Section 6.3*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) In normal operation V_{CC} is driven from a low impedance source through current limiting resistor. The resistor must be sized so that the V_{CC} voltage under all operating conditions is between Vcc Zener clamp voltage and undervoltage lockout threshold. Absolute maximum V_{CC} is defined based on internal Zener clamp voltage in Electrical Characteristics such that I_{CC} does not exceed 25mA. Failure to limit V_{CC} and I_{CC} to these limits may result in permanent damage of the device.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1500	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_{CC}	Bias supply voltage	UC2842L, UC2844L		18	30	V
		UC2843L, UC2845L		10	30	
V_{FB}, V_{RC}, V_{VFB}	Voltage on analog pins	FB, ISENSE, and RT/CT pins	–0.1		5	V
V_{OUT}	Gate driver output voltage		–0.1		V_{CC}	V
I_{VCC}	Supply bias current	VCC pin			25	mA
I_{VREF}	Output current	VREF pin			10	mA
f_{OSC}	Oscillator frequency				500	kHz
T_A	Operating free-air temperature		–40		125	°C

6.4 Thermal Information

THERMAL METRIC[1]		D (SOIC) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	117.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	51.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	61	°C/W
ψ_{JT}	Junction-to-top characterization parameter	7.8	°C/W
ψ_{JB}	Junction-to-board characterization parameter	60.2	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	—	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

Unless otherwise stated, these specifications apply for T_A = –40°C to 125°C, $T_A = T_J$; V_{CC} = 15V[4]; R_T = 10kΩ; C_T = 3.3nF.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
REFERENCE						
	Output voltage	T_J = 25°C, I_O = 1mA	4.95	5	5.05	V
	Line regulation	12V ≤ V_{IN} ≤ 25V		6	20	mV
	Load regulation	1mA ≤ I_O ≤ 20mA		6	25	mV
	Temperature stability	See (1) (6)		0.2	0.4	mV/°C
	Total output variation	Line, Load, Temperature	4.9		5.1	V
	Output noise voltage	10Hz ≤ f ≤ 10kHz; T_J = 25°C[1]		50		μV
	Long-term stability	T_A = 125°C, 1000hrs[1]		5	25	mV
	Output short circuit		–30	–100	–180	mA
OSCILLATOR						
	Initial accuracy	T_J = 25°C[5]	47	52	57	kHz
	Voltage stability	12V ≤ V_{CC} ≤ 25V		0.2	1	%
	Temperature stability	T_{MIN} ≤ T_A ≤ T_{MAX} [1]		5		%
	Amplitude	$V_{RT/CT}$ peak to peak[1]		1.7		V
	Discharge current	$V_{RT/CT}$ = 2V[7]		8.3		mA
ERROR AMPLIFIER						
	Input voltage	V_{COMP} = 2.5V	2.45	2.5	2.55	V
	Input bias current			–0.3	–1	μA
				–0.3	–2	
A_{VOL}	Open-loop gain	2V ≤ V_O ≤ 4V	65	90		dB
	Unity gain bandwidth	T_J = 25°C[1]	0.7	1		MHz
CMRR	Common mode rejection ratio	12V ≤ V_{CC} ≤ 25V	60	70		dB
	Output sink current	V_{FB} = 2.7V, V_{COMP} = 1.1V	2	6		mA
	Output source current	V_{FB} = 2.3V, V_{COMP} = 5V	–0.5	–0.8		mA
	V_{OUT} high	V_{FB} = 2.3V, R_L = 15kΩ to ground	5	6		V
	V_{OUT} low	V_{FB} = 2.7V, R_L = 15kΩ to VREF		0.7	1.1	V
CURRENT SENSE						
	Gain	See (2) (3)	2.85	3	3.15	V/V
	Maximum input signal	V_{COMP} = 5V[2]	0.9	1	1.1	V
PSRR	Power supply rejection ratio	12V ≤ V_{CC} ≤ 25V[2]		70		dB
	Input bias current			–2	–10	μA

6.5 Electrical Characteristics (continued)

Unless otherwise stated, these specifications apply for T_A = –40°C to 125°C, T_A = T_J; V_{CC} = 15V(4); R_T = 10kΩ; C_T = 3.3nF.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Delay to output	V_{ISENSE} = 0V to 2V(1)		100	200	ns
OUTPUT					
Output low level	I_{SINK} = 20mA		0.05	0.11	V
	I_{SINK} = 200mA		0.55	1.1	
Output high level	I_{SOURCE} = 20mA	13.2	13.6		V
	I_{SOURCE} = 200mA	13.1	13.5		
Rise time	T_J = 25°C, C_L = 1nF(1)		25	75	ns
Fall time	T_J = 25°C, C_L = 1nF(1)		25	75	ns
UVLO saturation	V_{CC} = 5V, I_{SINK} = 10mA		0.7	1.2	V
UNDERVOLTAGE LOCKOUT					
Start threshold	UC2842L, UC2844L	15	16	17	V
	UC2843L, UC2845L	7.8	8.4	9	
Minimum operation voltage after turnon	UC2842L, UC2844L	9	10	11	V
	UC2843L, UC2845L	7	7.6	8.2	
PWM					
Maximum duty cycle	UC2842L, UC2843L	92	96	100	%
	UC2844L, UC2845L	46	48	50	%
Minimum duty cycle				0	%
TOTAL STANDBY CURRENT					
Start-up current			0.25	0.5	mA
Operating supply current	V_{FB} = V_{ISENSE} = 0V		11	15	mA
V_{CC} Zener voltage	I_{CC} = 25mA	36			V

(1) Ensured by design, but not 100% production tested.
(2) Parameter measured at trip point of latch with V_{FB} = 0V.
(3) Gain defined as: A = ΔV_{COMP} / ΔV_{ISENSE}; 0V ≤ V_{ISENSE} ≤ 0.8V.
(4) Adjust V_{CC} above the start threshold before setting at 15V.
(5) Output frequency is one half oscillator frequency.
(6) Temperature stability, sometimes referred to as *average temperature coefficient*, is described by: Temperature stability = ($V_{REF(max)}$ – $V_{REF(min)}$) / ($T_{J(max)}$ – $T_{J(min)}$). $V_{REF(max)}$ and $V_{REF(min)}$ are the maximum and minimum reference voltage measured over the appropriate temperature range. Note that the extremes in voltage do not necessarily occur at the extremes in temperature.
(7) This parameter is measured with R_T = 10kΩ to V_{REF}. This contributes approximately 300µA of current to the measurement. The total current flowing into the RT/CT pin is approximately 300µA higher than the measured value.

6.6 Typical Characteristics

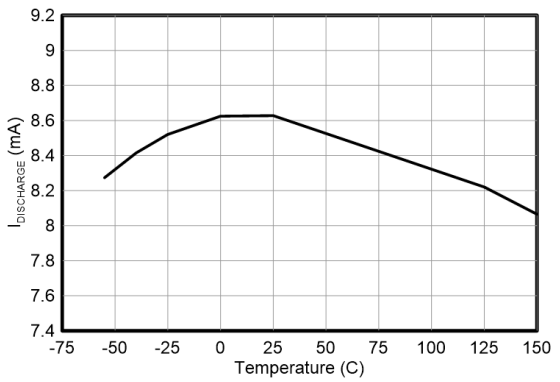


Figure 6-1. Oscillator Discharge Current vs Temperature for V_{CC} = 15 V and $V_{RT/CT}$ = 2V

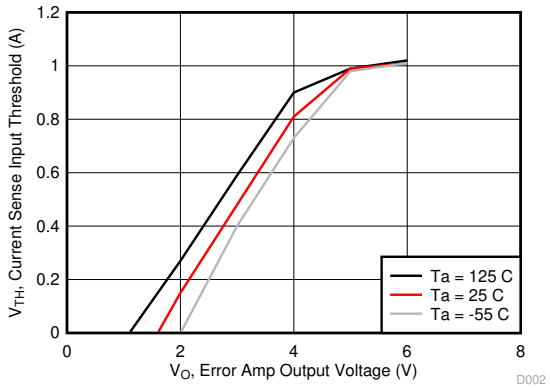


Figure 6-2. Current Sense Input Threshold vs Error Amplifier Output Voltage for V_{CC} = 15 V

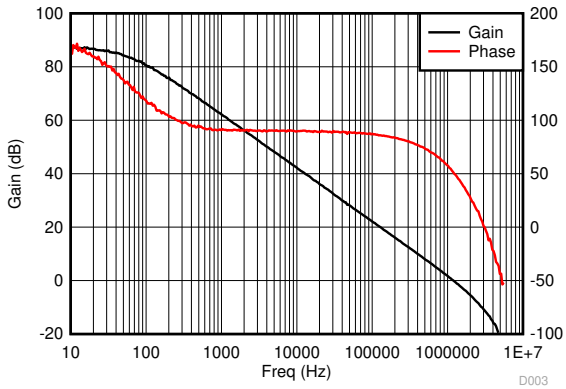


Figure 6-3. Error Amplifier Open-Loop Gain and Phase vs Frequency V_{CC} = 15 V, R_L = 100 kΩ, and T_A = 25 °C

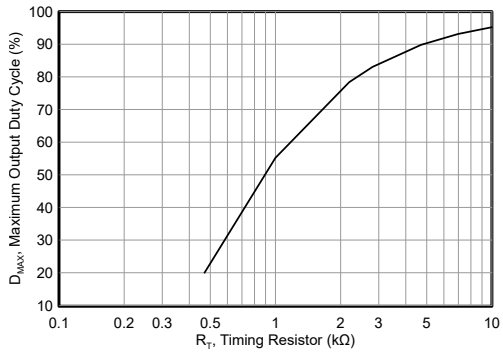


Figure 6-4. Max Output Duty Cycle vs Timing Resistor for V_{CC} = 15, C_T = 3.3 nF, T_A = 25 °C

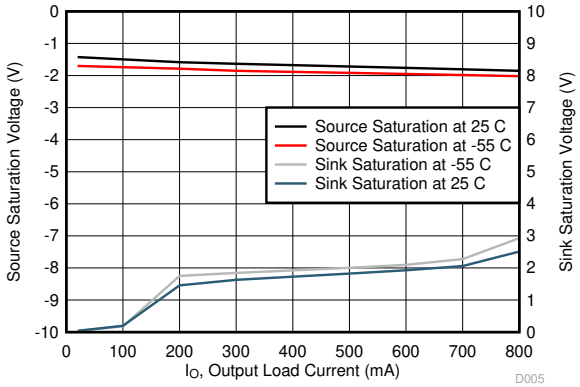


Figure 6-5. Output Saturation Voltage vs Load Current for V_{CC} = 15 V with 5-ms Input Pulses

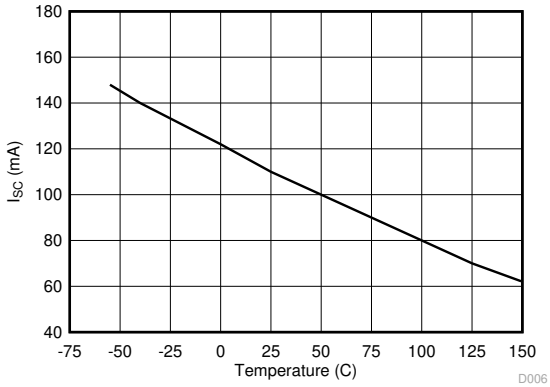


Figure 6-6. Reference Short Circuit Current vs Temperature for V_{CC} = 15 V

6.6 Typical Characteristics (continued)

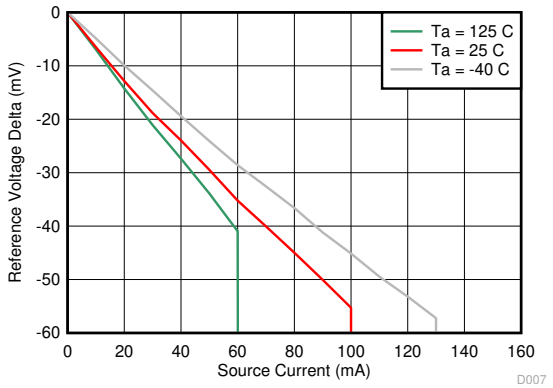


Figure 6-7. Reference Voltage vs Source Current

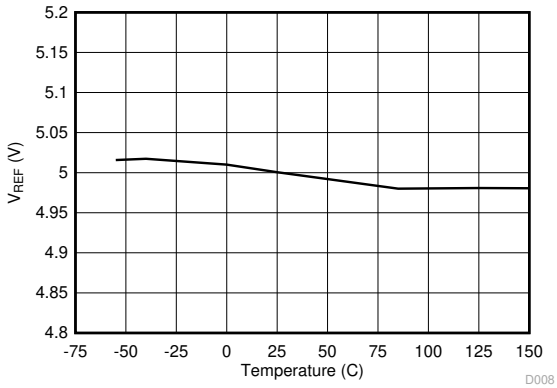


Figure 6-8. Reference Voltage vs Temperature

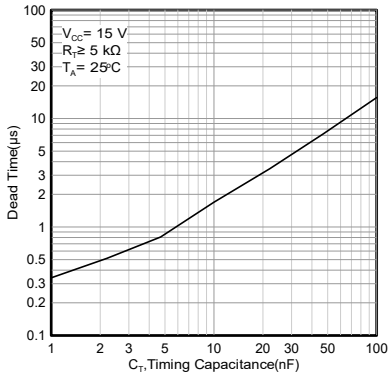


Figure 6-9. Dead Time vs Timing Capacitance

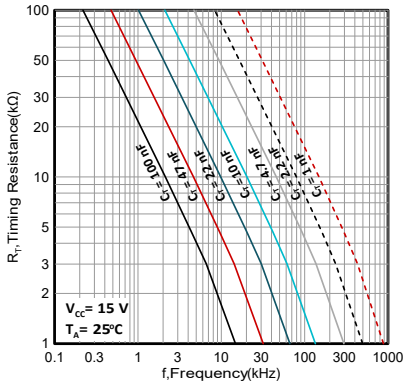


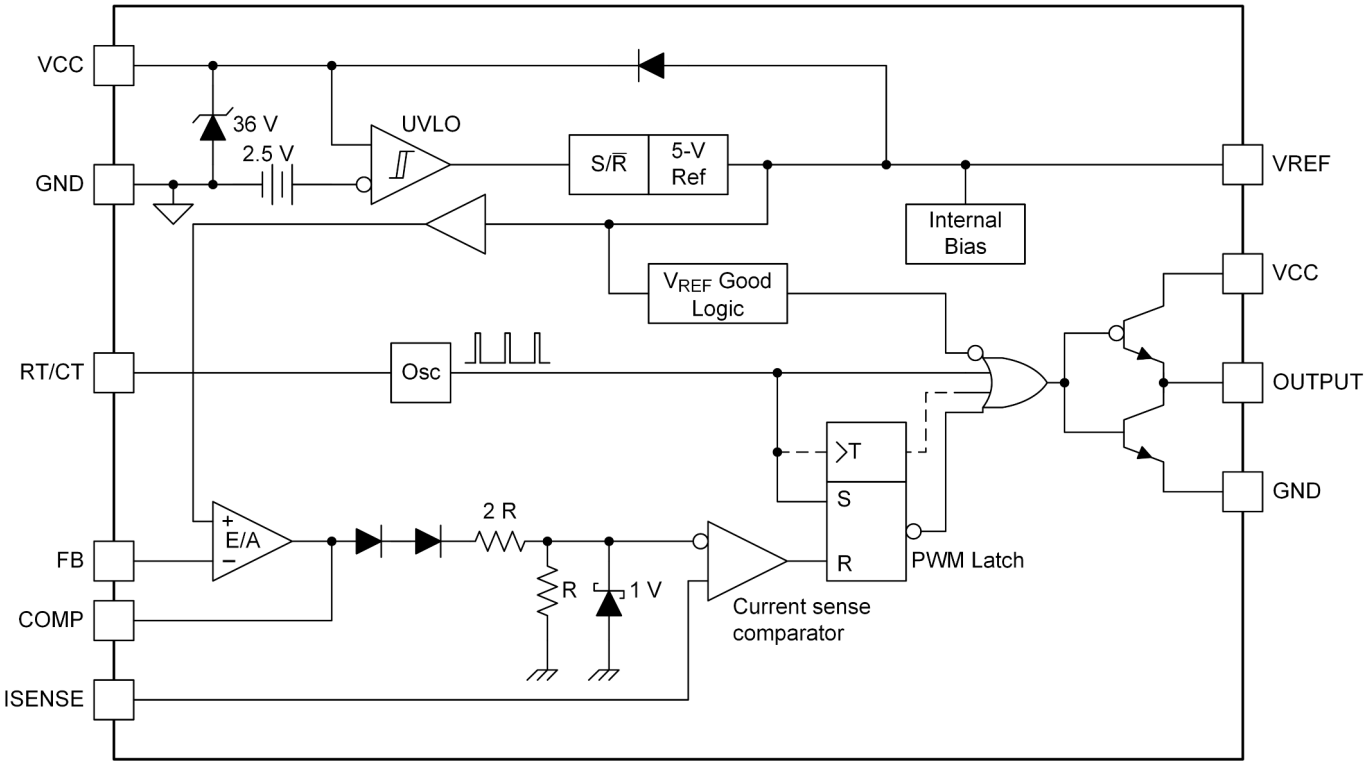
Figure 6-10. Timing Resistance vs Frequency

7 Detailed Description

7.1 Overview

The UC284xL device is a fixed-frequency pulse-width-modulator (PWM) controller and designed to operate at switching frequencies of 500kHz. These controllers are designed for peak current mode (PCM) and can be used in isolated and non-isolated power supply designs. These controllers can drive FETs directly from the output, which is capable of sourcing and sinking up to 1A of gate driver current. These devices also have a built-in low-impedance amplifier that can be used in non-isolated designs to control the power supply output voltage and feedback loop.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Pulse-by-Pulse Current Limiting

Pulse-by-pulse limiting is inherent in the current mode control scheme. An upper limit on the peak current can be established by simply clamping the error voltage. Accurate current limiting allows optimization of magnetic and power semiconductor elements while ensuring reliable supply operation.

7.3.2 Current Sense Circuit

Peak current (I_S) is determined by Equation 1:

$$I_{S(max)} \times \frac{1\,V}{R_S} \tag{1}$$

A small RC filter may be required to suppress switch transients.

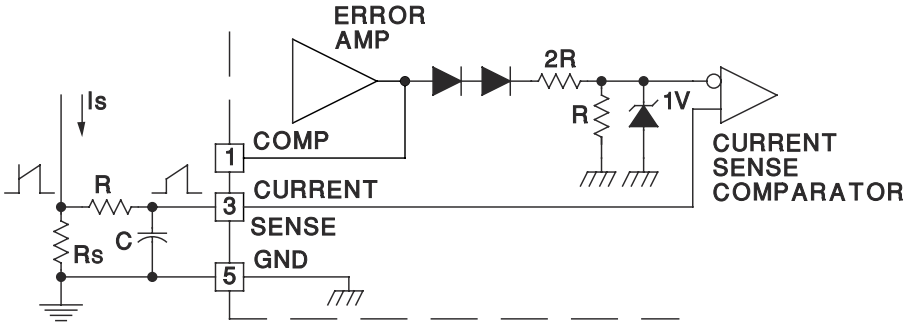


Figure 7-1. Current Sense Circuit Diagram

7.3.3 Error Amplifier Configuration

The error amplifier can source up to 0.8mA, and sink up to 6mA.

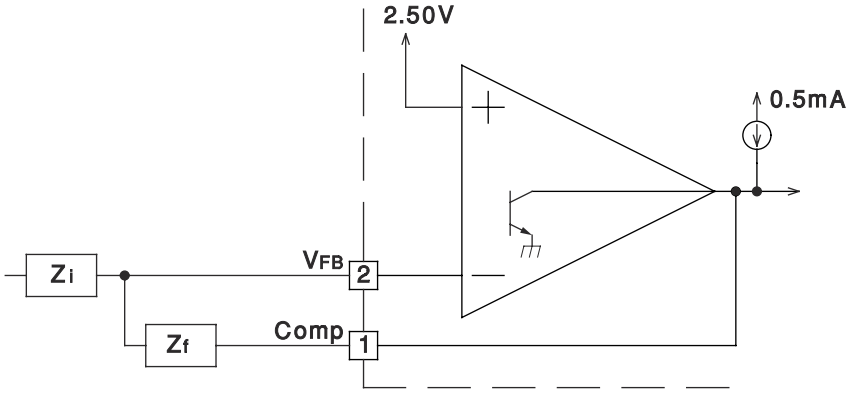


Figure 7-2. Error Amplifier Configuration Diagram

7.3.4 Undervoltage Lockout

The UC284xL device is featured with undervoltage lockout protection circuits for controlled operation during power-up and power-down sequences.

During UVLO the IC draws typically 0.25mA of supply current. This lower VCC current than the UC284x family results in lower power drawn from the line. The reduced start-up current is of particular concern in off-line supplies where the IC is *powered-up* from the high-voltage DC rail, then bootstrapped to an auxiliary winding on the main transformer. Power is then dissipated in the start-up resistor which is sized by the IC's start-up current. Once crossing the turnon threshold the IC supply current increases typically to about 11mA, During undervoltage lockout, the UC284xL prevents the power MOSFET from parasitically turning on due to the *Miller* effect at power-up. This improved design to the lower totem-pole transistor's operation during undervoltage lockout allows the IC to sink higher currents, up to 10mA, at saturation voltages as low as 0.7V.

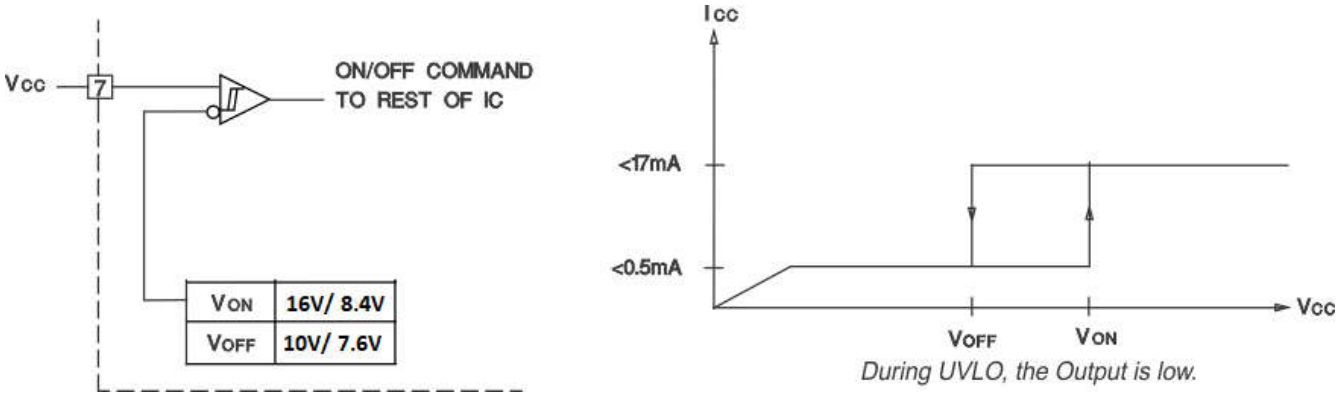
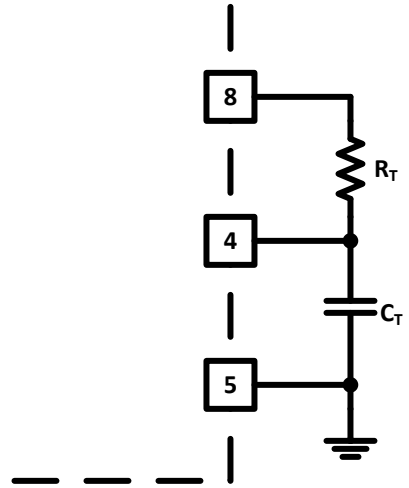


Figure 7-3. Undervoltage Lockout

7.3.5 Oscillator



$$\text{For } R_T > 5\text{ k} \quad f \approx \frac{1.72}{R_T \times C_T}$$

Figure 7-4. Oscillator Section

Precision operation at high frequencies with an accurate maximum duty cycle, see Figure 6-10, can now be obtained with the UC284xL family of devices due to its trimmed oscillator discharge current. This nullifies the effects of production variations in the initial discharge current or dead time. Note the UC284xL OUTPUT frequency is half of the oscillator frequency and associated maximum duty cycle is 50%.

7.4 Device Functional Modes

7.4.1 Normal Operation

The IC can be used in peak current mode (PCM) control or voltage mode (VM) control. When the converter is operating in PCM, the voltage amplifier output will regulate the converter's peak current and duty cycle. When the IC is used in VM control, the voltage amplifier output will regulate the power converter's duty cycle. The regulation of the system's peak current and duty cycle can be achieved with the use of the integrated error amplifier and external feedback circuitry.

7.4.2 Undervoltage Lockout (UVLO) Start-Up

During system start-up, VCC voltage starts to rise from 0V. Before the VCC voltage reaches its corresponding start threshold, the IC is operating in UVLO mode. After the UVLO turn start-up threshold is met the device will become active and the reference will come up to 5V.

7.4.3 UVLO Turnoff Mode

If the bias voltage to VCC drops below the UVLO minimum operating voltage, PWM switching stops and the reference will become inactive, returning to 0V. The device can be restarted by applying a voltage greater than the UVLO start threshold to the VCC pin.

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The UC284xL controller is a peak-current mode pulse-width modulator. The controller has an onboard amplifier and can be used in isolated or non-isolated power supply designs. There is an onboard totem-pole gate driver capable of delivering 1A of peak current. This is a high-speed PWM capable of operating at switching frequencies up to 500kHz. The typical applications can be referred to UC284xA families as shown in *UC2842A data sheet*, and can be found at www.ti.com/product/UC2842A or UCx84x/UCx84xA/UC284xAQ/TL284x/TL284xB families product pages, for details.

8.2 Typical Application

A typical application for the UC2842L in an off-line flyback converter is shown in Figure 8-1. The UC2842L uses an inner current control loop that contains a small current sense resistor which senses the primary inductor current ramp. This current sense resistor transforms the inductor current waveform to a voltage signal that is input directly into the primary side PWM comparator. This inner loop determines the response to input voltage changes. An outer voltage control loop involves comparing a portion of the output voltage to a reference voltage at the input of an error amplifier. When used in an off-line isolated application, the voltage feedback of the isolated output is accomplished using a secondary-side error amplifier and adjustable voltage reference, such as the TL431. The error signal crosses the primary to secondary isolation boundary using an opto-isolator whose collector is connected to the VREF pin and the emitter is connected to FB. The outer voltage control loop determines the response to load changes.

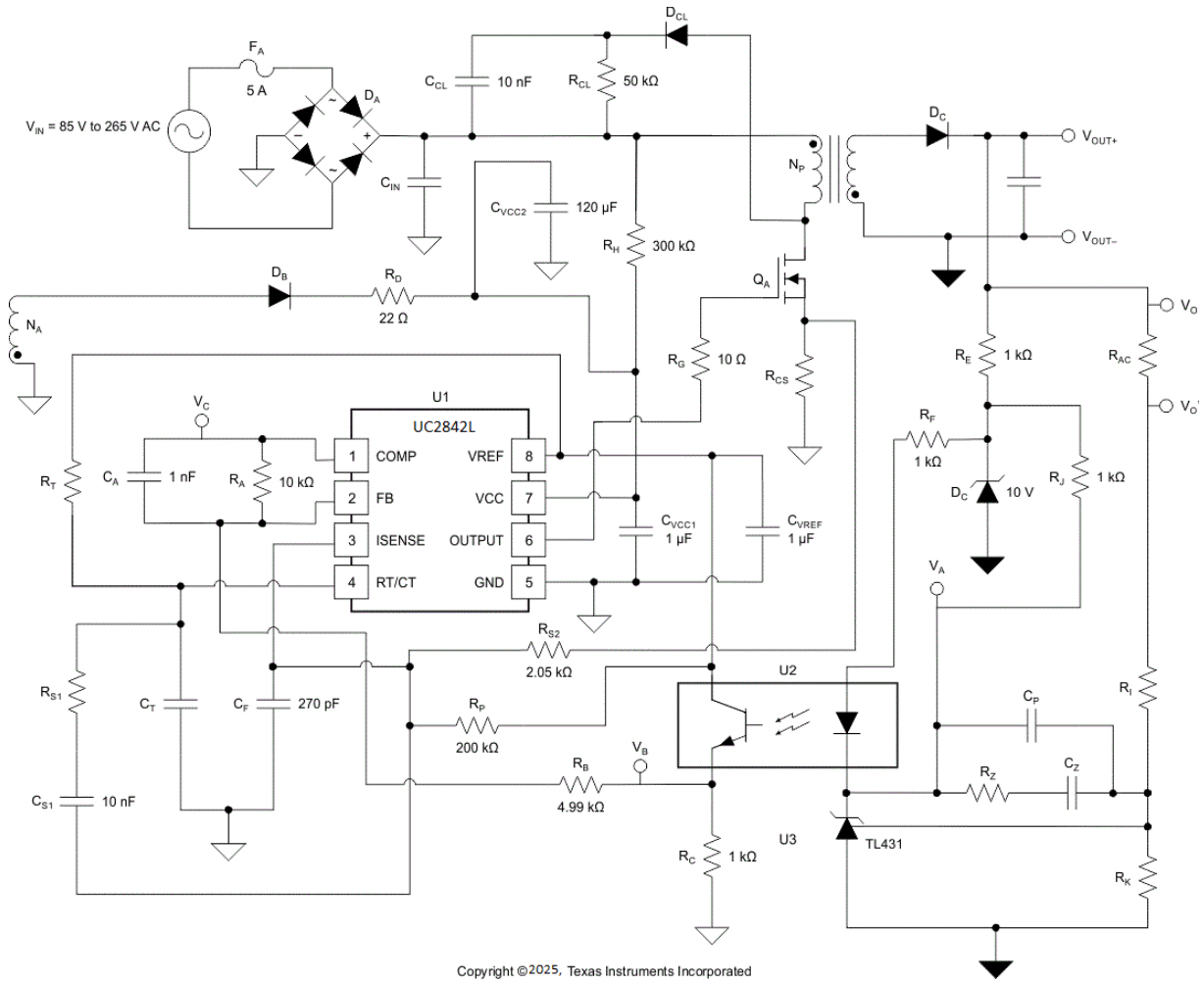


Figure 8-1. Typical Flyback Application Circuit

8.2.1 Design Requirements

For this design example, use the parameters listed in Table 8-1 as the input parameters.

Table 8-1. Design Parameters

PARAMETER		MIN	TYP	MAX	UNIT
INPUT CHARACTERISTICS					
V_{IN}	Input voltage (RMS)	85		265	V
f_{LINE}	Line frequency	47		63	Hz
OUTPUT CHARACTERISTICS					
V_{OUT}	Output voltage	11.75	12	12.25	V
	Output ripple voltage		50		mV_{PP}
I_{OUT}	Output current		4	4.33	A
	Load step	11.75		12.25	V
SYSTEMS CHARACTERISTICS					
η	Maximum load efficiency	86%			

8.2.2 Detailed Design Procedure

8.2.2.1 Custom Design With WEBENCH® Tools

Click here to create a custom design using the UC284x (corresponding to equivalent GPN for UC284xL) device with the WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

8.2.2.2 UC2842L Design Procedure

This application design procedure shows how to setup and use the UC2842L peak current mode controller in an offline flyback converter, with universal input to a 12-V, 48-W regulated output.

Setting up and designing with the UC2842L peak current mode controller in a continuous mode flyback application requires knowing some things about the power stage. First, calculate the required input bulk capacitance (C_{IN}) based on output power level (P_{OUT}), efficiency (η), minimum input voltage ($V_{IN(min)}$), line frequency (f_{LINE}) and minimum bulk voltage. For this design example let $V_{BULK(min)}$ = 95V.

$$V_{INripple} = \frac{2 \times \frac{P_{OUT}}{\eta} \times \left[0.25 + \frac{1}{\pi} \times \arcsin \times \left(\frac{V_{BULK(min)}}{\sqrt{2} \times V_{IN(min)}} \right) \right]}{\left(2 \times V_{IN(min)}^2 - V_{BULK(min)}^2 \right) \times f_{LINE}} \quad (2)$$

$$C_{IN} = \frac{2 \times \frac{P_{OUT}}{\eta} \times \left[0.25 + \frac{1}{\pi} \times \arcsin \times \left(\frac{V_{BULK(min)}}{\sqrt{2} \times V_{IN(min)}} \right) \right]}{\left(2 \times V_{IN(min)}^2 - V_{BULK(min)}^2 \right) \times f_{LINE}} \approx 180\ \mu F \quad (3)$$

The output capacitor (C_{OUT}) is sized so the output voltage does not droop more than 10% during a large-signal transient response. The voltage-loop crossover frequency (f_C) is estimated to be 2.5kHz at this point in the design.

$$C_{OUT} \geq \frac{\frac{I_{OUT}}{f_C}}{V_{OUT} \times 10\%} \approx 1.33 mF \quad (4)$$

The C_{OUT} selected for the design is a 2200-µF capacitor, with an equivalent series resistance (ESR) of 45mΩ.

Next calculate the maximum primary to secondary turns ratio (N_{PS}) of the transformer, based on the minimum input voltage and output voltage.

$$N_{PS} \leq \frac{V_{IN(min)} \times \sqrt{2}}{V_{OUT}} = \frac{85\ V \times \sqrt{2}}{12\ V} \approx 10 \quad (5)$$

Next calculate the auxiliary to secondary turns ratio (N_{AS}) of the transformer, based on the output voltage and the bias voltage of the UC2842A.

$$N_{AS} \leq \frac{V_{VCC}}{V_{OUT}} = \frac{12\ V}{12\ V} = 1 \tag{6}$$

Once the transformer turns ratios have been determined, the minimum primary magnetizing inductance (L_{PM}) of the transformer can be calculated based on minimum bulk voltage, Duty Cycle (D), reflected output current and efficiency. The transformer used in this design has an L_{PM} of 1.7mH, N_{PS} = 10, and a N_{AS} = 1, f_{sw} = 100kHz

$$D = \frac{N_{PS} \times V_{OUT}}{V_{BULK(min)} + N_{PS} \times V_{OUT}} \approx 0.56 \tag{7}$$

$$L_{PM} \geq \frac{V_{BULK\,(min)} \times D}{\frac{70\% \times I_{OUT} \times f_{sw}}{\eta \times N_{PS}}} = 1.632\text{mH} \approx 1.7\text{mH} \tag{8}$$

After the transformer has been selected, the primary peak current (I_{LpPK}) of the transformer can be calculated based on the primary magnetizing inductance ripple (I_{LPM}) and the reflected output current across the transformer.

$$I_{LPM} = \frac{V_{BULK(min)} \times D}{f_{SW} \times L_M} \approx 0.31\ A \tag{9}$$

$$I_{LpPK} = \frac{I_{OUT}}{N_{PS} \times (1-D)} + \frac{I_{LM}}{2} \approx 1.1\ A \tag{10}$$

Once the primary peak current has been calculated the current sense resistor (R_{CS}) can be selected.

$$R_{CS} = \frac{1\ V}{I_{LpPK} \times 1.3} = 0.725\ \Omega \approx 0.75\ \Omega \tag{11}$$

Resistors R_{S1} and R_{S2} are used to set the slope compensation of the design. Capacitor C_{S1} is a DC blocking capacitor, and pull-up resistor R_P is used to provide some offset to the current sense signal for noise immunity. R_P and R_{S2} were preselected to add a DC offset of 50mV to the current sense signal.

R_{S1} is selected to set the slope compensation to one-half of the ripple current down slope of the flyback inductor. This can be accomplished by calculating the secondary magnetizing inductance (L_{SM}) and using the following calculation for R_{S1}. The 1.7V in the R_{S1} equation is the peak-to-peak ripple voltage amplitude of the oscillator.

$$R_{S1} = \frac{1.7\ V \times R_{S2} \times f_{SW} \times (2 \times L_{SM} \times N_{PS})}{V_{OUT} \times (1-D) \times R_{CS}} - R_{S2} = 27.72\ k\Omega \approx 27.4\ k\Omega \tag{12}$$

where

- $R_{S2} = 2.05\ k\Omega$

Resistors R_I and R_K are selected to the output reference and can be calculated by preselecting a value for R_K and knowing the TL431 reference voltage ($V_{TL431REF}$). After choosing 2.49 kΩ for R_K, R_I is calculated and a standard resistor value of 9.53kΩ is chosen for this resistor.

$$R_I = \frac{R_K \times (V_{OUT} - V_{TL431REF})}{V_{TL431REF}} = \frac{2.49\ k\Omega \times (12\ V - 2.5\ V)}{2.5\ V} = 9.462\ k\Omega \approx 9.53\ k\Omega \quad (13)$$

This design using the UC2842L controller has an interesting control loop with many components. $G_{OPTO}(f)$ is the approximate transfer function across the opto isolator in the design. The pole frequency of the opto isolator is represented by f_P. The opto isolator used in this design has a current transfer ratio of 1 and pole frequency of roughly 5kHz. See Figure 8-1 for component placement and node voltages. The voltage loop (f_C) must cross-over less than the opto isolator pole for simplified compensation.

$$s(f) = 2 \times \pi \times 1i \times f \quad (14)$$

$$f_P = 5\ kHz \quad (15)$$

$$G_{OPTO}(f) = \frac{\Delta V_B}{\Delta V_A} = \frac{R_C}{R_F} \times \frac{ctr}{\frac{s(f)}{2 \times \pi \times f_P} + 1} \quad (16)$$

$G_{BC}(f)$ is an estimate of the transfer function from the output of the opto isolator to the PWM's control voltage .

$$G_{BC}(f) = \frac{\Delta V_C}{\Delta V_B} = \frac{R_A}{R_B} \times \frac{1}{s(f) \times R_A \times C_A + 1} \quad (17)$$

The duty cycle varies with the bulk input voltage (V_{BULK}). V_{BULK} varies from 95V to 375V during normal operation. This causes the duty cycle to vary from 24% to 56%.

$$D = \frac{N_{PS} \times V_{OUT}}{V_{BULK} + N_{PS} \times V_{OUT}} = 0.24 \text{ to } 0.56 \quad (18)$$

$G_{CO}(f)$ is an estimate of the control (V_C) to output transfer function, where variable Q is the quality factor.

$$G_{CO}(f) = \frac{\Delta V_{OUT}}{\Delta V_C} = N_{PS} \times \frac{1 - D}{1 + D} \times \left[\frac{s(f) \times ESR \times C_{OUT} + 1}{s(f) \times R_{OUT} \times C_{OUT} + 1}\right] \times \left[1 - \frac{s(f) L_{SM} \times D}{R_{OUT} \times (1 - D)^2}\right] \times \frac{\frac{1}{3}}{1 + \frac{s(f)}{2 \times \pi \times \frac{f_{SW}}{2} \times Q} + \left(\frac{s(f)}{2 \times \pi \times \frac{f_{SW}}{2}}\right)^2} \quad (19)$$

The quality factor (Q) is defined by the primary magnetizing inductance change in voltage (S_N) as a function of duty cycle; as well as, the added slope compensation (S_E).

$$S_N = \frac{V_{BULK} \times R_{CS}}{L_{PM}} \quad (20)$$

$$S_E = 1.7\ V \times \frac{R_{S2} \times f_{SW}}{R_{S1} + R_{S2}} \quad (21)$$

$$Q = \frac{1}{\pi \left[\left(1 + \frac{S_E}{S_N}\right) \times (1 - D) - 0.5\right]} \quad (22)$$

To ensure that the voltage loop is stable, the crossover frequency must be less than one half of the right-half-plane zero frequency (f_{RHPZ}) of the flyback converter. The right-half-plane zero frequency at the minimum bulk voltage would be roughly 9.8kHz. For this design example the target crossover of the voltage loop is at 1kHz. The actual f_C may be higher or lower than the target.

$$f_{RHPz} = \frac{(N_{PS})^2}{\frac{2 \times \pi \times Lpm}{R_{OUT}} \frac{D}{(1-D)^2}} \approx 9.8kHz \quad (23)$$

$$f_C \leq \frac{f_{RHPz}}{2} \approx 5\ kHZ \quad (24)$$

The DC gain of $G_{CO}(f)$ moves with the bulk input voltage. Resistor R_Z is selected to crossover the voltage loop when input to the converter is at $V_{BULK(min)}$ and to crossover at 1/5th the maximum crossover frequency.

$$R_Z = \frac{R_I}{\left|G_{OPTO}(f_C/5) \times G_{BC}(f_C/5) \times G_O \times G_{CO}(f_C/5)\right|} = 23.95\ k\Omega, \text{ a } 23.7\ k\Omega \text{ was used} \quad (25)$$

Capacitor C_Z is selected to add 45° of phase margin at voltage loop crossover. For this design example a 6.8-nF capacitor was used.

$$C_Z = \frac{1}{2\pi \times \frac{f_C}{5} \times R_Z} \approx 6.7\ nF \quad (26)$$

Capacitor C_P is selected to attenuate the high frequency gain of the control loop.

$$C_P = \frac{C_Z}{10} = 680\ pF \quad (27)$$

$G_C(f)$ is the estimated transfer function of the TL431 compensation.

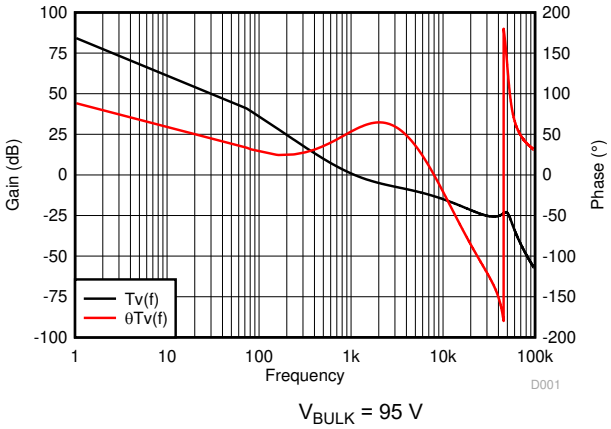
$$G_C(f) = \frac{\Delta V_C}{\Delta V_O'} = \frac{s(f) \times R_Z \times C_Z + 1}{s(f) \times R_I \times (C_Z + C_P) \times \left(\frac{s(f) \times R_Z \times C_Z \times C_P}{C_Z + C_P} + 1\right)} \quad (28)$$

$T_V(f)$ is the estimated theoretical transfer function of the close-loop gain of the system. The feedback loop response may be different in the actual circuit and may have to be adjusted with a network analyzer to meet actual circuit performance and reliability. The feedback loop response must be evaluated over worse case variations in design parameters.

$$T_V(f) = G_C(f) \times G_{OPTO}(f) \times G_{BC}(f) \times G_O \times G_{CO}(f_C) \quad (29)$$

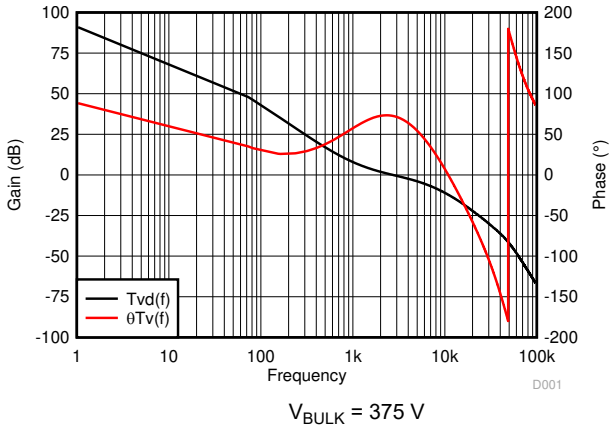
For this application example, this design technique generated a theoretical feedback loop ($T_V(f)$) crossover at 1kHz with roughly 55° of phase margin at a minimum input bulk voltage of 95V. The theoretical voltage loop at high-line crossed over at 2.7kHz with a phase margin of 72°. See Figure 8-2 and Figure 8-3. $T_V(f)$ must be evaluated with a network analyzer and adjust the loop compensation as necessary based on the actual circuitry behavior. Also conduct transient testing to ensure that the device remains stable.

8.2.3 Application Curves



V_{BULK} = 95 V

Figure 8-2. Voltage Loop Gain



V_{BULK} = 375 V

Figure 8-3. Voltage Loop Gain

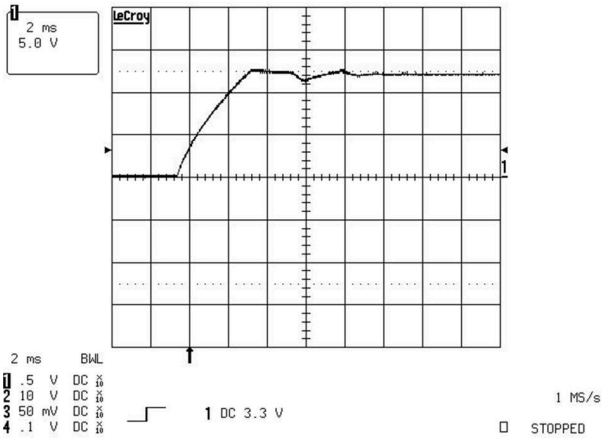


Figure 8-4. V_{OUT} Start-Up Full Load

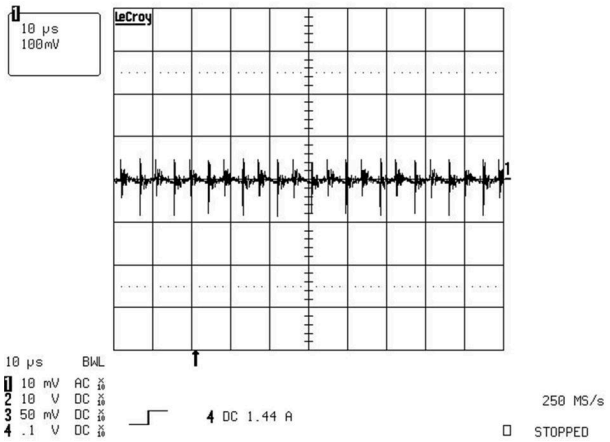


Figure 8-5. V_{OUT} Ripple Voltage

8.3 Power Supply Recommendations

TI recommends using the UC284xL in isolated or non-isolated peak current mode control power supplies. The device can be used in buck, boost, flyback, and forwarded converter-based power supply topologies.

8.4 Layout

8.4.1 Layout Guidelines

- Star grounding techniques must be used.
- Current loops must be kept as short and narrow as possible.
- The IC ground and power ground must meet at the return for the input bulk capacitor. Ensure that high frequency and high current from the power stage does not go through the signal ground paths.
- A high-frequency bypass capacitor (C_{VCC1}) must be placed across VCC and GND pins as close as possible to the pins.
- Resistor R_{S2} and capacitor C_F form a low-pass filter for the current sense signal. C_F must be as close to CS and GND pins as possible.
- Capacitor C_{VREF} must be as close to VREF and GND pins as possible.
- Figure 8-6 shows the SMD components arranged for wave-solder on a single-layer board. If multiple layers are used, some components may be rearranged for easier interconnection and reduced current-loop areas. If the solder process allows, placing the SMD components in perpendicular orientations may improve interconnections and loop areas.

8.4.2 Layout Example

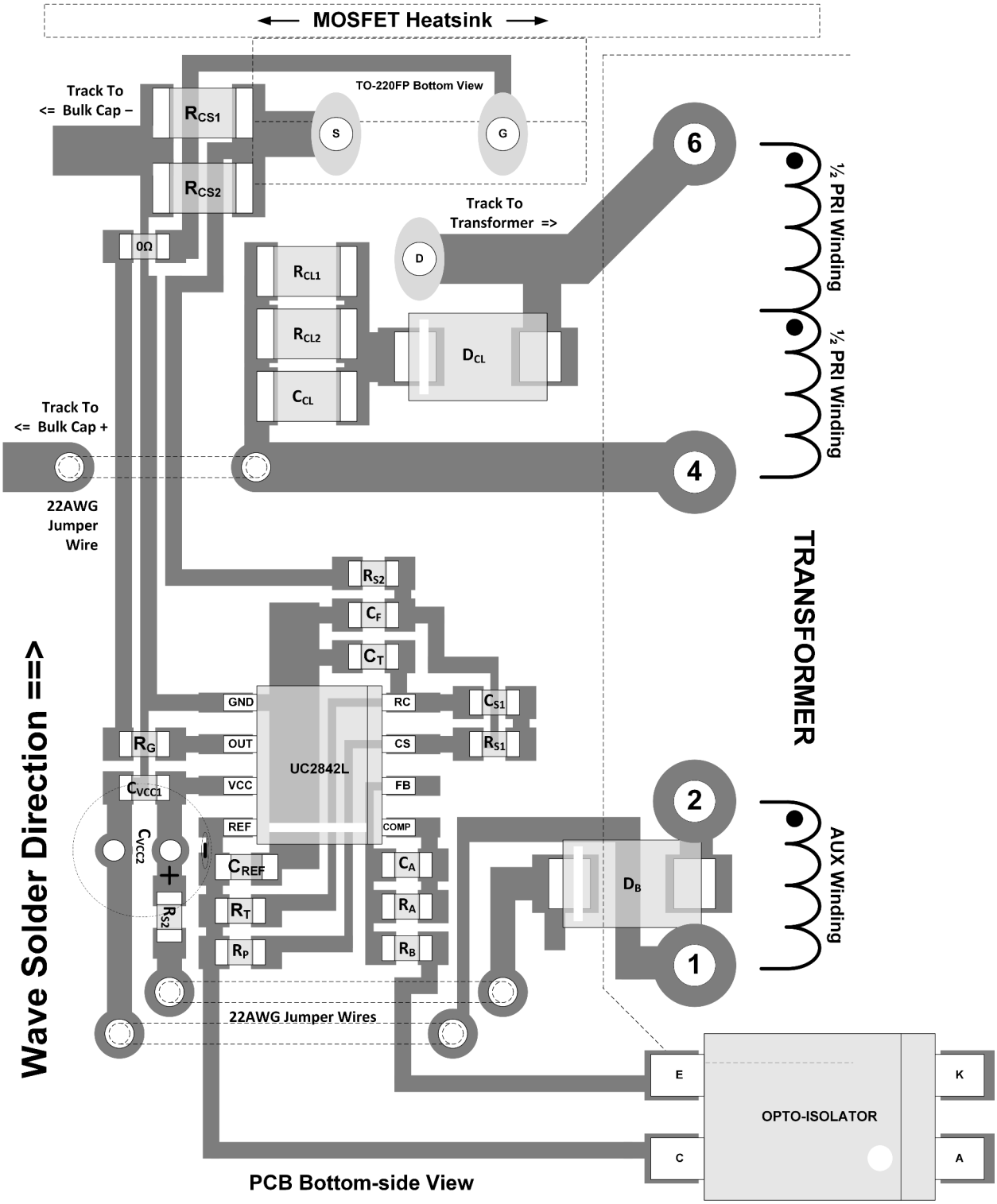


Figure 8-6. Layout Diagram

9 Device and Documentation Support

9.1 Device Support

9.1.1 Device Nomenclature

C_{IN}	Input bulk capacitance
C_{OUT}	Output capacitance
D	Duty cycle
ESR	Equivalent series resistance
$G_{BC}(f)$	An estimate of the transfer function from the output of the opto-isolator to the PWM control voltage.
G_O	The DC gain of the control to output transfer function.
$G_{OPTO}(f)$	The approximate transfer function across the opto-isolator in the design.
I_{LPM}	Transformer primary average current
I_{LpPK}	Peak transformer primary current
L_{PM}	Transformer primary magnetizing inductance
L_{SM}	Transformer secondary magnetizing inductance
N_{PS}	Primary to secondary transformer turns ratio
N_{AS}	Auxiliary to secondary transformer turns ratio
$T_V(f)$	is the feedback control loop transfer function.
$V_{INripple}$	Input ripple voltage

9.2 Documentation Support

9.2.1 Related Documentation

For related documentation see the following:

Design Review: 150 Watt Current-Mode Flyback (SLUP078)

UCx84x/UCx84xA/UC284xAQ/TL284x/TL284xB data sheets or product pages for more reference design

9.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

9.5 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

9.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.7 Glossary

TI Glossary This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
March 2025	*	Initial Release

11 Mechanical, Packaging, and Orderable Information

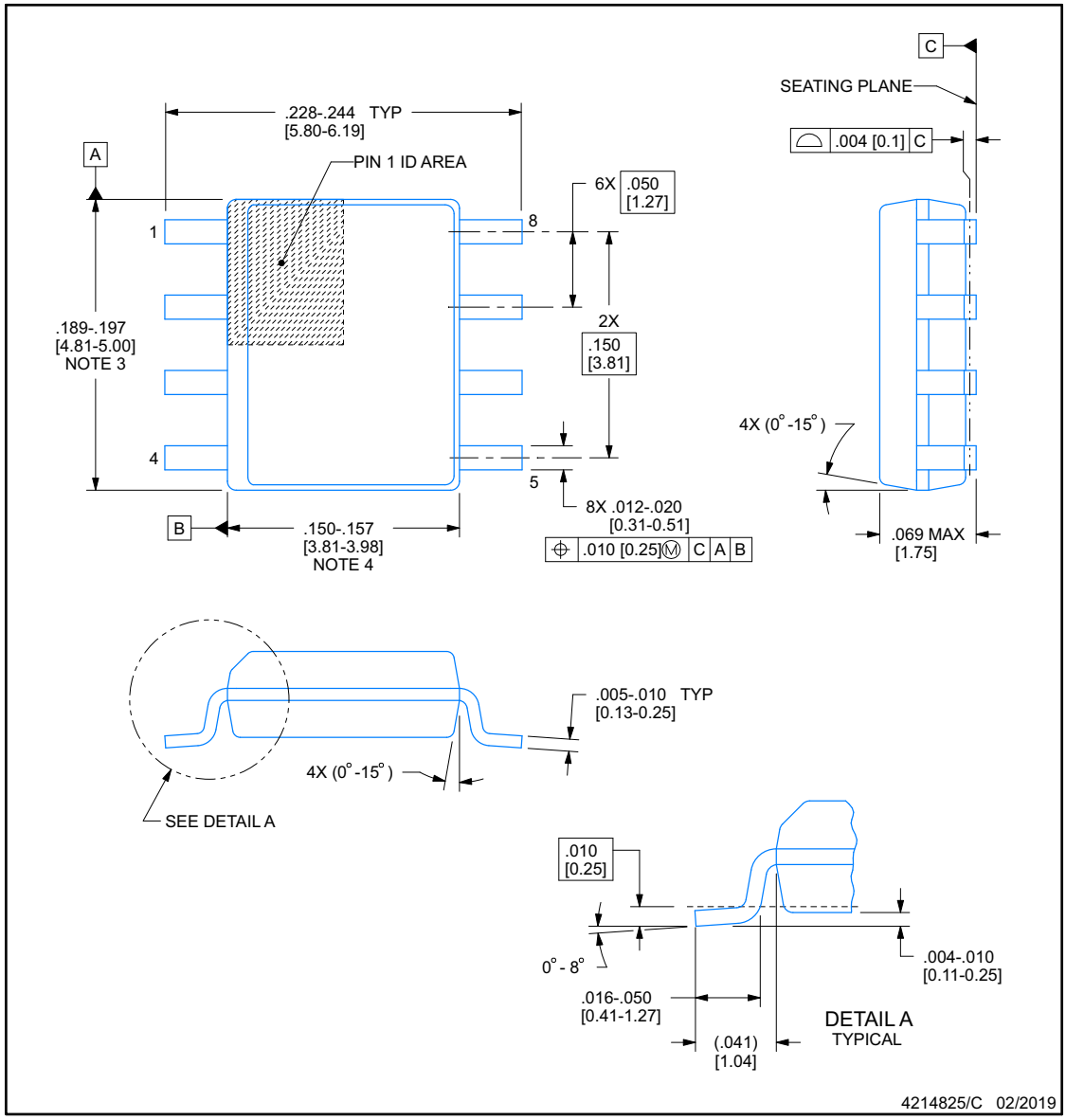
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGE OUTLINE

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



NOTES:

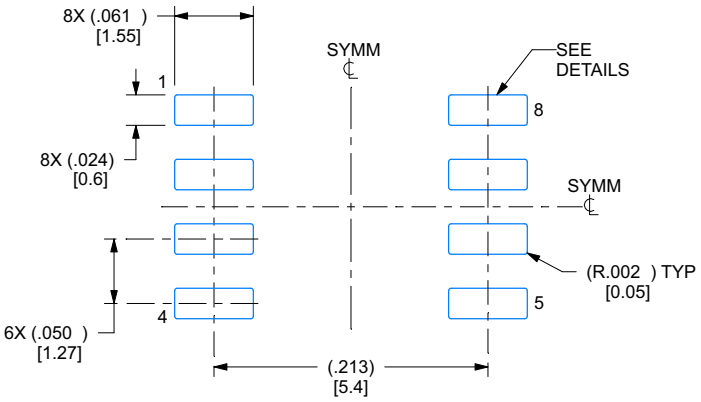
1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

EXAMPLE BOARD LAYOUT

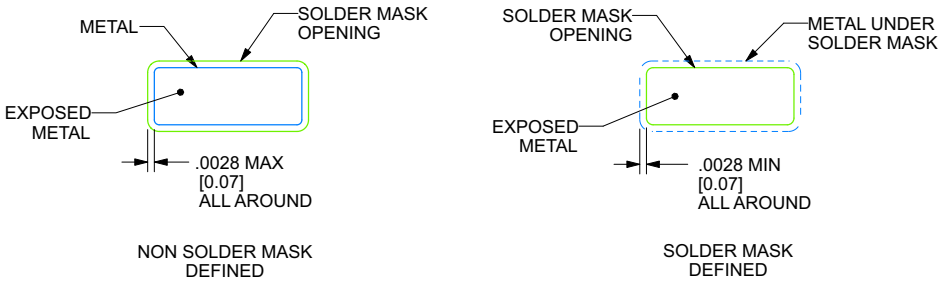
D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

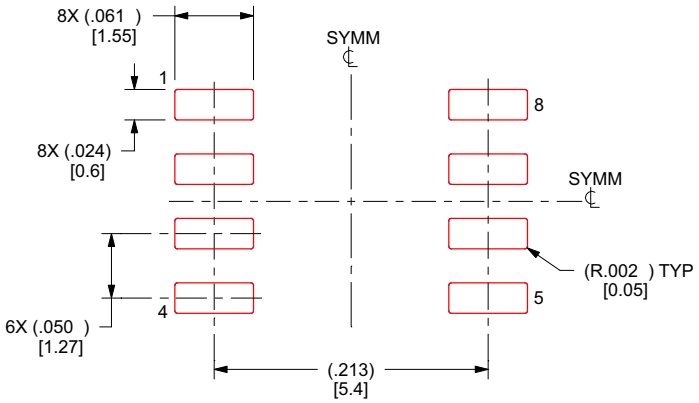
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A — **SOIC - 1.75 mm max height**

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
UC2842LDR-8	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	U2842L
UC2842LDR-8.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	U2842L
UC2843LDR-8	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	U843BL
UC2843LDR-8.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	U843BL
UC2844LDR-8	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	U2844L
UC2844LDR-8.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	U2844L
UC2845LDR-8	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	U2845L
UC2845LDR-8.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	U2845L

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

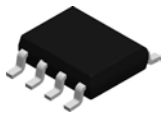
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF UC2843L, UC2844L, UC2845L :

- Automotive : UC2843L-Q1, UC2844L-Q1, UC2845L-Q1

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

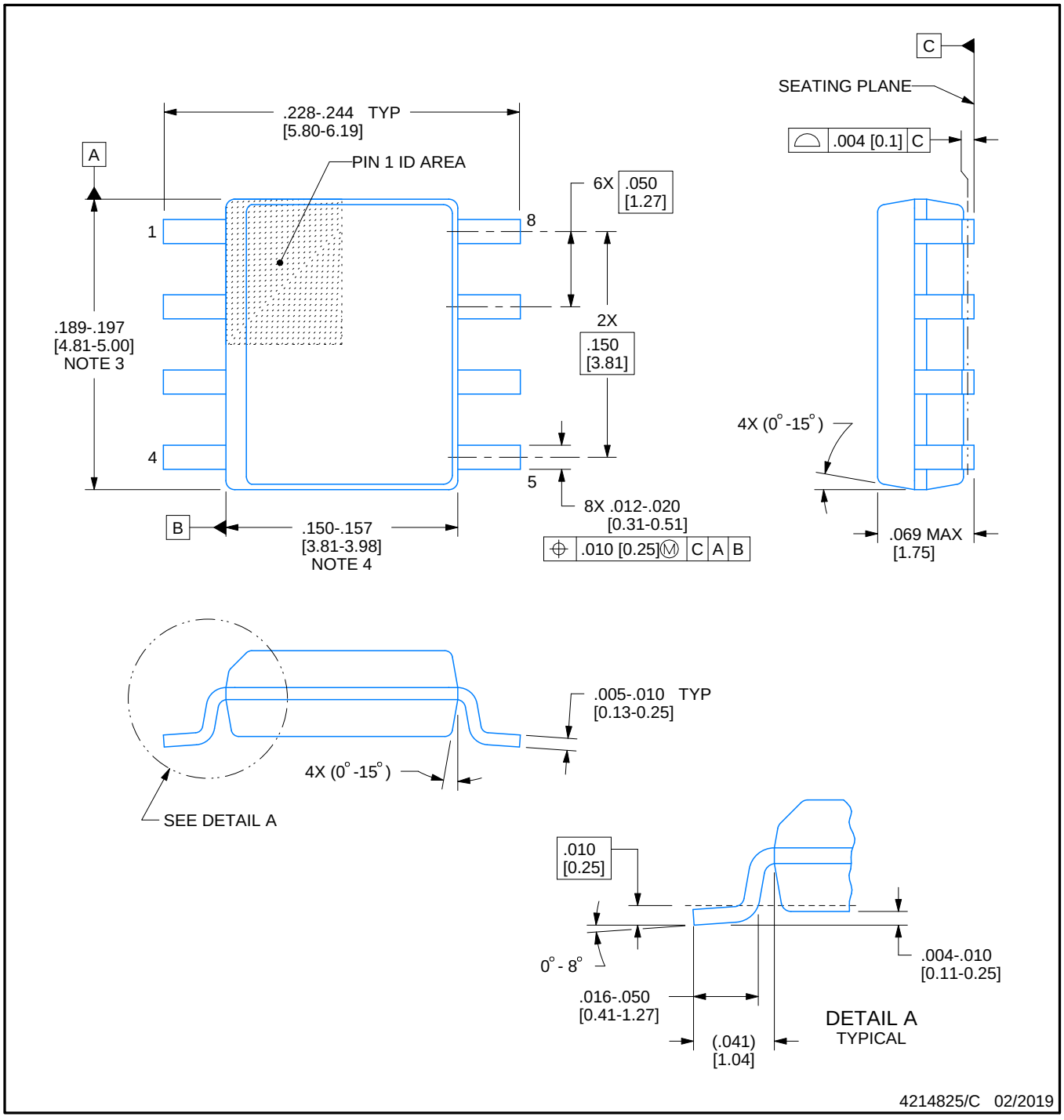


PACKAGE OUTLINE

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



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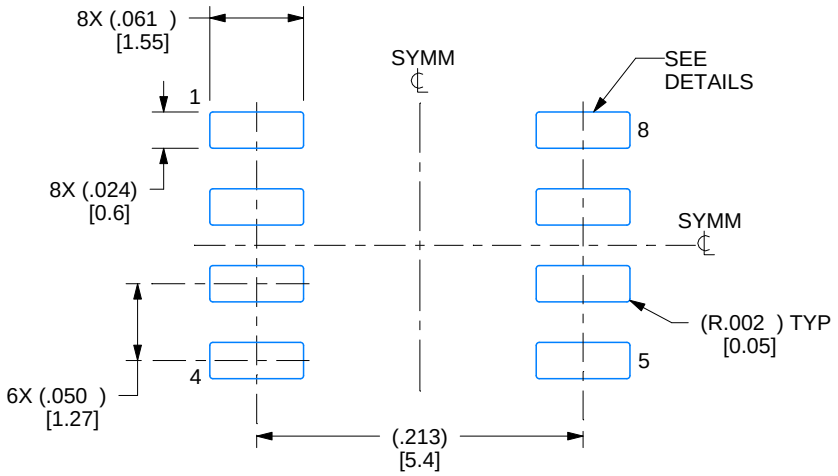
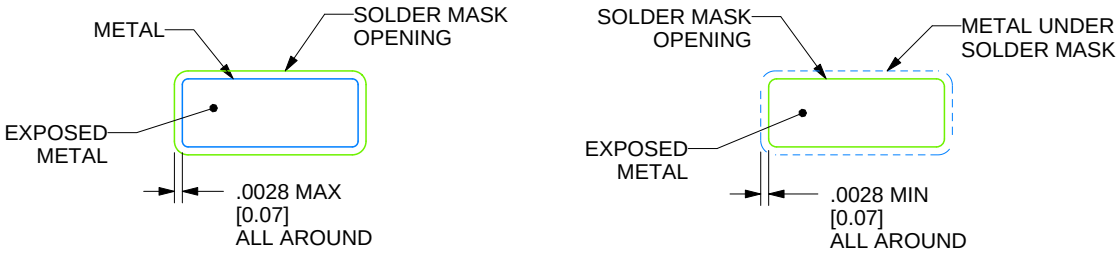
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

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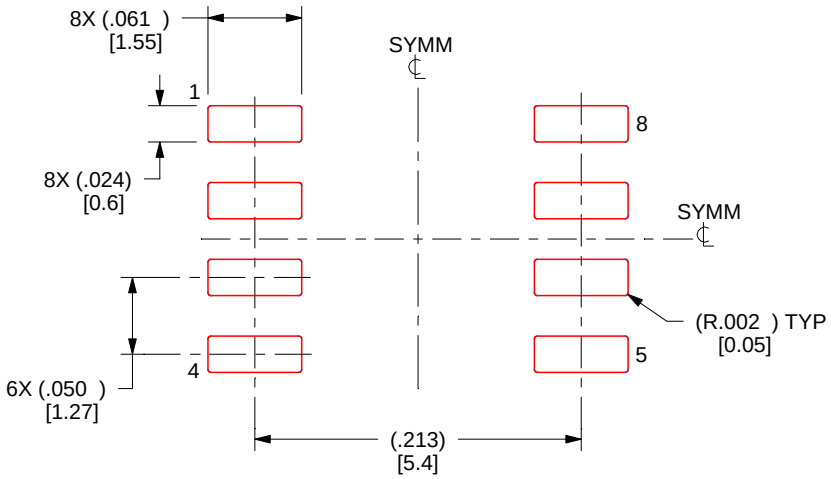
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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