SLUS339B – JUNE 1993 – REVISED DECEMBER 2004

DUAL SCHOTTKY DIODE BRIDGE

FEATURES

- **Monolithic Eight-Diode Array**
- **Exceptional Efficiency**
- **Low Forward Voltage**
- **Fast Recovery Time**
- **High Peak Current**
- **Small Size**

DESCRIPTION

This eight-diode array is designed for high-current, low duty-cycle applications typical of flyback voltage clamping for inductive loads. The dual bridge connection makes this device particularly applicable to bipolar driven stepper motors.

The use of Schottky diode technology features high efficiency through lowered forward voltage drop and decreased reverse recovery time.

This single monolithic chip is fabricated in both hermetic CERDIP and copper-leaded plastic packages. The UC1610 in ceramic is designed for –55°C to 125°C environments but with reduced peak current capability. The UC2610 in plastic and ceramic is designed for –25°C to 125°C environments also with reduced peak current capability; while the UC3610 in plastic has higher current rating over a 0°C to 70°C temperature range.

AVAILABLE OPTIONS

$T_A = T_J$	Packaged Devices		
	SOIC Wide (DW)	DIL (J)	DIL (N)
–55°C to 125°C	UC1610DW	UC1610J	UC1610N
–25°C to 125°C	UC2610DW	UC2610J	UC2610N
0°C to 70°C	UC3610DW	UC3610J	UC3610N

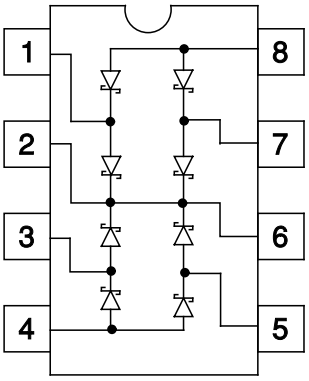
THERMAL INFORMATION

PACKAGE	θja	θjc
SOIC (DW) 16 pin	50 – 100(1)	27
DIP (J) 8 pin	125 – 160	20(2)
DIP (N) 8 pin	103(1)	50

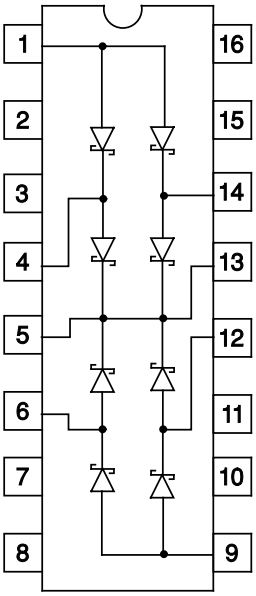
NOTES: 1. Specified θja (junction-to-ambient) is for devices mounted to 5-in^2 FR4 PC board with one ounce copper where noted. When resistance range is given, lower values are for 5-in^2 aluminum PC board. Test PWB was 0.062 in thick and typically used 0.635-mm trace widths for power packages and 1.3-mm trace widths for non-power packages with a 100-mil x 100-mil probe land area at the end of each trace.

2. θjc data values stated were derived from MIL–STD–1835B. MIL–STD–1835B states that the baseline values shown are worst case (mean + 2s) for a 60-mil x 60-mil microcircuit device silicon die and applicable for devices with die sizes up to 14400 square mils. For device die sizes greater than 14400 square mils use the following values; dual-in-line, 11°C/W; flat pack, 10°C/W; pin grid array, 10°C/W.

N OR J PACKAGE
TOP VIEW



DW PACKAGE
TOP VIEW



absolute maximum ratings over operating free-air temperature (unless otherwise noted)†‡

Peak inverse voltage (per diode) . . . . . 50 V
Peak forward current
UC1611 . . . . . 1 A
UC2610 . . . . . 1 A
UC3611 . . . . . 3 A
Power dissipation at T_A = 70°C . . . . . 1 W
Storage temperature range, T_{stg} . . . . . –65°C to 150°C
Lead temperature (soldering, 10 seconds) . . . . . 300°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

‡ Consult packaging section of databook for thermal limitations and considerations of package.

electrical characteristics, all specifications apply to each individual diode, T_J = 25°C, $T_A = T_J$, (except as noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Forward voltage drop	I_F = 100 mA	0.35	0.5	0.7	V
	I_F = 1 A	0.8	1.0	1.3	V
Leakage current	V_R = 40 V		0.01	0.1	mA
	V_R = 40 V, T_J = 100°C		0.1	1.0	mA
Reverse recovery	0.5 A forward to 0.5 A reverse		15		ns
Forward recovery	1 A forward to 1.1 V recovery		30		ns
Junction capacitance	V_R = 5 V		70		pF

NOTE: At forward currents of greater than 1.0 A, a parasitic current of approximately 10 mA may be collected by adjacent diodes.

APPLICATION INFORMATION

REVERSE CURRENT vs VOLTAGE

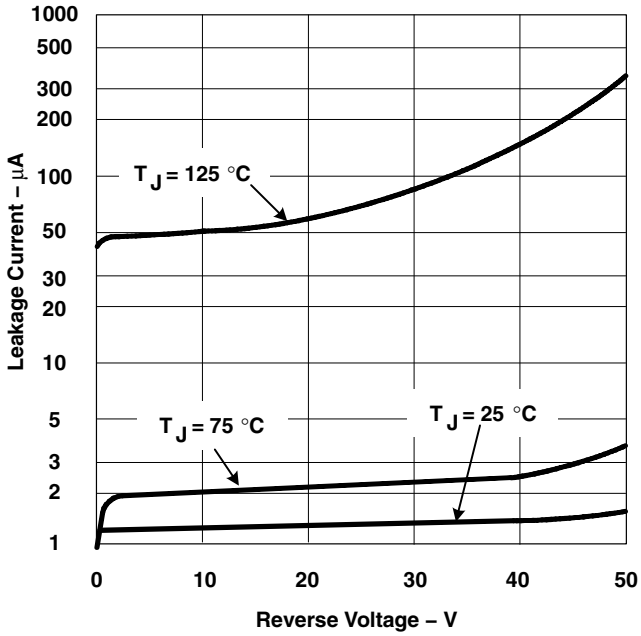


Figure 1

FORWARD CURRENT vs VOLTAGE

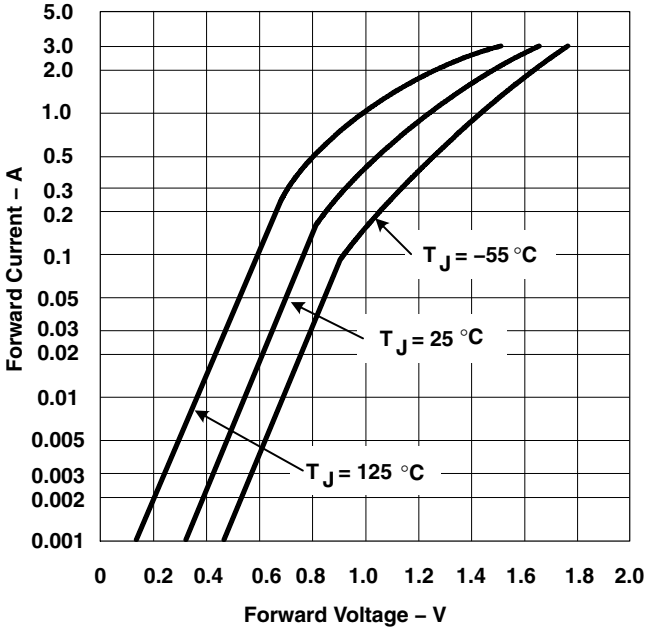


Figure 2

REVERSE RECOVERY CHARACTERISTICS

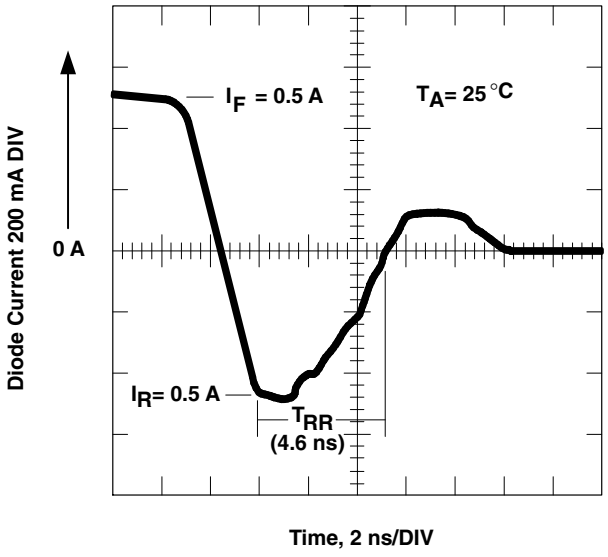


Figure 3

FORWARD RECOVERY CHARACTERISTICS

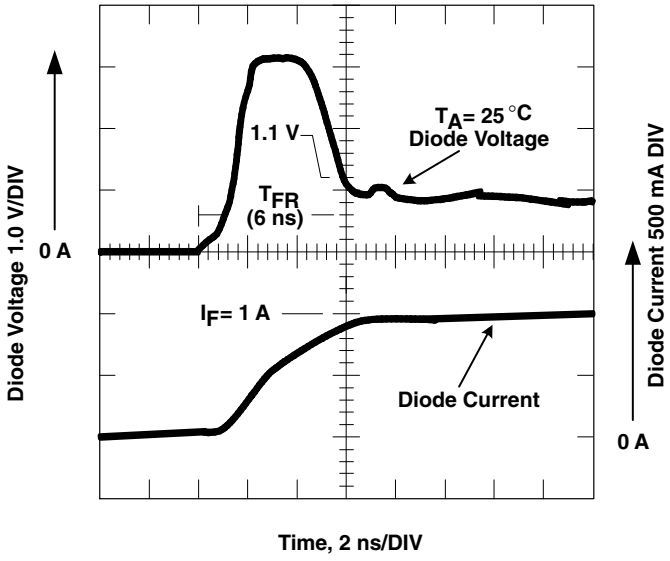


Figure 4

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
UC2610N	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	UC2610N
UC2610N.A	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	UC2610N
UC3610DW	Active	Production	SOIC (DW) | 16	40 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	0 to 70	UC3610DW
UC3610DW.A	Active	Production	SOIC (DW) | 16	40 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	0 to 70	UC3610DW
UC3610DWTR	Active	Production	SOIC (DW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	0 to 70	UC3610DW
UC3610DWTR.A	Active	Production	SOIC (DW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	0 to 70	UC3610DW
UC3610N	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	UC3610N
UC3610N.A	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	UC3610N

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

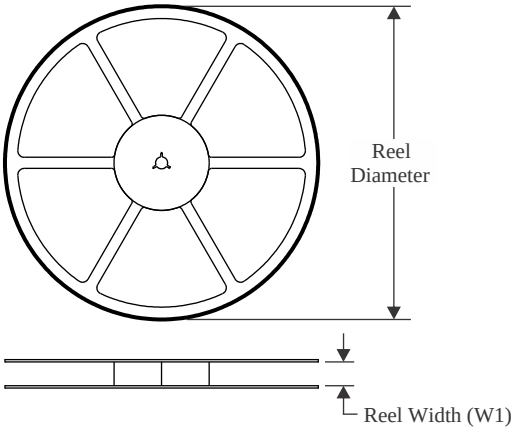
(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

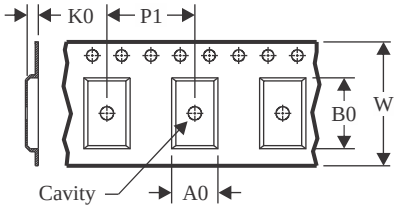
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

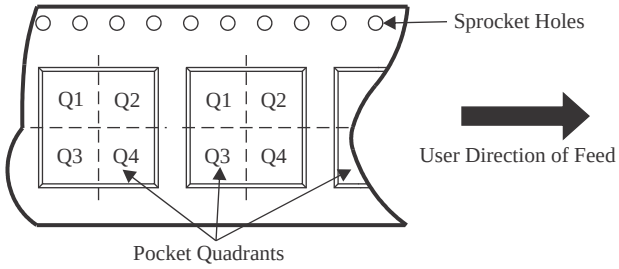


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

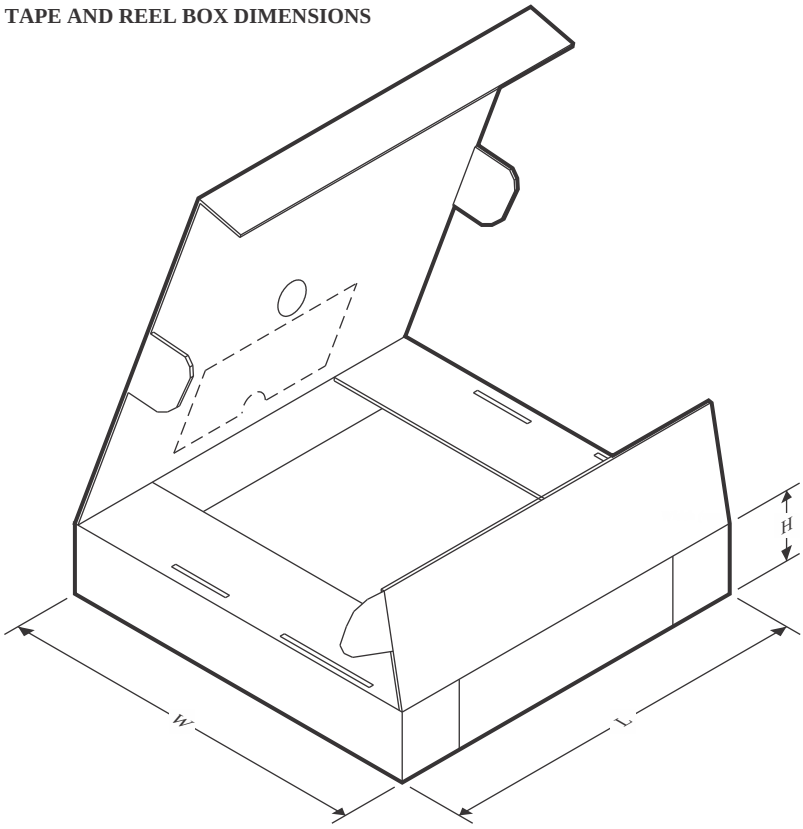
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UC3610DWTR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1

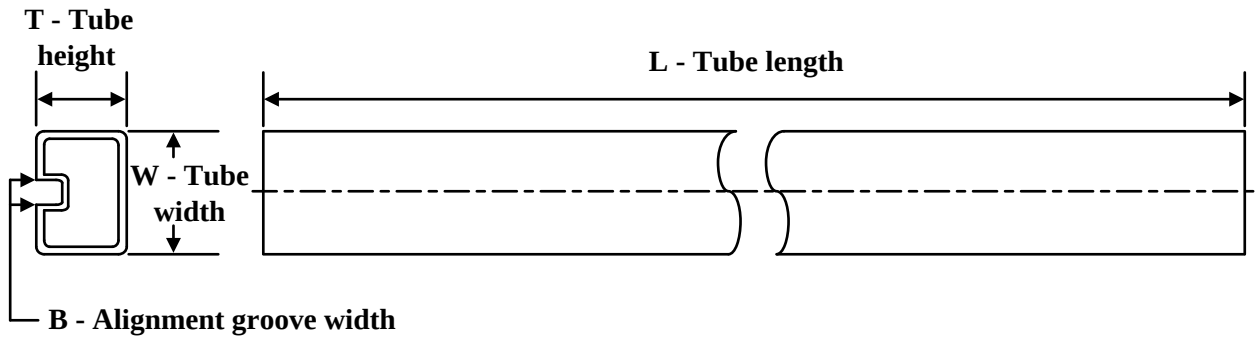
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UC3610DWTR	SOIC	DW	16	2000	356.0	356.0	35.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
UC2610N	P	PDIP	8	50	506	13.97	11230	4.32
UC2610N.A	P	PDIP	8	50	506	13.97	11230	4.32
UC3610DW	DW	SOIC	16	40	507	12.83	5080	6.6
UC3610DW.A	DW	SOIC	16	40	507	12.83	5080	6.6
UC3610N	P	PDIP	8	50	506	13.97	11230	4.32
UC3610N.A	P	PDIP	8	50	506	13.97	11230	4.32

GENERIC PACKAGE VIEW

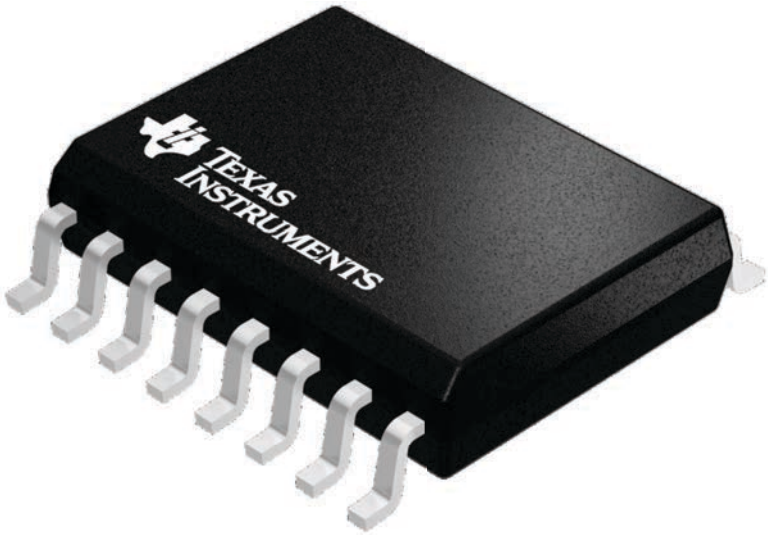
DW 16

SOIC - 2.65 mm max height

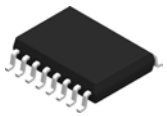
7.5 x 10.3, 1.27 mm pitch

SMALL OUTLINE INTEGRATED CIRCUIT

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4224780/A

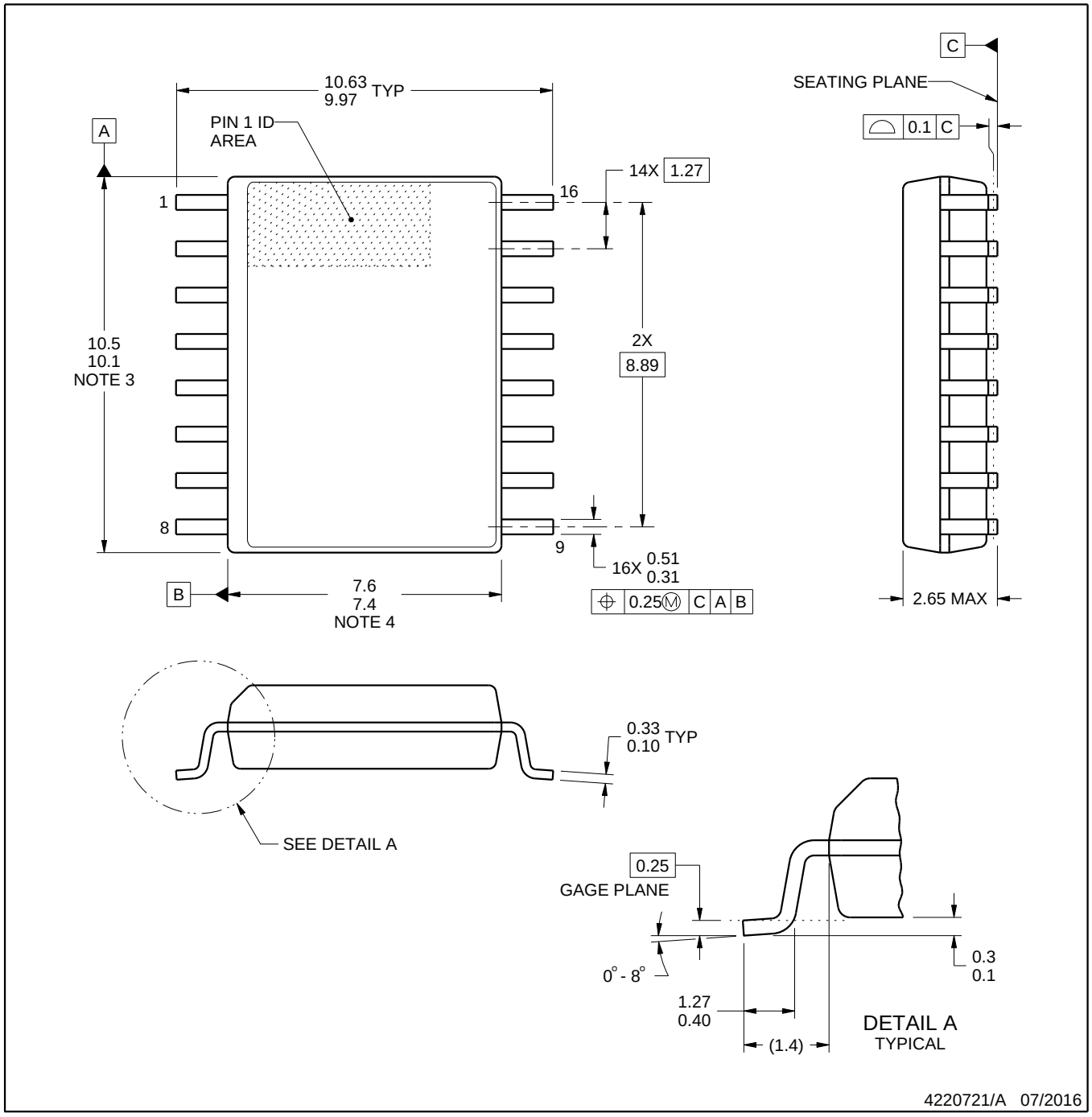


PACKAGE OUTLINE

DW0016A

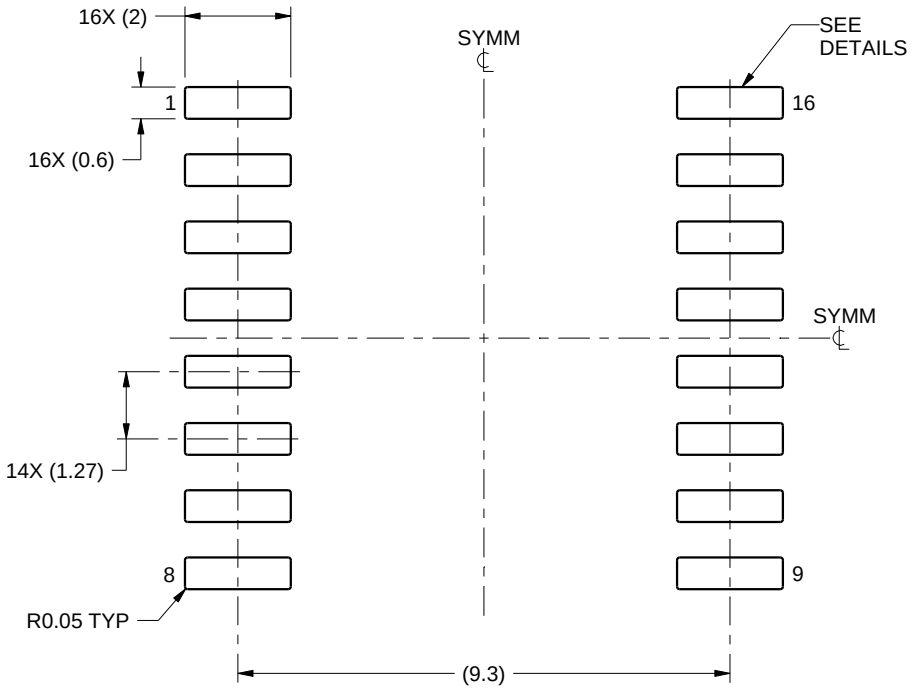
SOIC - 2.65 mm max height

SOIC

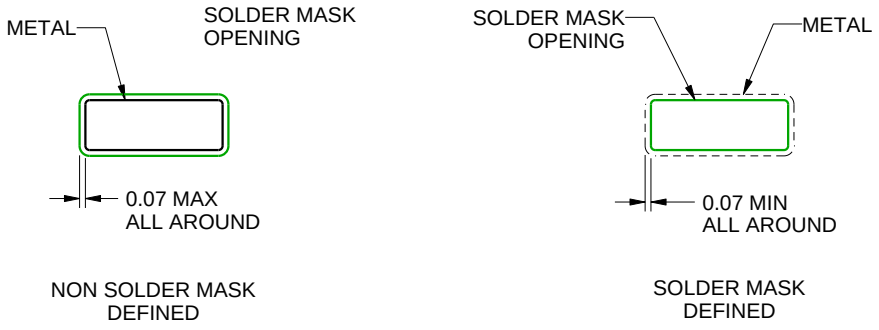


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.
5. Reference JEDEC registration MS-013.



LAND PATTERN EXAMPLE
SCALE:7X

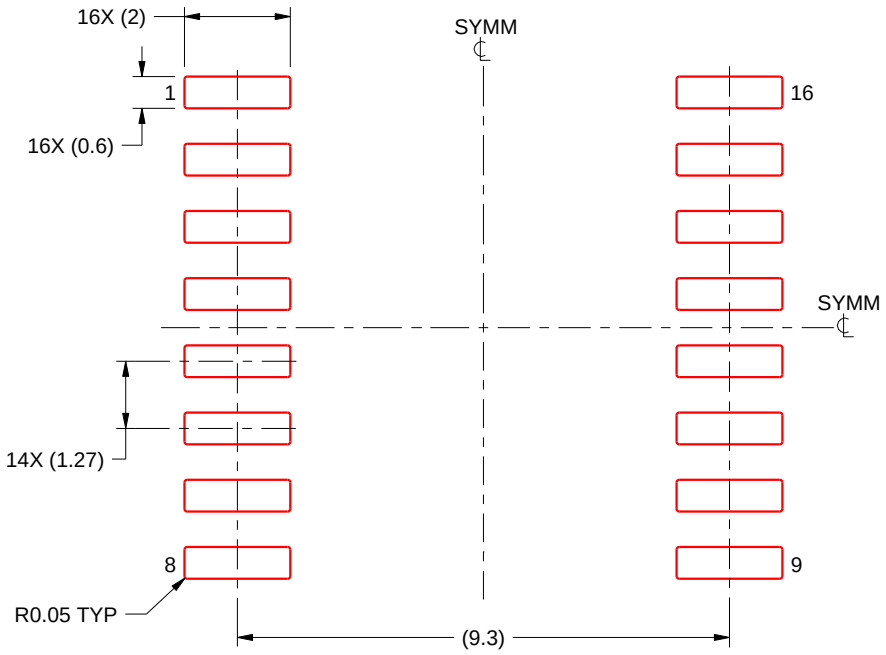


SOLDER MASK DETAILS

4220721/A 07/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



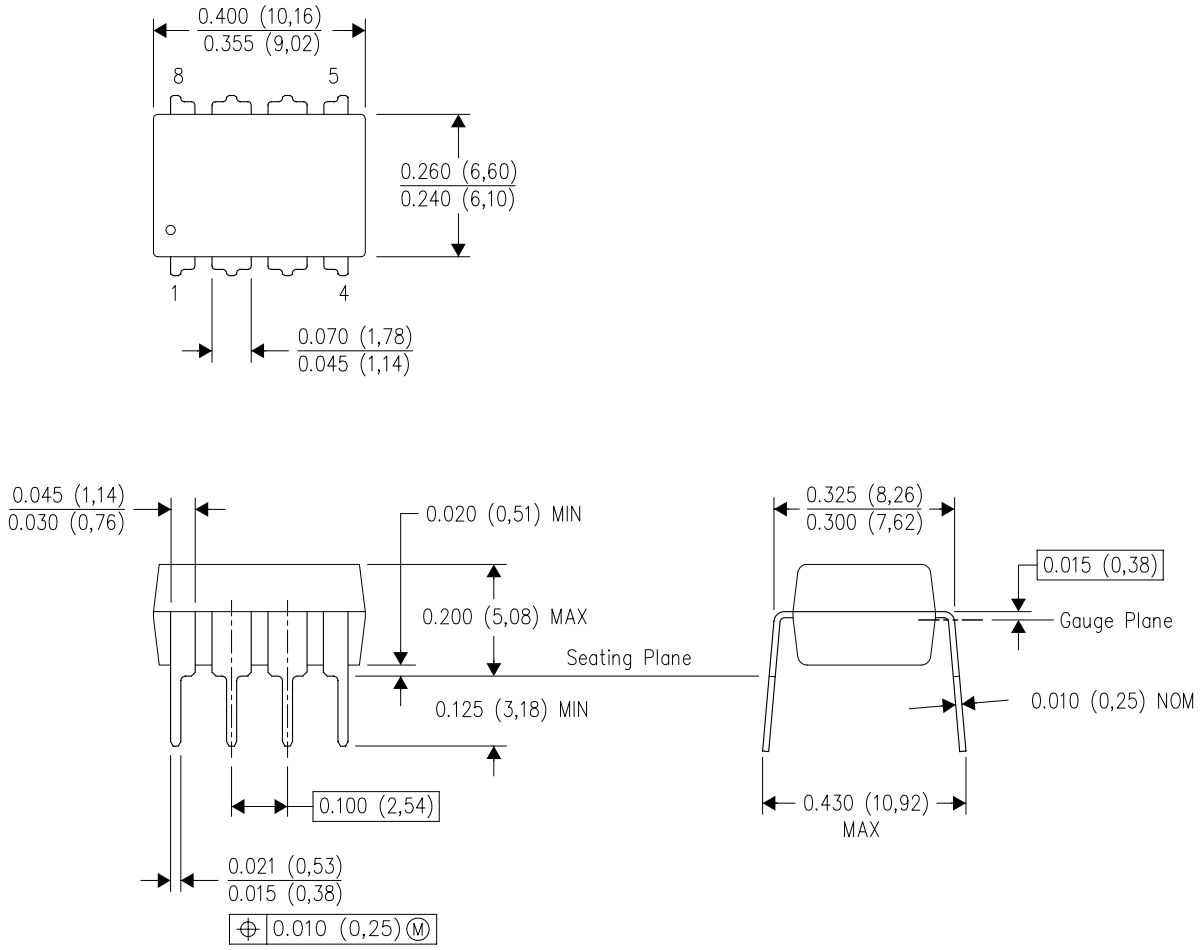
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:7X

4220721/A 07/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

P (R–PDIP–T8) PLASTIC DUAL–IN–LINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001 variation BA.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265