UA78M-Q1 Automotive, 500mA, Positive-Voltage Linear Regulator

1 Features

- AEC-Q100 qualified for automotive applications:
  – Temperature grade 1: -40°C to 125°C, T_J
- Input voltage range (V_{IN}) (M3 version): 5.3V to 30V
- Absolute maximum input voltage:
  – Non-M3 version only: 35V
  – M3 version only: 45V
- Output voltage (V_{OUT}): 3.3V and 5V
- Output current (I_{OUT}): Up to 500mA
- Built-in, short-circuit current limiting and thermal protection
- Stable without any external components
- Package:
  – DCY (4-pin SOT-223), $R_{\theta JA}$: 77.7°C/W

2 Applications

- Onboard charging
- Traction inverters
- Starters and generators

3 Description

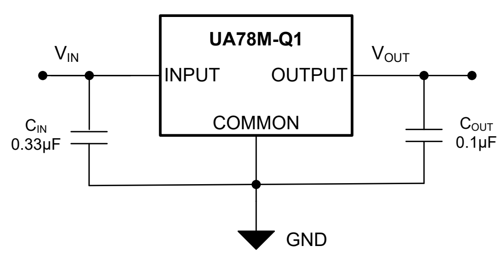
The UA78M-Q1 fixed-voltage, integrated-circuit voltage regulator is designed for a wide range of applications. The UA78M-Q1 also functions with power-pass transistors to make high-current voltage regulators. The UA78M-Q1 delivers up to 500mA of output current. Additionally, the UA78M-Q1 does not need an external capacitor for stable operation across the load current range. The internal current-limiting and thermal shutdown features of this regulator help protect the device from overload.

The UA78M-Q1 is characterized for the junction temperature range of –40°C to +125°C. See the *Device Nomenclature* table for more details.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
UA78M-Q1	DCY (SOT-223, 4)	6.5mm × 7mm

(1) For more information, see the *Mechanical, Packaging, and Orderable Information*.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Simplified Application Schematic

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4 Pin Configuration and Functions

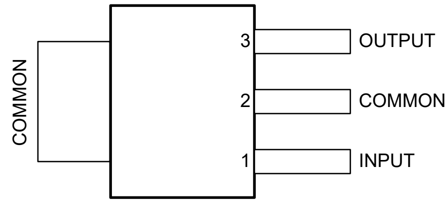


Figure 4-1. DCY Package, 4-Pin SOT-223 (Top View)

Table 4-1. Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
COMMON	2,4	—	Ground
INPUT	1	I	Input pin. Use the recommended capacitor value as listed in the *Recommended Operating Conditions* table. Place the input capacitor as close to the INPUT and COMMON pins of the device as possible.
OUTPUT	3	O	Output pin. Use the recommended capacitor value as listed in the *Recommended Operating Conditions* table. Place the output capacitor as close to the OUTPUT and COMMON pins of the device as possible.

5 Specifications

5.1 Absolute Maximum Ratings

over operating temperature range (unless otherwise noted)(1)

	MIN	MAX	UNIT
Input voltage, V_I (for non-M3 version only)		35	V
Input voltage, V_I (for M3 version only)		45	V
Output voltage, V_o (for M3 version only)	-0.3	12	V
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds (for non-M3 version only)		260	°C
Junction temperature, T_J		150	°C
Storage temperature, T_{stg}	–65	150	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1)	±2500	V
		Charged-device model (CDM), per AEC Q100-011	±2000	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordancewith the ANSI/ESDA/JEDEC JS-001 specification.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)[1]

			MIN	TYP	MAX	UNIT
VIN	Input voltage	UA78M33 (non-M3 version only)	5.3		25	V
		UA78M33 (M3 version only)	5.3		30	
		UA78M05 (non-M3 version only)	7		25	
		UA78M05 (M3 version only)	7		30	
C_{IN} [2]	Input capacitor [3]			0.33		μF
C_{OUT} [2]	Output capacitor [4]			0.1	470	μF
I_O	Output current				500	mA
T_J	Operating junction temperature		–40		125	°C

(1) All voltages are with respect to GND.
(2) UA78M-Q1 regulator does not need any external capacitors for LDO stability.
(3) An input capacitor with value of 0.33 μF is recommended to counteract the effect of source resistance and inductance, which can in some cases cause symptoms of system level instability such as ringing or oscillation, especially in the presence of load transients.
(4) An output capacitor with value of 0.1 μF is recommended to improve the load and line transient performance of the UA78M-Q1 regulator. The maximum output capacitor is guaranteed by design

5.4 Thermal Information

THERMAL METRIC [1]		UA78M-Q1		UNIT
		DCY (3 PINS)		
		non-M3 version	M3 version	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	53	77.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	4	44.6	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	–	–	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application note.

5.5 Electrical Characteristics: UA78M33Q (Both Legacy and New Chip)

specified at T_J = 25°C, V_I = 8 V, C_{IN} = 0.33 µF, C_{OUT} = 0.1µF, and I_O = 350 mA (unless otherwise noted)

PARAMETER	TEST CONDITIONS[1]			MIN	TYP	MAX	UNIT
Output voltage	V_I = 8V to 20V, and I_O = 5mA to 350mA			3.2	3.3	3.4	V
		T_J = full range	non-M3 version only	3.1	3.3	3.5	
		T_J = –40°C to 125°C	M3 version only	3.1	3.3	3.5	
Output voltage line regulation	I_O = 200mA, V_{IN} = 5.3V to 25V	non-M3 version only			9	100	mV
		M3 chip version only			28	50	
	I_O = 200mA, V_{IN} = 8V to 25V	non-M3 version only			3	50	
		M3 chip version only			9	20	
Ripple rejection	V_I = 8V to 18V, f = 120Hz	I_O = 100mA, T_J = full range	non-M3 version only	62			dB
		I_O = 100mA, T_J = –40°C to 125°C	M3 version only	57			
		I_O = 300mA	non-M3 version only	62	80		
			M3 version only	56	62		
Output voltage load regulation	V_I = 8V and I_O = 5mA to 500mA	non-M3 version only			20	100	mV
		M3 version only			20	40	
Temperature coefficient of output voltage	I_O = 5mA	T_J = full range	non-M3 version only		–1		mV/°C
		T_J = –40°C to 125°C	M3 version only		–1		
Output noise voltage	f = 10 Hz to 100 kHz, and T_J = 25°C	non-M3 version only			40	200	µV
		M3 version only			80	200	
Dropout voltage		non-M3 version only			2.0		V
		M3 version only			2.0		
Bias current		non-M3 version only			4.5	6	mA
		M3 version only		3.5	4.5	6	
Bias current change	V_I = 8V to 25V, I_O = 200mA	T_J = full range	non-M3 version only			0.8	mA
		T_J = –40°C to 125°C	M3 version only			0.8	
	I_O = 5 mA to 350mA	T_J = full range	non-M3 version only			0.5	
		T_J = –40°C to 125°C	M3 version only			0.5	
Short-circuit output current	V_I = 35V	non-M3 version only			300		mA
	V_I = 30V	M3 version only			400		
Peak output current		non-M3 version only			700		mA
		M3 version only			735		

(1) All characteristics are measured with a 0.33µF capacitor across the input and a 0.1µF capacitor across the output. Thermal effects must be taken into account separately.Pulse-testing techniques maintain T_J as close to T_A as possible. Thermal effects must be taken into account separately.

5.6 Electrical Characteristics: UA78M05Q (Both Legacy and New Chip)

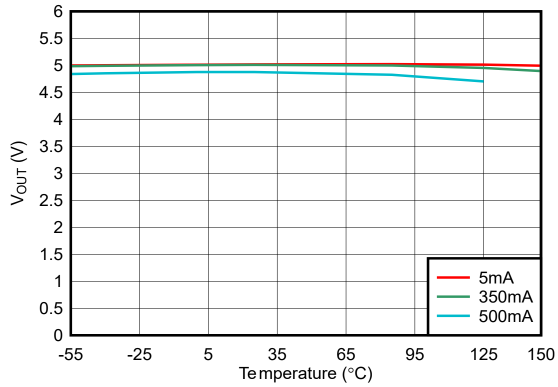
specified at T_J = 25°C, V_I = 10V, C_{IN} = 0.33 µF, C_{OUT} = 0.1µF, and I_O = 350mA (unless otherwise noted)

PARAMETER	TEST CONDITIONS[(1)]			MIN	TYP	MAX	UNIT
Output voltage	V_I = 7V to 20V, and I_O = 5mA to 350mA			4.8	5	5.2	V
		T_J = full range	non-M3 version only	4.75		5.25	
	V_I = 7.2V to 20V, and I_O = 5mA to 350mA	T_J = –40°C to 125°C	M3 version only	4.75		5.25	
Output voltage line regulation	I_O = 200mA, V_{IN} = 7V to 25V	non-M3 version only			3	100	mV
	I_O = 200mA, V_{IN} = 7.2V to 25V	M3 version only			13	30	
	I_O = 200mA, V_{IN} = 8V to 25V	non-M3 version only			1	50	
		M3 version only			13	30	
Ripple rejection	V_I = 8V to 18V, f = 120Hz	I_O = 100mA, T_J = full range	non-M3 version only	62			dB
		I_O = 100mA, T_J = –40°C to 125°C	M3 version only	56			
		I_O = 300mA	non-M3 version only	62	80		
			M3 version only	50	58		
Output voltage load regulation	I_O = 5mA to 500mA	non-M3 version only			20	100	mV
		M3 version only			25	60	
	I_O = 5mA to 200mA	non-M3 version only			10	50	
		M3 version only			5	20	
Temperature coefficient of output voltage	I_O = 5mA	T_J = full range	non-M3 version only		–1		mV/°C
		T_J = –40°C to 125°C	M3 version only		–1		
Output noise voltage	f = 10 Hz to 100 kHz	non-M3 version only			40	200	µV
		M3 version only			120	200	
Dropout voltage		non-M3 version only			2.0		V
		M3 version only			2.0		
Bias current		non-M3 version only			4.5	6	mA
		M3 version only		3.5	4.5	6	
Bias current change	V_I = 8V to 25V, I_O = 200mA	T_J = full range	non-M3 version only			0.8	mA
		T_J = –40°C to 125°C	M3 version only			0.8	
	I_O = 5 mA to 350mA	T_J = full range	non-M3 version only			0.5	
		T_J = –40°C to 125°C	M3 version only			0.5	
Short-circuit output current	V_I = 35V	non-M3 version only			300		mA
	V_I = 30V	M3 version only			400		
Peak output current		non-M3 version only			700		mA
		M3 version only			760		

(1) All characteristics are measured with a 0.33µF capacitor across the input and a 0.1µF capacitor across the output. Thermal effects must be taken into account separately.Pulse-testing techniques maintain T_J as close to T_A as possible. Thermal effects must be taken into account separately.

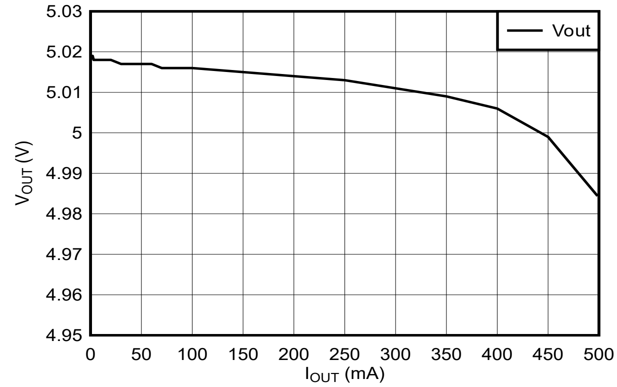
5.7 Typical Characteristics

specified at T_J = 25°C, C_{IN} = 0.33µF, and C_{OUT} = 0.1µF, and I_O = 1mA (unless otherwise noted)



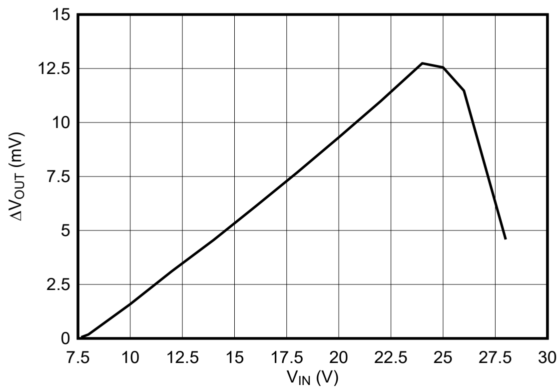
V_{OUT} = 5V, V_{IN} = 10V

Figure 5-1. Output Voltage vs Temperature (M3 version)



V_{OUT} = 5V, V_{IN} = 10V

Figure 5-2. Load Regulation at T_J = 25°C (M3 version)



V_{IN} = 10V, V_{OUT} = 5V, I_{OUT} = 350mA

Figure 5-3. Line Regulation at T_J = 25°C (M3 version)

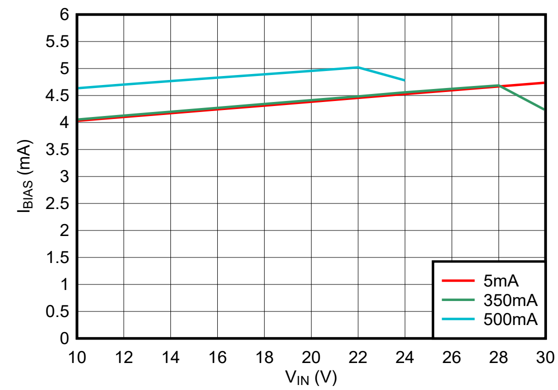
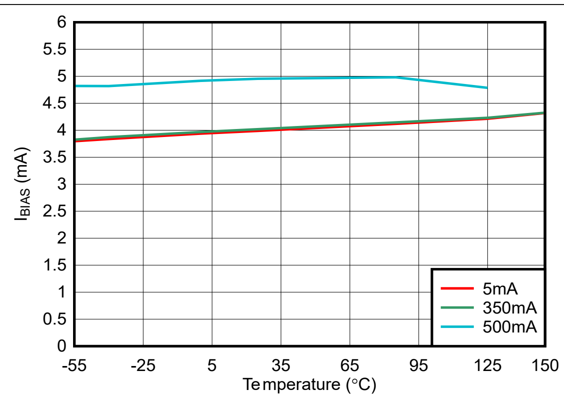
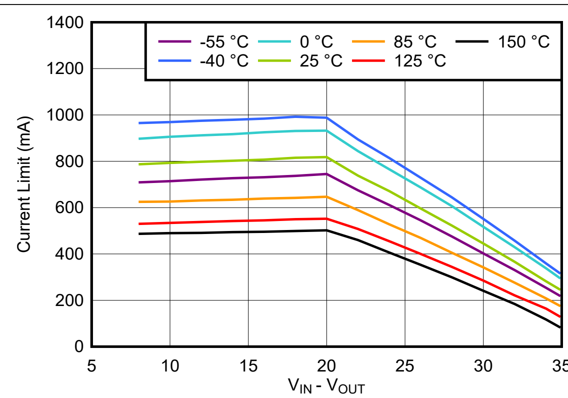


Figure 5-4. Bias Current vs Input Voltage at T_J = 25°C (M3 version)



V_{OUT} = 5V, V_{IN} = 10V

Figure 5-5. Bias Current vs Temperature (M3 version)

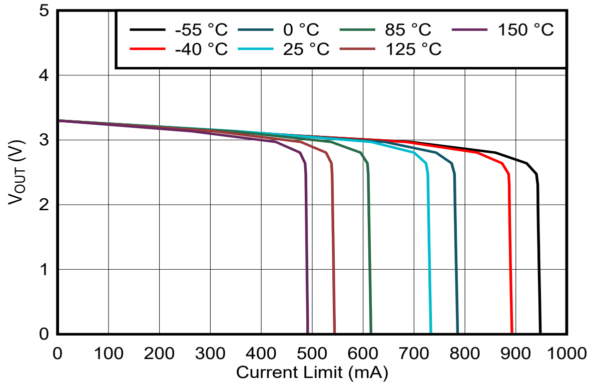


V_{IN} = 10V, V_O = 0V

Figure 5-6. I_{CL} vs Input Voltage (M3 version)

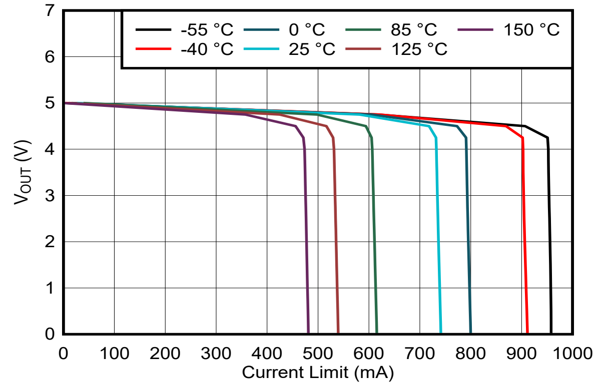
5.7 Typical Characteristics (continued)

specified at T_J = 25°C, C_{IN} = 0.33μF, and C_{OUT} = 0.1μF, and I_O = 1mA (unless otherwise noted)



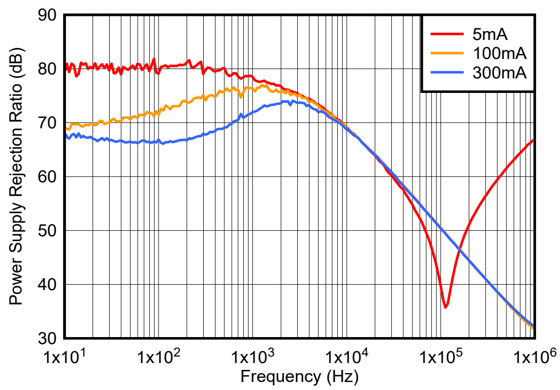
V_{IN} = 8V, V_O = 3.3V

Figure 5-7. Output Voltage vs I_{CL} (M3 version)



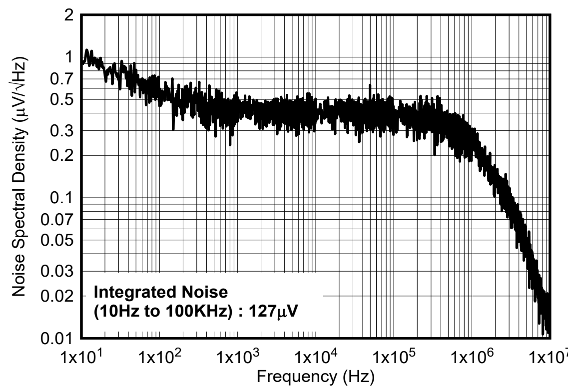
V_{IN} = 10V, V_O = 5V

Figure 5-8. Output Voltage vs I_{CL} (M3 version)



V_I = 13V, V_O = 5V

Figure 5-9. PSRR vs Frequency and I_O (M3 version)



V_{IN} = 10V, V_{OUT} = 5V, I_{OUT} = 100mA, C_{OUT} = 0.1μF

Figure 5-10. Noise vs Frequency (M3 version)

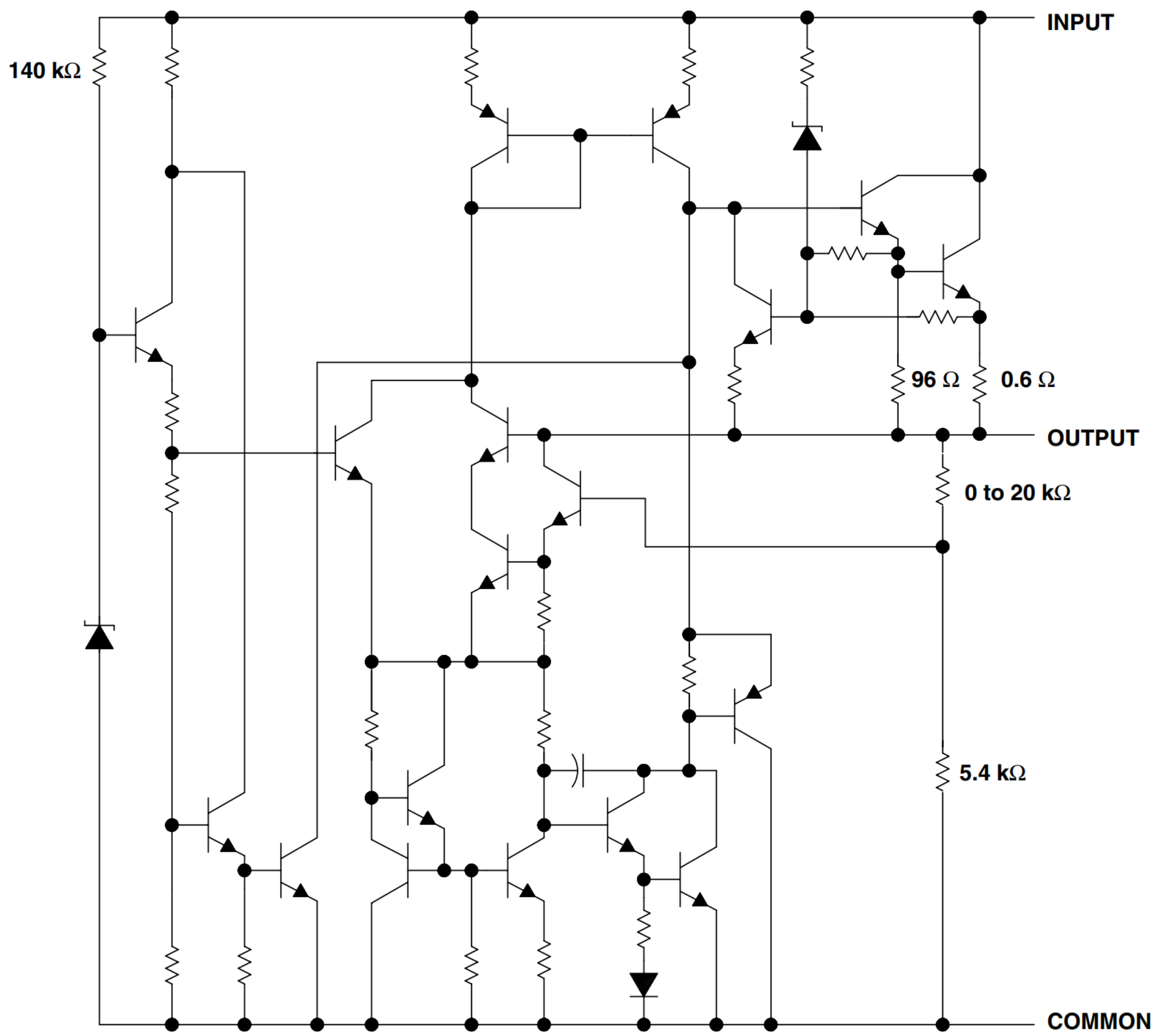
6 Detailed Description

6.1 Overview

The UA78M-Q1 fixed-voltage, integrated-circuit voltage regulator is designed for a wide range of applications. The UA78M-Q1 supports a wide range of input voltages and delivers 500mA of load current.

This device features internal current-limiting and thermal shutdown mechanisms. To provide reliable operation across wide V_I ranges, the current-limiting mechanism modulates the load current capacity. The mechanism monitors the V_O level and the difference between the V_I and V_O voltage levels. The operating ambient temperature range of the device is –40°C to +125°C for all variants.

6.2 Functional Block Diagrams



Resistor values shown are nominal.

Figure 6-1. Functional Block Diagram (Non-M3 Version)

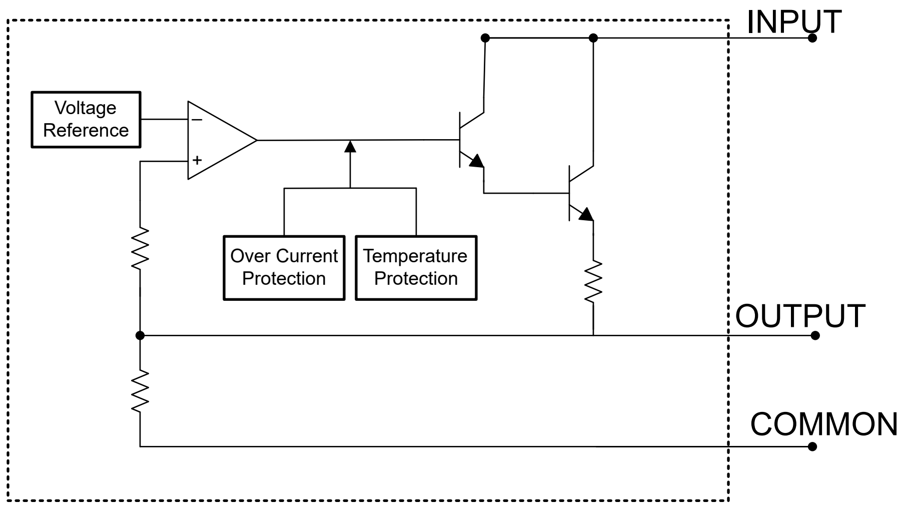


Figure 6-2. Functional Block Diagram (M3 Version)

6.3 Feature Description

6.3.1 Current Limit

The device has an internal current-limit circuit that protects the regulator during transient high-load current faults or shorting events. In a high-load current fault, the current limit scheme limits the output current to the current limit (I_{CL}). I_{CL} is listed in the *Electrical Characteristics* table.

The output voltage is not regulated when the device is in current limit. When a current-limit event occurs, the device begins to heat up because of the increase in power dissipation. When the device is in current limit, the pass transistor dissipates power [(V_I – V_O) × I_{CL}]. For more information on current limits, see the *Know Your Limits* application note.

To achieve a safe operation across a wide range of input voltage, the UA78M-Q1 also has a built-in protection mechanism with current limit. The protection mechanism decreases the current limit as input-to-output voltage increases. This mechanism also keeps the power transistor inside a safe operating region for all values of input-to-output voltage. This protection is designed to provide some output current at all values of input-to-output voltage limits defined in the *Recommended Operating Conditions* table. Figure 6-3 shows the behavior of the current limit variation.

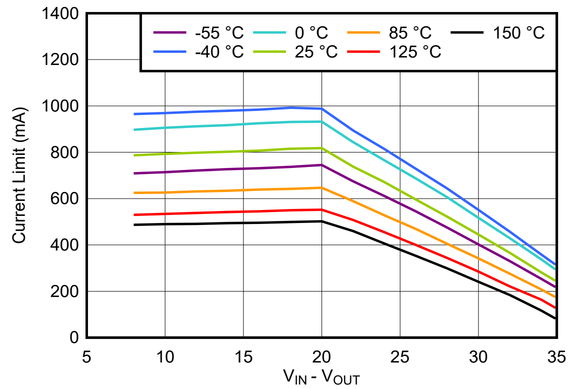


Figure 6-3. Current Limit vs $V_{Head\text{-}room}$ Behavior (M3 version)

6.3.2 Dropout Voltage (V_{DO})

Dropout voltage (V_{DO}) is defined as V_{IN} – V_{OUT} at the rated output current (I_{RATED}), where the pass transistor is fully on. V_{IN} is the input voltage, V_{OUT} is the output voltage, and I_{RATED} is the maximum I_{OUT} listed in the *Recommended Operating Conditions* table. At this operating point, the pass transistor is driven fully on. Dropout voltage indirectly specifies a minimum input voltage greater than the nominal programmed output voltage where the output voltage is expected to stay in regulation. If the input voltage falls to less than the nominal output regulation, then the output voltage falls as well.

6.3.3 Thermal Shutdown

The device contains a thermal shutdown protection circuit to disable the device when the junction temperature (T_J) of the pass transistor rises to $T_{SD(shutdown)}$ (typical). Thermal shutdown hysteresis makes sure that the device resets (turns on) when the temperature falls to $T_{SD(reset)}$ (typical).

The thermal time-constant of the semiconductor die is fairly short. Thus the device cycles on and off when thermal shutdown is reached until power dissipation is reduced. Power dissipation during start-up is high from large V_I – V_O voltage drops across the device or from high inrush currents charging large output capacitors. Under some conditions, the thermal shutdown protection disables the device before start-up completes.

For reliable operation, limit the junction temperature to the maximum listed in the *Section 5.4* table. Operation above this maximum temperature causes the device to exceed operational specifications. Although the device internal protection circuitry is designed to protect against thermal overload conditions, this circuitry is not intended to replace proper heat sinking. Continuously running the device into thermal shutdown or above the maximum recommended junction temperature reduces long-term reliability.

6.4 Device Functional Modes

Table 6-1 provides a quick comparison between the normal and dropout modes of operation.

Table 6-1. Device Functional Mode Comparison

OPERATING MODE	PARAMETER	
	V_I	I_O
Normal	$V_I > V_{OUT(nom)} + V_{DO}$	$I_O < I_{CL}$
Dropout	$V_I < V_{OUT(nom)} + V_{DO}$	$I_O < I_{CL}$

6.4.1 Normal Operation

The device regulates to the nominal output voltage under the following conditions:

- The input voltage is greater than the nominal output voltage plus the dropout voltage ($V_{OUT(nom)} + V_{DO}$)
- The output current is less than the current limit ($I_O < I_{CL}$)
- The device junction temperature is greater than –40°C and less than +125°C

6.4.2 Dropout Operation

If the input voltage is lower than the nominal output voltage plus the specified dropout voltage, but all other conditions are met for normal operation, the device operates in dropout mode. In this mode, the output voltage tracks the input voltage. During this mode, the transient performance of the device becomes significantly degraded because the pass transistor is in the ohmic or triode region, and acts as a switch. Line or load transients in dropout can result in large output voltage deviations.

When the device is in a steady dropout state (defined as when the device is in dropout, $V_I < V_{OUT(NOM)} + V_{DO}$, directly after being in a normal regulation state, but *not* during start up), the pass transistor is driven into the ohmic or triode region. When the input voltage returns to a value greater than or equal to the nominal output voltage plus the dropout voltage ($V_{OUT(NOM)} + V_{DO}$), the output voltage can overshoot for a short period of time while the device pulls the pass transistor back into the linear region.

7 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Application Information

The UA78M-Q1 is designed for use as a linear regulator with only a few external components needed. Use the UA78M-Q1 to clean power-supply noise by attenuating ripple on the input signal. This device is used as a fixed-voltage regulator. Additionally, use this device with external components to obtain adjustable output voltages and currents. This device also functions as the power-pass transistor in precision regulators.

7.2 Typical Application

The UA78M-Q1 is typically used as a fixed-output linear regulator, sourcing current up to 500mA into a load.

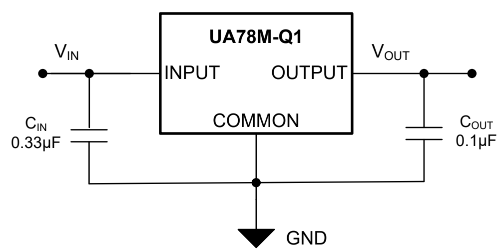


Figure 7-1. Fixed-Output Regulator

7.2.1 Design Requirements

Tie the COMMON pin to ground to set the OUTPUT pin to the desired fixed output voltage.

Although not required, a 0.33µF bypass capacitor is recommended on the input, and a 0.1µF bypass capacitor is recommend on the output.

7.2.2 Detailed Design Procedure

7.2.2.1 Input and Output Capacitor Requirements

Although the input and output capacitors are not required for stability, good analog design practice is to connect a capacitor from INPUT to COMMON and from OUTPUT to COMMON. The input capacitor counteracts reactive input sources and improves transient response, input ripple, and PSRR. Use an input capacitor if the source impedance is more than 0.5Ω. Use a higher value capacitor if large, fast rise-time load or line transients are anticipated or if the device is located several inches from the input power source.

Dynamic performance of the device is improved by using a large output capacitor. Use an output capacitor within the range specified in the *Recommended Operating Conditions* table for stability.

7.2.2.2 Power Dissipation (P_D)

Circuit reliability requires consideration of the device power dissipation, location of the circuit on the PCB, and correct sizing of the thermal plane. Make sure the printed circuit board (PCB) area around the regulator has few or no other heat-generating devices that cause added thermal stress.

To first-order approximation, power dissipation in the regulator depends on the input-to-output voltage difference and load conditions. The following equation calculates power dissipation (P_D).

$$P_D = (V_I - V_O) \times I_O \tag{1}$$

Note

Power dissipation is minimized, and therefore greater efficiency be achieved, by correct selection of the system voltage rails. For the lowest power dissipation, use the minimum input voltage required for correct output regulation.

For devices with a thermal pad, the primary heat conduction path for the device package is through the thermal pad to the PCB. Solder the thermal pad to a copper pad area under the device. This pad area contains an array of plated vias that conduct heat to additional copper planes for increased heat dissipation.

The maximum power dissipation determines the maximum allowable ambient temperature (T_A) for the device. Power dissipation and junction temperature are most often related by the $R_{\theta JA}$ of the combined PCB and device package and the T_A. $R_{\theta JA}$ is the junction-to-ambient thermal resistance and T_A is the temperature of the ambient air. The following equation describes this relationship.

$$T_J = T_A + (R_{\theta JA} \times P_D) \quad (2)$$

Thermal resistance ($R_{\theta JA}$) is highly dependent on the heat-spreading capability built into the particular PCB design, and therefore varies according to the total copper area, copper weight, and location of the planes. The junction-to-ambient thermal resistance listed in the *Thermal Information* table is determined by the JEDEC standard PCB and copper-spreading area. $R_{\theta JA}$ is used as a relative measure of package thermal performance. $R_{\theta JA}$ is improved by 35% to 55% compared to the *Thermal Information* table value with the PCB board layout optimization. See the *An empirical analysis of the impact of board layout on LDO thermal performance* application note.

7.2.2.3 Estimating Junction Temperature

The JEDEC standard now recommends using psi (Ψ) thermal metrics to estimate the linear regulator junction temperatures when in-circuit on a typical PCB board application. These metrics are not thermal resistance parameters and instead offer a practical and relative way to estimate junction temperature. These psi metrics are determined to be significantly independent of the copper area available for heat-spreading. The *Thermal Information* table lists the primary thermal metrics, which are the junction-to-top characterization parameter (ψ_{JT}) and junction-to-board characterization parameter (ψ_{JB}). These parameters provide two methods for calculating the junction temperature (T_J), as described in the following equations. Use the junction-to-top characterization parameter (ψ_{JT}) with the temperature at the center-top of device package (T_T) to calculate the junction temperature. Use the junction-to-board characterization parameter (ψ_{JB}) with the printed circuit board (PCB) surface temperature 1mm from the device package (T_B) to calculate the junction temperature.

$$T_J = T_T + \psi_{JT} \times P_D \quad (3)$$

where:

- P_D is the dissipated power
- T_T is the temperature at the center-top of the device package

$$T_J = T_B + \psi_{JB} \times P_D \quad (4)$$

where:

- T_B is the PCB surface temperature measured 1mm from the device package and centered on the package edge

For detailed information on the thermal metrics and how to use them, see the *Semiconductor and IC Package Thermal Metrics* application note.

7.2.2.4 External Capacitor Requirements

The UA78M-Q1 is designed to be stable without any external component. Multilayer ceramic capacitors have become the industry standard for these types of applications and are recommended, but use good judgment. Ceramic capacitors that employ X7R-, X5R-, and C0G-rated dielectric materials provide relatively good capacitive stability across temperature. Using Y5V-rated capacitors is discouraged because of large variations in capacitance.

Regardless of the ceramic capacitor type selected, the effective capacitance varies with operating voltage and temperature. Generally, expect the effective capacitance to decrease by as much as 50%. The input and output capacitors recommended in the *Recommended Operating Conditions* table account for an effective capacitance of approximately 50% of the nominal value.

7.2.2.5 Overload Recovery

Because the input voltage rises when power is first turned on, the output follows the input, allowing the regulator to start up into very heavy loads. The input-to-output voltage differential is small during start up when the input voltage is rising, allowing the regulator to supply large output currents. With a high input voltage, a problem occurs where removing an output short does not allow the output voltage to recover. Other regulators also exhibit this phenomenon, so the behavior is not unique to the UA78M-Q1.

The problem occurs with a heavy output load when the input voltage is high and the output voltage is low. Common situations occur immediately when removing a short circuit after the input voltage is already turned on. The load line for such a load potentially intersects the output current curve at two points. If this condition happens, there are two stable output operating points for the regulator. With this double intersection, the input power supply is potentially cycled down to zero. Bringing the power supply up again causes the output to recover to the desired voltage operating point.

7.2.2.6 Reverse Current

Excessive reverse current potentially damages this device. Reverse current flows through the emitter-base junction of the pass transistor instead of the normal conducting channel. At high magnitudes, this current flow degrades the long-term reliability of the device.

Conditions where reverse current occur are outlined in this section, all of which exceed the absolute maximum rating of $V_O \leq V_I + 0.7V$. These conditions are:

- If the device has a large C_{OUT} and the input supply collapses with little or no load current
- The output is biased when the input supply is not established
- The output is biased above the input supply

If reverse current flow is expected in the application, use external protection to protect the device. Reverse current is not limited in the device, so external limiting is required if extended reverse voltage operation is anticipated. Limit reverse current to 5% or less of the rated output current of the device in the event this current cannot be avoided.

Figure 7-2 shows one approach for protecting the device.

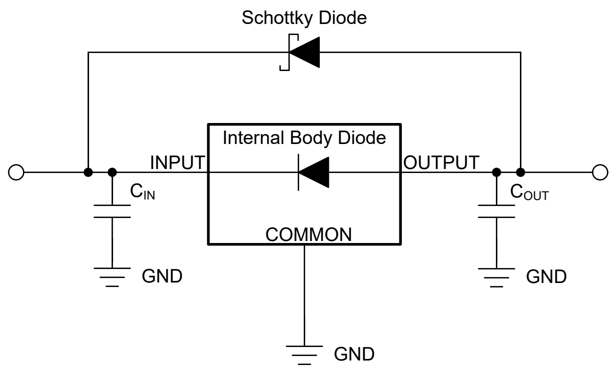


Figure 7-2. Example Circuit for Reverse Current Protection Using a Schottky Diode

7.2.2.7 Polarity Reversal Protection

In many applications, a voltage regulator powers a load that is not connected to ground. Instead, the regulator is connected to a voltage source of the opposite polarity (for example, operational amplifiers, level-shifting circuits, and so on). During start-up and short-circuit events, this connection leads to polarity reversal of the regulator output and potentially damages the internal components of the regulator.

To avoid polarity reversal on the regulator output, use external protection to protect the device.

Figure 7-3 shows one approach for protecting the device.

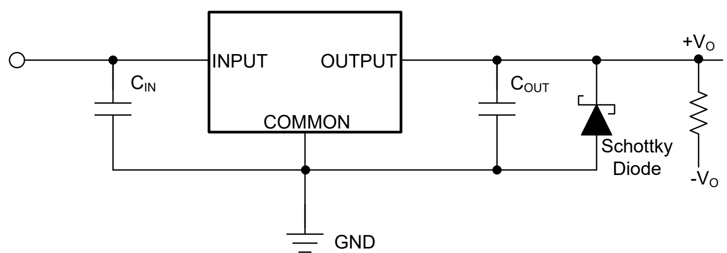
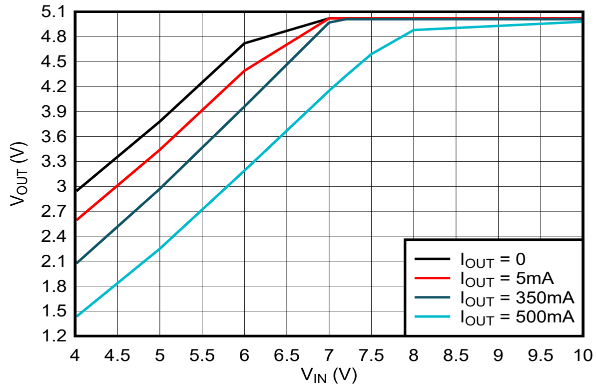


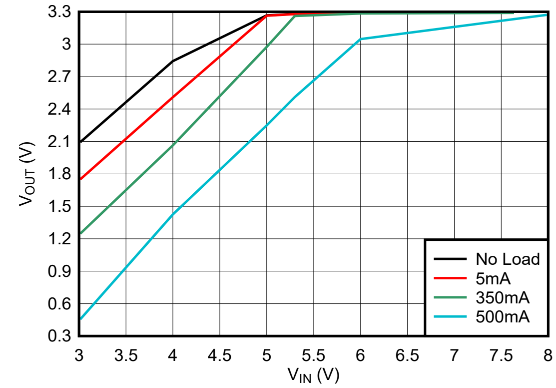
Figure 7-3. Example Circuit for Polarity Reversal Protection Using a Schottky Diode

7.2.3 Application Curves



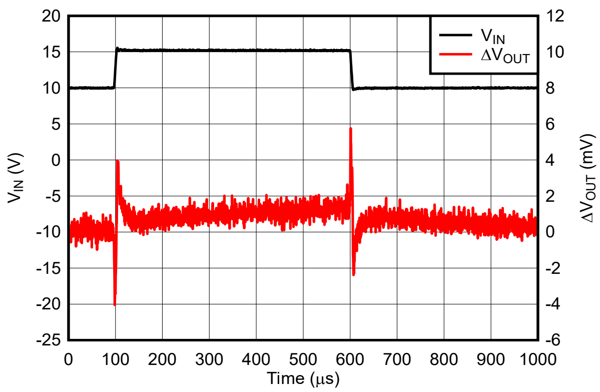
V_{OUT} = 5V

Figure 7-4. V_{IN} vs V_{OUT} at T_J = 25°C (M3 version)



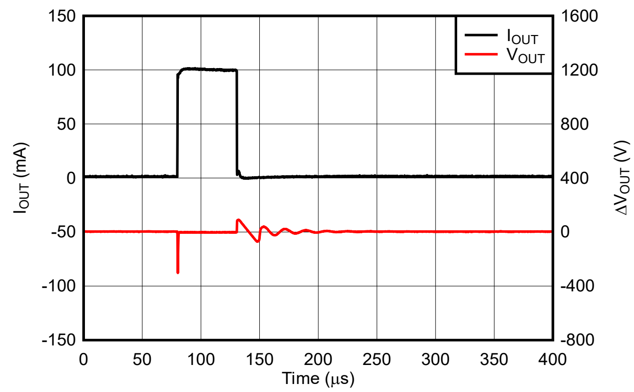
V_{OUT} = 3.3V

Figure 7-5. V_{IN} vs V_{OUT} at T_J = 25°C (M3 version)



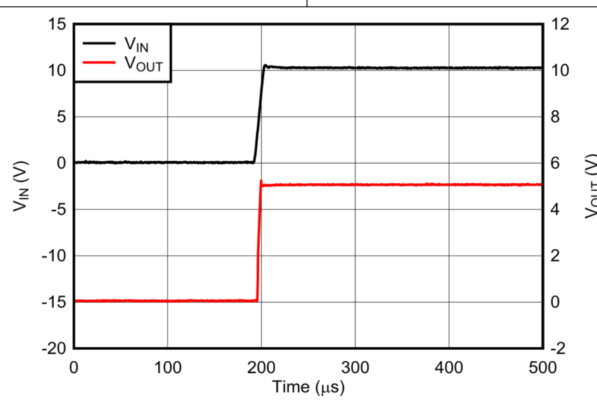
V_O = 5V, dV_{IN}/dt = 1V/µs, I_{OUT} = 350mA, C_{OUT} = 0.1µF

Figure 7-6. Line Transient Behavior (M3 version)



V_{IN} = 10V, V_{OUT} = 5V, I_{OUT} = 1mA to 100mA, dI/dt = 1A/µs, C_{OUT} = 0.1µF

Figure 7-7. Load Transient Behavior (M3 version)



V_{IN} = 0V to 10V, V_{OUT} = 5V, I_{OUT} = 100mA, dV_{IN}/dt = 1V/µs, C_{OUT} = 0.1µF

Figure 7-8. Start-Up (M3 version)

7.3 Power Supply Recommendations

See the *Recommended Operating Conditions* for the recommended power supply voltages for each variation of the UA78M-Q1. Different orderable part numbers are able to tolerate different levels of voltage. Also, place a decoupling capacitor on the output to limit noise on the input.

7.4 Layout

7.4.1 Layout Guidelines

Keep trace widths large enough to eliminate problematic I×R voltage drops at the input and output pins. Place bypass capacitors as close to the UA78M-Q1 as possible. Additional copper and vias connected to ground facilitate additional thermal dissipation, preventing the device from reaching thermal overload.

7.4.2 Layout Example

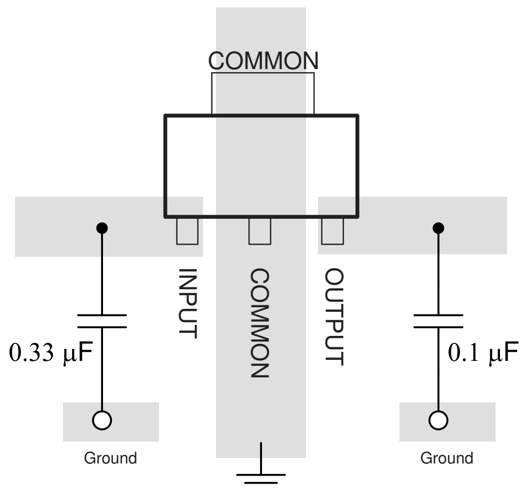


Figure 7-9. Layout Diagram

8 Device and Documentation Support

8.1 Device Support

8.1.1 Development Support

8.1.1.1 Evaluation Module

An evaluation module (EVM) is available to assist in the initial circuit performance evaluation using the UA78L. Request the UA78MEVM (and related user guide) at the Texas Instruments web site through the product folders or purchased directly from the TI eStore.

8.1.2 Device Nomenclature

Table 8-1. Device Nomenclature

PRODUCT[(1)]	DESCRIPTION
UA78M**xx**Q ***yyyz*M3**Q1	**xx** is the nominal output voltage (for example, 05 = 5.0V, 33 = 3.3V). **yyy** is the package designator. **z** is the package quantity. Devices ship with the non-M3 version (CSO: SFB) or the M3 version (CSO: RFB). The reel packaging label provides CSO information to distinguish which chip is used. Device performance for non-M3 and M3 versions is denoted throughout the document. **M3** is the suffix designator only significant for the material with CSO:RFB, which uses the latest manufacturing flow.

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

8.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

8.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

8.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.6 Glossary

TI Glossary This glossary lists and explains terms, acronyms, and definitions.

9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (September 2008) to Revision C (May 2025) **Page**

- Updated the numbering format for tables, figures, and cross-references throughout the document................. 1
- Added *Applications*, *Device Information* table, *Pin Functions* table, *ESD Ratings* table, *Thermal Information* table, *Typical Characteristics*, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section................... 1
- Changed entire document to align with current family format.. 1
- Removed obsolete part information from document...1
- Removed Ordering Information table... 1
- Added M3 devices to document.. 1
- Changed pin names from *IN*, *GND*, and *OUT* to *INPUT*, *COMMON*, and *OUTPUT* throughout document for consistency...1

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
UA78M05QDCYRG4Q1	Active	Production	SOT-223 (DCY) | 4	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	C5Q
UA78M05QDCYRG4Q1.A	Active	Production	SOT-223 (DCY) | 4	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	C5Q
UA78M05QDCYRM3Q1	Active	Production	SOT-223 (DCY) | 4	2500 | NOT REQUIRED	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	C5Q
UA78M05QDCYRQ1	Active	Production	SOT-223 (DCY) | 4	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	C5Q
UA78M33QDCYRG4Q1	Active	Production	SOT-223 (DCY) | 4	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	C3Q
UA78M33QDCYRG4Q1.A	Active	Production	SOT-223 (DCY) | 4	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	C3Q
UA78M33QDCYRM3Q1	Active	Production	SOT-223 (DCY) | 4	2500 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	C3Q

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF UA78M-Q1 :

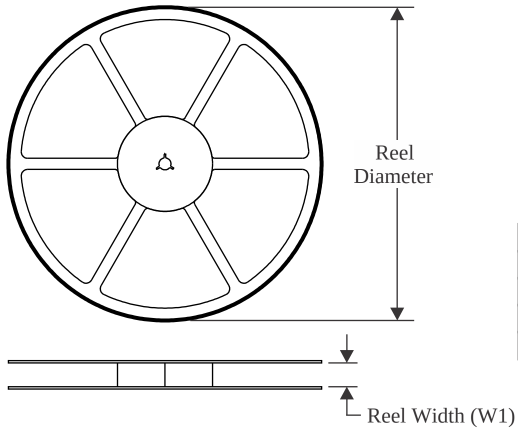
- Catalog : UA78M

NOTE: Qualified Version Definitions:

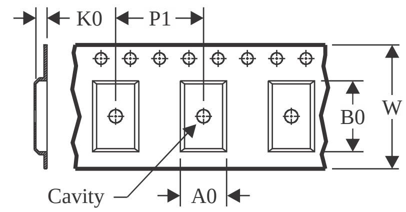
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

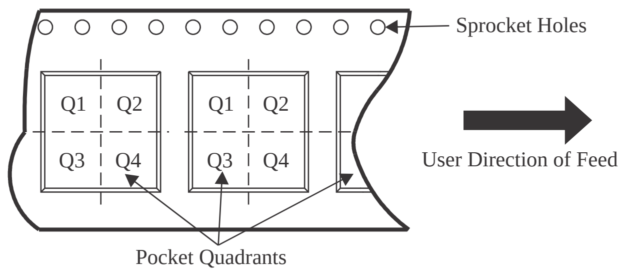


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

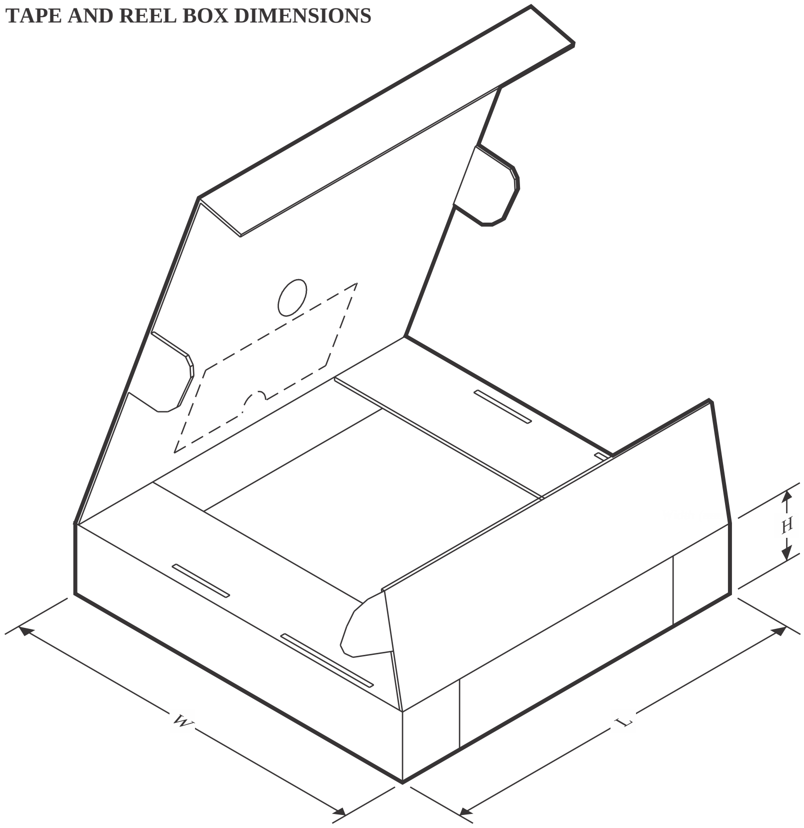
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UA78M05QDCYRG4Q1	SOT-223	DCY	4	2500	330.0	12.4	6.8	7.3	1.88	8.0	12.0	Q3
UA78M33QDCYRG4Q1	SOT-223	DCY	4	2500	330.0	12.4	6.83	7.42	1.88	8.0	12.0	Q3
UA78M33QDCYRM3Q1	SOT-223	DCY	4	2500	330.0	12.4	7.05	7.4	1.9	8.0	12.0	Q3

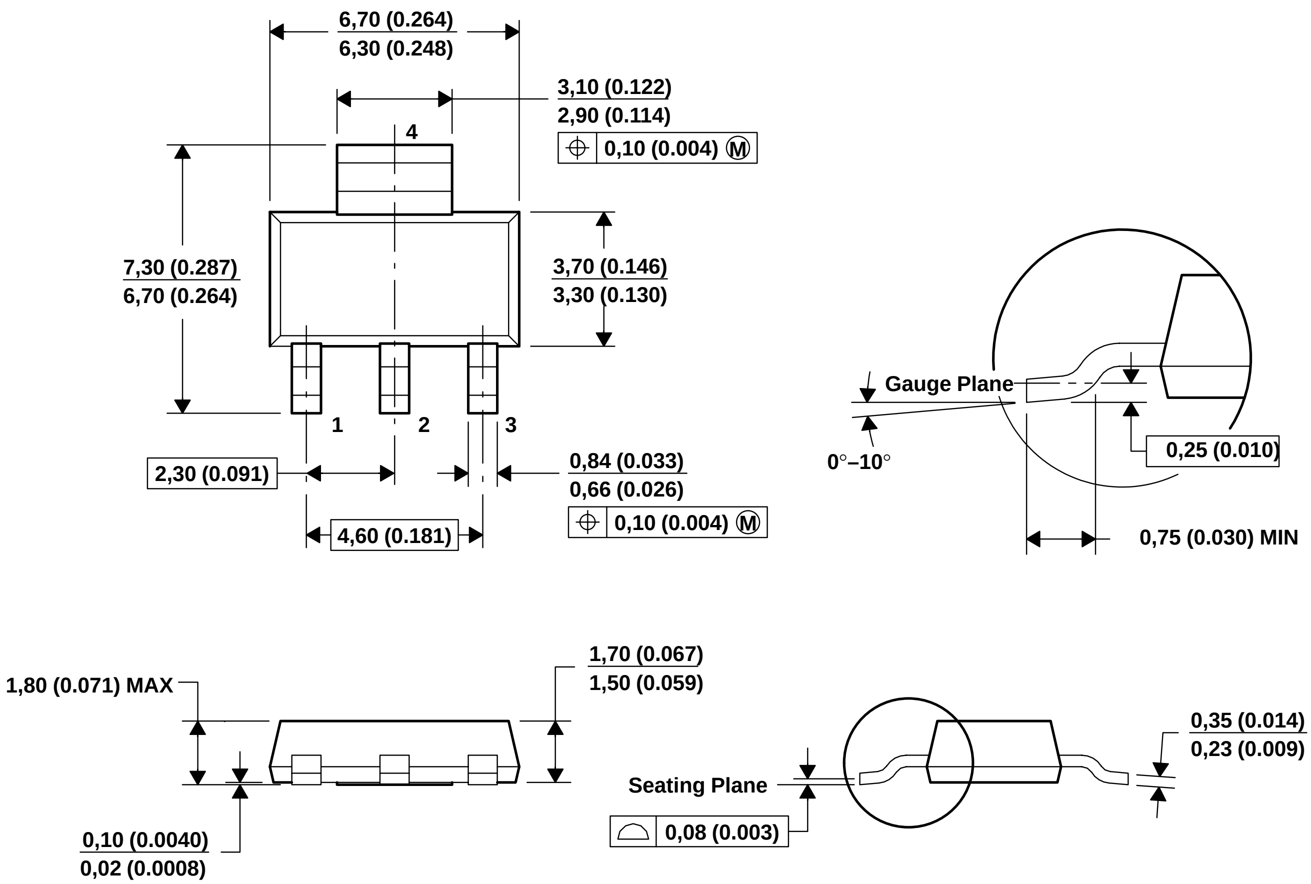
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

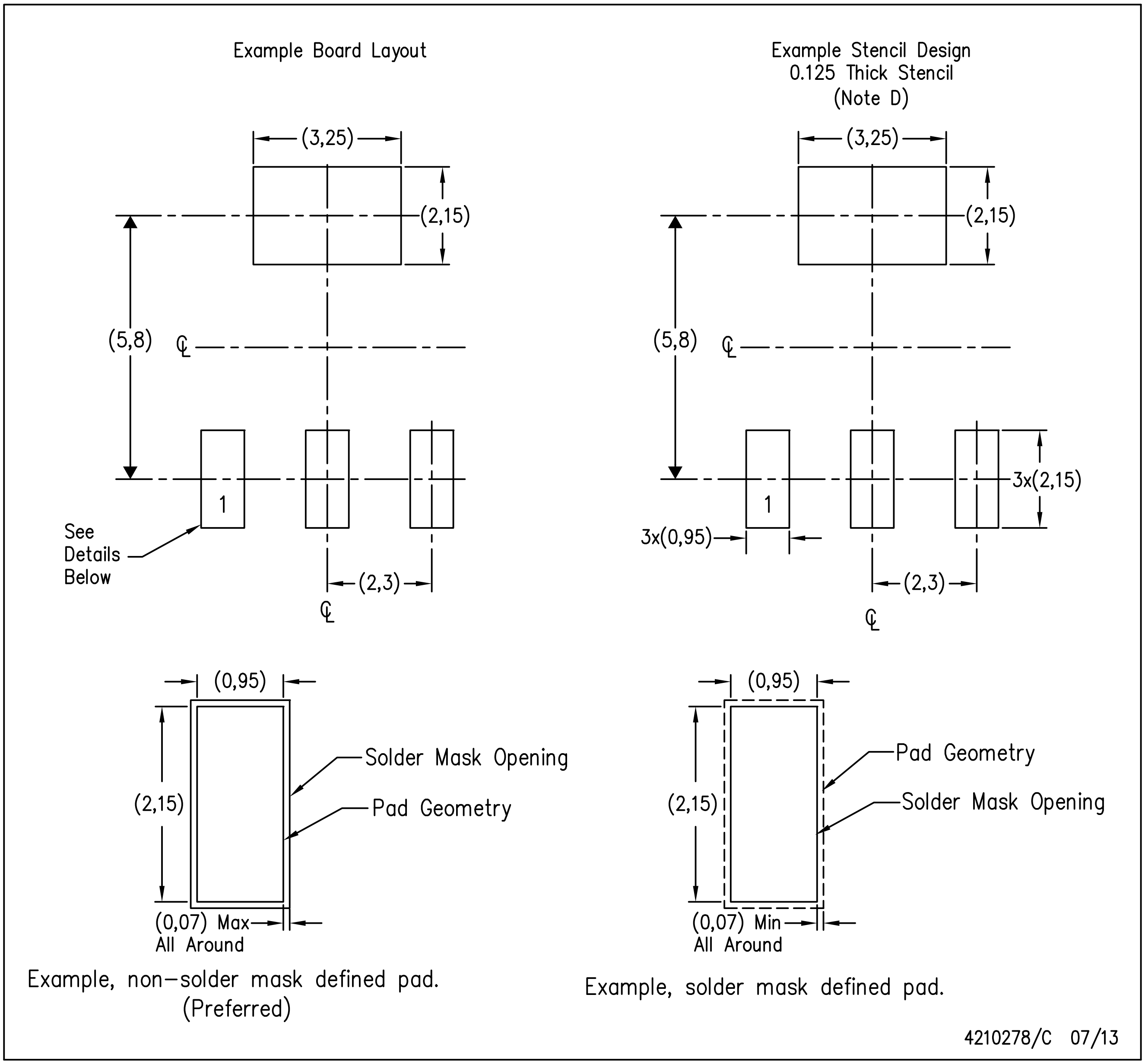
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UA78M05QDCYRG4Q1	SOT-223	DCY	4	2500	346.0	346.0	29.0
UA78M33QDCYRG4Q1	SOT-223	DCY	4	2500	346.0	346.0	29.0
UA78M33QDCYRM3Q1	SOT-223	DCY	4	2500	340.0	340.0	38.0

DCY (R-PDSO-G4) **PLASTIC SMALL-OUTLINE**



NOTES:
A. All linear dimensions are in millimeters (inches).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. Falls within JEDEC TO-261 Variation AA.

DCY (R–PDSO–G4) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil recommendations. Refer to IPC 7525 for stencil design considerations.