TXS0102-Q1 2-Bit Bidirectional Voltage-Level Translator for Open-Drain and Push-Pull Applications

1 Features

- Qualified for Automotive Applications
- AEC-Q100 Qualified With the Following Results:
  - Device Temperature Grade 1: –40°C to +125°C Ambient Operating Temperature Range
  - Device HBM ESD Classification Level 2
  - Device CDM ESD Classification Level C5
- ESD Protection per JESD 22
  - A Port
    - 2500V Human-Body Model (A114-B)
    - 750V Charged-Device Model (C101)
  - B Port
    - 8kV Human-Body Model (A114-B)
    - 750V Charged-Device Model (C101)
- No Direction-Control Signal Required
- Maximum Data Rates
  - 24Mbps Maximum (Push Pull)
  - 2Mbps (Open Drain)
- Available in the Texas Instruments NanoFree™ Package
- 1.65V to 3.6V on A port and 2.3V to 5.5V on B port ($V_{CCA} \leq V_{CCB}$)
- No Power-Supply Sequencing Required—V_{CCA} or V_{CCB} can be Ramped First

2 Applications

- Automotive Infotainment
- Advance Driver-Assistance Systems (ADAS)
- Isolates and Level-Translates Between Main Processor and Peripheral Modules
- I^2C or 1-Wire Voltage-Level Translation

3 Description

The TXS0102-Q1 device connects an incompatible logic communication from chip-to-chip due to voltage mismatch. This auto-direction translator can be conveniently used to bridge the gap without the need of direction control from the host. Each channel can be mixed and matched with different output types (open-drain or push-pull) and mixed data flows (transmit or receive) without intervention from the host. This 2-bit noninverting translator uses two separate configurable power-supply rails. The A and B ports are designed to track V_{CCA} and V_{CCB} respectively. The V_{CCB} pin accepts any supply voltage from 2.3V to 5.5V while the V_{CCA} pin accepts any supply voltage from 1.65V to 3.6V such that V_{CCA} is less than or equal to V_{CCB}. This tracking allows for low-voltage bidirectional translation between any of the 1.8V, 2.5V, 3.3V, and 5V voltage nodes.

When the output-enable (OE) input is low, all outputs are placed in the high-impedance state.

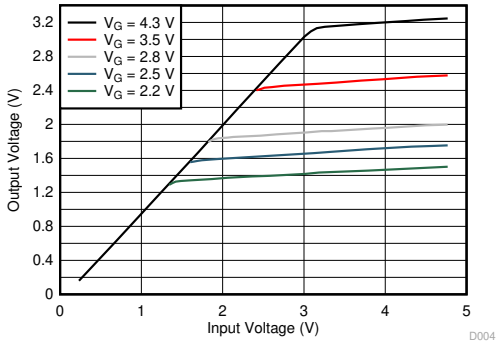
The TXS0102-Q1 device is designed so that the OE input circuit is supplied by V_{CCA}.

To put the device in the high-impedance state during power up or power down, the OE pin must be tied to the GND pin through a pulldown resistor; the minimum value of the resistor is determined by the current-sourcing capability of the driver.

Package Information

PART NUMBER	PACKAGE(1)	PACAKGE SIZE(2)
TXS0102-Q1	DCU (VSSOP, 8)	2mm × 3.1mm

(1) For more information, see Section 12.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Transfer Characteristics of an N-Channel Transistor

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4 Pin Configuration and Functions

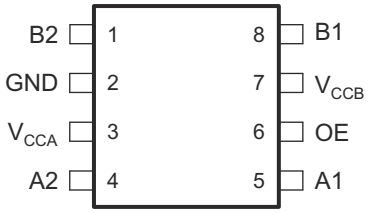


Figure 4-1. DCU Package 8-Pin VSSOP Top View

Table 4-1. Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
A1	5	I/O	Input-output 1 for the A port. This pin is referenced to V_{CCA}.
A2	4	I/O	Input-output 2 for the A port. This pin is referenced to V_{CCA}.
B1	8	I/O	Input-output 1 for the B port. This pin is referenced to V_{CCB}.
B2	1	I/O	Input-output 2 for the B port. This pin is referenced to V_{CCB}.
GND	2	—	Ground
OE	6	I	Tri-state output-mode enable. Pull the OE pin low to place all outputs in tri-state mode. This pin is referenced to V_{CCA}.
V_{CCA}	3	—	A-port supply voltage. 1.65V ≤ V_{CCA} ≤ 3.6V and V_{CCA} ≤ V_{CCB}.
V_{CCB}	7	—	B-port supply voltage. 2.3V ≤ V_{CCB} ≤ 5.5V.

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CCA}	Supply voltage A		–0.5	4.6	V
V_{CCB}	Supply voltage B		–0.5	6.5	V
V_I	Input Voltage(2)	A Port	–0.5	4.6	V
		B Port	–0.5	6.5	
V_O	Voltage applied to any output in the high-impedance or power-off state(2)	A Port	–0.5	4.6	V
		B Port	–0.5	6.5	
V_O	Voltage applied to any output in the high or low state(2) (3)	A Port	–0.5	V_{CCA} + 0.5	V
		B Port	–0.5	V_{CCB} + 0.5	
I_{IK}	Input clamp current	V_I < 0		–50	mA
I_{OK}	Output clamp current	V_O < 0		–50	mA
I_O	Continuous output current			±50	mA
	Continuous current through V_{CC} or GND			±100	mA
T_j	Junction Temperature			150	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Section 5.1* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Section 5.3* Exposure beyond the limits listed in *Section 5.3* may affect device reliability.
(2) The input voltage and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
(3) The output positive-voltage rating may be exceeded up to 6.5V maximum if the output current rating is observed.

5.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002	A Port	±2500	V
			B Port	±8000	
		Charged device model (CDM), per AEC Q100-011	A Port	±750	
			B Port	±750	

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted) (1) (2) (3) (4)

			V_{CCA}	V_{CCB}	MIN	MAX	UNIT
V_{CCA}	Supply voltage A				1.65	3.6	V
V_{CCB}	Supply voltage B				2.3	5.5	V
V_{IH}	High-level input voltage	A-port I/O's	1.65V to 1.95V	2.3V to 5.5V	V_{CCA} - 0.2	V_{CCA}	V
			2.3V to 3.6V	2.3V to 5.5V	V_{CCA} - 0.4	V_{CCA}	
		B-port I/O's	1.65V to 3.6V	2.3V to 5.5V	V_{CCB} - 0.4	V_{CCB}	
		OE Input	1.65V to 3.6V	2.3V to 5.5V	V_{CCA} x 0.65	5.5	
V_{IL}	Low-level input voltage	A-port I/O's	1.65V to 3.6V	2.3V to 5.5V	0	0.15	V
		B-port I/O's	1.65V to 3.6V	2.3V to 5.5V	0	0.15	
		OE Input	1.65V to 3.6V	2.3V to 5.5V	0	V_{CCA} x 0.35	
Δt/Δv	Input transition rise and fall time	A-port I/O's	1.65V to 3.6V	2.3V to 5.5V		10	ns/V
		B-port I/O's	1.65V to 3.6V	2.3V to 5.5V		10	ns/V
		OE Input	1.65V to 3.6V	2.3V to 5.5V		10	ns/V
T_A	Operating free-air temperature				–40	125	°C

(1) V_{CCI} is the V_{CC} associated with the input port.
(2) V_{CCO} is the V_{CC} associated with the output port.
(3) V_{CCA} must be less than or equal to V_{CCB} , and V_{CCA} must not exceed 3.6V.
(4) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application note, Implications of Slow or Floating CMOS Inputs.

5.4 Thermal Information

THERMAL METRIC(1)		TXS0102-Q1 DCU 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	239.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	88.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	151.6	°C/W
Y_{JT}	Junction-to-top characterization parameter	30.9	°C/W
Y_{JB}	Junction-to-board characterization parameter	150.5	°C/W
$R_{\theta JC(bottom)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application note.

5.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)(1) (2) (3)

PARAMETER		TEST CONDITIONS	V_{CCA}	V_{CCB}	Operating free-air temperature (T_A)			UNIT
					–40°C to 125°C			
					MIN	TYP	MAX	
V_{OHA}	Port A output high voltage	I_{OH} = –20uA $V_{IB} \geq V_{CCB}$ - 0.4V	1.65V to 3.6V	2.3V to 5.5V	V_{CCA} x 0.67			V
V_{OLA}	Port A output low voltage	I_{OL} = 1mA $V_{IB} \leq$ 0.15V	1.65V to 3.6V	2.3V to 5.5V			0.4	
V_{OHB}	Port B output high voltage	I_{OH} = –20uA $V_{IB} \geq V_{CCB}$ - 0.4V	1.65V to 3.6V	2.3V to 5.5V	V_{CCB} x 0.67			
V_{OLB}	Port B output low voltage	I_{OL} = 1mA $V_{IB} \leq$ 0.15V	1.65V to 3.6V	2.3V to 5.5V			0.4	
I_I	Input leakage current	OE $V_I = V_{CC}$ or GND	1.65V to 3.6V	2.3V to 5.5V			±2	µA
I_{off}	Partial power down current	A port	0V	0V to 5.5V			±2	
	Partial power down current	B port	0V to 3.6V	0V			±2	
I_{OZ}	Tri-state output current	A or B Port: $V_I = V_{CCI}$ or GND $V_O = V_{CCO}$ or GND OE = GND	1.65V to 3.6V	2.3V to 5.5V	–2		2	µA
I_{CCA}	V_{CCA} supply current	$V_I = V_{CCI}$ or GND I_O = 0	1.65V to V_{CCB}	2.3V to 5.5V			5	µA
I_{CCA}	V_{CCA} supply current	$V_I = V_{CCI}$ or GND I_O = 0	3.6V	0V			2.2	µA
I_{CCA}	V_{CCA} supply current	$V_I = V_{CCI}$ or GND I_O = 0	0V	5.5V	–2			µA
I_{CCB}	V_{CCB} supply current	$V_I = V_{CCI}$ or GND I_O = 0	1.65V to V_{CCB}	2.3V to 5.5V			21	µA
I_{CCB}	V_{CCB} supply current	$V_I = V_{CCI}$ or GND I_O = 0	3.6V	0V	–1			µA
I_{CCB}	V_{CCB} supply current	$V_I = V_{CCI}$ or GND I_O = 0	0V	5.5V			3.5	µA
I_{CCA} + I_{CCB}	Combined supply current	$V_I = V_{CCI}$ or GND I_O = 0	1.65V to V_{CCB}	2.3V to 5.5V			25	µA
C_i	Input Capacitance	OE	3.3V	3.3V			3.5	pF
C_{io}	Input-to-output internal capacitance	A or B port	3.3V	3.3V		10		
C_{io}	Input-to-output internal capacitance	A port	3.3V	3.3V		6.5		pF
C_{io}	Input-to-output internal capacitance	B port	3.3V	3.3V		7.5		

(1) V_{CCI} is the V_{CC} associated with the input port
(2) V_{CCA} must be less than or equal to V_{CCB}, and V_{CCA} must not exceed 3.6V.
(3) V_{CCO} is the V_{CC} associated with the output port

5.6 Switching Characteristics, V_{CCA} = 1.8 ± 0.15V

PARAMETER		FROM	TO	Test Conditions		B-Port Supply Voltage (V_{CCB})									UNIT
						2.5 ± 0.2V			3.3 ± 0.3V			5.0 ± 0.5V			
						MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
t_{PHL}	Propagation Delay (Hight-to-Low)	A	B	Push-Pull	-40°C to 125°C			5.3			5.4			6.8	ns
		A	B	Open-Drain	-40°C to 125°C			8.8			9.6			10	
t_{PLH}	Propagation Delay (Low-to-High)	A	B	Push-Pull	-40°C to 125°C			6.8			7.1			7.5	
		A	B	Open-Drain	-40°C to 125°C			50			40			33	
t_{PHL}	Propagation Delay (Hight-to-Low)	B	A	Push-Pull	-40°C to 125°C			4.4			4.5			4.7	
		B	A	Open-Drain	-40°C to 125°C			5.3			4.4			4	
t_{PLH}	Propagation Delay (Low-to-High)	B	A	Push-Pull	-40°C to 125°C			5.3			4.5			0.5	
		B	A	Open-Drain	-40°C to 125°C			36			26			20	
t_{en}	Enable Time	OE	A or B		-40°C to 125°C			200			250			275	
t_{dis}	Disable Time	OE	A or B		-40°C to 125°C			200			200			200	
t_{rA}	Ouput Rise Time	B	A	Push-Pull	-40°C to 125°C			9.5			9.3			7.6	
		B	A	Open-Drain	-40°C to 125°C	38		165	30		132	22		95	
t_{rB}	Ouput Rise Time	A	B	Push-Pull	-40°C to 125°C			10.8			9.1			7.6	
		A	B	Open-Drain	-40°C to 125°C	34		145	23		106	10		58	
t_{fA}	Output Fall Time	B	A	Push-Pull	-40°C to 125°C			5.9			6			13.3	
		B	A	Open-Drain	-40°C to 125°C			6.9			6.4			6.1	
t_{fB}	Output Fall Time	A	B	Push-Pull	-40°C to 125°C			13.8			16.2			16.2	
		A	B	Open-Drain	-40°C to 125°C			13.8			16.2			16.2	

5.7 Switching Characteristics, V_{CCA} = 2.5 ± 0.2V

PARAMETER		FROM	TO	Test Conditions		B-Port Supply Voltage (V_{CCB})									UNIT
						2.5 ± 0.2V			3.3 ± 0.3V			5.0 ± 0.5V			
						MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
t_{PHL}	Propagation Delay (Hight-to-Low)	A	B	Push-Pull	-40°C to 125°C			3.2			3.7			3.8	ns
		A	B	Open-Drain	-40°C to 125°C			6.3			6			5.8	
t_{PLH}	Propagation Delay (Low-to-High)	A	B	Push-Pull	-40°C to 125°C			3.5			4.1			4.4	
		A	B	Open-Drain	-40°C to 125°C			3.5			4.1			4.4	
t_{PHL}	Propagation Delay (Hight-to-Low)	B	A	Push-Pull	-40°C to 125°C			3			3.6			4.3	
		B	A	Open-Drain	-40°C to 125°C			4.7			4.2			4	
t_{PLH}	Propagation Delay (Low-to-High)	B	A	Push-Pull	-40°C to 125°C			2.5			1.6			1	
		B	A	Open-Drain	-40°C to 125°C			2.5			1.6			1	
t_{en}	Enable Time	OE	A or B		-40°C to 125°C			200			200			250	
t_{dis}	Disable Time	OE	A or B		-40°C to 125°C			200			200			200	
t_{rA}	Ouput Rise Time	B	A	Push-Pull	-40°C to 125°C			7.4			6.6			5.6	
		B	A	Open-Drain	-40°C to 125°C	34		149	28		121	24		89	
t_{rB}	Ouput Rise Time	A	B	Push-Pull	-40°C to 125°C			8.3			7.2			6.1	
		A	B	Open-Drain	-40°C to 125°C	35		151	24		112	12		64	
t_{fA}	Output Fall Time	B	A	Push-Pull	-40°C to 125°C			5.7			5.5			5.3	
		B	A	Open-Drain	-40°C to 125°C			6.9			6.2			5.8	
t_{fB}	Output Fall Time	A	B	Push-Pull	-40°C to 125°C			7.8			6.7			6.6	
		A	B	Open-Drain	-40°C to 125°C			8.8			9.4			10.4	

5.8 Switching Characteristics, V_{CCA} = 3.3 ± 0.3V

PARAMETER		FROM	TO	Test Conditions		B-Port Supply Voltage (V_{CCB})						UNIT
						3.3 ± 0.3V			5.0 ± 0.5V			
						MIN	TYP	MAX	MIN	TYP	MAX	
t_{PHL}	Propagation Delay (Hight-to-Low)	A	B	Push-Pull	-40°C to 125°C			2.4			3.1	ns
		A	B	Open-Drain	-40°C to 125°C			4.2			4.6	
t_{PLH}	Propagation Delay (Low-to-High)	A	B	Push-Pull	-40°C to 125°C			4.2			4.4	
		A	B	Open-Drain	-40°C to 125°C			4.2			4.4	
t_{PHL}	Propagation Delay (Hight-to-Low)	B	A	Push-Pull	-40°C to 125°C			2.5			3.3	
		B	A	Open-Drain	-40°C to 125°C			2.5			3.3	
t_{PLH}	Propagation Delay (Low-to-High)	B	A	Push-Pull	-40°C to 125°C			2.5			2.6	
		B	A	Open-Drain	-40°C to 125°C			2.5			2.6	
t_{en}	Enable Time	OE	A or B		-40°C to 125°C			200			250	
t_{dis}	Disable Time	OE	A or B		-40°C to 125°C			200			200	
t_{rA}	Ouput Rise Time	B	A	Push-Pull	-40°C to 125°C			5.6			4.8	
		B	A	Open-Drain	-40°C to 125°C	25		116	19		85	
t_{rB}	Ouput Rise Time	A	B	Push-Pull	-40°C to 125°C			6.4			7.4	
		A	B	Open-Drain	-40°C to 125°C	26		116	14		72	
t_{fA}	Output Fall Time	B	A	Push-Pull	-40°C to 125°C			5.4			5	
		B	A	Open-Drain	-40°C to 125°C			6.1			5.7	
t_{fB}	Output Fall Time	A	B	Push-Pull	-40°C to 125°C			7.4			7.6	
		A	B	Open-Drain	-40°C to 125°C			7.6			8.3	

5.9 Switching Characteristics: T_{sk}, T_{MAX}

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CCA}	V_{CCB}	Operating free-air temperature (T_A)			UNIT
					-40°C to 125°C			
					MIN	TYP	MAX	
T_{MAX} - Maximum Data Rate	50% Duty Cycle Input One channel switching	Push-Pull Driving	1.8 ± 0.15V	2.5V ± 0.2V			21	Mbps
			1.8 ± 0.15V	3.3V ± 0.3V			22	
			1.8 ± 0.15V	5V ± 0.5V			24	
			2.5V ± 0.2V	2.5V ± 0.2V			20	
			2.5V ± 0.2V	3.3V ± 0.3V			22	
			2.5V ± 0.2V	5V ± 0.5V			24	
			3.3V ± 0.3V	3.3V ± 0.3V			23	
			3.3V ± 0.3V	5V ± 0.5V			24	
		Open-Drain Driving	1.8 ± 0.15V	1.8 ± 0.15V			2	
			1.8 ± 0.15V	2.5V ± 0.2V			2	
			1.8 ± 0.15V	3.3V ± 0.3V			2	
			1.8 ± 0.15V	5V ± 0.5V			2	
			2.5V ± 0.2V	2.5V ± 0.2V			2	
			2.5V ± 0.2V	3.3V ± 0.3V			2	
			2.5V ± 0.2V	5V ± 0.5V			2	
			3.3V ± 0.3V	3.3V ± 0.3V			2	
			3.3V ± 0.3V	5V ± 0.5V			2	

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CCA}	V_{CCB}	Operating free-air temperature (T_A) -40°C to 125°C			UNIT
					MIN	TYP	MAX	
t_w	Pulse Duration, Data Inputs	Push-Pull Driving	1.65V to 3.6V	2.3V to 5.5V	20			ns
		Open-Drain Driving	1.65V to 3.6V	2.3V to 5.5V	500			
t_{sk} - Output skew	Skew between any two outputs of the same package switching in the same direction	Push-Pull Driving	1.65V to 3.6V	2.3V to 5.5V			1	ns
		Open-Drain Driving	1.65V to 3.6V	2.3V to 5.5V			1	

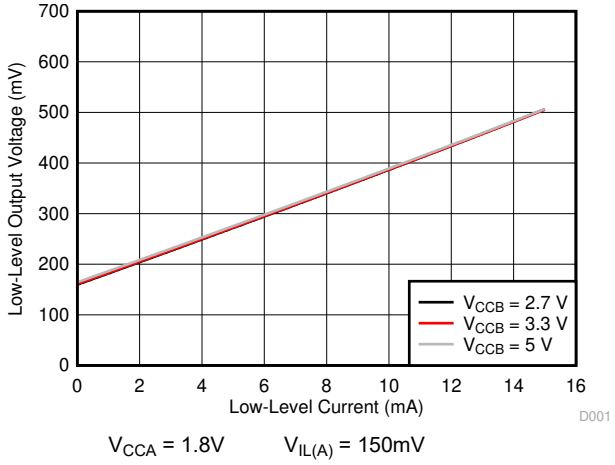
5.10 Operating Characteristics: V_{CCA} = 1.5V to 3.3V, V_{CCB} = 1.5V to 3.3V

T_A = 25°C (1)

PARAMETER		Test Conditions	Supply Voltage (V_{CCA} = V_{CCB} ,unless otherwise noted)			UNIT
			1.8 ± 0.15V	2.5 ± 0.2V	3.3 ± 0.3V	
			TYP	TYP	TYP	
C_{pdA} (2)	A-port input, B-port output to B: outputs enabled	A Port CL = 0, RL = Open f = 10MHz t_{rise} = t_{fall} = 1ns	4.1	4.2	4.7	pF
	B-port input, A-port output to B: outputs enabled		9.0	7.3	7.8	
C_{pdB} (3)	A-port input, B-port output to B: outputs enabled		11.0	9.9	9.2	
	B-port input, A-port output to B: outputs enabled		5.6	7.1	7.4	
C_{pdA} (2)	A-port input, B-port output to B: outputs disabled	B Port CL = 0, RL = Open f = 10MHz t_{rise} = t_{fall} = 1ns	0.1	0.1	0.1	pF
	B-port input, A-port output to B: outputs disabled		0.1	0.1	0.1	
C_{pdB} (3)	A-port input, B-port output to B: outputs disabled		0.2	0.2	0.2	
	B-port input, A-port output to B: outputs disabled		0.2	0.2	0.18	

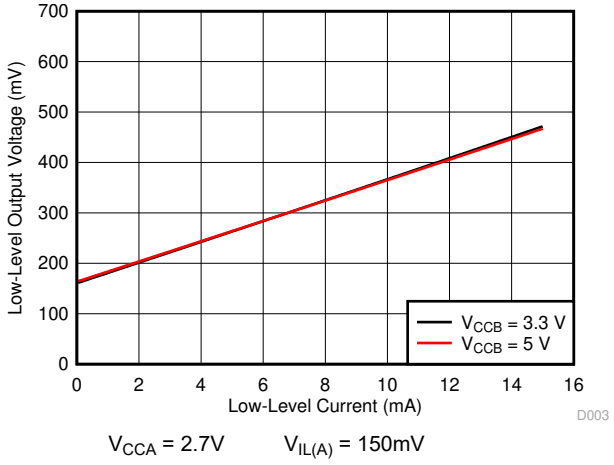
(1) For additional information about how power dissipation capacitance affects power consumption, see the CMOS Power Consumption and C_{pd} Calculation application note
(2) A-Port power dissipation capacitance per transceiver
(3) B-Port power dissipation capacitance per transceiver

6 Typical Characteristics



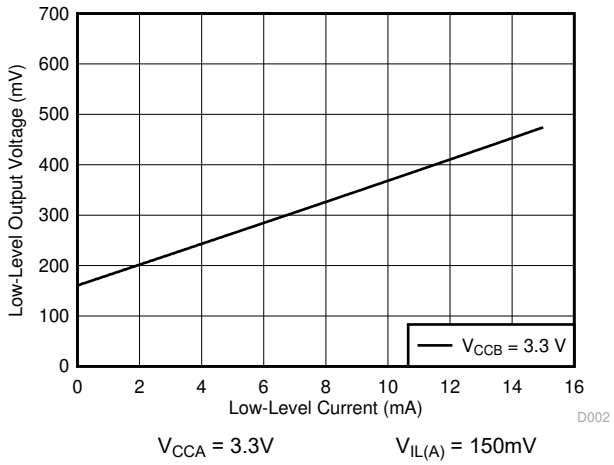
V_{CCA} = 1.8V $V_{IL(A)}$ = 150mV

Figure 6-1. Low-Level Output Voltage ($V_{OL(Bx)}$) vs Low-Level Current ($I_{OL(Bx)}$)



V_{CCA} = 2.7V $V_{IL(A)}$ = 150mV

Figure 6-2. Low-Level Output Voltage ($V_{OL(Bx)}$) vs Low-Level Current ($I_{OL(Bx)}$)



V_{CCA} = 3.3V $V_{IL(A)}$ = 150mV

Figure 6-3. Low-Level Output Voltage ($V_{OL(Bx)}$) vs Low-Level Current ($I_{OL(Bx)}$)

7 Parameter Measurement Information

7.1 Load Circuits

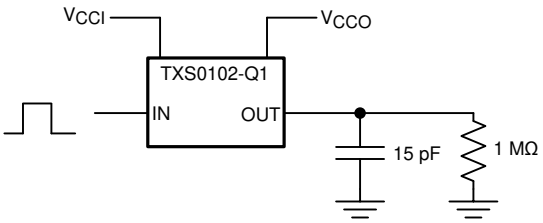


Figure 7-1. Data Rate, Pulse Duration, Propagation Delay, Output Rise-Time and Fall-Time Measurement Using a Push-Pull Driver

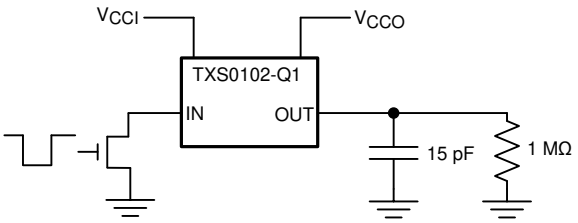
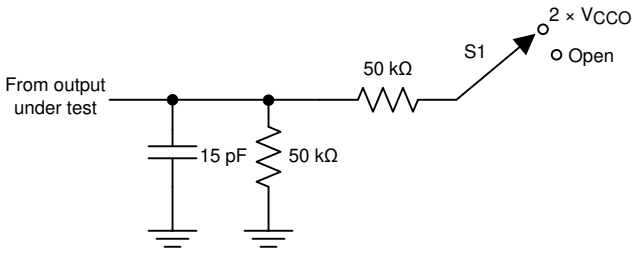


Figure 7-2. Data Rate, Pulse Duration, Propagation Delay, Output Rise-Time and Fall-Time Measurement Using an Open-Drain Driver



TEST	S1
t_{PZL} / t_{PLZ} (t_{dis})	2 × V_{CCO}
t_{PHZ} / t_{PZH} (t_{en})	Open

Figure 7-3. Load Circuit for Enable-Time and Disable-Time Measurement

1. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
2. t_{PZL} and t_{PZH} are the same as t_{en}.
3. V_{CCI} is the V_{CC} associated with the input port.
4. V_{CCO} is the V_{CC} associated with the output port.

7.2 Voltage Waveforms

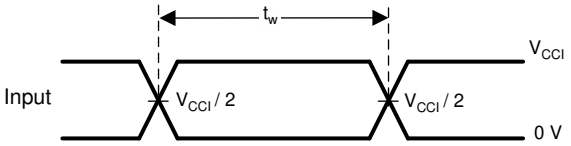


Figure 7-4. Pulse Duration

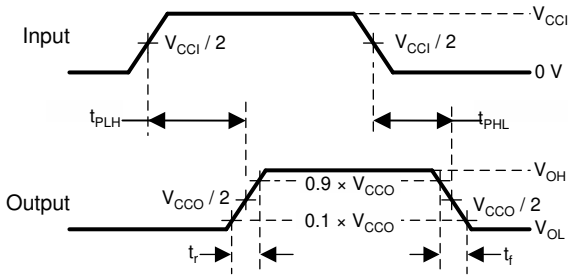


Figure 7-5. Propagation Delay Times

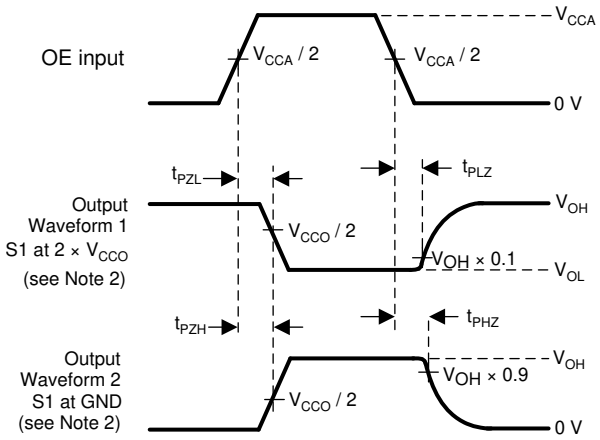


Figure 7-6. Enable and Disable Times

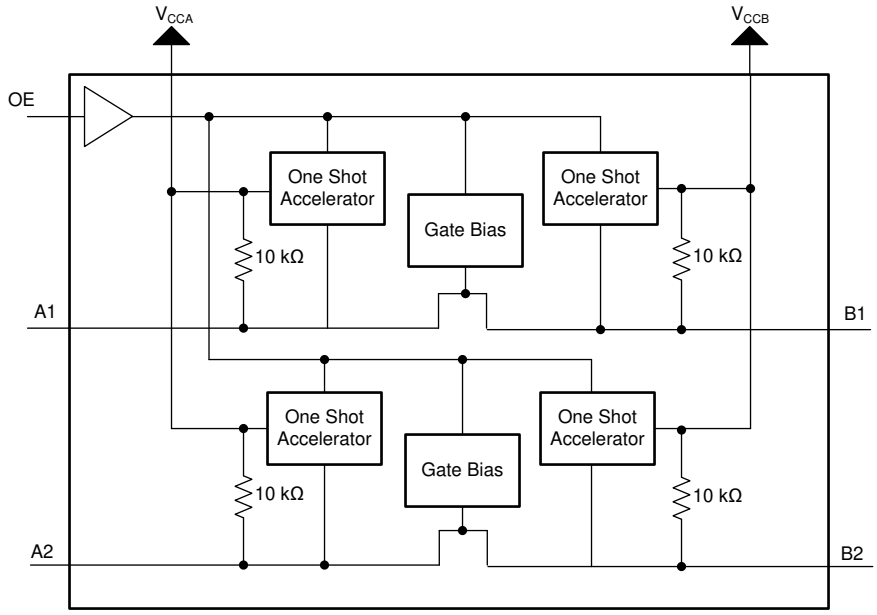
1. C_L includes probe and jig capacitance.
2. Waveform 1 in Figure 7-6 is for an output with internal such that the output is high, except when OE is high (see Figure 7-3). Waveform 2 in Figure 7-6 is for an output with conditions such that the output is low, except when OE is high.
3. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10MHz, Z_O = 50Ω, dv/dt ≥ 1V/ns.
4. The outputs are measured one at a time, with one transition per measurement.
5. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
6. t_{PZL} and t_{PZH} are the same as t_{en}.
7. t_{PLH} and t_{PHL} are the same as t_{pd}.
8. V_{CCI} is the V_{CC} associated with the input port.
9. V_{CCO} is the V_{CC} associated with the output port.

8 Detailed Description

8.1 Overview

The TXS0102-Q1 device is a directionless voltage-level translator specifically designed for translating logic voltage levels. The A port is able to accept I/O voltages ranging from 1.65V to 3.6V, while the B port can accept I/O voltages from 2.3V to 5.5V. The device is a pass gate architecture with edge rate accelerators (one shots) to improve the overall data rate. 10kΩ pullup resistors, commonly used in open drain applications, have been conveniently integrated so that an external resistor is not needed. While this device is designed for open drain applications, the device can also translate push-pull CMOS logic outputs.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Architecture

The TXS0102-Q1 architecture (see Figure 8-1) does not require a direction-control signal in order to control the direction of data flow from A to B or from B to A.

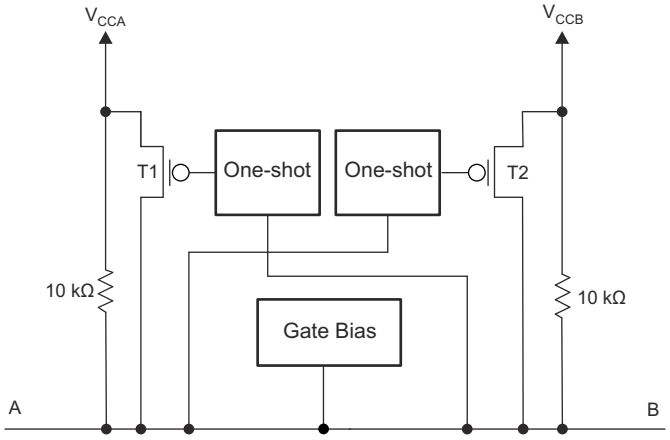


Figure 8-1. Architecture of a TXS01xx Cell

Each A-port I/O has an internal 10kΩ pullup resistor to V_{CCA}, and each B-port I/O has an internal 10kΩ pullup resistor to V_{CCB}. The output one-shots detect rising edges on the A or B ports. During a rising edge, the one-shot turns on the PMOS transistors (T1, T2) for a short duration which speeds up the low-to-high transition.

8.3.2 Input Driver Requirements

The fall time (t_{fA}, t_{fB}) of a signal depends on the output impedance of the external device driving the data I/Os of the TXS0102-Q1 device. Similarly, the t_{PHL} and maximum data rates also depend on the output impedance of the external driver. The values for t_{fA}, t_{fB}, t_{PHL}, and maximum data rates in the data sheet assume that the output impedance of the external driver is less than 50Ω.

8.3.3 Power Up

During operation, assure that $V_{CCA} \leq V_{CCB}$ at all times. During power-up sequencing, $V_{CCA} \geq V_{CCB}$ does not damage the device, so any power supply can be ramped up first.

8.3.4 Enable and Disable

The TXS0102-Q1 device has an OE input that disables the device by setting OE low, which places all I/Os in the high-impedance state. The disable time (t_{dis}) indicates the delay between the time when the OE pin goes low and when the outputs actually enter the high-impedance state. The enable time (t_{en}) indicates the amount of time the user must allow for the one-shot circuitry to become operational after the OE pin is taken high.

8.3.5 Pullup and Pulldown Resistors on I/O Lines

Each A-port I/O has an internal 10kΩ pullup resistor to V_{CCA}, and each B-port I/O has an internal 10kΩ pullup resistor to V_{CCB}. If a smaller value of pullup resistor is required, an external resistor must be added from the I/O to V_{CCA} or V_{CCB} (in parallel with the internal 10kΩ resistors).

8.4 Device Functional Modes

The TXS0102-Q1 device has two functional modes, enabled and disabled. To disable the device set the OE input low, which places all I/Os in a high impedance state. Setting the OE input high will enable the device.

9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The TXS0102-Q1 device can be used in level-translation applications for interfacing devices or systems operating at different interface voltages with one another. The TXS0102-Q1 device is ideal for use in applications where an open-drain driver is connected to the data I/Os.

9.2 Typical Application

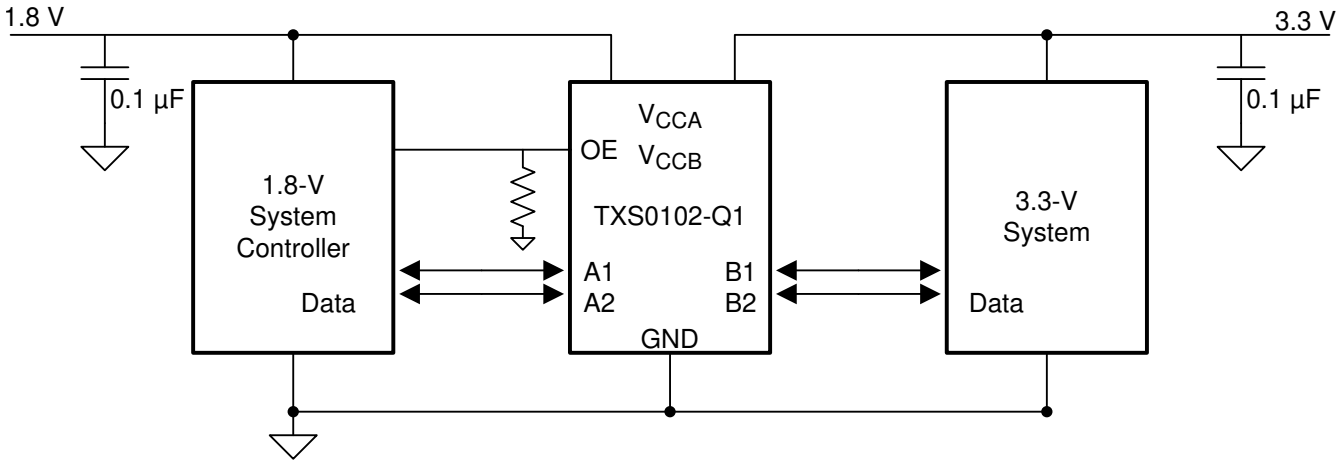


Figure 9-1. Application Schematic

9.2.1 Design Requirements

For this design example, use the parameters listed in Table 9-1.

Table 9-1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage range	1.65 to 3.6V
Output voltage range	2.3 to 5.5V

9.2.2 Detailed Design Procedure

To begin the design process, determine the following:

- Input voltage range
  - Use the supply voltage of the device that is driving the TXS0102-Q1 device to determine the input voltage range. For a valid logic high the value must exceed the V_{IH} of the input port. For a valid logic low the value must be less than the V_{IL} of the input port.
- Output voltage range
  - Use the supply voltage of the device that the TXS0102-Q1 device is driving to determine the output voltage range.
  - The TXS0102-Q1 device has 10kΩ internal pullup resistors. External pullup resistors can be added to reduce the total RC of a signal trace if necessary.

- An external pull down resistor decreases the output V_{OH} and V_{OL}. Use Equation 1 to calculate the V_{OH} as a result of an external pull down resistor.

$$V_{OH} = V_{CCx} \times R_{PD} / (R_{PD} + 10kq) \quad (1)$$

where

- V_{CCx} is the supply voltage on either V_{CCA} or V_{CCB}
- R_{PD} is the value of the external pull down resistor

9.2.3 Application Curve

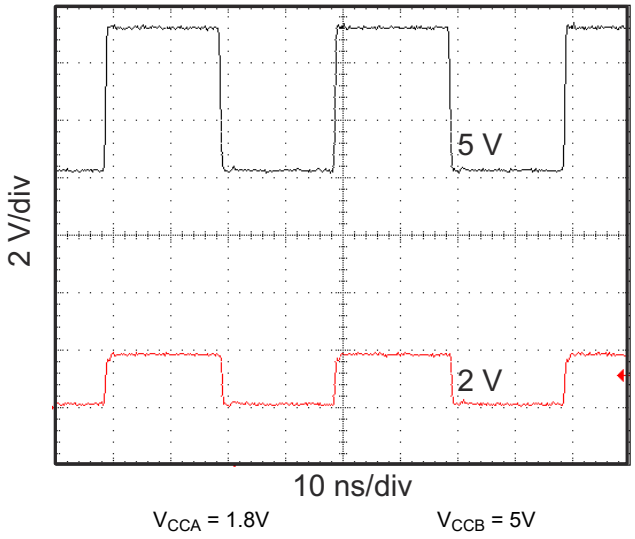


Figure 9-2. Level-Translation of a 2.5MHz Signal

9.3 Power Supply Recommendations

The TXS0102-Q1 device uses two separate configurable power-supply rails, V_{CCA} and V_{CCB}. V_{CCB} accepts any supply voltage from 2.3V to 5.5V and V_{CCA} accepts any supply voltage from 1.65V to 3.6V as long as V_{CCA} is less than or equal to V_{CCB}. The A port and B port are designed to track V_{CCA} and V_{CCB} respectively allowing for low-voltage bidirectional translation between any of the 1.8V, 2.5V, 3.3V, and 5V voltage nodes.

The TXS0102-Q1 device does not require power sequencing between V_{CCA} and V_{CCB} during power-up so the power-supply rails can be ramped in any order. A V_{CCA} value greater than or equal to V_{CCB} ($V_{CCA} \geq V_{CCB}$) does not damage the device, but during operation, V_{CCA} must be less than or equal to V_{CCB} ($V_{CCA} \leq V_{CCB}$) at all times.

The output-enable (OE) input circuit is designed so that it is supplied by V_{CCA} and when the (OE) input is low, all outputs are placed in the high-impedance state. To assure the high-impedance state of the outputs during power up or power down, the OE input pin must be tied to GND through a pulldown resistor and must not be enabled until V_{CCA} and V_{CCB} are fully ramped and stable. The minimum value of the pulldown resistor to ground is determined by the current-sourcing capability of the driver.

9.4 Layout

9.4.1 Layout Guidelines

To assure reliability of the device, following common printed-circuit board layout guidelines is recommended.

- Bypass capacitors should be used on power supplies.
- Short trace lengths should be used to avoid excessive loading.

- PCB signal trace-lengths must be kept short enough so that the round-trip delay of any reflection is less than the one shot duration, approximately 30ns, assuring that any reflection encounters low impedance at the source driver.
- To help adjust rise and fall times of signals depending on system requirements, place pads on the signal paths for loading capacitors or pullup resistors.

9.4.2 Layout Example

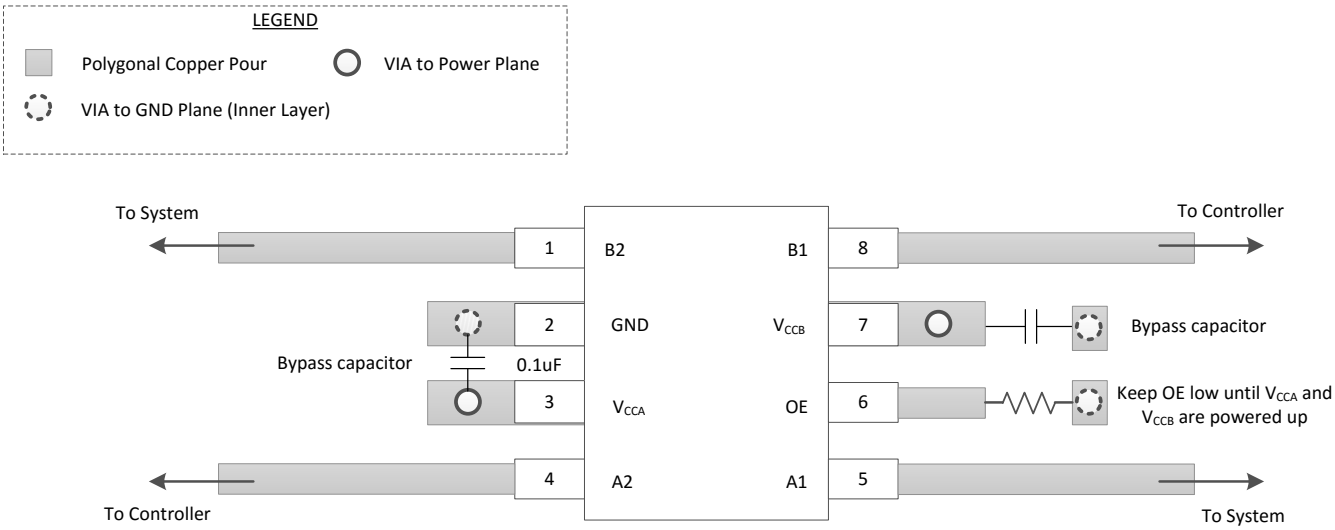


Figure 9-3. TXS0102-Q1 Layout Example

10 Device and Documentation Support

10.1 Documentation Support

10.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

10.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

10.4 Trademarks

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10.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

11 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (September 2017) to Revision B (August 2025)	Page
• Updated the numbering format for tables, figures, and cross-references throughout the document	1
• Updated 4-bit to 2-bit throughout the data sheet	1
• Updated thermals for all packages	4
• Updated degradation of ICCA/ ICCB	5

Changes from Revision * (May 2014) to Revision A (September 2017)	Page
• Changed *Functional Block Diagram* with new figure	13
• Changed *TXS0102-Q1 Layout Example* with new figure	17
• Added *Documentation Support*, *Receiving Notification of Documentation Updates* and *Community Resources*	18

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TXS0102QDCURQ1	Active	Production	VSSOP (DCU) | 8	3000 | LARGE T&R	Yes	NIPDAU | NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	(35TT, NG3R)
TXS0102QDCURQ1.A	Active	Production	null (null) |	3000 | LARGE T&R	-	NIPDAUAG	Level-2-260C-1 YEAR	See TXS0102QDCURQ1	(35TT, NG3R)
TXS0102QDCURQ1.B	Active	Production	null (null) |	3000 | LARGE T&R	-	NIPDAUAG	Level-2-260C-1 YEAR	See TXS0102QDCURQ1	(35TT, NG3R)

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

OTHER QUALIFIED VERSIONS OF TXS0102-Q1 :

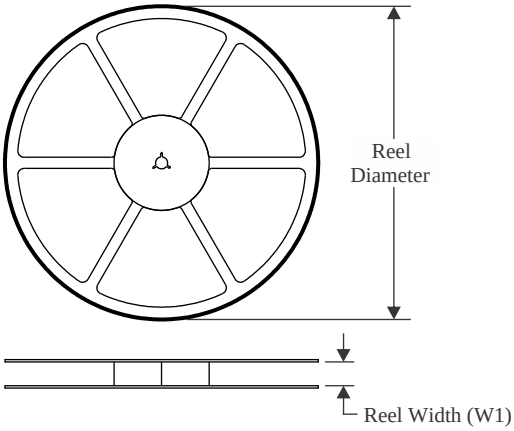
- Catalog : TXS0102

NOTE: Qualified Version Definitions:

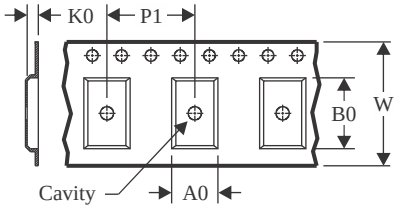
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

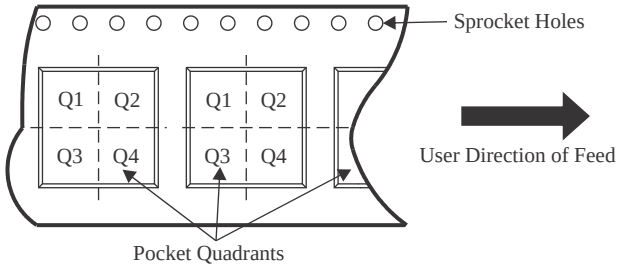


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

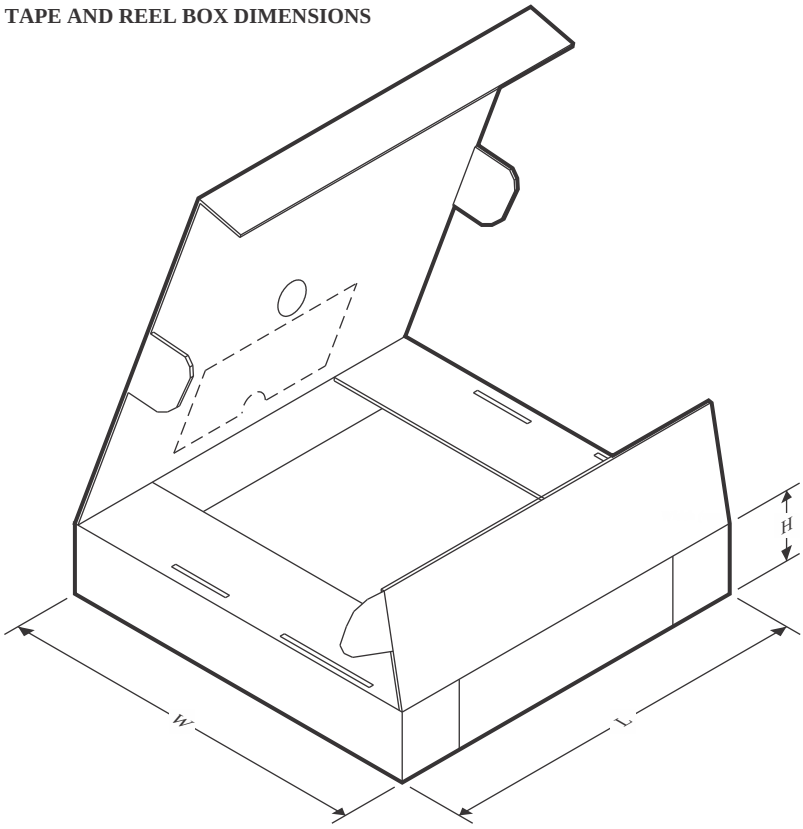
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TXS0102QDCURQ1	VSSOP	DCU	8	3000	180.0	8.4	2.25	3.35	1.05	4.0	8.0	Q3
TXS0102QDCURQ1	VSSOP	DCU	8	3000	178.0	9.0	2.25	3.35	1.05	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

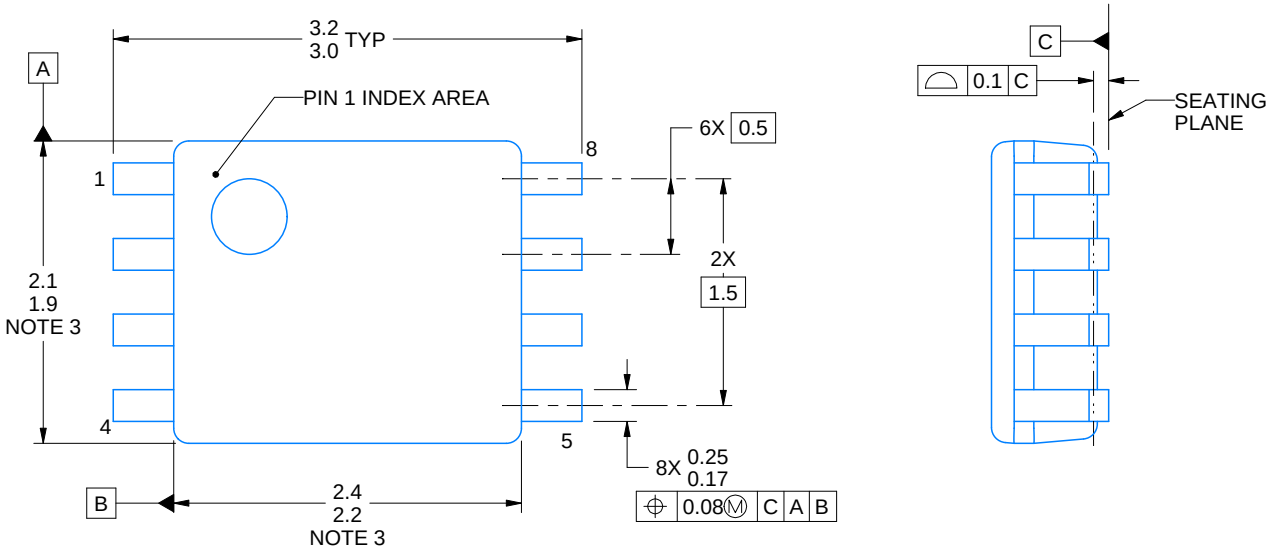
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TXS0102QDCURQ1	VSSOP	DCU	8	3000	213.0	191.0	35.0
TXS0102QDCURQ1	VSSOP	DCU	8	3000	180.0	180.0	18.0

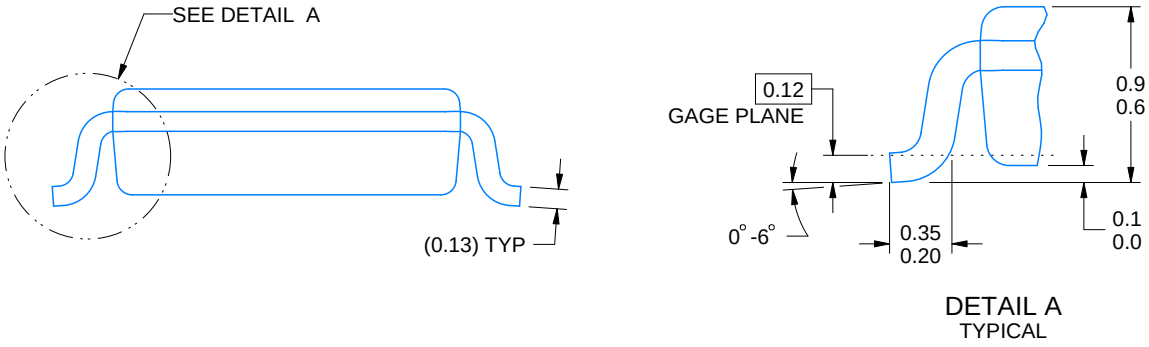
DCU0008A

PACKAGE OUTLINE

VSSOP - 0.9 mm max height

SMALL OUTLINE PACKAGE

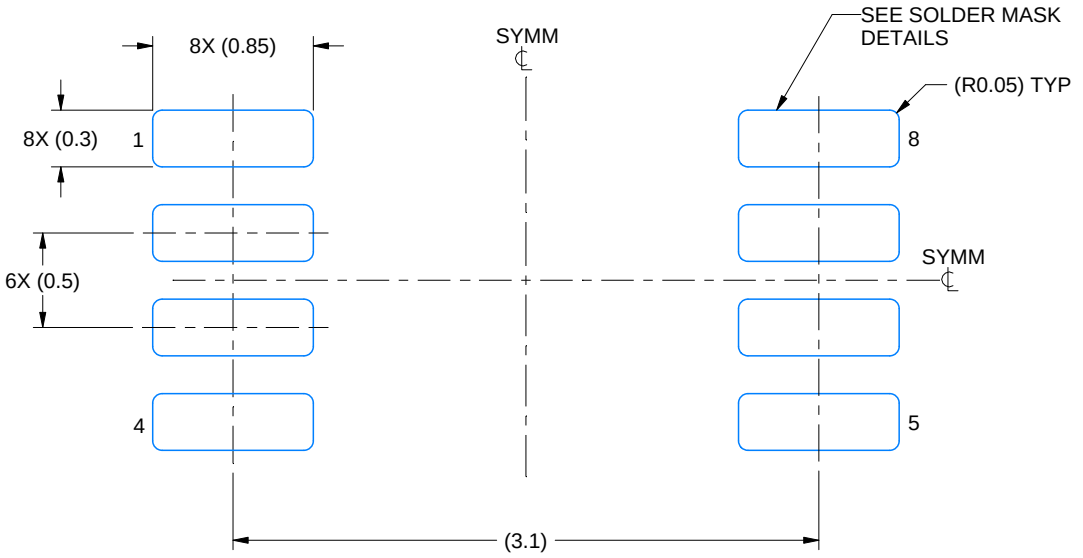




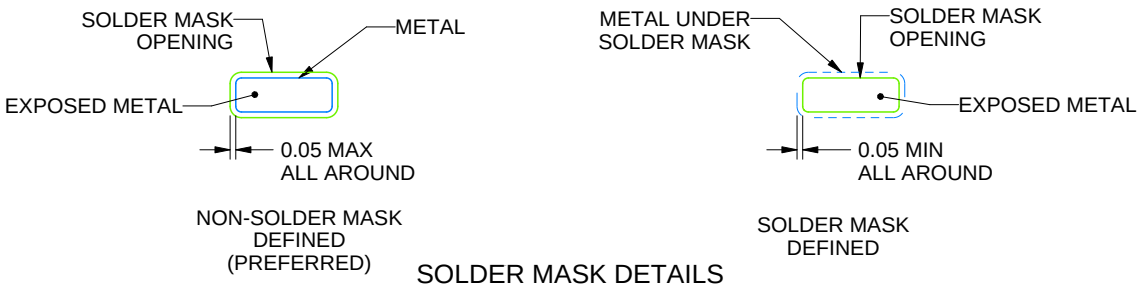
4225266/A 09/2014

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-187 variation CA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 25X

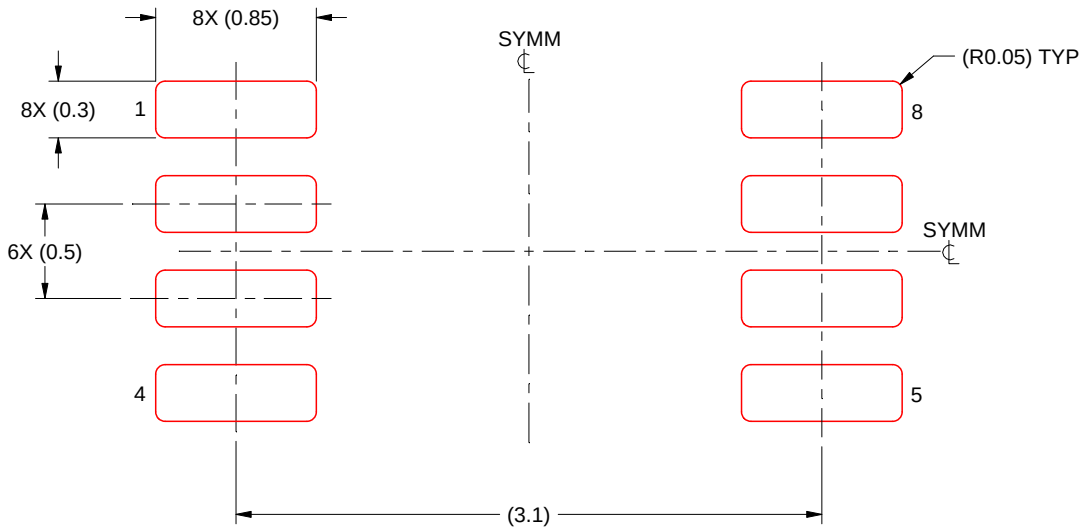


SOLDER MASK DETAILS

4225266/A 09/2014

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 25X

4225266/A 09/2014

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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