TXG8122-Q1 ±80V Bidirectional Ground-Level Translator for I2C

1 Features

- AEC-Q100 qualified for automotive applications
- Bidirectional I2C compatible communication
- Support for Standard-mode, Fast-mode, and Fast-mode Plus I2C operation
- Supports DV shifts up to ±80V
- Data rate up to 1MHz
- Side 1 Supply Range: 3V to 5.5V
- Side 2 Supply Range: 2.25V to 5.5V
- Maximum capacitive load:
  - 80pF (Side 1) and 550pF (Side 2)
- Open -drain outputs with current sink capability:
  - 3.5mA (Side 1) and 50mA (Side 2)
- Low power consumption at 400kHz (typical):
  - I_{CC1} = 3.1mA, I_{CC2} = 0.7mA
- Operating temperature from –40°C to +125°C
- CMTI of 500V/µs
- Latch-up performance exceeds 100mA per JESD 78, class II
- ESD protection exceeds JESD 22
  - 2000V human-body model
  - 500V charged-device model
- Package options provided: SOIC (8D), WSON (8DSG), SOT-23 (8DDF)

2 Applications

- Electric Power Steering
- Vehicle Control Unit
- Automotive Display
- Head Unit and Digital Cockpit

3 Description

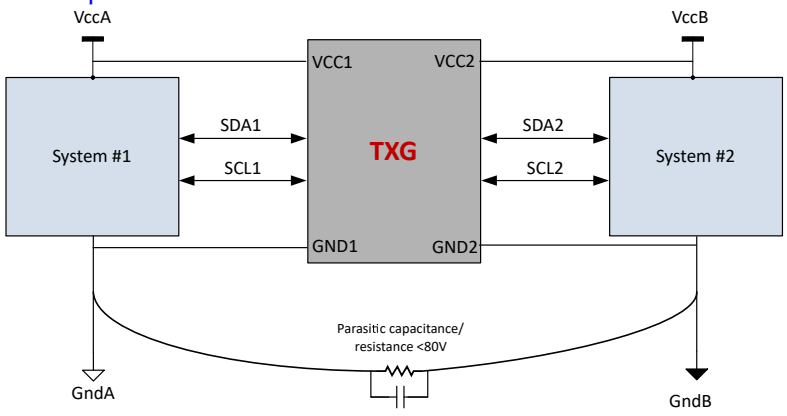
The TXG8122-Q1 device is a dual bidirectional, non-galvanic based voltage and ground-level translator for I2C. This device supports two separate configurable power-supply rails. Side 1 is designed to track VCC1 which accepts any supply voltage from 3V to 5.5V. Side 2 is designed to track VCC2 which accepts any supply voltage from 2.25V to 5.5V. Compared to traditional level shifters, the TXG8122-Q1 can solve the challenges of voltage translation across different ground levels up to ±80V. Both GNDA or GNDB can have an offset ground as long as the difference between GNDA and GNDB remains -80V to +80V.

The Simplified Block Diagram shows a common use case where DC shift occurs between GNDA to GNDB due to parasitic resistance or capacitance. The TXG8122-Q1 is able to support I2C-based communication between systems that have different supply voltages and different ground references. The leakage between GNDA and GNDB is typically 50nA when VCC to GND is shorted.

Package Information

PART NUMBER	PACKAGE (1)	BODY SIZE (NOM)
TXG8122-Q1	DSG (WSON-8)	2.00mm × 2.00mm
	DDF (SOT-8)	2.80mm × 2.90mm
	D (SOIC-8)	4.90mm x 3.90mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



Simplified Block Diagram

ADVANCE INFORMATION

ADVANCE INFORMATION

Table of Contents

4 Pin Configuration and Functions—TXG8122-Q1

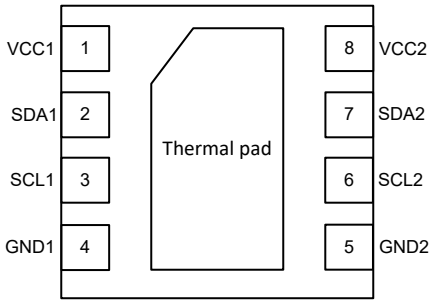


Figure 4-1. DSG 8-Pin WSON Top View

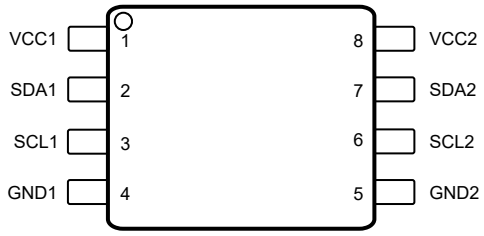


Figure 4-2. DDF Package 8-Pin SOT-23 and D Package 8-Pin SOIC Top View

Table 4-1. TXG8122-Q1 Pin Functions

PIN			I/O	DESCRIPTION
Name	DSG	DDF, D		
VCC1	1	1	—	Side 1 supply voltage
VCC2	8	8	—	Side 2 supply voltag
SDA1	2	2	I/O	Serial data input/output, side 1
SCL1	3	3	I/O	Serial clock input/output, side 1
SDA2	7	7	I/O	Serial data input/output, side 2
SCL2	6	6	I/O	Serial clock input/output, side 2
GND1	4	4	—	Ground reference for VCC1
GND2	5	5	—	Ground reference for VCC2
—	Thermal pad	—	—	Keep thermal pad floating.

ADVANCE INFORMATION

ADVANCE INFORMATION

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC1} to V_{GND1}	Supply voltage to ground voltage, Side 1		–0.5	6.5	V
V_{CC2} to V_{GND2}	Supply voltage to ground voltage, Side 2		–0.5	6.5	V
V_{GND1} to V_{GND2}	V_{GND1} to V_{GND2}	V_{GND1} to V_{GND2}	-82	82	V
V_I	SDA1, SCL1	I/O Ports (Side 1) to V_{GND1}	–0.5	V_{CC1} + 0.5	V
	SDA2, SCL2	I/O Ports (Side 2) to V_{GND2}	–0.5	V_{CC2} + 0.5	
V_O	SDA1, SCL1	I/O Ports (Side 1) to V_{GND1}	–0.5	V_{CC1} + 0.5	V
	SDA2, SCL2	I/O Ports (Side 2) to V_{GND2}	–0.5	V_{CC2} + 0.5	
I_I	SDA1, SCL1	I/O Ports (Side 1) to V_{GND1}		20	mA
	SDA2, SCL2	I/O Ports (Side 2) to V_{GND2}		100	mA
I_O	SDA1, SCL1	I/O Ports (Side 1) to V_{GND1}		20	mA
	SDA2, SCL2	I/O Ports (Side 2) to V_{GND2}		100	mA
T_j	Junction Temperature			150	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Section 5.1* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Section 5.3* Exposure beyond the limits listed in *Section 5.3* may affect device reliability.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002(2)	±500	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted) (1)

			MIN	MAX	UNIT
V_{CC1}	Supply voltage - V_{CC1} to GND1		3.0	5.5	V
V_{CC2}	Supply voltage - V_{CC2} to GND2		2.25	5.5	V
V_{GND1} to V_{GND2}	Voltage Between GND1 and GND2		-80	80	V
V_{UVLO+}	Positive-Going Undervoltage Lockout Voltage	Side 1			V
V_{UVLO+}	Positive-Going Undervoltage Lockout Voltage	Side 2			V
V_{UVLO-}	Negative-Going Undervoltage Lockout Voltage	Side 1			V
V_{UVLO-}	Negative-Going Undervoltage Lockout Voltage	Side 2			V
V_{UVLO_Hys}	Undervoltage Lockout Hysteresis	Side 1			V
V_{UVLO_Hys}	Undervoltage Lockout Hysteresis	Side 2			V
V_{SDA1}, V_{SCL1}	I2C input and output signal voltages	Side 1		V_{CC1}	V
V_{SDA2}, V_{SCL2}	I2C input and output signal voltages	Side 2		V_{CC2}	V
V_{IL1}	Low-level input voltage	Side 1		606	mV
V_{IH1}	High-level input voltage	Side 1	0.7 x V_{CC1}		V
V_{IL2}	Low-level input voltage	Side 2		0.35 x V_{CC2}	V
V_{IH2}	High-level input voltage	Side 2	0.47 x V_{CC2}		V
I_{OL1}	Low-level output current	Side 1		3.5	mA
I_{OL2}	Low-level output current	Side 2		50	mA
C1	Capacitive load	Side 1		80	pF
C2	Capacitive load	Side 2		550	pF
f_{MAX}	I2C operating frequency			1	MHz
T_A	Operating free-air temperature		–40	125	°C

(1) All control inputs and data I/Os of this device have weak pulldowns to ensure the line is not floating when undefined external to the device. The input leakage from these weak pulldowns is defined by the I_I specification indicated under *Section 5.4*.

ADVANCE INFORMATION

ADVANCE INFORMATION

5.4 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	Operating free-air temperature (T_A)			UNIT
			–40°C to 125°C			
			MIN	TYP	MAX	
V_{ILT1}	Voltage input threshold low (SDA1 and SCL1)		481		606	mV
V_{IHT1}	Voltage input threshold high (SDA1 and SCL1)		528		663	mV
V_{HYST1}	Voltage input hystersis	V_{IHT1} - V_{ILT1}	45			mV
V_{OL1}	Low-level output voltage (SDA1 and SCL1)	0.5mA ≤ (I_{SDA1} and I_{SCL1}) ≤ 3.5mA			768	mV
ΔV_{OIT1}	Low-level output voltage to high-level input voltage threshold difference, SDA1 and SCL1	0.5mA ≤ (I_{SDA1} and I_{SCL1}) ≤ 3.5mA	51			mV
V_{ILT2}	Voltage input threshold low (SDA2 and SCL2)		0.34 x V_{CC2}		0.35 x V_{CC2}	V
V_{IHT2}	Voltage input threshold high (SDA2 and SCL2)		0.47 x V_{CC2}		0.48 x V_{CC2}	V
V_{HYST2}	Voltage input hystersis	V_{IHT2} - V_{ILT2}	0.13 x V_{CC2}			V
V_{OL2}	Low-level output voltage	0.5mA ≤ (I_{SDA1} and I_{SCL1}) ≤ 30mA			0.23	V
$I_{I\ (Side\ 1)}$	Input leakage current (SDA1, SCL1)	V_{SDA1}, V_{SCL1} = V_{CC1} = 5.5V			0.71	µA
$I_{I\ (Side\ 2)}$	Input leakage current (SDA2, SCL2)	V_{SDA2}, V_{SCL2} = V_{CC2} = 5.5V			0.42	µA
C_i	Input capacitance to local ground	V_I = 0.4 × sin (2E6*πt) + V_{DD}x / 2			6	pF
C_{GND}	Cap between grounds	All channels combined (V_{CC} both sides are powered on)			44	pF
		All channels combined (V_{CC} to GND shorted)			54	pF
Leakage	Current Leakage between GndA to GndB	All channels combined (VCC to GND shorted)		0.05	1.85	µA
		All channels combined (VCC both sides are powered on and inputs are all high)		0.06	1.85	µA
		All channels combined (VCC both sides are powered on and inputs are all low)		32	43	µA
CMTI	Common Mode Transient Immunity	Input static Ground shift up to 80V			0.5	kV/µs
V_{UVLO+}	Positive-Going Undervoltage Lockout Voltage	Side 1			2.9	V
		Side 2			2.25	V
V_{UVLO-}	Negative-Going Undervoltage Lockout Voltage	Side 1	2.3			V
		Side 2	1.7			V
V_{UVLO_Hys}	Undervoltage Lockout Hysteresis	Side 1	60			mV
		Side 2	60			mV

5.5 Supply Current Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC1}	V_{CC2}	Operating free-air temperature (T_A) –40°C to 125°C			UNIT
					MIN	TYP	MAX	
I_{CC1}	Supply current, Side 1	SDA1/SCL1 = V_{CC1}	3V – 5.5V	2.25V – 5.5V		2.8	3.31	mA
		SDA1/SCL1 = GND1				2.9	3.55	mA
		SDA1/SCL1 = 400kHz square wave				3.1	3.72	mA
		SDA1/SCL1 = 1MHz square wave				3.2	3.9	mA
I_{CC2}	Supply current, Side 2	SDA2/SCL2 = V_{CC2}	3V – 5.5V	2.25V – 5.5V		0.5	0.68	mA
		SDA2/SCL2 = GND2				0.7	0.91	mA
		SDA2/SCL2 = 400kHz square wave				0.7	0.92	mA
		SDA2/SCL2 = 1MHz square wave				1	1.19	mA
I_{CC1}	Supply current, Side 1	VSDA1, VSCL1 = GND1, VSDA2, VSCL2 = GND2, R1 and R2 = Open, C1 and C2 = Open		2.5V		2.5	3.08	mA
	Supply current, Side 1	VSDA1, VSCL1 = VCC1, VSDA2, VSCL2 = VCC2, R1 and R2 = Open, C1 and C2 = Open				2.7	3.18	mA
I_{CC2}	Supply current, Side 2	VSDA1, VSCL1 = GND1, VSDA2, VSCL2 = GND2, R1 and R2 = Open, C1 and C2 = Open				0.6	0.79	mA
	Supply current, Side 2	VSDA1, VSCL1 = VCC1, VSDA2, VSCL2 = VCC2, R1 and R2 = Open, C1 and C2 = Open				0.5	0.65	mA
I_{CC1}	Supply current, Side 1	VSDA1, VSCL1 = GND1, VSDA2, VSCL2 = GND2, R1 and R2 = Open, C1 and C2 = Open	3.3V	3.3V		2.7	3.13	mA
		VSDA1, VSCL1 = VCC1, VSDA2, VSCL2 = VCC2, R1 and R2 = Open, C1 and C2 = Open				2.8	3.19	mA
I_{CC2}	Supply current, Side 2	VSDA1, VSCL1 = GND1, VSDA2, VSCL2 = GND2, R1 and R2 = Open, C1 and C2 = Open				0.7	0.82	mA
		VSDA1, VSCL1 = VCC1, VSDA2, VSCL2 = VCC2, R1 and R2 = Open, C1 and C2 = Open				0.5	0.65	mA

ADVANCE INFORMATION

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC1}	V_{CC2}	Operating free-air temperature (T_A)			UNIT
					–40°C to 125°C			
					MIN	TYP	MAX	
I_{CC1}	Supply current, Side 1	VSDA1, VSCL1 = GND1, VSDA2, VSCL2 = GND2, R1 and R2 = Open, C1 and C2 = Open	5V	5V		2.8	3.43	mA
	Supply current, Side 1	VSDA1, VSCL1 = VCC1, VSDA2, VSCL2 = VCC2, R1 and R2 = Open, C1 and C2 = Open				2.8	3.26	mA
I_{CC2}	Supply current, Side 2	VSDA1, VSCL1 = GND1, VSDA2, VSCL2 = GND2, R1 and R2 = Open, C1 and C2 = Open				0.7	0.89	mA
	Supply current, Side 2	VSDA1, VSCL1 = VCC1, VSDA2, VSCL2 = VCC2, R1 and R2 = Open, C1 and C2 = Open				0.5	0.67	mA

ADVANCE INFORMATION

5.6 Switching Characteristics, V_{CCA} = 3.3 ± 0.3V

over recommended operating conditions, unless otherwise noted

PARAMETER		Test Conditions	Supply Voltage Side 2 (V_{CC2})									UNIT
			2.5 ± 0.25V			3.3 ± 0.3V			5.0 ± 0.5V			
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
t_{f1}	Output signal fall time (SDA1, SCL1)	0.7 × V_{CC1} ≥ V_O ≥ 0.3 × V_{CC1}, R1 = 300Ω, C1 = 80pF			21			21			21	ns
		0.9 × V_{CC1} ≥ V_O ≥ 900mV, R1 = 300Ω, C1 = 80pF			37			37			37	ns
t_{f2}	Output signal fall time (SDA2, SCL2)	0.7 × V_{CC2} ≥ V_O ≥ 0.3 × V_{CC2}, R2 = 260Ω, C2 = 550pF			64			26			36	ns
		0.9 × V_{CC2} ≥ V_O ≥ 400mV, R2 = 260Ω, C2 = 550pF			51			75			159	ns
$t_{r\ 1}$	Output signal rise time (SDA1, SCL1)	0.7 × V_{CC1} ≥ V_O ≥ 0.3 × V_{CC1}, R1 = 300Ω, C1 = 80pF			22			22			22	ns
t_{r2}	Output signal rise time (SDA2, SCL2)	0.7 × V_{CC2} ≥ V_O ≥ 0.3 × V_{CC2}, R2 = 260Ω, C2 = 550pF			104			104			104	ns
t_{pLH1-2}	Low-to-high propagation delay, side 1 to side 2	V_I = 535mV, V_O = 0.7 × V_{CC2}, R1 = 300Ω, R2 = 260Ω, C1 = 80pF, C2 = 550pF			209			209			209	ns
t_{pHL1-2}	High-to-low propagation delay, side 1 to side 2	V_I = 550mV, V_O = 0.7 × V_{CC2}, R1 = 300Ω, R2 = 260Ω, C1 = 80pF, C2 = 550pF			101			140			86	ns
t_{pLH2-1}	Low-to-high propagation delay, side 2 to side 1	V_I = 0.4 x V_{CC2}, V_O = 0.7 x V_{CC1}, R1 = 300Ω, R2 = 260 Ω, C1 = 80pF, C2 = 550pF			102			92			94	ns
t_{pHL2-1}	High-to-low propagation delay, side 2 to side 1	V_I = 0.4 x V_{CC2}, V_O = 0.3 × V_{CC1}, R1 = 300Ω, R2 = 260Ω, C1 = 80pF, C2 = 550pF			114			102			92	ns
PWD_{1-2}	Pulse width distortion $\lvert t_{pHL1-2} - t_{pLH1-2} \rvert$	R1 = 300Ω, R2 = 260Ω, C1 = 80pF, C2 = 550pF			167			160			170	ns
PWD_{2-1}	Pulse width distortion $\lvert t_{pHL2-1} - t_{pLH2-1} \rvert$	R1 = 300Ω, R2 = 260Ω, C1 = 80pF, C2 = 550pF			36			23.5			26	ns
t_{LOOP1}	Round-trip propagation delay on side 1	0.4V ≤ V_I ≤ 0.3 × VCC1, R1 = 300Ω, C1 = 80pF, R2 = 260Ω, C2 = 550pF			195			196			201	ns

ADVANCE INFORMATION

ADVANCE INFORMATION

5.7 Switching Characteristics, V_{CCA} = 5 ± 0.5V

over recommended operating conditions, unless otherwise noted

PARAMETER		Test Conditions	Supply Voltage Side 2 (V_{CC2})									UNIT
			2.5 ± 0.25V			3.3 ± 0.3V			5.0 ± 0.5V			
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
t_{f1}	Output signal fall time (SDA1, SCL1)	0.7 × V_{CC1} ≥ V_O ≥ 0.3 × V_{CC1}, R1 = 300Ω, C1 = 80pF			26			26			26	ns
		0.9 × V_{CC1} ≥ V_O ≥ 900mV, R1 = 300Ω, C1 = 80pF			51			51			51	ns
t_{f2}	Output signal fall time (SDA2, SCL2)	0.7 × V_{CC2} ≥ V_O ≥ 0.3 × V_{CC2}, R2 = 220Ω, C2 = 550pF			63			26			36	ns
		0.9 × V_{CC2} ≥ V_O ≥ 400mV, R2 = 220Ω, C2 = 550pF			51			75			160	ns
$t_{r\ 1}$	Output signal rise time (SDA1, SCL1)	0.7 × V_{CC1} ≥ V_O ≥ 0.3 × V_{CC1}, R1 = 300Ω, C1 = 80pF			22			22			22	ns
t_{r2}	Output signal rise time (SDA2, SCL2)	0.7 × V_{CC2} ≥ V_O ≥ 0.3 × V_{CC2}, R2 = 220Ω, C2 = 550pF			104			104			104	ns
t_{pLH1-2}	Low-to-high propagation delay, side 1 to side 2	V_I = 535mV, V_O = 0.7 × V_{CC2}, R1 = 300Ω, R2 = 220, C1 = 80pF, C2 = 550pF			215.5			215			215	ns
t_{pHL1-2}	High-to-low propagation delay, side 1 to side 2	V_I = 550mV, V_O = 0.7 × V_{CC2}, R1 = 300Ω, R2 = 220, C1 = 80pF, C2 = 550pF			94			133			79	ns
t_{pLH2-1}	Low-to-high propagation delay, side 2 to side 1	V_I = 0.4 x V_{CC2}, V_O = 0.7 x V_{CC1}, R1 = 300Ω, R2 = 220, C1 = 80pF, C2 = 550pF			103.5			94			97	ns
t_{pHL2-1}	High-to-low propagation delay, side 2 to side 1	V_I = 0.4 x V_{CC2}, V_O = 0.3 × V_{CC1}, R1 = 300Ω, R2 = 220, C1 = 80pF, C2 = 550pF			112			99			90	ns
PWD_{1-2}	Pulse width distortion $\lvert t_{pHL1-2} - t_{pLH1-2} \rvert$	R1 = 300Ω, R2 = 220, C1 = 80pF, C2 = 550pF			174			167			177	ns
PWD_{2-1}	Pulse width distortion $\lvert t_{pHL2-1} - t_{pLH2-1} \rvert$	R1 = 300Ω, R2 = 220, C1 = 80pF, C2 = 550pF			39			28			32	ns
t_{LOOP1}	Round-trip propagation delay on side 1	0.4V ≤ V_I ≤ 0.3 × VCC1, R1 = 300Ω, C1 = 80pF, R2 = 220Ω, C2 = 550pF			203			204			209	ns

5.8 Electrical Characteristics (85°C)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	Operating free-air temperature (T_A)			UNIT
			–40°C to 85°C			
			MIN	TYP	MAX	
V_{ILT1}	Voltage input threshold low (SDA1 and SCL1)		481		606	mV
V_{IHT1}	Voltage input threshold high (SDA1 and SCL1)		528		663	mV
V_{HYST1}	Voltage input hystersis	V_{IHT1} - V_{ILT1}	43		61	mV
V_{OL1}	Low-level output voltage (SDA1 and SCL1)	0.5 mA ≤ (I_{SDA1} and I_{SCL1}) ≤ 3.5 mA			768	mV
ΔV_{OIT1}	Low-level output voltage to high-level input voltage threshold difference, SDA1 and SCL1	0.5 mA ≤ (I_{SDA1} and I_{SCL1}) ≤ 3.5 mA	51			mV
V_{ILT2}	Voltage input threshold low (SDA2 and SCL2)		0.34 x V_{CC2}		0.35 x V_{CC2}	V
V_{IHT2}	Voltage input threshold high (SDA2 and SCL2)		0.47 x V_{CC2}		0.48 x V_{CC2}	V
V_{HYST2}	Voltage input hystersis	V_{IHT2} - V_{ILT2}	0.13 x V_{CC2}			V
V_{OL2}	Low-level output voltage	0.5 mA ≤ (I_{SDA1} and I_{SCL1}) ≤ 30 mA			0.49	V
$I_{I\ (Side\ 1)}$	Input leakage current (SDA1, SCL1)	V_{SDA1}, V_{SCL1} = V_{CC1} = 5.5V			TBD	µA
$I_{I\ (Side\ 2)}$	Input leakage current (SDA2, SCL2)	V_{SDA2}, V_{SCL2} = V_{CC2} = 5.5V				µA
C_i	Input capacitance to local ground	V_I = 0.4 × sin (2E6*πt) + V_{DD}x / 2			6	pF
C_{GND}	Cap between grounds	All channels combined (V_{CC} both sides are powered on)			44	pF
		All channels combined (V_{CC} to GND shorted)			51	pF
Leakage	Current Leakage between GndA to GndB	All channels combined (VCC to GND shorted)			0.37	µA
		All channels combined (VCC both sides are powered on and inputs are all high)			0.37	µA
		All channels combined (VCC both sides are powered on and inputs are all low)			43	µA
CMTI	Common Mode Transient Immunity	Input static Ground shift up to 80V			0.5	kV/µs
V_{UVLO+}	Positive-Going Undervoltage Lockout Voltage	Side 1			2.9	V
		Side 2			2.25	V
V_{UVLO-}	Negative-Going Undervoltage Lockout Voltage	Side 1	2.3			V
		Side 2	1.7			V
V_{UVLO_Hys}	Undervoltage Lockout Hysteresis	Side 1	87			mV
		Side 2	156			mV

ADVANCE INFORMATION

ADVANCE INFORMATION

5.9 Supply Current Characteristics (85°C)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC1}	V_{CC2}	Operating free-air temperature (T_A)			UNIT
					–40°C to 85°C			
					MIN	TYP	MAX	
I_{CC1}	Supply current, Side 1	SDA1/SCL1 = V_{CC1}	3V – 5.5V	2.25V – 5.5V			3.3	mA
		SDA1/SCL1 = GND1					3.5	mA
		SDA1/SCL1 = 400kHz square wave					3.67	mA
		SDA1/SCL1 = 1MHz square wave					3.9	mA
I_{CC2}	Supply current, Side 2	SDA2/SCL2 = V_{CC2}	3V – 5.5V	2.25V – 5.5V			0.64	mA
		SDA2/SCL2 = GND2					0.87	mA
		SDA2/SCL2 = 400kHz square wave					0.85	mA
		SDA2/SCL2 = 1MHz square wave					1.1	mA
I_{CC1}	Supply current, Side 1	VSDA1, VSCL1 = GND1, VSDA2, VSCL2 = GND2, R1 and R2 = Open, C1 and C2 = Open		2.5V			3.01	mA
	Supply current, Side 1	VSDA1, VSCL1 = VCC1, VSDA2, VSCL2 = VCC2, R1 and R2 = Open, C1 and C2 = Open					3.15	mA
I_{CC2}	Supply current, Side 2	VSDA1, VSCL1 = GND1, VSDA2, VSCL2 = GND2, R1 and R2 = Open, C1 and C2 = Open					0.72	mA
	Supply current, Side 2	VSDA1, VSCL1 = VCC1, VSDA2, VSCL2 = VCC2, R1 and R2 = Open, C1 and C2 = Open					0.58	mA
I_{CC1}	Supply current, Side 1	VSDA1, VSCL1 = GND1, VSDA2, VSCL2 = GND2, R1 and R2 = Open, C1 and C2 = Open	3.3V	3.3V			3.06	mA
		VSDA1, VSCL1 = VCC1, VSDA2, VSCL2 = VCC2, R1 and R2 = Open, C1 and C2 = Open					3.16	mA
I_{CC2}	Supply current, Side 2	VSDA1, VSCL1 = GND1, VSDA2, VSCL2 = GND2, R1 and R2 = Open, C1 and C2 = Open					0.76	mA
		VSDA1, VSCL1 = VCC1, VSDA2, VSCL2 = VCC2, R1 and R2 = Open, C1 and C2 = Open					0.59	mA

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC1}	V_{CC2}	Operating free-air temperature (T_A)			UNIT
					–40°C to 85°C			
					MIN	TYP	MAX	
I_{CC1}	Supply current, Side 1	VSDA1, VSCL1 = GND1, VSDA2, VSCL2 = GND2, R1 and R2 = Open, C1 and C2 = Open	5V	5V			3.38	mA
	Supply current, Side 1	VSDA1, VSCL1 = VCC1, VSDA2, VSCL2 = VCC2, R1 and R2 = Open, C1 and C2 = Open					3.25	mA
I_{CC2}	Supply current, Side 2	VSDA1, VSCL1 = GND1, VSDA2, VSCL2 = GND2, R1 and R2 = Open, C1 and C2 = Open					0.84	mA
	Supply current, Side 2	VSDA1, VSCL1 = VCC1, VSDA2, VSCL2 = VCC2, R1 and R2 = Open, C1 and C2 = Open					0.63	mA

ADVANCE INFORMATION

ADVANCE INFORMATION

5.10 Switching Characteristics, V_{CCA} = 3.3 ± 0.3V (85°C)

over recommended operating conditions, unless otherwise noted

PARAMETER		Test Conditions	Supply Voltage Side 2 (V_{CC2})									UNIT
			2.5 ± 0.25V			3.3 ± 0.3V			5.0 ± 0.5V			
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
t_{f1}	Output signal fall time (SDA1, SCL1)	0.7 × V_{CC1} ≥ V_O ≥ 0.3 × V_{CC1}, R1 = 300Ω, C1 = 80pF			20			20			20	ns
		0.9 × V_{CC1} ≥ V_O ≥ 900mV, R1 = 300Ω, C1 = 80pF			35			35			35	ns
t_{f2}	Output signal fall time (SDA2, SCL2)	0.7 × V_{CC2} ≥ V_O ≥ 0.3 × V_{CC2}, R2 = 220Ω, C2 = 550pF			56			24			32	ns
		0.9 × V_{CC2} ≥ V_O ≥ 400mV, R2 = 220Ω, C2 = 550pF			45			67			130	ns
$t_{r\ 1}$	Output signal rise time (SDA1, SCL1)	0.7 × V_{CC1} ≥ V_O ≥ 0.3 × V_{CC1}, R1 = 300Ω, C1 = 80pF			22			22			22	ns
t_{r2}	Output signal rise time (SDA2, SCL2)	0.7 × V_{CC2} ≥ V_O ≥ 0.3 × V_{CC2}, R2 = 220Ω, C2 = 550pF			104			104			104	ns
t_{pLH1-2}	Low-to-high propagation delay, side 1 to side 2	V_I = 535mV, V_O = 0.7 × V_{CC2}, R1 = 300Ω, R2 = 220, C1 = 80pF, C2 = 550pF			205			205			204	ns
t_{pHL1-2}	High-to-low propagation delay, side 1 to side 2	V_I = 550mV, V_O = 0.7 × V_{CC2}, R1 = 300Ω, R2 = 220, C1 = 80pF, C2 = 550pF			87			121			74	ns
t_{pLH2-1}	Low-to-high propagation delay, side 2 to side 1	V_I = 0.4 x V_{CC2}, V_O = 0.7 x V_{CC1}, R1 = 300Ω, R2 = 220, C1 = 80pF, C2 = 550pF			99			90			92	ns
t_{pHL2-1}	High-to-low propagation delay, side 2 to side 1	V_I = 0.4 x V_{CC2}, V_O = 0.3 × V_{CC1}, R1 = 300Ω, R2 = 220, C1 = 80pF, C2 = 550pF			107			98			90	ns
PWD_{1-2}	Pulse width distortion $\lvert t_{pHL1-2} - t_{pLH1-2} \rvert$	R1 = 300Ω, R2 = 220, C1 = 80pF, C2 = 550pF			167			160			170	ns
PWD_{2-1}	Pulse width distortion $\lvert t_{pHL2-1} - t_{pLH2-1} \rvert$	R1 = 300Ω, R2 = 220, C1 = 80pF, C2 = 550pF			35			22			27	ns
t_{LOOP1}	Round-trip propagation delay on side 1	0.4V ≤ V_I ≤ 0.3 × VCC1, R1 = 300Ω, C1 = 80pF, R2 = 220Ω, C2 = 550pF			189			189			194	ns

5.11 Switching Characteristics, V_{CCA} = 5 ± 0.5V (85°C)

over recommended operating conditions, unless otherwise noted

PARAMETER		Test Conditions	Supply Voltage Side 2 (V_{CC2})									UNIT
			2.5 ± 0.25V			3.3 ± 0.3V			5.0 ± 0.5V			
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
t_{f1}	Output signal fall time (SDA1, SCL1)	0.7 × V_{CC1} ≥ V_O ≥ 0.3 × V_{CC1}, R1 = 300Ω, C1 = 80pF			25			25			25	ns
		0.9 × V_{CC1} ≥ V_O ≥ 900mV, R1 = 300Ω, C1 = 80pF			49			49			49	ns
t_{f2}	Output signal fall time (SDA2, SCL2)	0.7 × V_{CC2} ≥ V_O ≥ 0.3 × V_{CC2}, R2 = 220Ω, C2 = 550pF			56			24			32	ns
		0.9 × V_{CC2} ≥ V_O ≥ 400mV, R2 = 220Ω, C2 = 550pF			45			67			130	ns
$t_{r\ 1}$	Output signal rise time (SDA1, SCL1)	0.7 × V_{CC1} ≥ V_O ≥ 0.3 × V_{CC1}, R1 = 300Ω, C1 = 80pF			22			22			22	ns
t_{r2}	Output signal rise time (SDA2, SCL2)	0.7 × V_{CC2} ≥ V_O ≥ 0.3 × V_{CC2}, R2 = 220Ω, C2 = 550pF			104			104			104	ns
t_{pLH1-2}	Low-to-high propagation delay, side 1 to side 2	V_I = 535mV, V_O = 0.7 × V_{CC2}, R1 = 300Ω, R2 = 220, C1 = 80pF, C2 = 550pF			212			212			211	ns
t_{pHL1-2}	High-to-low propagation delay, side 1 to side 2	V_I = 550mV, V_O = 0.7 × V_{CC2}, R1 = 300Ω, R2 = 220, C1 = 80pF, C2 = 550pF			83			116			69	ns
t_{pLH2-1}	Low-to-high propagation delay, side 2 to side 1	V_I = 0.4 x V_{CC2}, V_O = 0.7 x V_{CC1}, R1 = 300Ω, R2 = 220, C1 = 80pF, C2 = 550pF			101			93			94	ns
t_{pHL2-1}	High-to-low propagation delay, side 2 to side 1	V_I = 0.4 x V_{CC2}, V_O = 0.3 × V_{CC1}, R1 = 300Ω, R2 = 220, C1 = 80pF, C2 = 550pF			104			94			86	ns
PWD_{1-2}	Pulse width distortion $\lvert t_{pHL1-2} - t_{pLH1-2} \rvert$	R1 = 300Ω, R2 = 220, C1 = 80pF, C2 = 550pF			174			167			178	ns
PWD_{2-1}	Pulse width distortion $\lvert t_{pHL2-1} - t_{pLH2-1} \rvert$	R1 = 300Ω, R2 = 220, C1 = 80pF, C2 = 550pF			39			28			32	ns
t_{LOOP1}	Round-trip propagation delay on side 1	0.4 V ≤ V_I ≤ 0.3 × VCC1, R1 = 300Ω, C1 = 80pF, R2 = 220Ω, C2 = 550pF			198			197			203	ns

ADVANCE INFORMATION

ADVANCE INFORMATION

6 Detailed Description

6.1 Overview

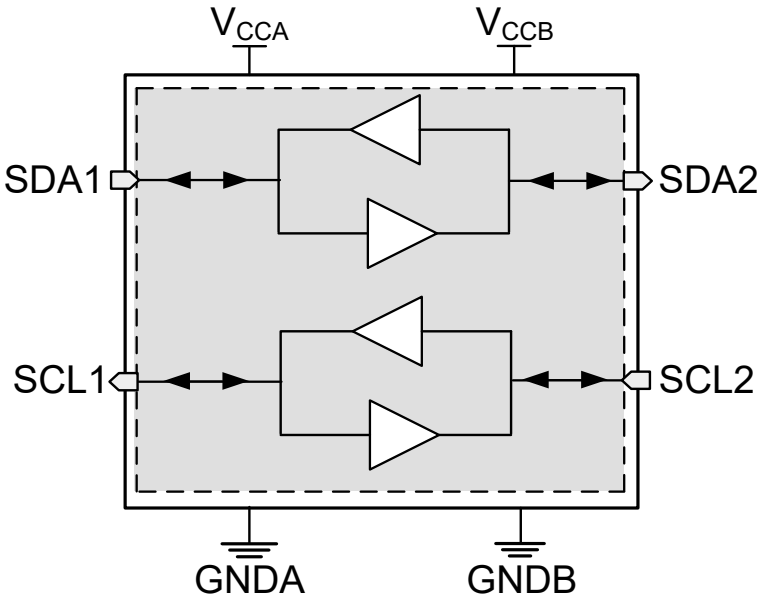
The TXG8122-Q1 is a dual bidirectional translator intended for I2C or SMBus systems. This translator is able to support logic-level shifting and ground-level shifting up to ±80V. As with standard I2C systems, SDA and SCL I/O lines are open-drain and require external pull-up resistors to the systems's supply rail.

- Idle state: When no device drives the bus, the pull-up resistors force SDA and SCL high, representing a logic '1'
- Active low: Any device can assert a logic '0' by pulling the respective line to ground.

Select the pull-up resistor value so the I2C rise-time specification is met for the measured bus capacitance and supply voltage. For more information, see I2C Bus Pullup Resistor Calculation. TXG8122-Q1 can support Standard-mode (≤100kHz), Fast-mode (≤400kHz), and Fast-mode Plus (≤1MHz).

The Side 1 of this device works from 3V to 5.5V and Side 2 works from 2.25V to 5.5V. For best signal integrity, connect Side 1 (SDA1, SCL1) to the host controller – the MCU, SoC, or any single-master node. Connect Side (SDA2, SCL2) to the shared I2C bus that links multiple peripherals. The maximum load on Side 1 is ≤80pF and maximum load on Side 2 is ≤550pF.

6.2 Functional Block Diagram



6.3 Feature Description

6.3.1 Bidirectional Level Translation

The TXG8122-Q1 can provide bidirectional voltage level translation (up-translation and down-translation) in mixed-mode applications. It is operational from 3V to 5.5V on Side 1 and 2.25V to 5.5V on Side 2.

6.4 Device Functional Modes

Table 6-1. Function Table

VCC1	VCC2	Input	Output
PU	PU	H or Open	H
		L	L

ADVANCE INFORMATION

7 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Application Information

The TXG8122-Q1 is used for level translation, enabling communication between devices or systems operating at different interface and ground voltages. The TXG8122-Q1 device is ideal for use in applications where an open-drain driver is connected to the data I/Os. Figure 7-1 is an example of two systems that translate from 3.3V to 5.5V across an I^2C interface while also seeing a ground shift of -5V on GND2 while GND1 remains at 0V. The ground shift occurs due to the parasitic resistance of the cable used to connect the 48V battery ground and 12V battery ground to the chassis of the car.

7.2 Typical Application

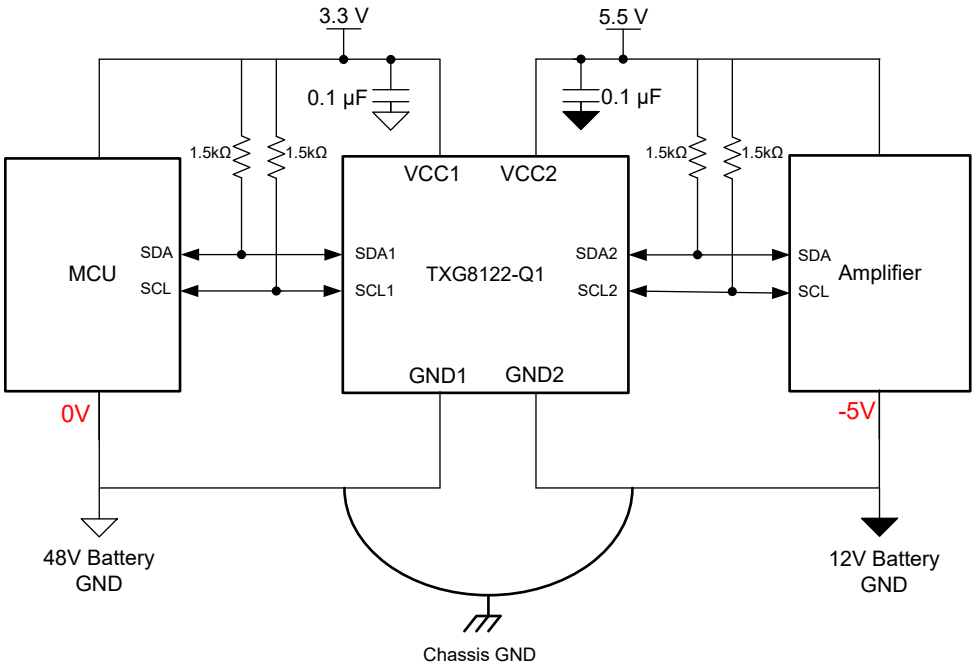


Figure 7-1. TXG8122-Q1 in Automotive

7.2.1 Design Requirements

Use the parameters listed in Table 7-1 for this design example.

Table 7-1. Design Parameters

DESIGN PARAMETERS	EXAMPLE VALUES
Input voltage range	1.71V to 5.5V
Output voltage range	1.71V to 5.5V

7.3 Power Supply Recommendations

Always apply a ground reference to the GND pins first. This device is designed for glitch free power sequencing without any supply sequencing requirements such as ramp order or ramp rate. Please make sure the difference between VCC and GND remains at 6.5V max at all times.

7.4 Layout

7.4.1 Layout Guidelines

To ensure reliability of the device, following common printed-circuit board layout guidelines are recommended:

- Use bypass capacitors on the power supply pins and place them as close to the device as possible. A 0.1µF capacitor is recommended, but transient performance can be improved by having 1µF and 0.1µF capacitors in parallel as bypass capacitors.
- A 0.1µF capacitor can be added between GNDA and GNDB to improve performances of CMTI.

7.4.2 Layout Example

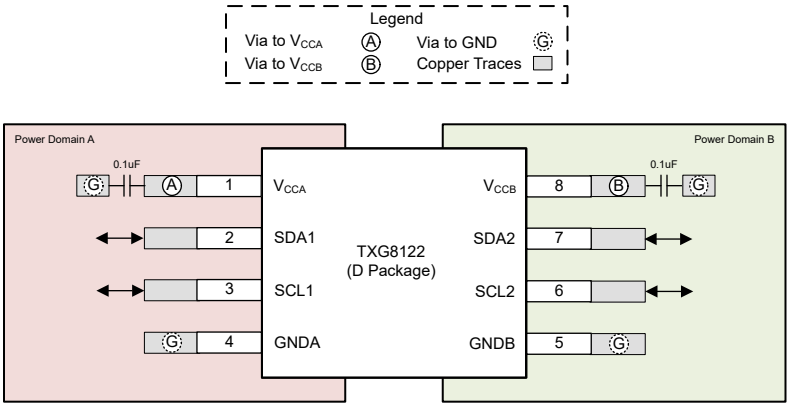


Figure 7-2. Layout Example – TXG8122-Q1

ADVANCE INFORMATION

8 Device and Documentation Support

8.1 Device Support

8.1.1 Regulatory Requirements

No statutory or regulatory requirements apply to this device.

There are no special characteristics for this product.

8.2 Documentation Support

8.2.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *Understanding Schmitt Triggers* application report
- Texas Instruments, *CMOS Power Consumption and C_{pd} Calculation* application report

8.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

8.5 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

8.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.7 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

ADVANCE INFORMATION

9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
June 2025	*	Initial Release

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

ADVANCE INFORMATION

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
PTXG8122QDRQ1	Active	Preproduction	SOIC (D) | 8	3000 | LARGE T&R	-	Call TI	Call TI	-40 to 125	

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

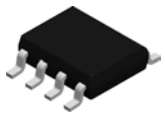
(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

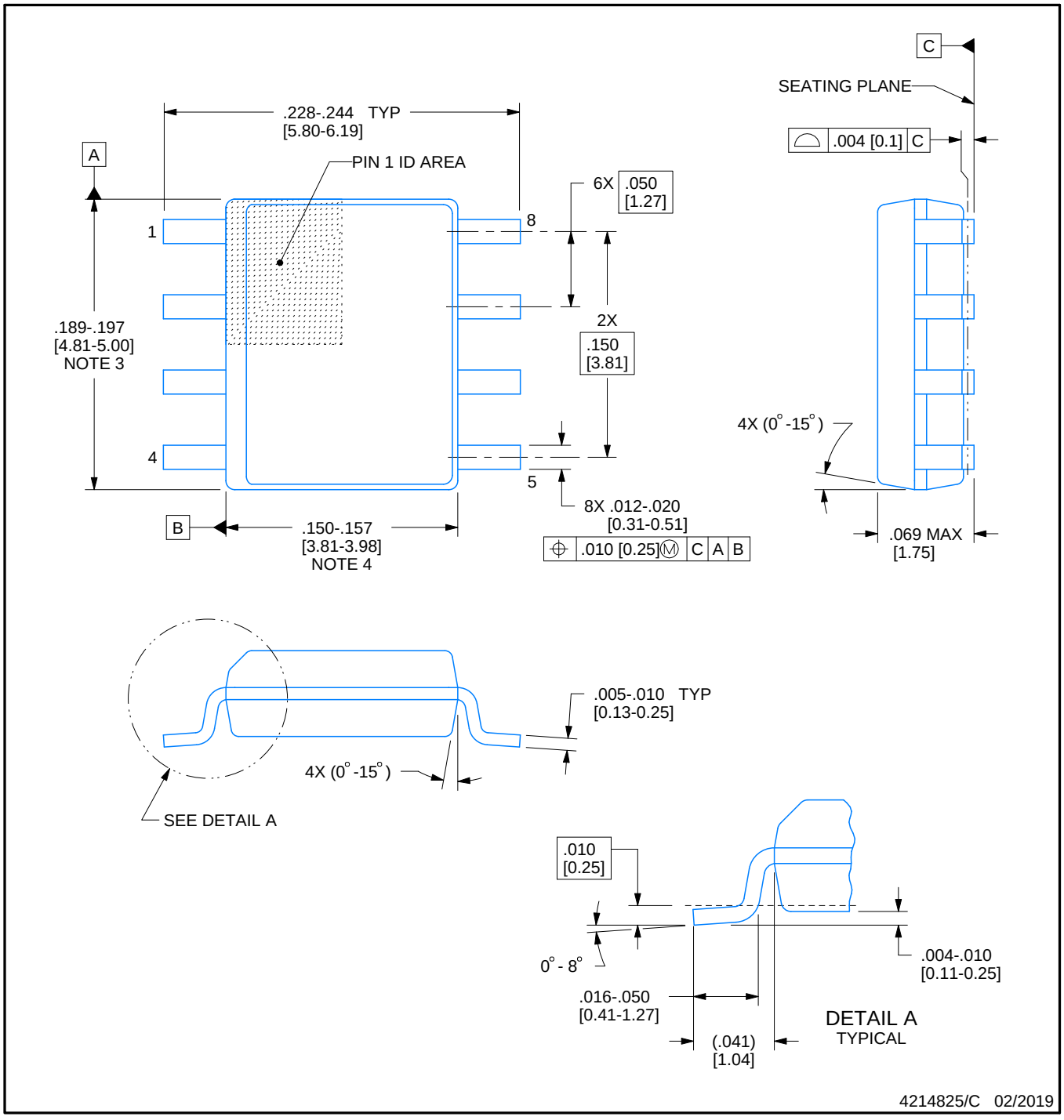


PACKAGE OUTLINE

D0008A

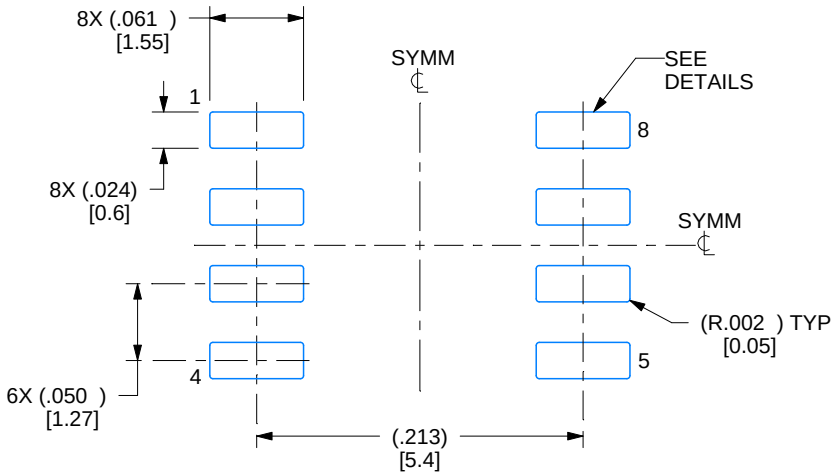
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

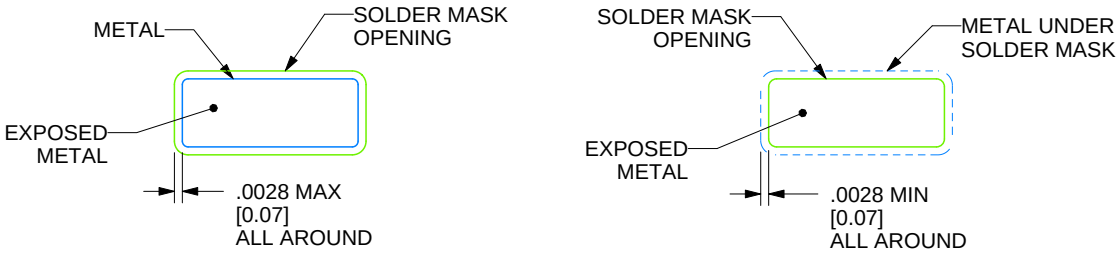


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

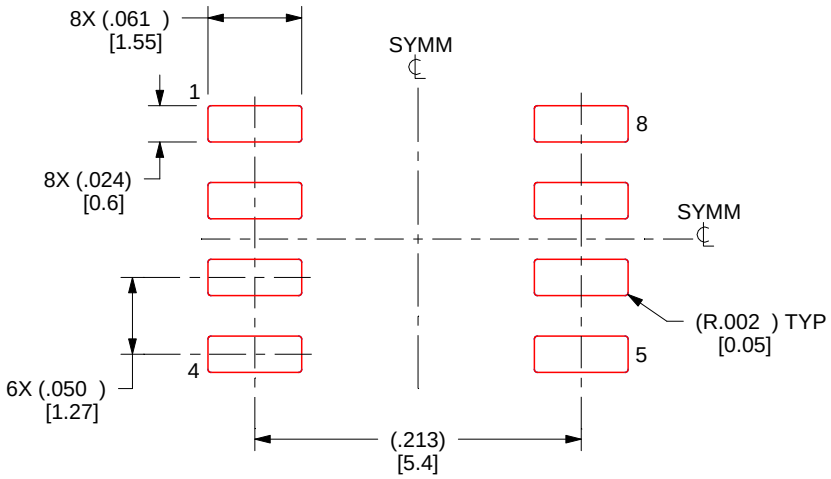
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265