# TXE81xx-Q1 Automotive 24-Bit SPI Bus I/O Expander with Interrupt Output, Reset Input, and I/O Configuration Registers

ADVANCE INFORMATION

## 1 Features

- AEC-Q100 qualified for automotive applications:
  - Temperature grade 1: –40°C to +125°C, $T_A$
- Functional safety-capable
  - Documentation available to aid in functional safety system design
- Operating power-supply voltage range of 1.65V to 5.5V
- Low standby current consumption of 6µA typical at 3.3V
- SPI SCLK Frequency
  - 10MHz from 3.3V to 5.5V
  - 5MHz from 1.65V to 5.5V
- Active-low reset input ($\overline{\text{RESET}}$)
- Configurable Fail-Safe Registers for I/O configuration to ensure redundancy
- Open-drain active-low interrupt output ($\overline{\text{INT}}$)
- Input or output configuration register
- Polarity inversion register
- 100kΩ Pull-Up/Pull-Down resistor configuration register
- Internal power-on reset
- Latched outputs with high-current drive maximum capability for directly driving LEDs
- Latch-up performance exceeds 100mA per AEC Q100-004
- ESD protection exceeds AEC - Q100 requirements
  - 2000V Human-body model (AEC - Q100-002)
  - 1000V Charged-device model (AEC - Q100-011)

## 2 Applications

- Automotive infotainment and cluster
- Body electronics and lighting
- Hybrid, electric and powertrain systems
- Products with GPIO-limited processors

## 3 Description

The TXE81xx-Q1 devices provide general purpose parallel input/output (I/O) expansion for the four wire Serial Peripheral Interface (SPI) protocol and is designed for 1.65V to 5.5V $V_{CC}$ operation.

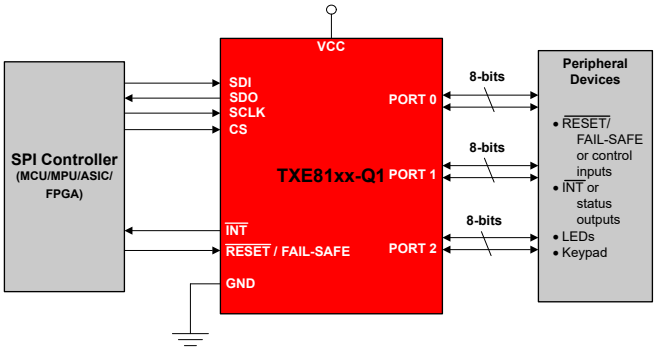
The device supports 10MHz from 3.3V to 5.5V and 5MHz from 1.65V to 5.5V. I/O expanders such as the TXE81xx-Q1 provide a simple solution when additional I/Os are needed for switches, sensors, push-buttons, LEDs, fans, and so on.

The TXE81xx-Q1 devices have I/O ports which include additional features designed to enhance the I/O performance in terms of speed, power consumption and EMI. The additional features are: programmable pull-up and pull-down resistors, latchable inputs, maskable interrupt, interrupt status register, programmable open-drain or push-pull outputs and a fail-safe register mode in situations of watchdog events.

**Package Information**

| PART NUMBER(1) | PACKAGE(2) | PACKAGE SIZE(3) |
|---|---|---|
| TXE8124-Q1 | (VSSOP, 32) | 8mm × 5mm |
| TXE8116-Q1 | (VSSOP, 24) | 6mm × 5mm |

(1) TXE8124-Q1 supports IO PORT 0, 1 and 2, TXE8116-Q1 supports IO PORT 0 and 1.
(2) For more information, see Section 11.
(3) The package size (length × width) is a nominal value and includes pins, where applicable.




**Simplified Schematic**

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# 4 Pin Configuration and Functions

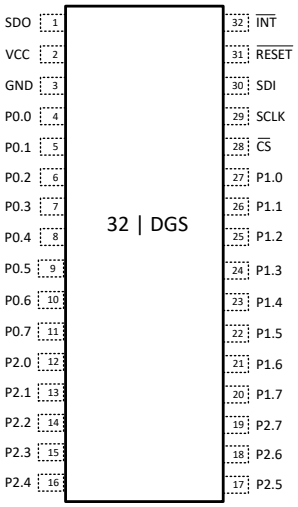


**Figure 4-1. TXE8124-Q1 DGS (VSSOP) Package, 32-Pin (Top View)**

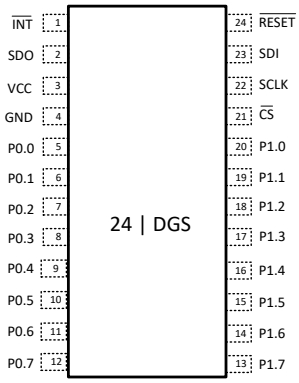


**Figure 4-2. TXE8116-Q1 DGS (VSSOP) Package, 24-Pin (Top View)**

**Table 4-1. Pin Functions**

| PIN | | | TYPE[1] | DESCRIPTION |
|---|---|---|---|---|
| NAME | VSSOP32 (DGS) | VSSOP24 (DGS) | | |
| P2.0 | 12 | - | I/O | P-port input/output. At power on, Port 2 - IO #1 is configured as an input |
| P2.1 | 13 | - | I/O | P-port input/output. At power on, Port 2 - IO #2 is configured as an input |
| P2.2 | 14 | - | I/O | P-port input/output. At power on, Port 2 - IO #3 is configured as an input |
| P2.3 | 15 | - | I/O | P-port input/output. At power on, Port 2 - IO #4 is configured as an input |
| P2.4 | 16 | - | I/O | P-port input/output. At power on, Port 2 - IO #5 is configured as an input |
| P2.5 | 17 | - | I/O | P-port input/output. At power on, Port 2 - IO #6 is configured as an input |
| P2.6 | 18 | - | I/O | P-port input/output. At power on, Port 2 - IO #7 is configured as an input |
| P2.7 | 19 | - | I/O | P-port input/output. At power on, Port 2 - IO #8 is configured as an input |
| P1.7 | 20 | 13 | I/O | P-port input/output. At power on, Port 1 - IO #8 is configured as an input |
| P1.6 | 21 | 14 | I/O | P-port input/output. At power on, Port 1 - IO #7 is configured as an input |
| P1.5 | 22 | 15 | I/O | P-port input/output. At power on, Port 1 - IO #6 is configured as an input |
| P1.4 | 23 | 16 | I/O | P-port input/output. At power on, Port 1 - IO #5 is configured as an input |
| P1.3 | 24 | 17 | I/O | P-port input/output. At power on, Port 1 - IO #4 is configured as an input |
| P1.2 | 25 | 18 | I/O | P-port input/output. At power on, Port 1 - IO #3 is configured as an input |
| P1.1 | 26 | 19 | I/O | P-port input/output. At power on, Port 1 - IO #2 is configured as an input |
| P1.0 | 27 | 20 | I/O | P-port input/output. At power on, Port 1 - IO #1 is configured as an input |
| $\overline{CS}$ | 28 | 21 | I | SPI chip select input. Internal pull-up resistor |
| SCLK | 29 | 22 | I | SPI serial clock input. Internal pull-down resistor |
| SDI | 30 | 23 | I | SPI serial data input. |
| $\overline{RESET}$/ $\overline{FAIL\text{-}SAFE}$ | 31 | 24 | I | Active Low reset or fail-safe input. Connect to $V_{CC}$ through a pull-up resistor. |
| $\overline{INT}$ | 32 | 1 | O | Open-Drain Interrupt output. Connect to $V_{CC}$ through a pull-up resistor. |
| SDO | 1 | 2 | O | SPI serial data output. Push-pull output |
| VCC | 2 | 3 | P | Supply voltage |
| GND | 3 | 4 | G | Ground |

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**Table 4-1. Pin Functions (continued)**

| PIN | | | TYPE[1] | DESCRIPTION |
|---|---|---|---|---|
| NAME | VSSOP32 (DGS) | VSSOP24 (DGS) | | |
| P0.0 | 4 | 5 | I/O | P-port input/output. At power on, Port 0 - IO #1 is configured as an input |
| P0.1 | 5 | 6 | I/O | P-port input/output. At power on, Port 0 - IO #2 is configured as an input |
| P0.2 | 6 | 7 | I/O | P-port input/output. At power on, Port 0 - IO #3 is configured as an input |
| P0.3 | 7 | 8 | I/O | P-port input/output. At power on, Port 0 - IO #4 is configured as an input |
| P0.4 | 8 | 9 | I/O | P-port input/output. At power on, Port 0 - IO #5 is configured as an input |
| P0.5 | 9 | 10 | I/O | P-port input/output. At power on, Port 0 - IO #6 is configured as an input |
| P0.6 | 10 | 11 | I/O | P-port input/output . At power on, Port 0 - IO #7 is configured as an input |
| P0.7 | 11 | 12 | I/O | P-port input/output. At power on, Port 0 - IO #8 is configured as an input |

(1) I = Input, O = Output, I/O = Input or Output, G = Ground, P = Power

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# 5 Specifications

## 5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

| | | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | | –0.5 | 6.5 | V |
| $V_I$ | Input voltage(2) | | | –0.5 | 6.5 | V |
| $V_O$ | Output voltage(2) | | | –0.5 | 6.5 | V |
| $I_{IK}$ | Input clamp current | $\overline{RESET}$, SCLK, $\overline{CS}$ | $V_I < 0$ | | -20 | mA |
| $I_{OK}$ | Output clamp current | $\overline{INT}$ | $V_O < 0$ | | -20 | mA |
| $I_{IOK}$ | Input-output clamp current | | $V_O < 0$ or $V_O > V_{CC}$ | | ±20 | mA |
| $I_{OL}$ | Continuous output low current | | $V_O$ = 0 to $V_{CC}$ | | 50 | mA |
| $I_{OH}$ | Continuous output high current | | $V_O$ = 0 to $V_{CC}$ | | –50 | mA |
| $I_{CC}$ | Continuous current through GND | | | | -200 | mA |
| $I_{CC}$ | Continuous current through $V_{CC}$ | | | | 160 | mA |
| $T_J$ | Junction temperature | | | | 150 | °C |
| $T_{stg}$ | Storage temperature | | | | 150 | °C |

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.

## 5.2 ESD Ratings

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human body model (HBM), per AEC Q100-002, all pins(1) | ±2000 | V |
| | | Charged device model (CDM), per AEC Q100-011, all pins | ±1000 | |

(1) AEC Q100-002 indicates that HBM stressing must be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

## 5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | 1.71 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | P-Ports | 0.7 * $V_{CC}$ | 5.5 | V |
| | | SCLK, SDI, $\overline{CS}$, $\overline{RESET}$, | 0.7 * $V_{CC}$ | 5.5 | |
| $V_{IL}$ | Low-level input voltage | P-Ports | -0.5 | 0.3 * $V_{CC}$ | V |
| | | SCLK, SDI, $\overline{CS}$, $\overline{RESET}$, | -0.5 | 0.3 * $V_{CC}$ | |
| $I_{OH}$ | High-level output current | P0.0 - P2.7 | | –10 | mA |
| $I_{OL}$ | Low-level output current | P0.0 - P2.7 | | 25 | mA |
| $I_{OH}$ (Total of all ports) | High-level output current ($V_{CC}$ - $V_{OH}$ ≤ 0.3V) | P0.0 - P2.7 | | –160 | mA |
| $T_A$ | Ambient temperature | | –40 | 125 | °C |
| $T_J$ | Junction temperature | | | 150 | °C |

(1) When the internal pull up resistors are enabled, input voltages above $V_{CC}$ will result in current flowing to VCC from the port.

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## 5.4 Thermal Information

| THERMAL METRIC (1) | | Package DGS (VSSOP) 32 PINS | Package DGS (VSSOP) 24 PINS | UNIT |
|---|---|---|---|---|
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 80.1 | 86.5 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 35.4 | 34.5 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 44.1 | 48.2 | °C/W |
| $\Psi_{JT}$ | Junction-to-top characterization parameter | 2.0 | 1.4 | °C/W |
| $\Psi_{JB}$ | Junction-to-board characterization parameter | 43.7 | 47.8 | °C/W |
| $R_{\theta JC(bot)}$ | Junction-to-case (bottom) thermal resistance | n/a | n/a | °C/W |

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application note.

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## 5.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | | | TEST CONDITIONS | $V_{CCP}$ $V_{CC}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| $V_{IK}$ | Input diode clamp voltage | | $I_I$ = –18mA | VCC | –1.2 | | | V |
| $V_{PORR}$ | Power-on reset voltage, $V_{CC}$ rising | | $V_I$ = $V_{CC}$ or GND, $I_O$ = 0 | VCC | | | 1.3 | V |
| $V_{PORF}$ | Power-on reset voltage, $V_{CC}$ falling | | | | 1.05 | | | V |
| $V_{OH}$ | High-level output voltage (1) | P Port | $I_{OH}$ = 8mA | 1.65V | 0.65 | | | V |
| | | | | 2.3V | 1.73 | | | |
| | | | | 3V | 2.87 | | | |
| | | | | 4.5V | 4.0 | | | |
| | | | | 5.5V | 4.95 | | | |
| | | SDO | $I_{OH}$ = 3mA | 1.65V to 5.5V | VCC - 0.4 | | | V |
| $V_{OL}$ | Low-level output voltage | P Ports | $I_{OL}$ = -8mA | 1.65V | | | 0.61 | V |
| | | | | 2.3V | | | 0.36 | |
| | | | | 3V | | | 0.25 | |
| | | | | 4.5V | | | 0.17 | |
| | | | | 5.5V | | | 0.15 | |
| | | SDOUT | $I_{OL}$ = -3mA | 1.65V to 5.5V | | | 0.4 | V |
| $I_{OL}$ | Low-level output current | $\overline{INT}$ | $V_{OL}$ = 0.4V | 1.65V to 5.5V | 4 | | | mA |
| $I_I$ | Input leakage current | P Ports | $V_I$ = $V_{CC}$ or GND | 1.65V to 5.5V | | | ±1 | µA |
| | | | $V_I$ = 3.6V | 0V | | | ±1 | |
| | | SDI, $\overline{RESET}$ | $V_I$ = VCC or GND | 1.65V to 5.5V | | | ±1 | |
| $I_I$ | Input leakage current | SCLK | $V_I$ = GND | 1.65V to 5.5V | | | ±1 | µA |
| $I_I$ | Input leakage current | SCLK | $V_I$ = $V_{CC}$ | 1.65V to 5.5V | | | ±65 | µA |
| $I_I$ | Input leakage current | $\overline{CS}$ | $V_I$ = $V_{CC}$ | 1.65V to 5.5V | | | ±1 | µA |
| $I_I$ | Input leakage current | $\overline{CS}$ | $V_I$ = GND | 1.65V to 5.5V | | | ±65 | µA |
| $I_{CC}$ | Quiescent current | Standby mode | SDI, $\overline{CS}$ and $\overline{RESET}$ = $V_{CC}$, P port = $V_{CC}$ or GND, I/O = inputs, $I_O$ = 0mA, $f_{SCLK}$ = 0MHz, –40°C < $T_A$ ≤ 85°C, IO resistors disabled | 5.5V | | | 8 | µA |
| $I_{CC}$ | Quiescent current | Standby mode | SDI, $\overline{CS}$ and $\overline{RESET}$ = $V_{CC}$, P port = $V_{CC}$ or GND, I/O = inputs, $I_O$ = 0mA, $f_{SCLK}$ = 0MHz, –40°C < $T_A$ ≤ 85°C, IO resistors disabled | 3.6V | | | 7.5 | µA |
| $I_{CC}$ | Quiescent current | Standby mode | SDI, $\overline{CS}$ and $\overline{RESET}$ = $V_{CC}$, P port = $V_{CC}$ or GND, I/O = inputs, $I_O$ = 0mA, $f_{SCLK}$ = 0MHz, –40°C < $T_A$ ≤ 85°C, IO resistors disabled | 2.7V | | | 7.2 | µA |
| $I_{CC}$ | Quiescent current | Standby mode | SDI, $\overline{CS}$ and $\overline{RESET}$ = $V_{CC}$, P port = $V_{CC}$ or GND, I/O = inputs, $I_O$ = 0mA, $f_{SCLK}$ = 0MHz, –40°C < $T_A$ ≤ 85°C, IO resistors disabled | 1.95V | | | 7 | µA |

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over operating free-air temperature range (unless otherwise noted)

| PARAMETER | | | TEST CONDITIONS | $V_{CCP}$ $V_{CC}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| $I_{CC}$ | Quiescent current | Standby mode | SDI, $\overline{CS}$ and $\overline{RESET}$ = $V_{CC}$, P port = $V_{CC}$ or GND, I/O = inputs, $I_O$ = 0mA $f_{SCLK}$ = 0MHz, –40°C < $T_A$ ≤ 125°C, IO resistors disabled | 5.5V | | | 26 | µA |
| | | | | 3.6V | | | 24 | |
| | | | | 2.7V | | | 23.6 | |
| | | | | 1.95V | | | 23.4 | |
| | Active current | Active mode (5MHz) | SDI, $\overline{CS}$ and $\overline{RESET}$ = $V_{CC}$, P port = $V_{CC}$ or GND, I/O = inputs, $I_O$ = 0 mA $f_{SCLK}$ = 5MHz, continuous register reading with 100pF load on SDO | 5.5V | | | 4000 | µA |
| | | | | 3.6V | | | 3200 | |
| | | | | 2.7V | | | 3000 | |
| | | | | 1.95V | | | 2800 | |
| | | Active mode (10MHz) | SDI, $\overline{CS}$ and $\overline{RESET}$ = $V_{CC}$, P port = $V_{CC}$ or GND, I/O = inputs, $I_O$ = 0mA $f_{SCLK}$ = 10MHz, continuous register reading with 100pF load on SDO | 5.5V | | | 5200 | µA |
| | | | | 3.6V | | | 4200 | |
| | | | | 2.7V | | | 4000 | |
| | | | | 1.95V | | | 3600 | |
| $I_{BHL}$ | Bus-hold low sustaining current | | $V_I$ = 0.58 | 1.65V | 20 | | | uA |
| | | | $V_I$ = 0.70 | 2.3V | 45 | | | |
| | | | $V_I$ = 0.80 | 3V | 80 | | | |
| | | | $V_I$ = 1.35 | 4.5V | 100 | | | |
| $I_{BHH}$ | Bus-hold high sustaining current | | $V_I$ = 1.07 | 1.65V | | | -20 | uA |
| | | | $V_I$ = 1.70 | 2.3V | | | -45 | |
| | | | $V_I$ = 2.00 | 3V | | | -75 | |
| | | | $V_I$ = 3.15 | 4.5V | | | -100 | |
| $I_{BHLO}$ | Bus-hold low overdrive current | | Ramp input up VI = 0 to VCCI | 1.95V | | | 190 | uA |
| | | | | 2.7V | | | 250 | |
| | | | | 3.6V | | | 300 | |
| | | | | 5.5V | | | 450 | |
| $I_{BHHO}$ | Bus-hold high overdrive current | | Ramp input down VI = VCCI to 0 | 1.95V | -170 | | | uA |
| | | | | 2.7V | -250 | | | |
| | | | | 3.6V | -320 | | | |
| | | | | 5.5V | -490 | | | |
| $R_{pu(int)}$ | internal pull-up resistance | P port | | | 70 | 100 | 140 | kΩ |
| $R_{pd(int)}$ | internal pull-down resistance | | | | | | | |
| $C_I$ | Input pin capacitance | SCLK | $V_I$ = $V_{CC}$ or GND | 1.65V to 5.5V | | | 8 | pF |
| | | SDI | | | | | 8 | pF |
| | | $\overline{CS}$ | | | | | 8 | pF |
| | | $\overline{RESET}$ | | | | | 8 | pF |
| $C_{IO}$ | Input-output pin capacitance | P port | $V_{IO}$ = $V_{CC}$ or GND | 1.65V to 5.5V | | | 8.5 | pF |

(1) Each I/O must be externally limited to a maximum of 10mA

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## 5.6 Timing Requirements

over operating free-air temperature range (unless otherwise noted)

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| **$\overline{\text{RESET}}$** | | | | | |
| $t_w$ | Reset pulse duration, SDO $C_{LOAD}$ = 100pF | | 100 | | ns |
| $t_{REC}$ | Reset recovery time, SDO $C_{LOAD}$ = 100pF | | | 100 | ns |
| $t_{RESET}$ | Time to reset, SDO $C_{LOAD}$ = 100pF | | | 80 | ns |
| **Power-On Reset** | | | | | |
| $t_{FT}$ | Fall rate | | 0.1 | 2000 | ms |
| $t_{RT}$ | Rise rate | | 0.1 | 2000 | ms |
| $t_{TRR\_GND}$ | Time to re-ramp (when VCC drops to GND) | | 1 | | µs |
| $t_{TRR\_POR50}$ | Time to re-ramp (when VCC drops to VPOR_MIN – 50mV) | | 1 | | µs |
| $V_{CC\_GH}$ | Level that $V_{CC}$ can glitch down to, but not cause a functional disruption when $V_{CC\_GW}$ = 1µs | | | 1.2 | V |
| $T_{GW}$ | Glitch width that will not cause a functional disruption when $V_{CC\_GH}$ = 0.5 × $V_{CC}$ | | | 10 | µs |
| $V_{PORF}$ | Voltage trip point of POR on falling $V_{CC}$ | | 0.6 | | V |
| $V_{PORR}$ | Voltage trip point of POR on rising $V_{CC}$ | | | 1.0 | V |
| **Failsafe** | | | | | |
| $fs_{EN}$ | Failsafe IO enable time (100pF load) | Ouput High in normal mode and Output Low in fail safe mode | | 100 | ns |
| $fs_{EN}$ | Failsafe IO enable time (100pF load) | Output Low in normal mode and output high in fail safe mode | | 100 | ns |
| $fs_{EN}$ | Failsafe IO enable time (100pF load) | Ouput high in normal mode and input in fail safe mode (500ohm pull down load) | | 35 | ns |
| $fs_{EN}$ | Failsafe IO enable time (100pF load) | Output low in normal mode and input in fail safe mode (500ohm pull down load) | | 29 | ns |
| $fs_{DIS}$ | Failsafe IO disable time (100pF load) | Ouput High in normal mode and Output Low in fail safe mode | | 100 | ns |
| $fs_{DIS}$ | Failsafe IO disable time (100pF load) | Output Low in normal mode and output high in fail safe mode | | 100 | ns |
| $fs_{DIS}$ | Failsafe IO disable time (100pF load) | Input in normal mode and output high in fail safe mode (500ohm pull down load) | | 91 | ns |
| $fs_{DIS}$ | Failsafe IO disable time (100pF load) | Input in normal mode and output low in fail safe mode (500ohm pull down load) | | 63 | ns |
| **Digital IO** | | | | | |
| $T_{GW}$ | Digital glitch filter width | | 70 | 230 | ns |

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## 5.7 SPI Bus Timing Requirements

over operating free-air temperature range (unless otherwise noted)

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| **SPI Bus - 10MHz** | | | | |
| $f_{SCLK}$ | SPI clock frequency; 3.3V < $V_{CC}$ < 5.5V | | 10 | MHz |
| $t_{CSS}$ | $\overline{CS}$ to SCLK Rise Setup Time, SDO $C_{LOAD}$ = 100pF | 50 | | ns |
| $t_{CSH}$ | SCLK Fall to $\overline{CS}$ De-asserted Hold Time, SDO $C_{LOAD}$ = 100pF | 50 | | ns |
| $t_{CSD}$ | $\overline{CS}$ Disable Time, SDO $C_{LOAD}$ = 100pF | 50 | | ns |
| $t_{DS}$ | SDI to SCLK Setup Time, SDO $C_{LOAD}$ = 100pF | 10 | | ns |
| $t_{DH}$ | SDI to SCLK Hold Time, SDO $C_{LOAD}$ = 100pF | 10 | | ns |
| $t_{LOW}$ | SCLK Low Time, SDO $C_{LOAD}$ = 100pF | 45 | | ns |
| $t_{HIGH}$ | SCLK High Time, SDO $C_{LOAD}$ = 100pF | 45 | | ns |
| $t_{V\ (SDO)}$ | SDO Valid Time, $C_{LOAD}$ = 100pF | 0 | | ns |
| $t_{DIS\ (SDO)}$ | SDO Disable Time, $C_{LOAD}$ = 100pF | | 100 | ns |
| **SPI Bus - 5MHz** | | | | |
| $f_{SCLK}$ | SPI clock frequency; 1.71V < $V_{CC}$ < 5.5V | | 5 | MHz |
| $t_{CSS}$ | $\overline{CS}$ to SCLK Rise Setup Time, SDO $C_{LOAD}$ = 100pF | 50 | | ns |
| $t_{CSH}$ | SCLK Fall to $\overline{CS}$ De-asserted Hold Time, SDO $C_{LOAD}$ = 100pF | 100 | | ns |
| $t_{CSD}$ | $\overline{CS}$ Disable Time, SDO $C_{LOAD}$ = 100pF | 100 | | ns |
| $t_{DS}$ | SDI to SCLK Setup Time, SDO $C_{LOAD}$ = 100pF | 10 | | ns |
| $t_{DH}$ | SDI to SCLK Hold Time, SDO $C_{LOAD}$ = 100pF | 10 | | ns |
| $t_{LOW}$ | SCLK Low Time, SDO $C_{LOAD}$ = 100pF | 90 | | ns |
| $t_{HIGH}$ | SCLK High Time, SDO $C_{LOAD}$ = 100pF | 90 | | ns |
| $t_{V\ (SDO)}$ | SDO Valid Time, $C_{LOAD}$ = 100pF | | 54 | ns |
| $t_{DIS\ (SDO)}$ | SDO Disable Time, $C_{LOAD}$ =100pF | | 100 | ns |

## 5.8 Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | | FROM (INPUT) | TO (OUTPUT) | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $t_{iv}$ | Interrupt valid time, INT $C_{LOAD}$ = 100pF and $R_{PU}$ = 4.7kΩ | P port | $\overline{INT}$ | | | 0.2 | µs |
| $t_{ir}$ | Interrupt reset delay time, INT $C_{LOAD}$ = 100pF and $R_{PU}$ = 4.7kΩ | SCLK | $\overline{INT}$ | | | 0.4 | µs |
| $t_{pv}$ | Output data valid time, SDO $C_{LOAD}$ = 100pF | SCLK | P port | | | 100 | ns |
| $t_{ps}$ | Input data setup time, SDO $C_{LOAD}$ = 100pF | P port | SCLK | 26 | | | ns |
| $t_{ph}$ | Input data hold time, SDO $C_{LOAD}$ = 100pF | SCLK | P port | 2.5 | | | ns |

# 6 Parameter Measurement Information

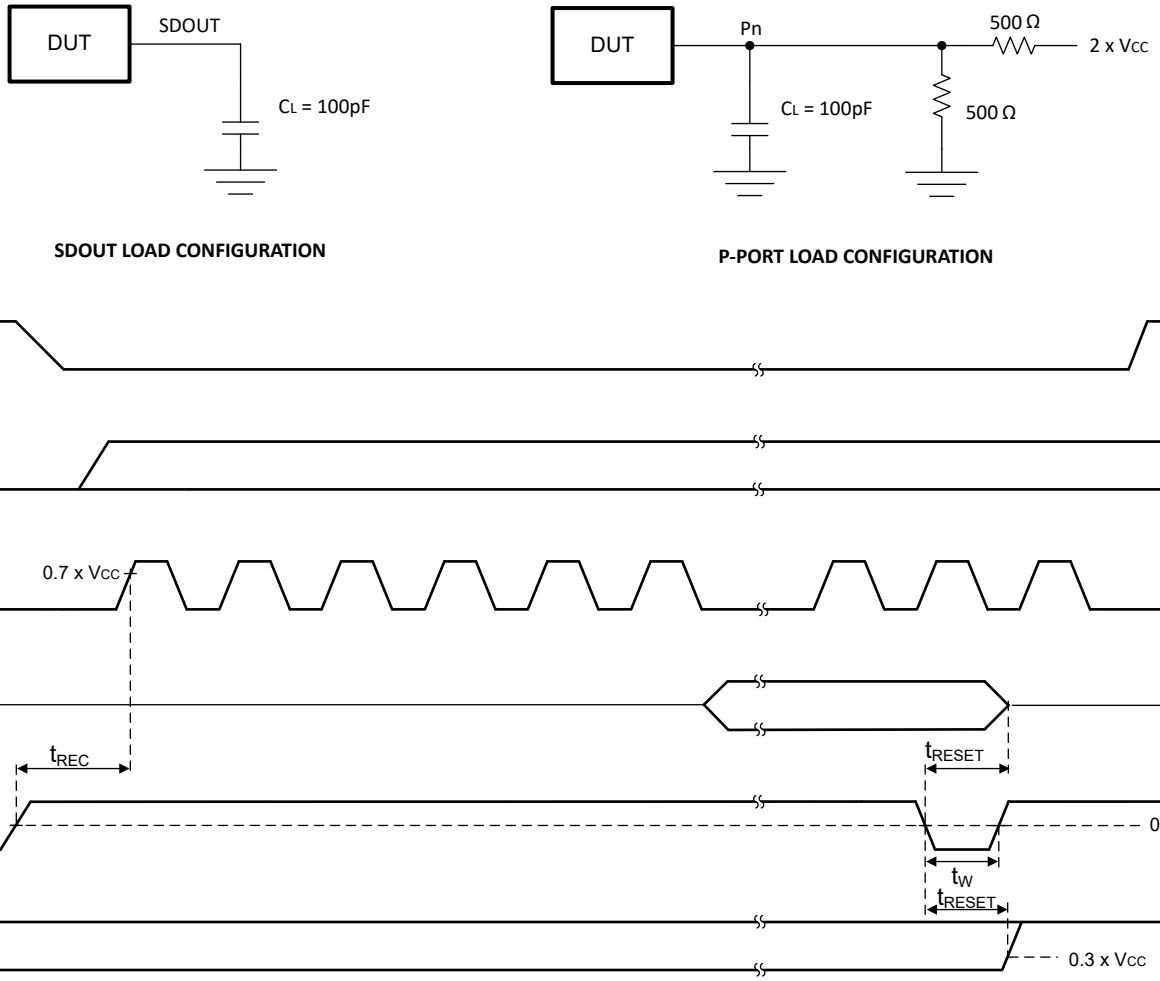


**Figure 6-1. Reset Load Configuration**

A. 1. $C_L$ includes probe and jig capacitance.
2. All inputs are supplied by generators having the following characteristics: PRR ≤ 10MHz; Zo = 50Ω; tr/tf ≤ 30ns.
3. All parameters and waveforms are not applicable to all devices.

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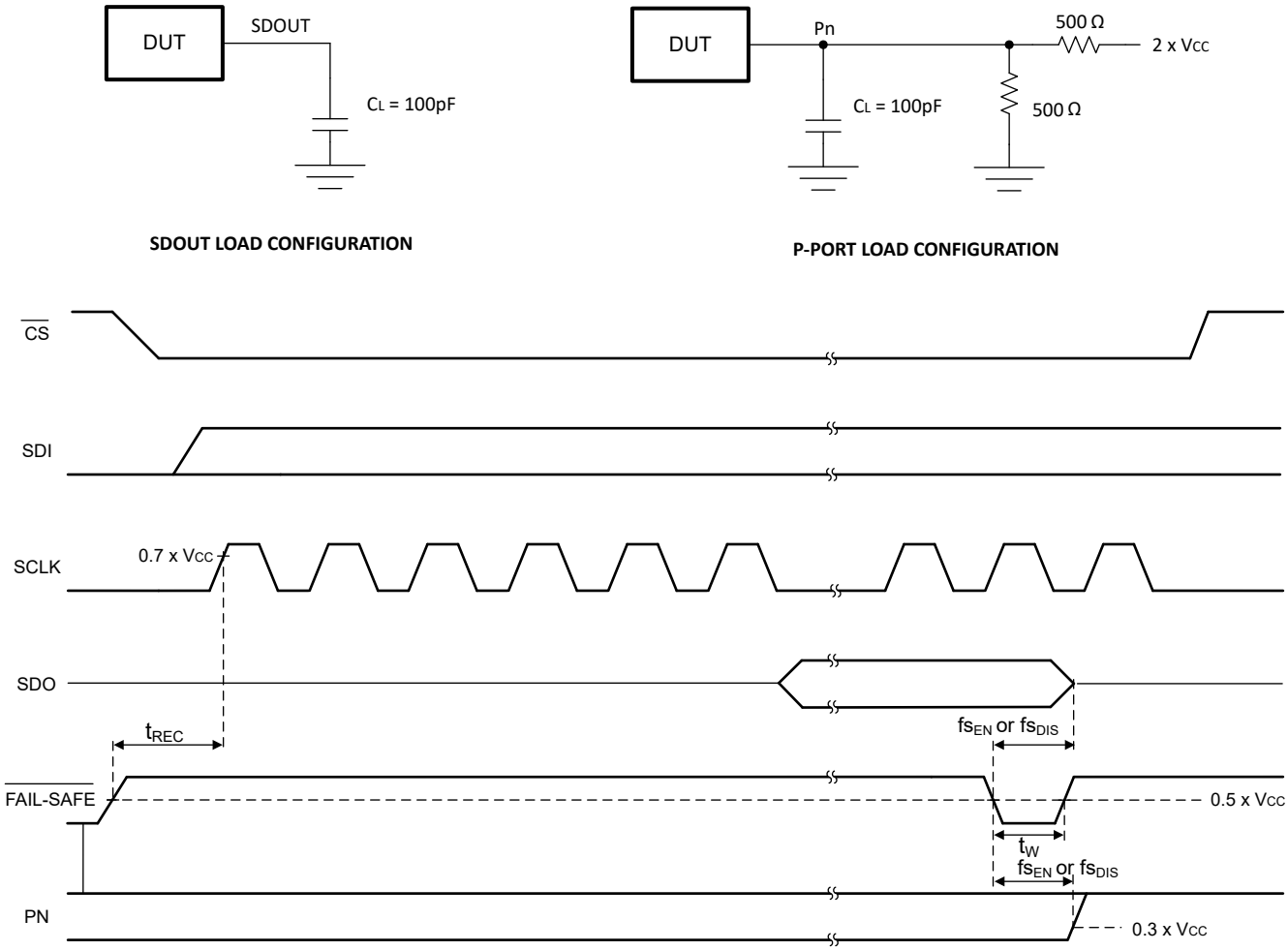
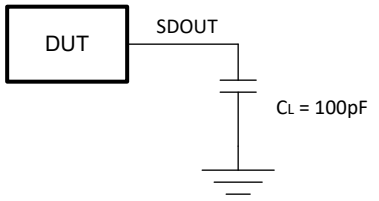



**Figure 6-2. Fail-safe Load Configuration**

A. 1. $C_L$ includes probe and jig capacitance.
2. All inputs are supplied by generators having the following characteristics: PRR ≤ 10MHz; Zo = 50Ω; tr/tf ≤ 30ns.
3. FAIL-SAFE pin is a shared pin with RESET pin.
4. All parameters and waveforms are not applicable to all devices.




**SDOUT LOAD CONFIGURATION**

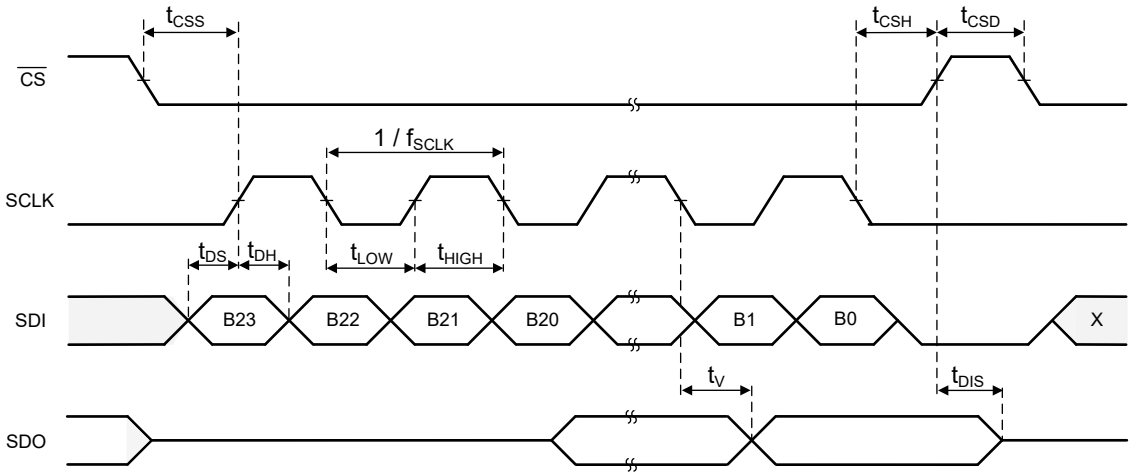
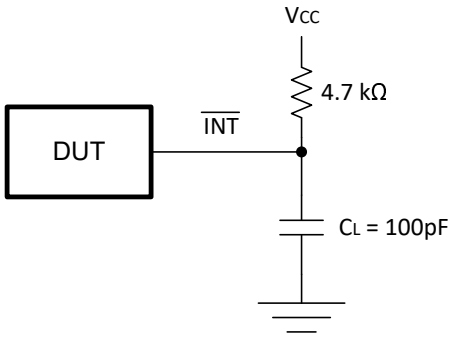



**Figure 6-3. SPI Timing Diagram - Input**

A. $C_L$ includes probe and jig capacitance.




**INTERRUPT LOAD CONFIGURATION**

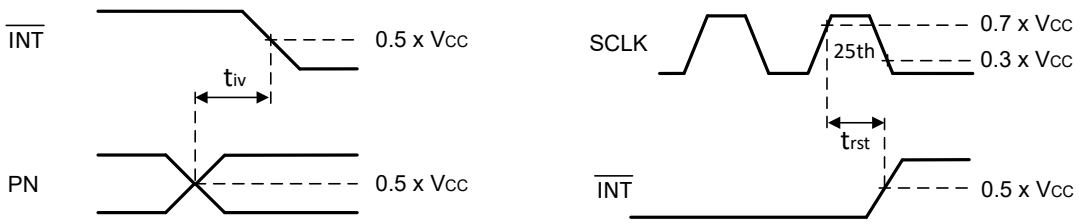



**Figure 6-4. Interrupt Load Configuration**

A. 1. $C_L$ includes probe and jig capacitance.

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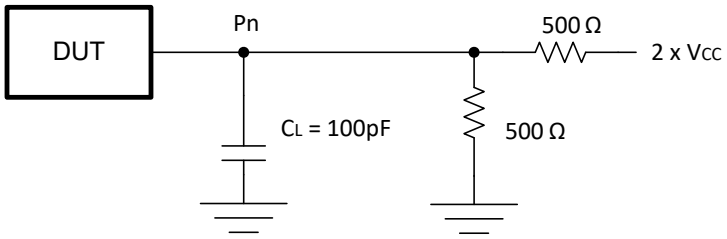
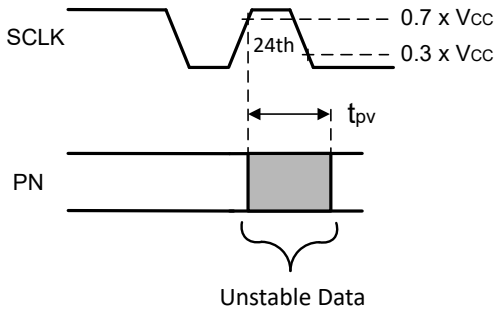
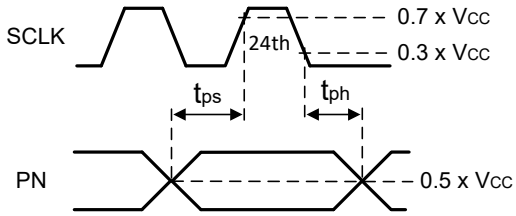
2. All inputs are supplied by generators having the following characteristics: PRR ≤ 10MHz; Zo = 50Ω; tr/tf ≤ 30ns.




**P-PORT LOAD CONFIGURATION**




**WRITE MODE (R/$\overline{W}$ = 0)**




**READ MODE ($\overline{R}$/W = 1)**

**Figure 6-5. P-Port Load Configuration and Timing Waveforms**

A. 1. $C_L$ includes probe and jig capacitance.
2. $t_{pv}$ is measured from 0.7 × $V_{CC}$ on SCLK to 50 % I/O (Pn) output.
3. All inputs are supplied by generators having the following characteristics: PRR ≤ 10MHz; Zo = 50Ω; tr/tf ≤ 30ns.

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# 7 Detailed Description

## 7.1 Overview

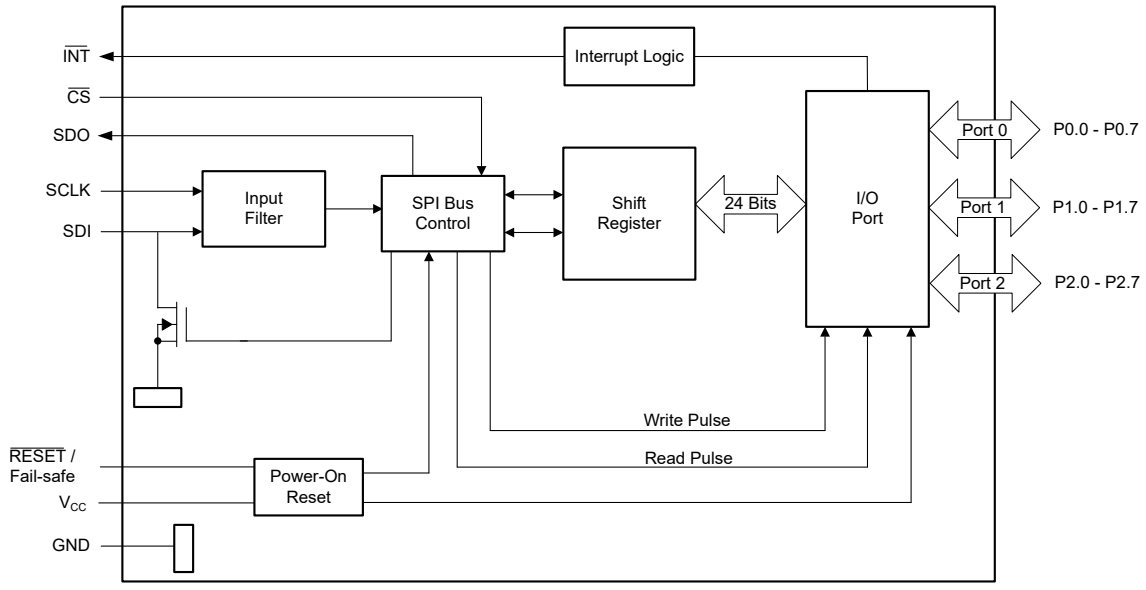
The TXE81xx-Q1 digital core consists of 24-bit registers which allow the user to configure the I/O port characteristics. At power on or after a reset, the I/Os are configured as inputs. However, the system controller can configure the I/Os as either inputs or outputs by writing to the direction configuration registers. The data for each input or output is kept in the corresponding Input Port or Output Port register. The polarity of the Input Port register can be inverted with the Polarity Inversion register. All registers except software reset register can be read by the system controller. Additionally, the TXE81xx-Q1 has Agile I/O functionality which is specifically targeted to enhance the I/O ports. The Agile I/O features and registers include programmable pull-up and pull-down resistors, latchable inputs, maskable interrupts, interrupt status register, and individual programmable open-drain or push-pull outputs. These configuration registers improve the I/O by increasing flexibility and allowing the user to optimize their design for power consumption, speed, and EMI.

Other features of the device include an interrupt that is generated on the $\overline{INT}$ pin whenever an input port changes state. The device can be reset to its default state by applying a low logic level to the $\overline{RESET}$ pin, issuing a software reset command, or by cycling power to the device and causing a power-on reset.

The TXE81xx-Q1 open-drain interrupt ($\overline{INT}$) output is activated when any input state differs from its corresponding Input Port register state and is used to indicate to the system controller that an input state has changed. The $\overline{INT}$ pin can be connected to the interrupt input of a processor. By sending an interrupt signal on this line, the device can inform the processor if there is incoming data on the remote I/O ports without having to communicate via the SPI bus. Thus, the device can remain a simple target device.

The system controller can reset the device in the event of a timeout or other improper operation by asserting a low on the $\overline{RESET}$ input pin or by cycling the power to the $V_{CC}$ pin and causing a power-on reset (POR). A reset puts the registers in their default state and initializes the SPI state machine. The $\overline{RESET}$ feature and a POR cause the same reset/initialization to occur, but the $\overline{RESET}$ feature does so without needing to power down the device.

## 7.2 Functional Block Diagrams




A. All I/Os are set to inputs at reset.

**Figure 7-1. Logic Diagram**

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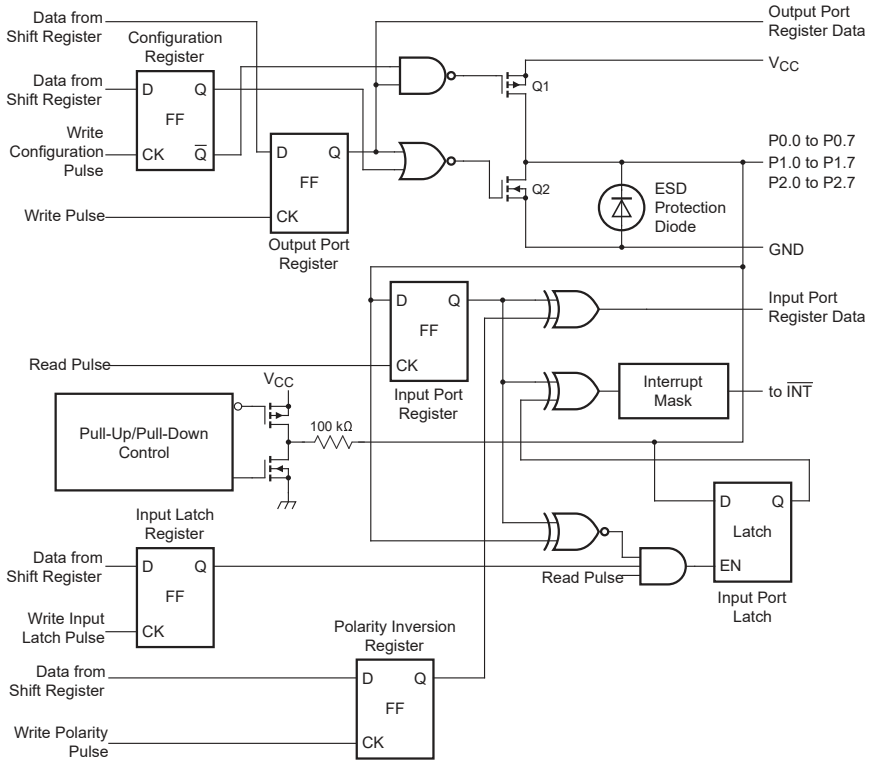



A. On power up or reset, all registers return to default values.

**Figure 7-2. Simplified Schematic of P0.0 to P2.7**

## 7.3 Feature Description

### *7.3.1 I/O Port*

When an I/O is configured as an input, FETs Q1 and Q2 are off (see Figure 7-2), which creates a high-impedance input. The input voltage may be raised above the supply voltage to a maximum of 5.5V.

If the I/O is configured as an output, Q1 or Q2 is enabled, depending on the state of the output port register. In this case, there are low-impedance paths between the I/O pin and either supply or GND. The external voltage applied to this I/O pin should not exceed the recommended levels for proper operation.

### *7.3.2 Interrupt Output ($\overline{INT}$)*

An interrupt is generated by any rising or falling edge of the port inputs in the input mode provided the interrupt feature is unmasked. After time $t_{iv}$, the $\overline{INT}$ signal is valid. Resetting the interrupt circuit is achieved when data on the port is changed back to the original setting or when data is read from the Interrupt Flag Status register. Resetting occurs in the read mode after the rising edge of the SCLK signal. Interrupts can be lost (or be very short) due to the resetting of the interrupt during this pulse. Each change of the I/Os after resetting is detected and is transmitted as $\overline{INT}$.

Reading from or writing to another device does not affect the interrupt circuit, and a pin configured as an output cannot cause an interrupt. Changing an I/O from an output to an input may cause a false interrupt to occur if the state of the pin does not match the contents of the input port register.

The $\overline{INT}$ output has an open-drain structure and requires an external pull-up resistor to$V_{CC}$ if the interrupt feature is required, otherwise it may be left floating.

### *7.3.3 Reset Input ($\overline{RESET}$)*

The $\overline{RESET}$ input can be asserted to initialize the system while keeping the $V_{CC}$ supply at its operating level. A reset can be accomplished by holding the $\overline{RESET}$ pin low for a minimum of $t_W$. The TXE81xx-Q1 registers and

SPI state machine are changed to their default state once $\overline{\text{RESET}}$ is set LOW. When $\overline{\text{RESET}}$ is set HIGH, the I/O levels at the P port can be changed externally or through the controller. This input requires a pull-up resistor to $V_{CC}$, if no active connection is used. When $\overline{\text{RESET}}$ is toggled the input port register is updated to reflect the state of the GPIO pins.

### *7.3.4 Fail-safe Mode*

The SPI controller has the option to set TXE81xx-Q1 to be in a failsafe state by configuring the reset pin as a failsafe pin. The SPI controller needs to to program the Fail-safe Enable Register to enable this feature and change the functionality of the pin from reset to fail-safe.

This register can get cleared during a POR event or other fault scenarios. The SPI controller has to rewrite this register every time if there is a fault scenario which will generate an interrupt to the SPI controller. After the interrupt is generated, the SPI controller can read the fault flag register to understand the source of the interrupt.

The bit 0 in fail-safe enable register must be 1 to configure TXE81xx-Q1 to be fail-safe mode.

Two device configuration registers have to be written to program I/O configuration to ensure redundancy. If either of these registers get corrupted, and the contents don't match, an interrupt will be generated.

### *7.3.5 Software Reset Call*

The software reset call is a command sent from the controller on the SPI bus that instructs the SPI target devices that support the command to be reset to the power-up default state.

TXE81xx--Q1 devices use a 24-bit SPI frame for communication. For example, to trigger register reset via software reset command, the controller can configure the SPI frame as the following:

| B23 | B22 | B21 | B20 | B19 | B18 | B17 | B16 | B15 | B14 | B13 | B12 | B11 | B10 | B9 | B8 | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |

Here is the sample code for this command on the controller side:

```
// Define the SPI register addresses
#define REGISTER_ADDRESS 0x1A00 // Register address of reset register
#define DATA_BITS 0x2 // Set B1 as 1 and B0 as 0 to trigger register reset
#define READ_WRITE_BIT 0 // 0 for Write operation, 1 for Read operation

// Function to send a 24-bit SPI frame to the I/O expander (MSB First)
void SPI_Send(uint32_t data) {
    // Using a hardware SPI peripheral to send the 24-bit data bit by bit (MSB first)
    for (int i = 23; i >= 0; i--) {
    SPI_Transmit((data >> i) & 0x01); // Shift out MSB first
    }
}
// Function to send software reset command to the SPI I/O expander
void SPI_Software_Reset(void) {
    uint32_t frame = 0;

    // Set the Read/Write bit (bit 23)
    frame |= (READ_WRITE_BIT << 23);
```

```
    // Set the Register Address (bits 20-16)
    frame |= (REGISTER_ADDRESS << 16);

    // Set the Data bits (bits 7-0)
     frame |= (DATA_BITS & 0xFF); // Ensure we only use the lower 8 bits

    // Pull CS low to select the target device
    CS_LOW();
    // Send the constructed SPI frame (MSB first)
    SPI_Send(frame);

    // Pull CS high to deselect the device after transmission
    CS_HIGH();
}
```

### 7.3.6 Burst Mode

In Burst Mode Read Transactions, the initial address is specified by the controller device and sent to the peripheral. For subsequent accesses, the address is automatically incremented to the next valid address (second address byte) corresponding to the next port. This automatic address increment continues as long as the CS remains active low and SCLK pulses are received by the peripheral device.

The burst mode transaction continues sequentially, automatically advancing the address for each valid port address, until the last port address is reached for the specified feature (first address byte). Once the last valid port address is reached, the peripheral will output all 0s from SDO, indicating the end of the valid data sequence.

It is important to note that Burst Mode will not automatically increment to a new feature address after reaching the last port address of a given feature. The controller must manually specify the new feature address if needed for further transactions.

### 7.3.7 Daisy Chain

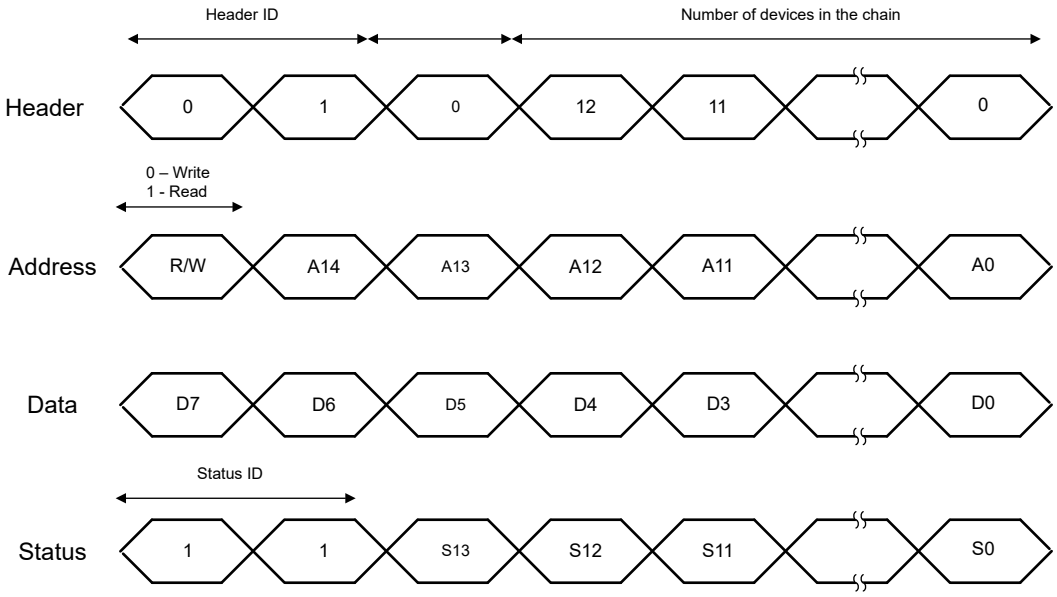
Multiple TXE81XX devices can be connected in a daisy chain configuration to expand the number of I/O ports supported. The controller first transmits the register address of the farthest device in the chain (the device furthest from the controller's SDI and closest to the controller's SDO). Following the header, this register address is sent first, initiating communication with the farthest device.

As the communication progresses along the chain, the register address of each subsequent device is transmitted in order. Finally, the register address of the closest device to the controller (connected to the SDI closest to the controller) is sent last. This ensures that data flows sequentially through the chain, with each device receiving and forwarding data to the next device in the sequence.

Each SPI transaction consists of 4 types of segments: Status, Header, Address (Register Address) and Data as shown below. Header is an optional segment, present only when daisy chain is enabled.

The SPI data input data on SDI is sampled on the low to high edge of SCLK. The SPI output data on SDO is changed on the high to low edge of SCK.

Following are the frames for the daisy chained transaction. The same sequencing is repeated throughout the entire chain until the final device is reached.




**Header segment**

Bit 15 and 14 in Header segment are the Header ID. This is used by the device controller to detect that a header segment is being received.

Bit [15:14]: the Header ID which are 0 and 1 to indicate this is a Header segment.

Bit [13]: Reserved.

Bit [12:0]: Bit 12 to 0 in Header segment determine the number of devices in the daisy chain.

**Address segment (Register Address)**

Bit 15 indicates SPI mode of operation (1 = Read operation 0 = Write operation). Refer to the first and second byte in Figure 7-3

**Status segment**

Status segment is 16 bits and the following is the data format:

Bit [15:14]: Both of Bit 15 and 14 are 1 to indicate this is a Status segment.

Bit [13:8]: Bit 5 to 0 in the Fault status register, refer to Fault status register.

Bit [7:0]: Bit 7 to 0 are 0.

For example, if there is a SPI daisy chain topology for a MCU and two SPI peripheral devices, the following is the diagram and data format between the devices:

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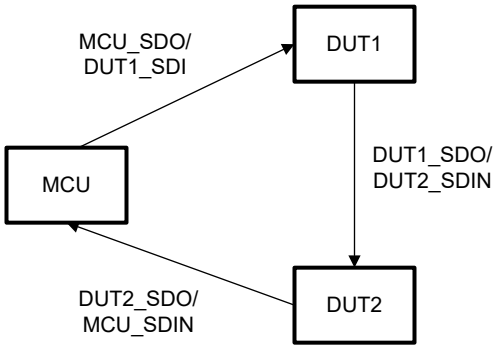


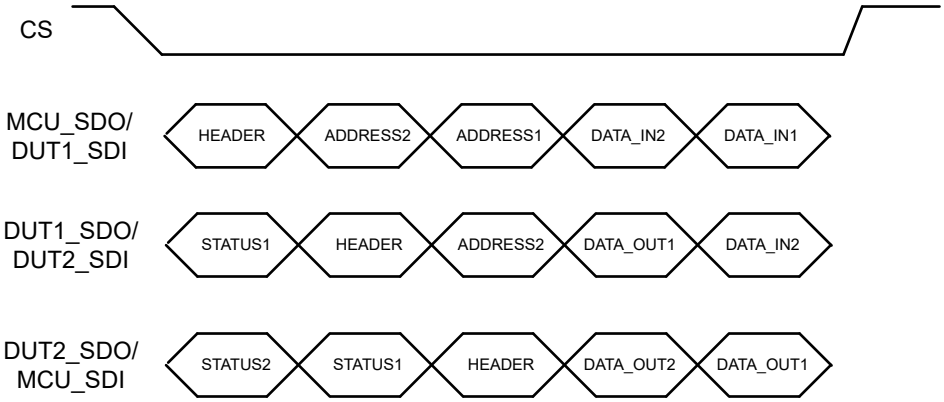


The register address of the farthest device (farthest from MCU's SDI/closest to MCU's SDO) is sent first by the MCU after the Header and address of the closest device (SDI closest) is sent last by the MCU.

### *7.3.8 Multi Port*

The LSB of the second byte enables the multi-port feature. When this bit is 1, each bit of the data byte refers to individual ports. So, LSB bit B0 refers to P0 port, B1 refers to P1 port, B2 refers to P2 port. All I/Os in a particular port will have the same configuration when multi-port programming is used.

For example, to set all I/Os in P1 as 1, the controller can configure the GPIO direction as output and then set P1 port.

Here is the sample code for this command on the controller side:

```
// Define the SPI register addresses
#define REGISTER_ADDR_DIR 0x400 // Register address of Direction Configuration Register
#define REGISTER_ADDR_OUTPUT 0x300 // Register address of Output Port Register
#define DATA_BITS 0x2 // Set B1 as 1 and B0 as 0 to set P1 port
#define READ_WRITE_BIT 0 // 0 for Write operation, 1 for Read operation

// Function to send a 24-bit SPI frame to the I/O expander (MSB First)
void SPI_Send(uint32_t data) {
    // Using a hardware SPI peripheral to send the 24-bit data bit by bit (MSB first)
    for (int i = 23; i >= 0; i--) {
```

```
        SPI_Transmit((data >> i) & 0x01); // Shift out MSB first
    }
}
// Function to send multi-port command to the SPI I/O expander
void SPI_Multi_Port_Dir(void) {
    uint32_t frame = 0;
    // Set the Read/Write bit (bit 23)
    frame |= (READ_WRITE_BIT << 23);
    // Set the Register Address (bits 20-16)
    frame |= (REGISTER_ADDR_DIR << 16);
    // Set the Data bits (bits 7-0)
    frame |= (DATA_BITS & 0xFF); // Ensure we only use the lower 8 bits
    // Pull CS low to select the target device
    CS_LOW();
    // Send the constructed SPI frame (MSB first)
    SPI_Send(frame);
    // Pull CS high to deselect the device after transmission
    CS_HIGH();
}
void SPI_Multi_Port_Output(void) {
    uint32_t frame = 0;
    // Set the Read/Write bit (bit 23)
    frame |= (READ_WRITE_BIT << 23);
    // Set the Register Address (bits 20-16)
    frame |= (REGISTER_ADDR_OUTPUT << 16);
    // Set the Data bits (bits 7-0)
    frame |= (DATA_BITS & 0xFF); // Ensure we only use the lower 8 bits
    // Pull CS low to select the target device
    CS_LOW();
    // Send the constructed SPI frame (MSB first)
    SPI_Send(frame);
    // Pull CS high to deselect the device after transmission
    CS_HIGH();
}
```

## 7.4 Device Functional Modes

### 7.4.1 Power-On Reset

When powering the device from 0V is applied to $V_{CC}$, an internal power-on reset holds the TXE81xx-Q1 in a reset condition until the supply has reached $V_{POR}$. At that time, the reset condition is released, and the TXE81xx-Q1 registers and SPI state machine initializes to their default states. After that, $V_{CC}$ must be lowered to below $V_{PORF}$ and back up to the operating voltage for a power-reset cycle.

## 7.5 Programming

### 7.5.1 SPI Interface

The TXE81xx-Q1 uses a SPI interface to set device configurations, operating parameters and read out diagnostic information. The SPI protocol uses three inputs and one output; serial clock (SCLK), active LOW chip select ($\overline{CS}$), serial data in (SDI) and serial data out (SDO). $\overline{CS}$ must be driven low before clock pulses and data into the device. When $\overline{CS}$ is high, the device ignores all activity on SCLK and SDIN.

The TXE81xx-Q1 devices support SPI mode 0 which means both SDIN and SDO are 0, other SPI modes are not supported.

Besides SPI bus with independent chip select, daisy chain configuration is also supported in TXE81xx-Q1. It allows multiple peripherals to be connected in series, with the output of one device feeding into the input of the next. Daisy chain is benefitial to reduce the number of $\overline{CS}$ lines, as only one is needed for the entire chain. Data is shifted through all devices in the chain during each clock cycle.

### 7.5.2 SPI Data Format

The data format of the TXE81xx-Q1 is shown in Figure 7-3.

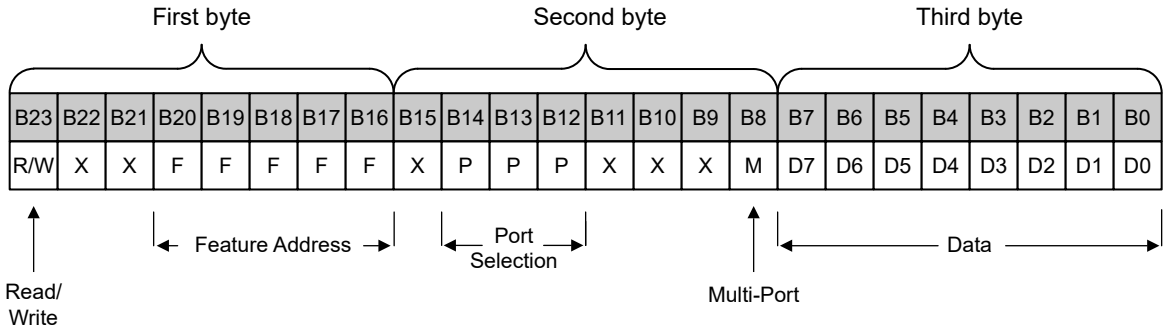


**Figure 7-3. TXE81xx-Q1 SPI Word Address**

The length of TXE81xx-Q1 SPI word is 24 bits, shift 24 bits of data into the device in a MSB first fashion. SPI data must be stable during the rising edge of SCLK.

SDI data length must be at least 24 bits or [16 + (N*8)] bits (N is number of data byte to write; N ≥ 1). For reading data output via SDO, the data bytes start to be read back after the first 16 address bits.

### 7.5.3 Writes

SPI Write operation is used to send data from the controller device to the peripheral device. This operation is performed over the SPI bus , where the controller device controls the clock (SCLK) and sends data to the peripheral. SPI Write is commonly used to configure peripherals, send control commands, or transfer data.

**SPI Write Steps**

1. Drive CS low. This enables the internal shift register.
2. Shift 24 bits of data into the device in a MSB first fashion, MSB bit . Data must be stable during the rising edge of SCLK.
3. The MSB bit must be a '0' indicating it is a write operation.
4. 16 bits of status is sent out on SDO. The first 2 bits are 2’b11 (indicating it to be a status segment). The next 6 bits are the Bit 5 to 0 of the Fault status register. The last 8 bits are all 0s.
5. After the last bit of data is transferred, drive SCLK low if there is no more data to be transferred.
6. The previous content of the register is sent out on SDO as the data byte is driven on SDIN
7. De-assert CS (drive it high) to end of write cycle.

### 7.5.4 Reads

The SPI Read operation for TXE81xx is used to retrieve data from a specific register.

This operation involves sending a command to the TXE81xx to access a register and read its data.

**SPI Read Operation Steps :**

1. Drive CS low. This enables the internal shift register.
2. Shift 24 bits of data into the device in a MSB first fashion. Data must be stable during the rising edge of SCLK
3. The MSB bit must be a '1' indicating it is a read only transfer.
4. The third data byte is NOP (no operation) which is dummy data byte.
5. 16 bits of status is sent out on SDO. The first 2 bits are 2’b11 (indicating it to be a status segment). The next 6 bits are the bit 5 to 0 of the Fault status register. The last 8 bits are all 0s.
6. The read data is shifted out on SDO following the status bits.
7. After the last bit of data is transferred, drive SCLK low if there is no more data to be transferred.
8. De-assert CS (drive it high) to end of read cycle.

## 7.6 Register Maps

### *7.6.1 Control Register: Read/Write and Feature Address (B23 - B16)*

Communication is initiated by taking the $\overline{CS}$ pin low and clocking the SCLK pin. The first byte of the communciation are read/write configuration as well as various feature settings. The command address controls the function (input, output, polarity inversion, fail-safe etc.) while the Port address selects which ports are used. The enable/disable multi-port bit is the LSB of the second byte (B8).

Once a new command has been sent, the register that was addressed continues to be accessed by reads until a new command byte has been sent. Upon power-up, hardware reset, or software reset, the control register defaults to 0x0.

| CONTROL REGISTER (FEATURE ADDRESS) | | | | | COMMAND BYTE (HEX) | REGISTER | MULTI PORT | PROTOCOL | POWER-UP DEFAULT |
|---|---|---|---|---|---|---|---|---|---|
| B20 | B19 | B18 | B17 | B16 | | | | | |
| 0 | 0 | 0 | 0 | 0 | 0x0 | Scratch Register | No | Read/write byte | 0x0 |
| 0 | 0 | 0 | 0 | 1 | 0x1 | Device_ID | No | Read byte | 0x0 - TXE8116<br>0x1 - TXE8124 |
| 0 | 0 | 0 | 1 | 0 | 0x2 | Input Port Register | Yes | Read byte | 0x0 |
| 0 | 0 | 0 | 1 | 1 | 0x3 | Output Port Register | Yes | Read/write byte | 0x0 |
| 0 | 0 | 1 | 0 | 0 | 0x4 | Direction Configuration Register | Yes | Read/write byte | 0x0 |
| 0 | 0 | 1 | 0 | 1 | 0x5 | Polarity Inversion Register | Yes | Read/write byte | 0x0 |
| 0 | 0 | 1 | 1 | 0 | 0x6 | Push Pull / Open Drain Selection Register | Yes | Read/write byte | 0x0 |
| 0 | 0 | 1 | 1 | 1 | 0x7 | Open Drain Configuration Register | Yes | Read/write byte | 0x0 |
| 0 | 1 | 0 | 0 | 0 | 0x8 | Pull Up or Pull Down Enable Register | Yes | Read/write byte | 0x0 |
| 0 | 1 | 0 | 0 | 1 | 0x9 | Pull Up or Pull Down Selection Register | Yes | Read/write byte | 0x0 |
| 0 | 1 | 0 | 1 | 0 | 0xA | Bus Holder Register | Yes | Read/write byte | 0x0 |
| 0 | 1 | 1 | 0 | 0 | 0xB | Smart Interrupt Register | No | Read/write byte | 0x0 |
| 0 | 1 | 1 | 0 | 1 | 0xC | Interrupt Mask Register | Yes | Read/write byte | 0xFF |
| 0 | 1 | 1 | 1 | 0 | 0xD | Input Glitch Filter Enable Register | No | Read/write byte | 0x0 |
| 0 | 1 | 1 | 1 | 1 | 0xE | Interrupt Flag Status Register | No | Read byte | 0x0 |
| 1 | 0 | 0 | 0 | 0 | 0xF | Interrupt Port Status Register | No | Read byte | 0x0 |
| 1 | 0 | 0 | 1 | 0 | 0x12 | Fail-safe Enable Register 1 | No | Read/write byte | 0x0 |
| 1 | 0 | 0 | 1 | 1 | 0x13 | Fail-safe Enable Register 2 | Yes | Read/write byte | 0x0 |
| 1 | 0 | 1 | 0 | 0 | 0x14 | Fail-safe Direction Configuration Register 1 | Yes | Read/write byte | 0x0 |
| 1 | 0 | 1 | 0 | 1 | 0x15 | Fail-safe Direction Configuration Register 2 | Yes | Read/write byte | 0x0 |
| 1 | 0 | 1 | 1 | 0 | 0x16 | Fail-safe Output Register 1 | Yes | Read/write byte | 0x0 |
| 1 | 0 | 1 | 1 | 1 | 0x17 | Fail-safe Output Register 2 | Yes | Read/write byte | 0x0 |

| CONTROL REGISTER (FEATURE ADDRESS) | | | | | COMMAND BYTE (HEX) | REGISTER | MULTI PORT | PROTOCOL | POWER-UP DEFAULT |
|---|---|---|---|---|---|---|---|---|---|
| B20 | B19 | B18 | B17 | B16 | | | | | |
| 1 | 1 | 0 | 0 | 0 | 0x18 | Fail-safe Redundancy Check Register | No | Read/write byte | 0x0 |
| 1 | 1 | 0 | 0 | 1 | 0x19 | Fault Status Register | No | Read byte | 0x1 |
| 1 | 1 | 0 | 1 | 0 | 0x1A | Software Reset Register | No | Write byte | 0x0 |

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### 7.6.2 Control Register: Port Selection and Multi Port (B15 - B8)

The second byte specifies which I/O port will be configured and the multi port enable/disable. The multi port bit allows the device to handle the multiple ports in parallel. When this bit is set to 1, each bit in the data byte (third byte) refers to the individual port. For example, bit 0 in the data byte refers to P0 port, bit 1 refers to P1 port and bit 2 refers to P2 port. All I/Os in a particular port have the same configuration when multi port is enabled.

| CONTROL REGISTER (PORT SELECTION) | | | Port |
|---|---|---|---|
| B14 | B13 | B12 | |
| 0 | 0 | 0 | IO Port 0 |
| 0 | 0 | 1 | IO Port 1 |
| 0 | 1 | 0 | IO Port 2 |

### 7.6.3 Register Descriptions

This chapter gives the descriptions for each register, Register Address is the first and second byte in TXE81xx-Q1 SPI word, and Default Value is the power up default value in the register which is the third byte in TXE81xx-Q1 SPI word.

B23 (read/write bit) and B8 (multi port bit) are not considered in this chapter. A high (1) on B23 selects a read operation, while a low (0) on B23 selects a write operation. To enable multi port, a high (1) on B8 needs to be set.

**Scratch Register (Register Address: 0x0, Default Value: 0x0)**

The scratch register is a test register to read/write code from/to a blank register and resolve any coding issues.

**Device ID Register (Register Address: 0x100, Default Value: 0x0)**

Device ID register is a read-only register that has the device ID, DEV_ID = 0x0.

**Input Port Register (Register Address: 0x200 - 0x220, Default Value: 0x0)**

The input port registers reflect the incoming logic levels of the IO pins. The Input port registers are read only; writing to these registers have no effect.

**Table 7-1. Input Port Register 0, 1 and 2**

| Port ID | Register Address | Bit Value |
|---|---|---|
| 0 | 0x200 | 0 - Low; 1 - high |
| 1 | 0x210 | |
| 2 | 0x220 | |

**Output Port Register (Register Address: 0x300 - 0x320, Default Value: 0x0)**

The output port registers show the outgoing logic levels of the IO pins defined as outputs by the direction configuration register. Bit values in these registers have no effect on IO pins defined as inputs.

**Table 7-2. Output Port Register 0, 1 and 2**

| Port ID | Register Address | Bit Value |
|---|---|---|
| 0 | 0x300 | 0 - Low; 1 - high |
| 1 | 0x310 | |
| 2 | 0x320 | |

**Direction Configuration Register (Register Address: 0x400 - 0x420, Default Value: 0x0)**

The Direction Configuration registers configure the direction of the I/O pins. If a bit in these registers is set to 0, the corresponding port pin is enabled as a high-impedance input. If a bit in these registers is set to 1, the corresponding port pin is enabled as an output.

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**Table 7-3. Direction Configuration Register 0, 1 and 2**

| Port ID | Register Address | Bit Value |
|---|---|---|
| 0 | 0x400 | 0 - Input; 1 - Output |
| 1 | 0x410 | |
| 2 | 0x420 | |

### Polarity Inversion Register (Register Address: 0x500 - 0x520, Default Value: 0x0)

The polarity inversion registers allow polarity inversion of IO pins defined as inputs or outputs by the direction configuration register. If a bit in these registers is set to 1, the polarity of the corresponding port pin is inverted in the input register. If a bit in this register is set to 0, the polarity of the corresponding port is not inverted.

While in input mode, if polarity inversion is enabled, although there is an internal state toggle, no interrupt will be generated.

**Table 7-4. Polarity Inversion Register 0, 1 and 2**

| Port ID | Register Address | Bit Value |
|---|---|---|
| 0 | 0x500 | 0 - Non inverted; 1 - Inverted |
| 1 | 0x510 | |
| 2 | 0x520 | |

### Push Pull / Open Drain Selection Register (Register Address: 0x600 - 0x620, Default Value: 0x0)

The push pull / open drain selection registers configure the output type. If a bit in these registers is set to 0, the corresponding port pin is enabled as a push pull output. If a bit in these registers is set to 1, the corresponding port pin is enabled as an open drain output.

**Table 7-5. Push Pull / Open Drain Selection Register 0, 1 and 2**

| Port ID | Register Address | Bit Value |
|---|---|---|
| 0 | 0x600 | 0 - Push pull; 1 - Open drain |
| 1 | 0x610 | |
| 2 | 0x620 | |

### Open Drain Configuration Register (Register Address: 0x700 - 0x720, Default Value: 0x0)

If the Open Drain enable bit is set in the output configuration register, the open drain configuration register will determine whether the open drain in NMOS type or released.

**Table 7-6. Open Drain Configuration Register 0, 1 and 2**

| Port ID | Register Address | Bit Value |
|---|---|---|
| 0 | 0x700 | 0 - NMOS type; 1 - released |
| 1 | 0x710 | |
| 2 | 0x720 | |

### Pull Up or Pull Down Enable Register (Register Address: 0x800 - 0x820, Default Value: 0x0)

The pull-up or pull-down enable registers allow the user to enable or disable pull-up/pull-down resistors on the I/O pins. Setting the bit to 1 enables the selection of pull-up/pull-down resistors. Setting the bit to 0 disconnects the pull-up/pull-down resistors from the I/O pins.

**Table 7-7. Pull Up or Pull Down Enable Register 0, 1 and 2**

| Port ID | Register Address | Bit Value |
|---|---|---|
| 0 | 0x800 | 0 - Disable; 1 - Enable |
| 1 | 0x810 | |
| 2 | 0x820 | |

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### Pull Up or Pull Down Selection Register (Register Address: 0x900 - 0x920, Default Value: 0x0)

The I/O port can be configured to have pull-up or pull-down resistor by programming the pull-up/pull-down selection register. Setting a bit to 1 selects a 100kΩ pull-up resistor for that I/O pin. Setting a bit to 0 selects a 100kΩ pull-down resistor for that I/O pin. If the pull-up/down enable is 0, writing to this register will have no effect on I/O pin.

**Table 7-8. Pull Up or Pull Down Selection Register 0, 1 and 2**

| Port ID | Register Address | Bit Value |
|---|---|---|
| 0 | 0x900 | 0 - 100kΩ pull-down; 1 - 100kΩ pull-up |
| 1 | 0x910 | |
| 2 | 0x920 | |

### Bus Holder Register (Register Address: 0xA00 - 0xA20, Default Value: 0x0)

The bus holder registers enable or disable the input latch of the I/O pins. These registers are effective only when the IO pin is configured as an input pin. When a bit in bus holder register is 0, the state of the corresponding input IO pin is not latched.

**Table 7-9. Bus Holder Register Register 0, 1 and 2**

| Port ID | Register Address | Bit Value |
|---|---|---|
| 0 | 0xA00 | 0 - Disable; 1 - Enable |
| 1 | 0xA10 | |
| 2 | 0xA20 | |

### Smart Interrupt Register (Register Address: 0xB00, Default Value: 0x0)

When the smart interrupt register bit is set to 0 (smart interrupt enabled), a state change in any input pin generates an interrupt and if the input goes back to its initial state, the interrupt is cleared.

When the smart interrupt register bit is set to 1 (smart interrupt disabled), a state change in any input pin generates an interrupt and if the input goes back to its initial state, the interrupt is not cleared. A read of the interrupt status flag register will clear the interrupt.

This feature is enabled at the port level and individual I/Os cannot be configured. As there are 3 ports in this device, bit3 to bit7 are reserved.

**Table 7-10. Smart Interrupt Register**

| Register Address | Bit Value | | | |
|---|---|---|---|---|
| 0xB00 | B3 - B7 | B2 | B1 | B0 |
| | Reserved | 0 - Port 2 Enabled; 1 - Port 2 Disabled | 0 - Port 1 Enabled; 1 - Port 1 Disabled | 0 - Port 0 Enabled; 1 - Port 0 Disabled |

### Interrupt Mask Register (Register Address: 0xC00 - 0xC20, Default Value: 0xFF)

Interrupt mask registers are set to 1 by default. Interrupts can be enabled by setting corresponding mask bits to 0.

If the corresponding bit in the Interrupt mask register is set to 1, the interrupt is masked and the interrupt pin will not be asserted. If the corresponding bit in the Interrupt mask register is set to 0, the interrupt pin will be asserted. There are 3 interrupt mask registers in this device.

**Table 7-11. Interrupt Mask Register 0, 1 and 2**

| Port ID | Register Address | Bit Value |
|---|---|---|
| 0 | 0xC00 | 1 - Disable; 0 - Enable |
| 1 | 0xC10 | |
| 2 | 0xC20 | |

### Input Glitch Filter Enable Register (Register Address: 0xD00 - 0xD20, Default Value: 0x0)

Glitch filter is present at all inputs of the GPIOs. These filters are disabled by default. To enable the glitch filter, the corresponding bit of the I/O pin in the input glitch filter enable registers should be set to 1. There are 3 input glitch filter enable registers in this device.

**Table 7-12. Input Glitch Filter Enable Register 0, 1 and 2**

| Port ID | Register Address | Bit Value |
|---|---|---|
| 0 | 0xD00 | 0 - Disable; 1 - Enable |
| 1 | 0xD10 | |
| 2 | 0xD20 | |

### Interrupt Flag Status Register (Register Address: 0xE00 - 0xE20, Default Value: 0x0)

A state change in any input pin generates an interrupt and this sets the corresponding interrupt flag register for the input. If the input goes back to its initial state, the interrupt flag register remains at 1 until it is read and then the interrupt is cleared.

The read-only interrupt flag status registers are used to identify the source of an interrupt. If the value is 1, it indiates that the corresponding input pin is the source of the interrupt, else it indicates that the input pin is not the source of an interrupt.

When a corresponding bit in the interrupt mask register is set to 1 (masked), the interrupt status bit will return 0. There are 3 interrupt flag statue registers in this device.

**Table 7-13. Interrupt Flag Status Register 0, 1 and 2**

| Port ID | Register Address | Bit Value |
|---|---|---|
| 0 | 0xE00 | 0 - None; 1 - Interrupt Source |
| 1 | 0xE10 | |
| 2 | 0xE20 | |

### Interrupt Port Status Register (Register Address: 0xF00, Default Value: 0x0)

The read-only interrupt port status register is used to identify the IO port for the interrupt source. If the value is 1, it indicates that the source of the interrupt is from a pin in the given IO port. If the value is 0, it indicates that none of the input pins in the IO port is the source of an interrupt.

**Table 7-14. Interrupt Port Status Register**

| Register Address | Bit Value | | | |
|---|---|---|---|---|
| 0xF00 | B3 - B7 | B2 | B1 | B0 |
| | Reserved | 0 - None; 1 - Port 2 Interrupt | 0 - None; 1 - Port 1 Interrupt | 0 - None; 1 - Port 0 Interrupt |

### Fail-safe Enable Register (Register Address: 0x1200 - 0x1300, Default Value: 0x0)

The device is able to enter a fail-safe state by configuring the reset pin as a fail-safe pin. Fail-safe enable registers are used to change the functionality of the pin from reset to fail-safe. The contents of this register can get cleared during a POR event or other fault scenarios, the SPI controller has to rewrite this register every time

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if there is a fault scenario (which will generate an interrupt to the SPI controller, the fail-safe fault status register is to indicates the source of the interrupt).

Two fail-safe enable registers have to be written to program I/O configuration to ensure redundancy. If either of these registers get corrupted, and the contents don't match, an interrupt will be generated. There are two fail-safe enable registers in this device.

**Table 7-15. Fail-safe Enable Register 1, 2**

| Register Address | Bit Value | |
|---|---|---|
| | B1 - B7 | B0 |
| 0x1200 | Reserved | 0 - Disable; 1 - Enable |
| 0x1300 | Reserved | |

### Fail-safe Direction Configuration Register (Register Address: 0x1400 - 0x1520, Default Value: 0x0)

The Failsafe direction configuration registers configure the direction of the I/O pins when the device enters fail-safe state. If a bit in these registers is set to 0, the corresponding IO pin is enabled as a high-impedance input during fail-safe mode. If a bit in these registers is set to 1, the corresponding IO pin is enabled as an output during fail-safe mode.

Two fail-safe direction configuration registers have to be written to program I/O configuration to ensure redundancy. If either of these registers get corrupted, and the contents don't match, an interrupt will be generated.

**Table 7-16. Fail-safe Direction Configuration Registers**

| Port ID | Register Address | Bit Value |
|---|---|---|
| 0 | 0x1400 | 0 - Input; 1 - Output |
| | 0x1500 | |
| 1 | 0x1410 | |
| | 0x1510 | |
| 2 | 0x1420 | |
| | 0x1520 | |

### Fail-safe Output Register (Register Address: 0x1600 - 0x1720, Default Value: 0x0)

The fail-safe output registers show the outgoing level of the pins defined as outputs by the fail-safe direction configuration register. Bit values in these registers have no effect on IO pins defined as inputs.

Two fail-safe output registers have to be written to program I/O configuration to ensure redundancy. If either of these registers get corrupted, and the contents don't match, an interrupt will be generated.

**Table 7-17. Fail-safe Output Register 0, 1 and 2**

| Port ID | Register Address | Bit Value |
|---|---|---|
| 0 | 0x1600 | 0 - Low; 1 - high |
| | 0x1700 | |
| 1 | 0x1610 | |
| | 0x1710 | |
| 2 | 0x1620 | |
| | 0x1720 | |

### Fail-safe Redundancy Check Register (Register Address: 0x1800, Default Value: 0x0)

After writing all failsafe redundant registers (failsafe configuration + failsafe output + device configuration for failsafe pin if applicable), the SPI controller must enable the redundancy checks on these registers.

**Table 7-18. Fail-safe Redundancy Check Register**

| Register Address | Bit Value | |
|---|---|---|
| 0x1800 | B1 - B7 | B0 |
| | Reserved | 0 - Disable; 1 - Enable |

### Fault Status Register (Register Address: 0x1900, Default Value: 0x0)

Bits in the fault flag register are set during fault conditions. B0 bit is set 1 for POR recovery. B1 bit is set 1 when the fail-safe registers go out of sync. B2 bit is set when the device is in fail-safe mode. These flags are not cleared even the fault condition goes away, but they are cleared by read operation.

**Table 7-19. Fault Status Register**

| Register Address | Bit Value | | | |
|---|---|---|---|---|
| 0x1900 | B3 - B7 | B2 | B1 | B0 |
| | Reserved | duplicate fail-safe mode setting | register unmatch | POR |

### Software Reset Register (Register Address: 0x1A00, Default Value: 0x0)

B0 bit in software reset register is used to trigger a device reset, B1 as 1 and B0 as 0 is used to trigger a register reset. The register is auto cleared when the reset state is entered.

**Table 7-20. Software Reset Register**

| Register Address | Reset Mode | Bit Value | | |
|---|---|---|---|---|
| | | B2 - B7 | B1 | B0 |
| 0x1A00 | Device Reset | Reserved | | 1 |
| | Register Reset | Reserved | 1 | 0 |

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# 8 Application and Implementation

**Note**

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

## 8.1 Application Information

Applications of the TXE81xx-Q1 use this device connected as a target to a SPI controller (processor), and the SPI bus may contain any number of other target devices. The TXE81xx-Q1 is in a remote location from the controller, placed close to the GPIOs to which the controller needs to monitor or control.

## 8.2 Power Supply Recommendations

### *8.2.1 Power-On Reset Requirements*

In the event of a glitch or data corruption, TXE81xx-Q1 can be reset to its default conditions by using the power-on reset feature. Power-on reset requires that the device go through a power cycle to be completely reset. This reset also happens when the device is powered on for the first time in an application.

The two types of power-on reset are shown in Figure 8-1 and Figure 8-2.

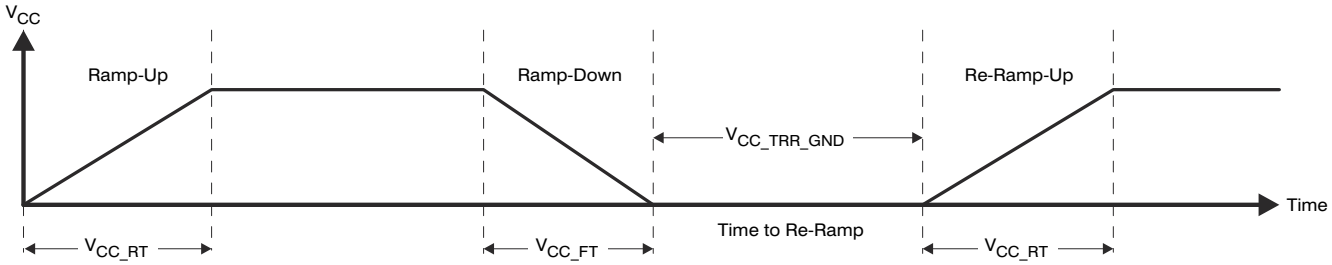


**Figure 8-1. VCC is ramped up from 0V or negative voltage**

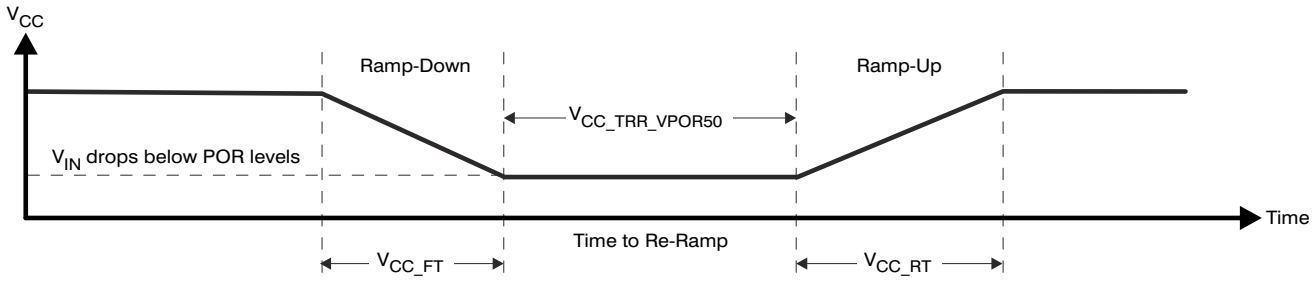


**Figure 8-2. VCC is lowered below the POR threshold, then ramped back up**

Glitches in the power supply can also affect the power-on reset performance of this device. The glitch width ($V_{CC\_GW}$) and height ($V_{CC\_GH}$) are dependent on each other. The bypass capacitance, source impedance, and device impedance are factors that affect power-on reset performance. Figure 8-3 and Figure 8-4 provide more information on how to measure these specifications.

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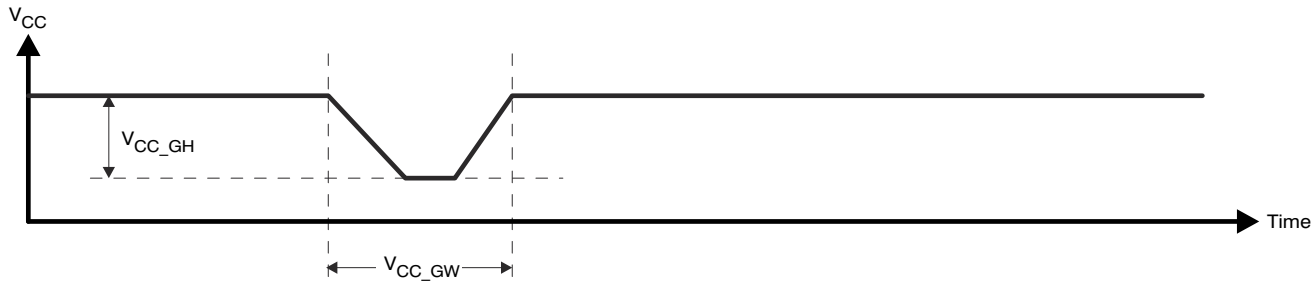


**Figure 8-3. Glitch Width and Glitch Height**

$V_{POR}$ is critical to the power-on reset. $V_{POR}$ is the voltage level at which the reset condition is released and all the registers and the SPI state machine are initialized to their default states. The value of $V_{POR}$ differs based on the VCC being lowered to or from 0. Figure 8-3 and Figure 8-4 provide more details on this specification.

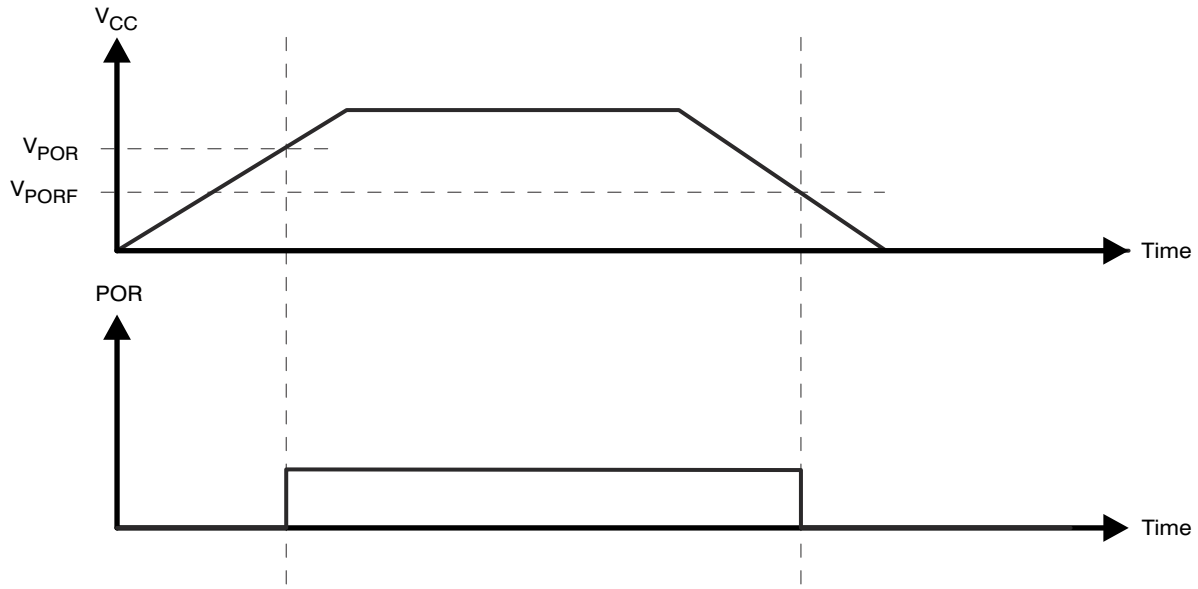


**Figure 8-4. $V_{POR}$**

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## 8.3 Layout

### *8.3.1 Layout Guidelines*

For printed circuit board (PCB) layout of the TXE81xx-Q1, common PCB layout practices should be followed but additional concerns related to high-speed data transfer such as matched impedance and differential pairs are not a concern for SPI signal speeds.

In all PCB layouts, it is a best practice to avoid right angles in signal traces, to fan out signal traces away from each other upon leaving the vicinity of an integrated circuit (IC), and to use thicker trace widths to carry higher amounts of current that commonly pass through power and ground traces. By-pass and decoupling capacitors are commonly used to control the voltage on the supply pins, using a larger capacitor to provide additional power in the event of a short power supply glitch and a smaller capacitor to filter out high-frequency ripple. These capacitors should be placed as close to the TXE81xx-Q1 as possible. These best practices are shown in Figure 8-5.

For the layout example provided in Figure 8-5, it is possible to fabricate a PCB with only 2 layers by using the top layer for signal routing and the bottom layer as a split plane for power and ground (GND). However, a 4 layer board is preferable for boards with higher density signal routing. On a 4 layer PCB, it is common to route signals on the top and bottom layer, dedicate one internal layer to a ground plane, and dedicate the other internal layer to a power plane. In a board layout using planes or split planes for power and ground, vias are placed directly next to the surface mount component pad which needs to attach to power or GND and the via is connected electrically to the internal layer or the other side of the board. Vias are also used when a signal trace needs to be routed to the opposite side of the board, but this technique is not demonstrated in Figure 8-5.

### 8.3.2 Layout Example

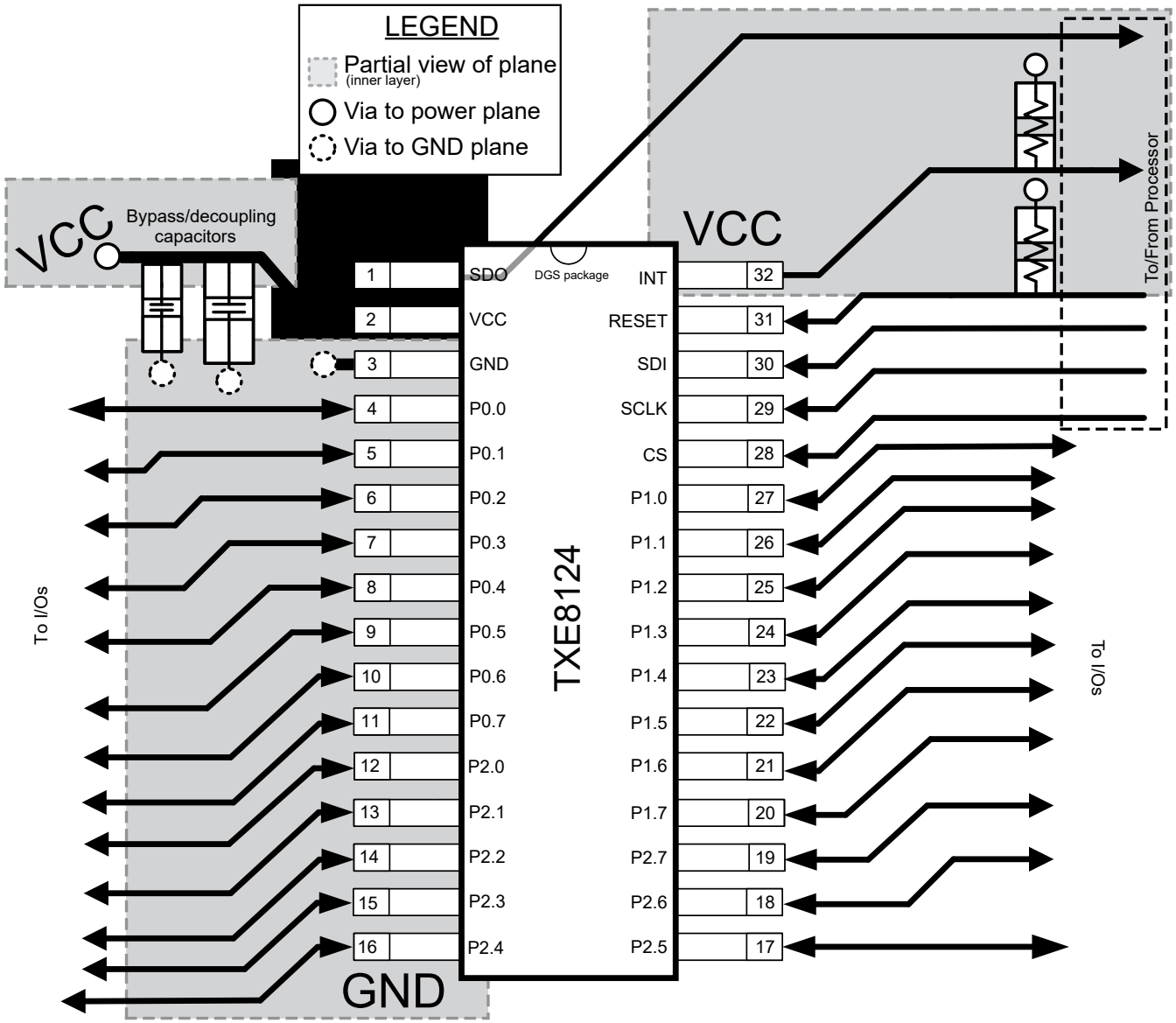


**Figure 8-5. TXE8124-Q1 Layout**

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# 9 Device and Documentation Support

## 9.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

## 9.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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## 9.3 Trademarks

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## 9.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## 9.5 Glossary

| | |
|---|---|
| TI Glossary | This glossary lists and explains terms, acronyms, and definitions. |

# 10 Revision History

| DATE | REVISION | NOTES |
|---|---|---|
| May 2025 | * | Initial Release |

# 11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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## PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| PTXE8116QDGSRQ1 | Active | Preproduction | VSSOP (DGS) \| 24 | 3000 \| LARGE T&R | - | Call TI | Call TI | -40 to 125 | |
| PTXE8124QDGSRQ1 | Active | Preproduction | VSSOP (DGS) \| 32 | 250 \| LARGE T&R | - | Call TI | Call TI | -40 to 125 | |

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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