

TXB0106-Q1 6-Bit Bidirectional Voltage-Level Translator With Auto-Direction Sensing and ±10kV ESD Protection

1 Features

- Qualified for Automotive Applications
- 1.2V to 3.6V on A Port and 1.65 to 5.5V on B Port $(V_{CCA} \leq V_{CCB})$
- V_{CC} Isolation Feature If Either V_{CC} Input Is at GND, All Outputs Are in the High-Impedance State
- OE Input Circuit Referenced to V_{CCA}
- Ioff Supports Partial-Power-Down Mode Operation
- ESD Protection Exceeds AEC-Q100
 - A Port
 - 2000V Human-Body Model
 - 1500V Charged-Device Model
 - - ±10kV Human-Body Model
 - 1500V Charged-Device Model

2 Applications

- Heating and Cooling
- **Telematics**
- Radar

3 Description

This 6-bit noninverting translator uses two separate configurable power-supply rails. The A port is designed to track V_{CCA}. V_{CCA} accepts any supply voltage from 1.2V to 3.6V. The B port is designed to track V_{CCB}. V_{CCB} accepts any supply voltage from 1.65V to 5.5V. This allows for universal low-voltage bidirectional translation between any of the 1.2V, 1.5V, 1.8V, 2.5V, 3.3V, and 5V voltage nodes. V_{CCA} should not exceed V_{CCB}.

When the output-enable (OE) input is low, all outputs are placed in the high-impedance state.

The TXB0106-Q1 device is designed so that the OE input circuit is supplied by V_{CCA}.

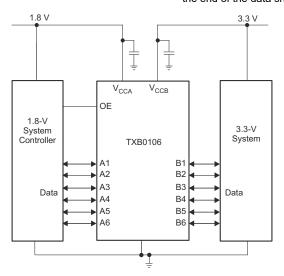
This device is fully specified for partial-power-down applications using Ioff. The Ioff circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

To ensure the high-impedance state during power up or power down, OE should be tied to GND through a pulldown resistor; the minimum value of the resistor is determined by the current-sourcing capability of the driver.

Package Information

PART NUMBER	PACKAGE (1)	BODY SIZE (NOM)
TXB0106-Q1	TSSOP (16)	5.00mm × 4.40mm
TXB0106-Q1	WQFN (16)	3.50mm x 2.50mm

For all available packages, see the orderable addendum at the end of the data sheet.



Typical Operating Circuit



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4 Pin Configuration and Functions

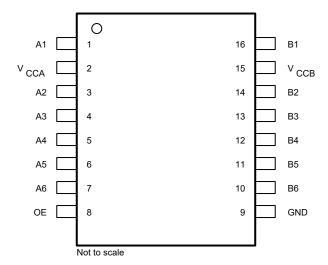


Figure 4-1. PW Package 16-Pin TSSOP Top View

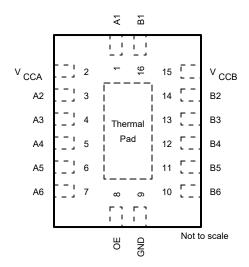


Figure 4-2. BQB Package 16-Pin WCSP Top View



Pin Functions

NAME	NO.	I/O	DESCRIPTION
A1	1	I/O	Input/output 1. Referenced to V _{CCA} .
A2	3	I/O	Input/output 2. Referenced to V _{CCA} .
A3	4	I/O	Input/output 3. Referenced to V _{CCA} .
A4	5	I/O	Input/output 4. Referenced to V _{CCA} .
A5	6	I/O	Input/output 5. Referenced to V _{CCA} .
A6	7	I/O	Input/output 6. Referenced to V _{CCA} .
B1	16	I/O	Input/output 1. Referenced to V _{CCB} .
B2	14	I/O	Input/output 2. Referenced to V _{CCB} .
В3	13	I/O	Input/output 3. Referenced to V _{CCB} .
B4	12	I/O	Input/output 4. Referenced to V _{CCB} .
B5	11	I/O	Input/output 5. Referenced to V _{CCB} .
B6	10	I/O	Input/output 6. Referenced to V _{CCB} .
GND	9	_	Ground
OE	8	I	Output enable. Pull OE low to place all outputs in the high-impedance state. Referenced to V _{CCA} .
V _{CCA}	2	- 1	A-port supply voltage. 1.2V \leq V _{CCA} \leq 3.6V, V _{CCA} \leq V _{CCB} .
V _{CCB}	15	- 1	B-port supply voltage. $1.65V \le V_{CCB} \le 5.5V$.

5 Specifications

5.1 Absolute Maximum Ratings

over operating ambient temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V _{CCA}	Supply voltage range		-0.5	4.6	V
V _{CCB}	Supply voltage range		-0.5	6.5	V
VI	Input voltage range (1)			6.5	V
	Voltage range applied to any output in the high-impedance or power	-0.5	6.5	V	
V _O	Voltage range applied to any output in the high or low state ⁽¹⁾ (2)	A inputs	-0.5	V _{CCA} + 0.5	V
	Voltage range applied to any output in the high of low state.	B inputs	-0.5	V _{CCB} + 0.5]
I _{IK}	Input clamp current	V _I < 0		-50	mA
I _{OK}	Output clamp current	V _O < 0		-50	mA
Io	Continuous output current	<u>, </u>		±50	mA
	Continuous current through V _{CCA} , V _{CCB} , or GND			±100	mA
TJ	Junction temperature			150	°C
T _{stg}	Storage temperature range		-65	150	°C

⁽¹⁾ The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.

5.2 ESD Ratings

				VALUE	UNIT
		Human-body model (HBM), per AEC Q100-	±2000		
V _(ESD)	Electrostatic discharge	Charged-device model (CDM), per AEC Q100-011	All pins	±1500	V

⁽¹⁾ AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

5.3 Recommended Operating Conditions

			V _{CCA}	V _{CCB}	MIN	MAX	UNIT	
V_{CCA}	Supply voltage				1.2	3.6	V	
V _{CCB}	- Supply Voltage				1.65	5.5	V	
V	High-level input voltage	Data inputs	1.2V to 3.6V	1.65V to 5.5V	V _{CCI} × 0.65 ⁽¹⁾	V_{CCI}	V	
V _{IH}	I ligit-level iliput voltage	OE	1.20 to 3.60	1.030 to 3.30	V _{CCA} × 0.65	5.5	V	
V	Low-level input voltage	Data inputs	1.2V to 5.5V	1.65V to 5.5V	0	V _{CCI} × 0.35 ⁽¹⁾	V	
V _{IL}	Low-level iliput voltage	OE	1.2V to 3.6V	1.030 to 3.30	0	V _{CCA} × 0.35	V	
		A-port inputs	1.2V to 3.6V	1.65V to 5.5V		40		
Δt/Δν	Input transition rise or fall rate	B-port inputs	1.2V to 3.6V	1.65V to 3.6V		40	ns/V	
		B-port inputs	1.2V to 3.6V	4.5V to 5.5V		30		
т.	Operating ambient temperature (Operating ambient temperature (TXB0106I)			-40	85	°C	
T _A	Operating ambient temperature (-40	125	°C		

⁽¹⁾ V_{CCI} is the supply voltage associated with the input port.

²⁾ The values of V_{CCA} and V_{CCB} are provided in the *Recommended Operating Conditions* table.



5.4 Thermal Information

		TXB0	TXB0106-Q1				
	THERMAL METRIC (1)	PW (TSSOP)	BQB (WQFN)	UNIT			
		16 PINS	16 PINS				
R _{0JA}	Junction-to-ambient thermal resistance	107.5	63.4	°C/W			
R _{0JC(top)}	Junction-to-case (top) thermal resistance	42.3	64.3	°C/W			
$R_{\theta JB}$	Junction-to-board thermal resistance	52.6	33.6	°C/W			
ΨЈТ	Junction-to-top characterization parameter	4.2	2.8	°C/W			
Ψ_{JB}	Junction-to-board characterization parameter	52	33.6	°C/W			
R _{0JC(bot)}	Junction-to-case (bottom) thermal resistance	-	16.2	°C/W			

⁽¹⁾ For more information about traditional and new thermal metrics, see the IC Package Thermal Metrics application note.

5.5 Electrical Characteristics (TXB0106I)

	PARAME	TED	TEST	V	V	TA	= 25°	С	-40°C to	85°C	UNIT	
	PARAME	IEK	CONDITIONS	V _{CCA}	V _{CCB}	MIN	TYP	MAX	MIN	MAX	UNII	
		Output high		1.2V			1.1					
V _{OHA}		voltage, A port	I _{OH} = -20μA	1.4V to 3.6V					V _{CCA} – 0.4		V	
\/		Output low	I = 20uA	1.2V			0.9				v	
V _{OLA}		voltage, A port	I _{OL} = 20μA	1.4V to 3.6V	1.4V to 3.6V		0.4	V				
V _{OHB}		Output high voltage, B port	I _{OH} = -20μA		1.65V to 5.5V				V _{CCB} – 0.4		V	
V _{OLB}		Output low voltage, B port	I _{OL} = 20μA		1.65V to 5.5V					0.4	V	
I _{lkg(I)}	OE	Input leakage current		1.2V to 3.6V	1.65V to 5.5V			±1		±2	μA	
	A port	Off-state		0V	0V to 5.5V			±1		±2		
I _{lkg(off)}	B port	leakage current		0V to 3.6V	0V			±1		±2	μA	
I _{OZ}	A or B port	High- impedance output current	OE = GND	1.2V to 3.6V	1.65V to 5.5V			±1		±2	μA	
		V _{CCA} supply current		1.2V	1.65V to 5.5V		0.06					
.			v _{CCA} supply	$V_I = V_{CCI}$ or	1.4V to 3.6V	1.050 10 5.50					9]
I _{CCA}					3.6V	0V					2	μA
				0V	5.5V					2		
				1.2V	1.65V to 5.5V		3.4					
		V _{CCB} supply	V _I = V _{CCI} or GND,	1.4V to 3.6V	1.030 to 5.50					9	μΑ	
I _{CCB}		current	$I_0 = 0$	3.6V	0V					-2	μΑ	
				0V	5.5V					2		
		Combined	$V_I = V_{CCI}$ or	1.2V			3.5					
I _{CCA} +	ICCB	supply current	GND, I _O = 0	1.4V to 3.6V	1.65V to 5.5V					18	μΑ	
		High-	$V_I = V_{CCI}$ or	1.2V			0.05					
I _{CCZA}		impedance V _{CCA} supply current	GND, I _O = 0, OE = GND	$_{0} = 0$, $1.4 \text{V to } 3.6 \text{V}$						5	μА	
		High- V _I = V _{CCI} or		1.2V			3.3					
I _{CCZB}		impedance V _{CCB} supply current	GND, I _O = 0, OE = GND	1.4V to 3.6V	1.65V to 5.5V					5	μА	

over recommended operating ambient temperature range (unless otherwise noted)(1) (2)

PARAMETER		TEST	V V		T _A = 25°C			-40°C to 85°C		UNIT		
	PARAMETER		CONDITIONS		V _{CCB}	MIN	TYP	MAX	MIN	MAX	ONII	
Cı	OE	Input capacitance		1.2V to 3.6V	1.65V to 5.5V		5			5.5	pF	
C	A port			1.2V to 3.6V	1.65V to 5.5V		5			6.5	pF	
C _{io}	B port			1.20 10 3.00	1.050 to 5.50		8			10	PΓ	

- V_{CCI} is the supply voltage associated with the input port. V_{CCO} is the supply voltage associated with the output port.

5.6 Electrical Characteristics (TXB0106)

	PARAME	TED	TEST V _{CCA}	V _{CCB}	TA	= 25°	С	-40°C to 125°C		UNIT		
	PARAIVIE	IEK	CONDITIONS	VCCA	V CCB	MIN	TYP	MAX	MIN	MAX	UNII	
		Output high		1.2V			1.1					
V _{OHA}		voltage, A port	I _{OH} = -20μA	1.4V to 3.6V					V _{CCA} - 0.4		V	
M		Output low	I _{OL} = 20μΑ	1.2V			0.9				V	
V _{OLA}		voltage, A port	10L - 20µA	1.4V to 3.6V						0.4	\ \ \	
V _{OHB}		Output high voltage, B port	I _{OH} = -20μA		1.65V to 5.5V				V _{CCB} – 0.4		V	
V_{OLB}		Output low voltage, B port	I _{OL} = 20μA		1.65V to 5.5V					0.4	V	
I _{lkg(I)}	OE	Input leakage current		1.2V to 3.6V	1.65V to 5.5V			±1		±2	μА	
l	A port	Off-state		0V	0V to 5.5V			±1		±2	μA	
I _{lkg(off)}	B port	leakage current		0V to 3.6V	0V			±1		±2	μΛ	
l _{oz}	A or B port	High- impedance output current	OE = GND	1.2V to 3.6V	1.65V to 5.5V			±1		±2	μA	
				1.2V			0.4					
		V _{CCA} supply current	V _I = V _{CCI} or	1.4V to 3.6V	1.65V to 5.5V					10	Δ	
I _{CCA}				3.6V	0V					7.5		
				0V	5.5V					-2		
				1.2V			3.4					
		V _{CCB} supply	$V_I = V_{CCI}$ or	1.4V to 3.6V	1.65V to 5.5V					31.5		
I _{CCB}		current	GND, I _O = 0	3.6V	0V					-2	μA	
				0V	5.5V					30.5		
		Combined	$V_I = V_{CCI}$ or	1.2V			3.5					
I _{CCA} +	I _{CCB}	supply current	GND, I _O = 0	1.4V to 3.6V	1.65V to 5.5V					38.5	μA	
		High-	V _I = V _{CCI} or	1.2V			0.4					
I _{CCZA}		impedance V _{CCA} supply current	GND, I _O = 0, OE = GND	1.4V to 3.6V	1.65V to 5.5V					7	μA	
		High- V _I = V _{CCI} or		1.2V			3.3					
I _{CCZB}		impedance V _{CCB} supply current	GND, I _O = 0, OE = GND	1.4V to 3.6V	1.65V to 5.5V					31	μA	
Cı	OE	Input capacitance		1.2V to 3.6V	1.65V to 5.5V		5			6.5	pF	

over recommended operating ambient temperature range (unless otherwise noted)(1) (2)

	PARAMETER		TEST	V	V	T _A = 25°C			-40°C to 125°C	UNIT
PARAMETER			CONDITIONS V _{CCA}	V _{CCB}	MIN	TYP	MAX	MIN MAX	UNIT	
C	A port			1.2V to 3.6V	1.65V to 5.5V		5		6.5	pF
C _{io}	B port			1.20 10 3.00	1.030 (0 5.50		8		13.5	PF

- V_{CCI} is the supply voltage associated with the input port. V_{CCO} is the supply voltage associated with the output port.

5.7 Timing Requirements – V_{CCA} = 1.2V, T_A = 25°C

			V _{CCB} = 1.8V	V _{CCB} = 2.5V	V _{CCB} = 3.3V	V _{CCB} = 5V	UNIT
			TYP	TYP	TYP	TYP	ONIT
	Data rate		20	20	20	20	Mbps
t _w	Pulse duration	Data inputs	50	50	50	50	ns

5.8 Timing Requirements – V_{CCA} = 1.5V ± 0.1V

over recommended operating ambient temperature range (unless otherwise noted)

						V _{CCB} = 2.5V ± 0.2V		3.3V 3V	V _{CCB} = 5V ± 0.5V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
	Data rate			50		50		50		50	Mbps
t _w	Pulse duration	Data inputs	20		20		20		20		ns

5.9 Timing Requirements – V_{CCA} = 1.8V ± 0.15V

over recommended operating ambient temperature range (unless otherwise noted)

				1.8V 5V	V _{CCB} = ± 0.2		V _{CCB} = ± 0.3		V _{CCB} = ± 0.5		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
	Data rate			52		60		60		60	Mbps
t _w	Pulse duration	Data inputs	19		17		17		17		ns

5.10 Timing Requirements – $V_{CCA} = 2.5V \pm 0.2V$

over recommended operating ambient temperature range (unless otherwise noted)

			V _{CCB} = 2.5V ± 0.2V		V _{CCB} = 3.3V ± 0.3V		V _{CCB} = 5V ± 0.5V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
	Data rate			70		100		100	Mbps
t _w	Pulse duration Data inputs		14		10		10		ns

5.11 Timing Requirements – V_{CCA} = 3.3V ± 0.3V

				V _{CCB} = 3.3V V _{CCB} = 5V ± 0.5V		5V /	UNIT
			MIN	MAX	MIN	MAX	
	Data rate			100		100	Mbps
t _w	Pulse duration	Data inputs	10		10		ns

5.12 Switching Characteristics $-V_{CCA} = 1.2V$, $T_A = 25$ °C

PARAMETER	FROM	то	V _{CCB} = 1.8V	V _{CCB} = 2.5V	V _{CCB} = 3.3V	V _{CCB} = 5V	UNIT
PARAMETER	(INPUT)	(OUTPUT)	TYP	TYP	TYP	TYP	UNIT
t .	A	В	9.5	7.9	7.6	8.5	ns
t _{pd}	В	Α	9.2	8.8	8.4	8	115
+	OE	Α	1	1	1	1	II.C
t _{en}	OL	В	1	1	1	1	- µs
t _{dis} (1)	OE	A	20	17	17	18	ns
'dis '	OL	В	20	16	15	15	115
t _{rA} , t _{fA}	A-port rise a	ind fall times	4.1	4.4	4.1	3.9	ns
t _{rB} , t _{fB}	B-port rise and fall times		5	5	5.1	5.1	ns
t _{SK(O)}	Channel-to-channel skew		2.4	1.7	1.9	7	ns
Max. data rate			20	20	20	20	Mbps

⁽¹⁾ Test procedure uses a 25MHz sine wave on the input.

5.13 Switching Characteristics – V_{CCA} = 1.5V ± 0.1V (TXB0106I)

over recommended operating ambient temperature range (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CCB} = 1.8V ± 0.15V		V _{CCB} = 2.5V ± 0.2V		V _{CCB} = 3.3V ± 0.3V		V _{CCB} = 5V ± 0.5V		UNIT
	(INFOT)	(OUTPUT)	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
.	Α	В	1.4	13.5	1.2	10.5	1.1	10.5	8.0	10.1	ns
t _{pd}	В	Α	0.9	15.2	0.7	13.8	0.4	13.8	0.3	13.7	115
	OE	Α		1		1		1		1	ш
t _{en}	OE	В		1		1		1		1	μs
t _{dis} ⁽¹⁾	OE	Α	6.6	33	6.4	25.3	6.1	23.1	5.9	24.6	
dis (1)	OE	В	6.6	35.6	5.8	25.6	5.5	22.1	5.6	20.6	ns
t _{rA} , t _{fA}	A-port rise a	ind fall times	0.8	6.5	0.8	6.3	0.8	6.3	0.8	6.3	ns
t _{rB} , t _{fB}	B-port rise a	ind fall times	1	7.3	0.7	4.9	0.7	4.6	0.6	4.6	ns
t _{SK(O)}	Channel-to-c	channel skew		2.6		1.9		1.6		1.3	ns
Max data rate			50		50		50		50		Mbps

5.14 Switching Characteristics – V_{CCA} = 1.5V ± 0.1V (TXB0106)

PARAMETER	FROM (INPUT)	TO (OUTPUT)		V _{CCB} = 1.8V ± 0.15V		V _{CCB} = 2.5V ± 0.2V		3.3V 3V	V _{CCB} = 5V ± 0.5V		UNIT
	(INFOT)	(OUTFUT)	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
+	Α	В	1.4	13.5	1.2	10.5	1.1	10.5	0.8	10.1	ns
t _{pd}	В	Α	0.9	15.2	0.7	13.8	0.4	13.8	0.3	13.7	115
+	OE	A		1		1		1		1	
t _{en}	OE .	В		1		1		1		1	μs
t _{dis} ⁽¹⁾	OE	А	278	394	236	305	236	305	236	305	ns
'dis '	OL	В	278	394	236	305	236	305	236	305	
t _{rA} , t _{fA}	A-port rise a	nd fall times	0.8	6.5	0.8	6.3	0.8	6.3	0.8	6.3	ns
t _{rB} , t _{fB}	B-port rise a	ind fall times	1	7.3	0.7	4.9	0.7	4.6	0.6	4.6	ns
t _{SK(O)}	Channel-to-c	channel skew		2.6		1.9		1.6		1.3	ns
Max data rate			50		50		50		50		Mbps



5.15 Switching Characteristics – V_{CCA} = 1.8V ± 0.15V (TXB0106I)

over recommended operating ambient temperature range (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CCB} = 1.8V ± 0.15V		V _{CCB} = 2.5V ± 0.2V		V _{CCB} = 3.3V ± 0.3V		V _{CCB} = 5V ± 0.5V		UNIT
	(INFOT)	(001101)	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
	Α	В	1.6	12	1.4	7.7	1.3	6.8	1.2	6.5	
t _{pd}	В	Α	1.5	13.5	1.2	10	0.8	8.2	0.5	8	ns
	OE	Α		1		1		1		1	
t _{en}	OE .	В		1		1		1		1	μs
+ (1)	OE	Α	5.9	26.7	5.6	21.6	5.4	18.9	4.8	18.7	
t _{dis} (1)	OE .	В	6.1	33.9	5.2	23.7	5	19.9	5	17.6	ns
t _{rA} , t _{fA}	A-port rise a	and fall times	0.7	5.1	0.7	5	1	5	0.7	5	ns
t _{rB} , t _{fB}	B-port rise a	and fall times	1	7.3	0.7	5	0.7	3.9	0.6	3.8	ns
t _{SK(O)}	Channel-to-c	channel skew		0.8		0.7		0.6		0.6	ns
Max data rate			52		60		60		60		Mbps

5.16 Switching Characteristics – V_{CCA} = 1.8V ± 0.15V (TXB0106)

PARAMETER	FROM	FROM TO (INPUT) (OUTPUT)		1.8V 5V	V _{CCB} = 2.5V ± 0.2V		V _{CCB} = 3.3V ± 0.3V		V _{CCB} = 5V ± 0.5V		UNIT
	(INFOT)	(OUTPUT)	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
+	Α	В	1.6	12	1.4	7.7	1.3	6.8	1.2	6.5	ns
t _{pd}	В	Α	1.5	13.5	1.2	10	0.8	8.2	0.5	8	
+	OE	A		1		1		1		1	
t _{en}	OE	В		1		1		1		1	μs
t _{dis} ⁽¹⁾	OE	A	278	393	191	256	190	248	189	248	ns
'dis '	OL	В	278	393	191	256	190	248	189	248	
t _{rA} , t _{fA}	A-port rise a	and fall times	0.7	5.1	0.7	5	1	5	0.7	5	ns
t _{rB} , t _{fB}	B-port rise a	and fall times	1	7.3	0.7	5	0.7	3.9	0.6	3.8	ns
t _{SK(O)}	Channel-to-c	channel skew		0.8		0.7		0.6		0.6	ns
Max data rate			52		60		60		60		Mbps

5.17 Switching Characteristics – V_{CCA} = 2.5V ± 0.2V (TXB0106I)

over recommended operating ambient temperature range (unless otherwise noted)

PARAMETER	FROM (INPUT)	_		:.5V /	V _{CCB} = 3 ± 0.3\		V _{CCB} = ± 0.5\	UNIT	
	(INFOT)	(001101)	MIN	MAX	MIN	MAX	MIN	MAX	
+	Α	В	1.1	6.7	1	5.7	0.9	5	no
t _{pd}	В	Α	1	8.5	0.6	7	0.3	7	ns
+	OE	Α		1		1		1	
t _{en}	OE	В		1		1		1	μs
t _{dis} (1)	OE	А	5	16.9	4.9	15	4.5	13.8	
^L dis ^(*)	OE	В	4.8	21.8	4.5	17.9	4.4	15.2	ns
t _{rA} , t _{fA}	A-port rise a	nd fall times	0.8	3.6	0.6	3.6	0.5	3.5	ns
t _{rB} , t _{fB}	B-port rise a	nd fall times	0.6	4.9	0.7	3.9	0.6	3.2	ns
t _{SK(O)}	Channel-to-c	hannel skew		0.4		0.3		0.3	ns
Max data rate			70		100		100		Mbps

5.18 Switching Characteristics – V_{CCA} = 2.5V ± 0.2V (TXB0106)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CCB} = 2 ± 0.2\		V _{CCB} = 3 ± 0.3\		V _{CCB} = ± 0.5\	UNIT	
	(INFOT)	(OUTPUT)	MIN	MAX	MIN	MAX	MIN	MAX	
4	Α	В	1.1	6.7	1	5.7	0.9	5	ns
t _{pd}	В	А	1	8.5	0.6	7	0.3	7	1115
•	OE	A		1		1		1	
t _{en}	OE	В		1		1		1	μs
t _{dis} (1)	OE	Α	190	255	137	185	133	169	ns
'dis '	OL	В	190	255	137	185	133	169	
t _{rA} , t _{fA}	A-port rise a	and fall times	0.8	3.6	0.6	3.6	0.5	3.5	ns
t _{rB} , t _{fB}	B-port rise a	and fall times	0.6	4.9	0.7	3.9	0.6	3.2	ns
t _{SK(O)}	Channel-to-c	channel skew		0.4		0.3		0.3	ns
Max data rate			70		100		100		Mbps



5.19 Switching Characteristics – V_{CCA} = 3.3V ± 0.3V (TXB0106I)

over recommended operating ambient temperature range (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CCB} = 3.3V ± 0.3V	V	V _{CCB} = : ± 0.5\	UNIT	
	(INFOT)	(OUTFUT)	MIN	MAX	MIN	MAX	
+	Α	В	0.9	5.5	0.8	4.5	
t _{pd}	В	A	0.5	6.5	0.2	6	ns
+	OE	A		1		1	
t _{en}		В		1		1	μs
+ (1)	OE	Α	4.5	13.9	4.1	12.4	200
t _{dis} ⁽¹⁾	OE	В	4.1	17.3	4	14.4	ns
t _{rA} , t _{fA}	A-port rise and fall times		0.5	3	0.5	3	ns
t _{rB} , t _{fB}	B-port rise a	ind fall times	0.7	3.9	0.6	3.2	ns
t _{SK(O)}	Channel-to-c	channel skew		0.4		0.3	ns
Max data rate			100		100		Mbps

5.20 Switching Characteristics – V_{CCA} = 3.3V ± 0.3V (TXB0106)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CCB} = 3.3V ± 0.3V	V	V _{CCB} = ± 0.5	UNIT	
	(INFOT)	(OUTPUT)	MIN	MAX	MIN	MAX	
4	Α	В	0.9	5.5	0.8	4.5	
t _{pd}	В	Α	0.5	6.5	0.2	6	ns
	OE	Α		1		1	
t _{en}	OE .	В		1		1	μs
t _{dis} (1)	OE	Α	137	185	97.6	127	
dis (*/	OE	В	137	185	97.6	127	ns
t _{rA} , t _{fA}	A-port rise a	nd fall times	0.5	3	0.5	3	ns
t _{rB} , t _{fB}	B-port rise a	ind fall times	0.7	3.9	0.6	3.2	ns
t _{SK(O)}	Channel-to-c	channel skew		0.4		0.3	ns
Max data rate			100		100		Mbps



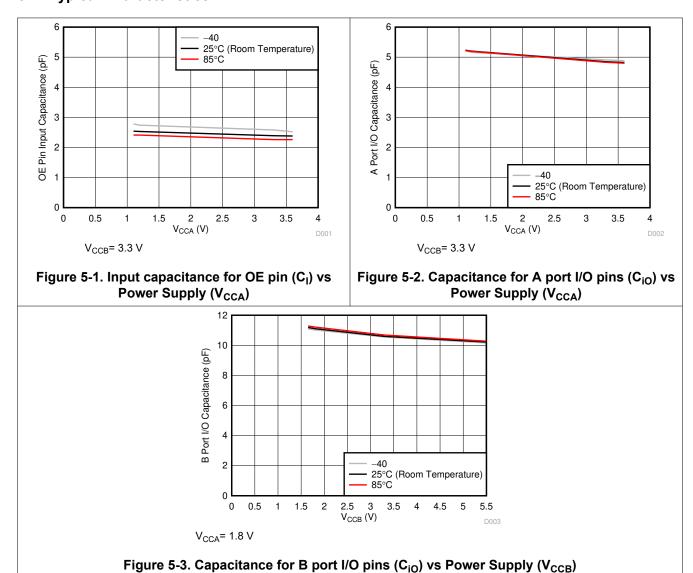
5.21 Operating Characteristics

T_A = 25°C

						V _{CCA}				
			1.2V	1.2V	1.5V	1.8V	2.5V	2.5V	3.3V	
			V _{CCB}							
	PARAMETER	TEST CONDITIONS	5V	1.8V	1.8V	1.8V	2.5V	5V	3.3V to 5V	UNIT
			TYP	TYP	TYP	TYP	TYP	TYP	TYP	
C	A-port input, B-port output	$C_1 = 0, f = 10MHz,$	9	8	7	7	7	7	8	pF
C _{pdA}	B-port input, A-port output	$t_r = t_f = 1$ ns,	12	11	11	11	11	11	11	
C	A-port input, B-port output	OE = V _{CCA}	35	26	27	27	27	27	28	pF
C _{pdB}	B-port input, A-port output	(outputs enabled)	26	19	18	18	18	20	21	pr
C	A-port input, B-port output	$C_1 = 0, f = 10MHz,$	0.01	0.01	0.01	0.01	0.01	0.01	0.01	
C _{pdA}	B-port input, A-port output	$t_r = t_f = 1 \text{ns},$	0.01	0.01	0.01	0.01	0.01	0.01	0.01	pF
C _{pdB}	A-port input, B-port output	OE = GND	0.01	0.01	0.01	0.01	0.01	0.01	0.03	pF
	B-port input, A-port output	(outputs disabled)	0.01	0.01	0.01	0.01	0.01	0.01	0.03	



5.22 Typical Characteristics



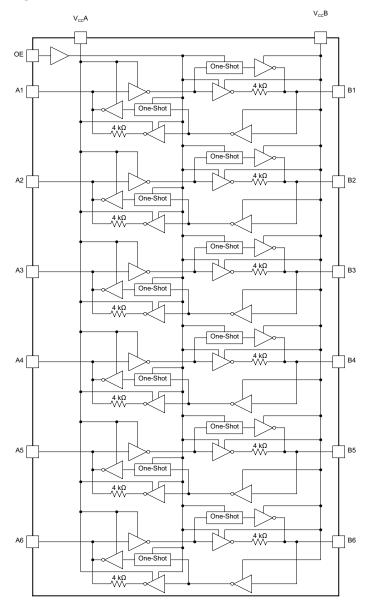


6 Detailed Description

6.1 Overview

The TXB0106-Q1 device is a 6-bit, directionless voltage-level translator specifically designed for translating logic voltage levels. The A port is able to accept I/O voltages ranging from 1.2V to 3.6V, while the B port can accept I/O voltages from 1.65V to 5.5V. The device is a buffered architecture with edge-rate accelerators (one-shots) to improve the overall data rate. This device can only translate push-pull CMOS logic outputs. For open-drain signal translation, see TI's TXS family of products.

6.2 Functional Block Diagram



6.3 Feature Description

6.3.1 Architecture

The TXB0106-Q1 architecture (see Figure 6-1) does not require a direction-control signal to control the direction of data flow from A to B or from B to A. In a dc state, the output drivers of the TXB0106-Q1 device can maintain a high or low, but are designed to be weak, so that they can be overdriven by an external driver when data on the bus starts flowing in the opposite direction.



The output one-shots detect rising or falling edges on the A or B ports. During a rising edge, the one-shot turns on the PMOS transistors (T1, T3) for a short duration, which speeds up the low-to-high transition. Similarly, during a falling edge, the one-shot turns on the NMOS transistors (T2, T4) for a short duration, which speeds up the high-to-low transition. The typical output impedance during output transition is 70Ω at $V_{CCO} = 1.2V$ to 1.8V, 50Ω at $V_{CCO} = 1.8V$ to 3.3V, and 40Ω at $V_{CCO} = 3.3V$ to 5V.

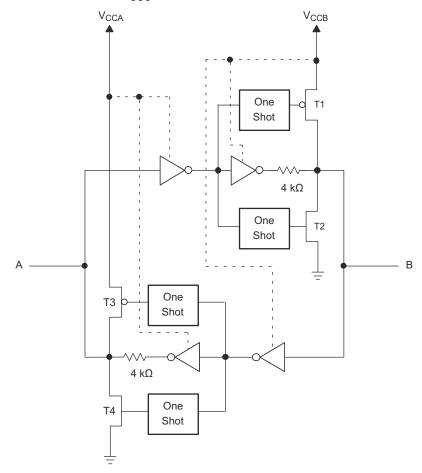
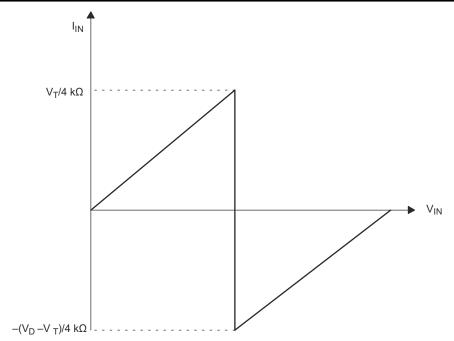


Figure 6-1. Architecture of the TXB0106-Q1 I/O Cell

6.3.2 Input Driver Requirements

Typical I_{IN} vs V_{IN} characteristics of the TXB0106-Q1 device are shown in Figure 6-2. For proper operation, the device driving the data I/Os of the TXB0106-Q1 device must have drive strength of at least ±2mA.



- A. V_T is the input threshold voltage of the TXB0106-Q1 device (typically V_{CCI} / 2).
- B. V_D is the supply voltage of the external driver.

Figure 6-2. Typical I_{IN} vs V_{IN} Curve

6.3.3 Power Up

During operation, ensure that $V_{CCA} \le V_{CCB}$ at all times. During power-up sequencing, $V_{CCA} \ge V_{CCB}$ does not damage the device, so any power supply can be ramped up first. The TXB0106-Q1 device has circuitry that disables all output ports when either V_{CC} is switched off ($V_{CCA/B} = 0V$).

6.3.4 Output Load Considerations

TI recommends careful PCB layout practices with short PCB trace lengths to avoid excessive capacitive loading and to ensure that proper one-shot (O.S.) triggering takes place. PCB signal trace-lengths should be kept short enough such that the round trip delay of any reflection is less than the O.S. duration. This improves signal integrity by ensuring that any reflection sees a low impedance at the driver. The O.S. circuits have been designed to stay on for approximately 10ns. The maximum capacitance of the lumped load that can be driven also depends directly on the O.S. duration. With very heavy capacitive loads, the O.S. can time out before the signal is driven fully to the positive rail. The O.S. duration has been set to best optimize trade-offs between dynamic I_{CC}, load driving capability, and maximum bit-rate considerations. Both PCB trace length and connectors add to the capacitance that the TXB0106-Q1 output sees, so it is recommended that this lumped-load capacitance be considered to avoid O.S. retriggering, bus contention, output signal oscillations, or other adverse system-level affects.

6.3.5 Enable and Disable

The TXB0106-Q1 device has an OE input that is used to disable the device by setting OE = low, which places all I/Os in the high-impedance (Hi-Z) state. The disable time (t_{dis}) indicates the delay between when OE goes low and when the outputs actually get disabled (Hi-Z). The enable time (t_{en}) indicates the amount of time the user must allow for the O.S. circuitry to become operational after OE is taken high.

6.3.6 Pullup or Pulldown Resistors on I/O Lines

The TXB0106-Q1 device is designed to drive capacitive loads of up to 70pF. The output drivers of the TXB0106-Q1 device have low dc drive strength. If pullup or pulldown resistors are connected externally to the data I/Os,

their values must be kept higher than $50k\Omega$ to ensure that they do not contend with the output drivers of the TXB0106-Q1 device.

For the same reason, the TXB0106-Q1 device should not be used in applications such as I²C or 1-Wire where an open-drain driver is connected on the bidirectional data I/O. For these applications, use a device from TI's TXS family of level translators.

6.4 Device Functional Modes

The TXB0106-Q1 device has two functional modes, enabled and disabled. To disable the device, set the OE input to low, which places all I/Os in a high-impedance state. Setting the OE input to high will enable the device.

Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

1 Application Information

The TXB0106-Q1 device can be used in level-translation applications for interfacing devices or systems operating at different interface voltages with one another. It can only translate push-pull CMOS logic outputs. For open-drain signal translation, see TI's TXS products. Any external pulldown or pullup resistors are recommended to be larger than 50 k Ω .

2 Typical Application

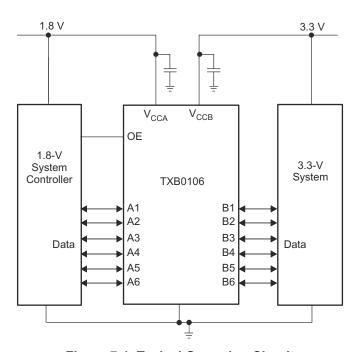


Figure 7-1. Typical Operating Circuit

2.1 Design Requirements

For this design example, use the parameters listed in Table 7-1. And make sure that V_{CCA} ≤ V_{CCB}.

Table 7-1. Design Parameters

DESIGN PARAMETERS	EXAMPLE VALUE			
Input voltage range	1.2V to 3.6V			
Output voltage range	1.65V to 5.5V			

2.2 Detailed Design Procedure

To begin the design process, determine the following:

- · Input voltage range
- Use the supply voltage of the device that is driving the TXB0106-Q1 device to determine the input voltage range. For a valid logic high the value must exceed the V_{IH} of the input port. For a valid logic low the value must be less than the V_{II} of the input port.
- Output voltage range
- Use the supply voltage of the device that the TXB0106-Q1 device is driving to determine the output voltage range.
- Avoid the use of external pullup or pulldown resistors, if possible. If not possible, it is recommended the value should be larger than 50 k Ω .
- An external pulldown or pullup resistor decreases the output V_{OH} and V_{OL} . Use the following equations to estimate the V_{OH} and V_{OL} as a result of an external pulldown and pullup resistor. See *Effects of External Pullup and Pulldown Resistors on TXS and TXB Devices* and *Factors Affecting VOL for TXS and LSF Auto-bidirectional Translation Devices*.

$$V_{OH} = V_{CCx} \times R_{PD} / (R_{PD} + 4.5 \text{ k}\Omega)$$
$$V_{OL} = V_{CCx} \times 4.5 \text{ k}\Omega / (R_{PU} + 4.5 \text{ k}\Omega)$$

Where

- V_{CCx} is the output port supply voltage on either V_{CCA} or V_{CCB}
- R_{PD} is the value of the external pulldown resistor
- R_{PU} is the value of the external pullup resistor
- 4.5 k Ω accounts for the tolerance of the serial 4-k Ω resistor in the I/O line.

2.3 Application Curve

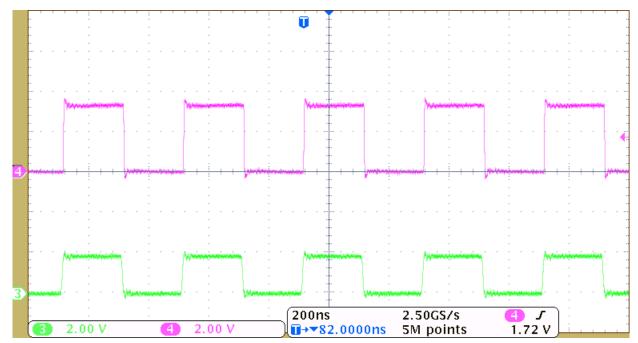


Figure 7-2. Level Translation of a 2.5MHz Signal

3 Power Supply Recommendations

During operation, ensure that $V_{CCA} \le V_{CCB}$ at all times. During power-up sequencing, $V_{CCA} \ge V_{CCB}$ does not damage the device, so any power supply can be ramped up first. The TXB0106-Q1 device has circuitry that disables all output ports when either V_{CC} is switched off (V_{CCA} or $V_{CCB} = 0V$). The output-enable (OE) input circuit is designed so that it is supplied by V_{CCA} , and when the (OE) input is low, all outputs are placed in the high-impedance state. To ensure the high-impedance state of the outputs during power up or power down, the OE input pin must be tied to GND through a pulldown resistor and must not be enabled until V_{CCA} and V_{CCB} are fully ramped and stable. The minimum value of the pulldown resistor to ground is determined by the current-sourcing capability of the driver.

4 Layout

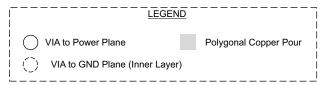
4.1 Layout Guidelines

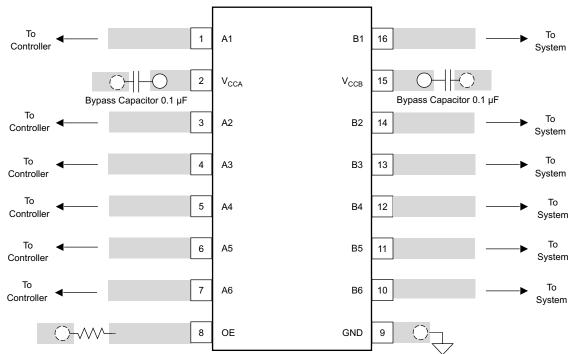
To ensure reliability of the device, the following common printed-circuit board layout guidelines are recommended:

- Bypass capacitors should be used on power supplies, and should be placed as close as possible to the V_{CCA} and V_{CCB} pins and the GND pin
- · Short trace-lengths should be used to avoid excessive loading.
- PCB signal trace-lengths must be kept short enough so that the round-trip delay of any reflection is less than
 the O.S. duration, approximately 10ns, ensuring that any reflection encounters low impedance at the source
 driver.



4.2 Layout Example





Keep OE Low Until V_{CCA} and V_{CCB} Are Powered Up



7 Device and Documentation Support

7.1 Third-Party Products Disclaimer

TI'S PUBLICATION OF INFORMATION REGARDING THIRD-PARTY PRODUCTS OR SERVICES DOES NOT CONSTITUTE AN ENDORSEMENT REGARDING THE SUITABILITY OF SUCH PRODUCTS OR SERVICES OR A WARRANTY, REPRESENTATION OR ENDORSEMENT OF SUCH PRODUCTS OR SERVICES, EITHER ALONE OR IN COMBINATION WITH ANY TI PRODUCT OR SERVICE.

7.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

7.3 Support Resources

TI E2E[™] support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

7.4 Trademarks

TI E2E[™] is a trademark of Texas Instruments.

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7.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

7.6 Glossary

TI Glossary

This glossary lists and explains terms, acronyms, and definitions.



8 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (April 2018) to Revision B (August 2025)	Page
Added Operating ambient temperature for TXB0106-Q1	5
Added BQB column in Section 5.4	6
Added Section 5.6 for TXB0106Q1	7
Added Section 5.14 for TXB0106-Q1	9
Added Section 5.16 for TXB0106-Q1	10
Added Section 5.18 for TXB0106-Q1	
Added Section 5.20 for TXB0106-Q1	12
Changes from Revision * (August 2009) to Revision A (April 2018)	Page
Added Applications section, ESD Ratings table, Feature Description section, Application and Implementation section, Power Supply Recommodure and Documentation Support section, and Mechanical, Packaging	tion, Device Functional Modes nendations section, Layout section,
section	
• Changed the entry in the TYPE column from "—" to "I" for V_{CCA} and V_{CC}	
Added row for junction temperature to Absolute Maximum Ratings	
Added parameter descriptions to Electrical Characteristics table	

DATE	REVISION	NOTES				
August 2009	*	Initial Release				

9 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most-current data available for the designated device. This data is subject to change without notice and without revision of this document. For browser-based versions of this data sheet, see the left-hand navigation pane.

21-May-2025 www.ti.com

PACKAGING INFORMATION

Orderable part number	Status	Material type	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material	MSL rating/ Peak reflow	Op temp (°C)	Part marking (6)
TXB0106IPWRQ1	Active	Production	TSSOP (PW) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	YE06Q1
TXB0106IPWRQ1.A	Active	Production	null (null)	2000 LARGE T&R	-	NIPDAU	Level-1-260C-UNLIM	See TXB0106IPWRQ1	YE06Q1
TXB0106IPWRQ1.B	Active	Production	null (null)	2000 LARGE T&R	-	NIPDAU	Level-1-260C-UNLIM	See TXB0106IPWRQ1	YE06Q1

⁽¹⁾ Status: For more details on status, see our product life cycle.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TXB0106-Q1:

Catalog: TXB0106

⁽²⁾ Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ RoHS values: Yes, No. RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

⁽⁴⁾ Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.



PACKAGE OPTION ADDENDUM

www.ti.com 21-May-2025

NOTE: Qualified Version Definitions:

 $_{\bullet}$ Catalog - TI's standard catalog product

PACKAGE MATERIALS INFORMATION

www.ti.com 25-Jul-2025

TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TXB0106IPWRQ1	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

PACKAGE MATERIALS INFORMATION

www.ti.com 25-Jul-2025

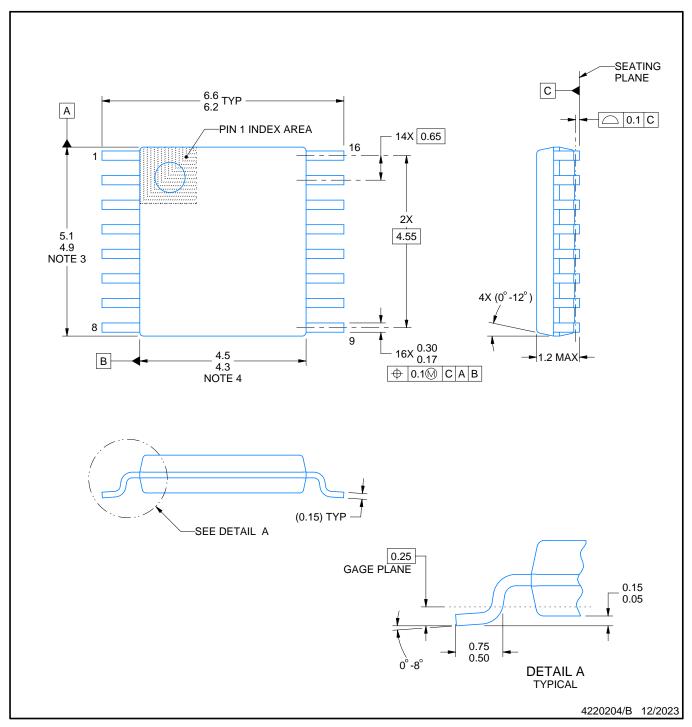


*All dimensions are nominal

	Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ı	TXB0106IPWRQ1	TSSOP	PW	16	2000	353.0	353.0	32.0



SMALL OUTLINE PACKAGE



NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

 2. This drawing is subject to change without notice.

 3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm per side.
- 4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
- 5. Reference JEDEC registration MO-153.



SMALL OUTLINE PACKAGE



NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SMALL OUTLINE PACKAGE



NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.



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