TSM36CA-Q1 Automotive Bidirectional Surge Protection Device in SOT-23

1 Features

- ISO 10605 (330pF, 330Ω) ESD protection:
  - ±30kV contact discharge
  - ±30kV air gap discharge
- IEC61000-4-5 surge protection:
  - 20A (8/20µs)
  - Clamping voltage: 55V at 20A (8/20µs)
- IO capacitance: 15pF (typical)
- Low leakage current: 100nA (maximum)
- Temperature range: -55°C to +150°C
- AEC-Q101 qualified
- Leaded package used for automatic optical inspection (AOI)

2 Applications

- I/O Protection
- Power line Protection
- Body Electronics & Lighting
- Hybrid, Electric, & Powertrain Systems

3 Description

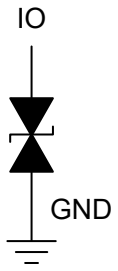
The TSM36A-Q1 is a 36V, bidirectional TVS protection diode designed for clamping harmful transients such as ESD and surge. The TSM36A-Q1 robustly shunts up to 20A of IEC 61000-4-5 fault current to protect systems from high power transients or lightning strikes.

Additionally, the TSM36A-Q1 is available in a small leaded SOT-23 (DBZ) package which is reduced in size by approximately 50 percent compared to the industry standard SMA package. The extremely low device leakage and capacitance ensures a minimal effect on the protected line.

Package Information

PART NUMBER	PACKAGE (1)	PACKAGE SIZE (2)
TSM36A-Q1	DBZ (SOT-23, 3)	2.92mm × 2.37mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Functional Block Diagram

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4 Pin Configuration and Functions

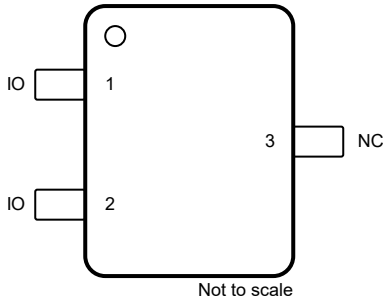

Figure 4-1. DBZ Package, 3-Pin SOT-23 (Top View)

Table 4-1. Pin Functions

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
IO	1,2	I/O	Surge and ESD protected IO. Connect other pin to ground.
NC	3	NC	Leave this pin floating for proper performance.

(1) I = Input, O = Output, I/O = Input or Output, NC = No connect

5 Specifications

5.1 Absolute Maximum Ratings

T_A = 25°C (unless otherwise noted) (1)

Parameter		MIN	MAX	UNIT
P_{PPM}	IEC 61000-4-5 Power (t_p - 8/20 µs) Peak Pulse Power at 25°C		1400	W
I_{PPM}	IEC 61000-4-5 Current (t_p - 8/20 µs) Peak Pulse Current at 25°C		20	A
T_A	Operating free-air temperature	–55	150	°C
T_{stg}	Storage temperature	–65	155	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

5.2 ESD Ratings—AEC Specification

Paraemter			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q101-002(1)	± 2500	V
		Charged device model (CDM), per AEC Q101-011(2)	± 1000	

(1) AEC Q101-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.
(2) AEC Q101-011 indicates that CDM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-002 specification.

5.3 ESD Ratings—IEC Specification

T_A = 25°C (unless otherwise noted)

Parameter			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	IEC 61000-4-2 Contact Discharge, all pins	±30000	V
		IEC 61000-4-2 Air-gap Discharge, all pins	±30000	

5.4 ESD Ratings - ISO Specifications

Parameter		Test Conditions		VALUE	UNIT
$V_{(ESD)}$	ISO 10605 Electrostatic Discharge	C = 150pF; R = 330Ω	Contact Discharge, all pins	±30000	V
			Air-gap Discharge, all pins	±30000	
		C = 330pF; R = 330Ω	Contact Discharge, all pins	±30000	
			Air-gap Discharge, all pins	±30000	

5.5 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

Parameter		MIN	NOM	MAX	UNIT
V_{IN}	Input voltage	–36		36	V
T_A	Operating free-air temperature	–55		150	°C

5.6 Thermal Information

THERMAL METRIC (1)		TSM36CA-Q1 DBZ (SOT-23) 3 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	203.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	105.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	36.7	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	8.5	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	36.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

5.7 Electrical Characteristics

T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{RWM}	Reverse stand-off voltage		–36		36	V
V_{BR}	Breakdown voltage(1)	I_{IO} = 10mA, IO to GND and GND to IO	37.8		44.2	V
V_{CLAMP}	Surge clamping voltage, t_p = 8/20µs (2)	I_{PP} = 10A, IO to GND		47	58	V
V_{CLAMP}	Surge clamping voltage, t_p = 8/20µs (2)	I_{PP} = 20A, IO to GND		55	71	V
I_{LEAK}	Leakage current	V_{IO} = +36V		25	100	nA
R_{DYN}	Dynamic resistance	t_p = 8/20µs, from IO to GND		1.0		Ω
C_{LINE}	Line capacitance	V_{IO} = 0V, f = 1MHz, V_{p-p} = 30mV		15	20	pF

(1) V_{BR} is defined as the voltage when ±10mA is applied in the positive-going direction.
(2) Device stressed with 8/20µs exponential decay waveform according to IEC 61000-4-5.

5.8 Typical Characteristics

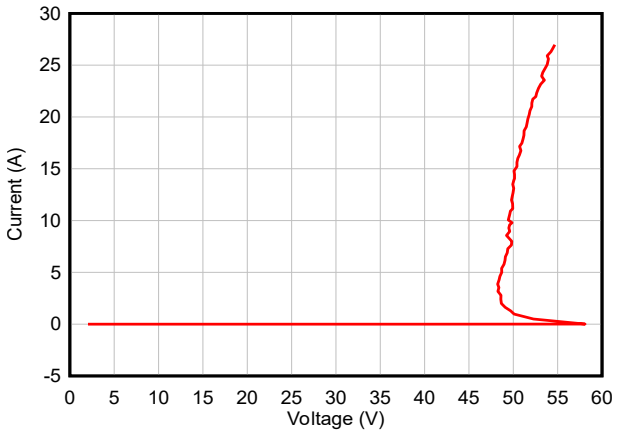

Figure 5-1. Positive TLP Curve

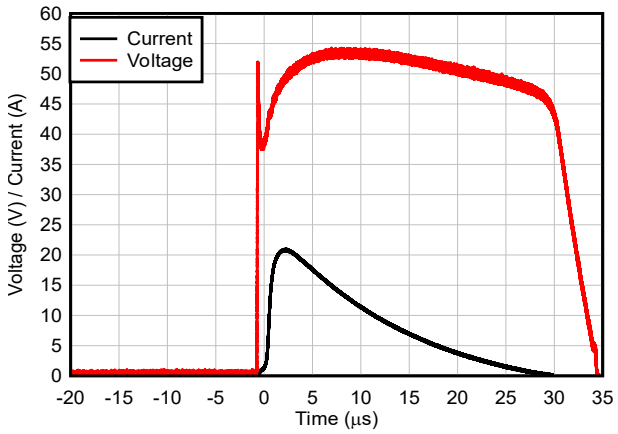

Figure 5-2. 8/20µs Surge Response

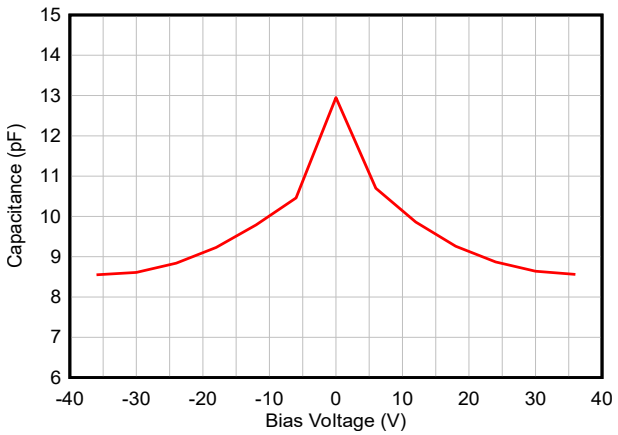

Figure 5-3. Capacitance vs Bias Voltage

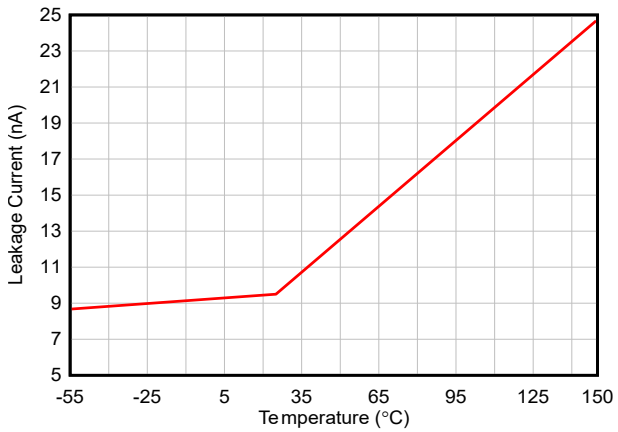

Figure 5-4. Leakage Current vs Temperature

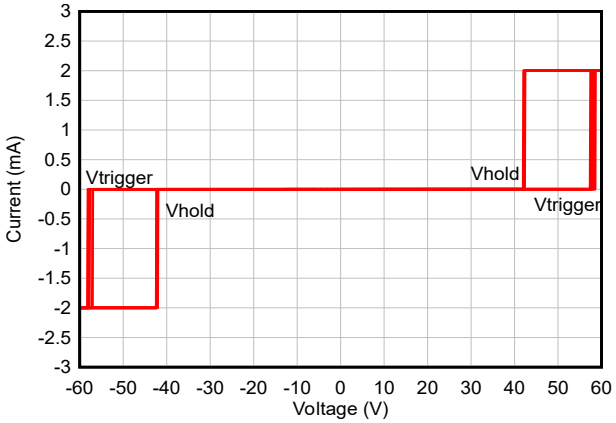

Figure 5-5. DC Voltage Sweep I-V Curve

6 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

6.1 Application Information

TSM36A-Q1 is a diode type TVS that provides a path to ground for dissipating transient voltage spikes, such as ESD or surge, on signal lines and power lines. Connect the device in parallel to the down stream circuitry for protection. As the current from the transient passes through the device, only a small voltage drop is present across the diode. This is the voltage presented to the protected IC. The low R_{DYN} of the triggered TVS holds this voltage (V_{CLAMP}) to a safe level for the protected IC. For more information on how to properly use this device, refer to the ESD Packaging and Layout Guide for details.

7 Device and Documentation Support

7.1 Documentation Support

7.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *TI's IEC 61000-4-x Testing* application note
- Texas Instruments, *ESD Layout Guide* user's guide
- Texas Instruments, *ESD Protection Diodes EVM* user's guide
- Texas Instruments, *Generic ESD Evaluation Module* user's guide
- Texas Instruments, *Reading and Understanding an ESD Protection Data Sheet* user's guide

7.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

7.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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7.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

7.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

8 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
January 2025	*	Initial Release

9 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TSM36CADBZRQ1	Active	Production	SOT-23 (DBZ) | 3	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-55 to 150	(3LFG, 3LI8)

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

OTHER QUALIFIED VERSIONS OF TSM36CA-Q1 :

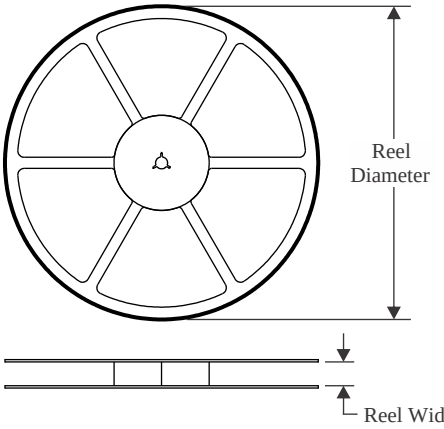
- Catalog : TSM36CA

NOTE: Qualified Version Definitions:

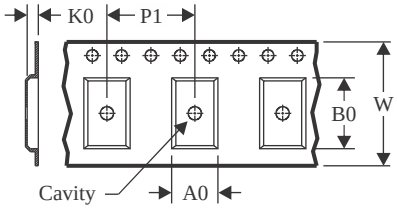
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

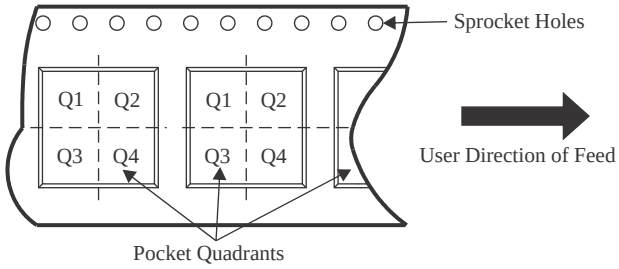


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

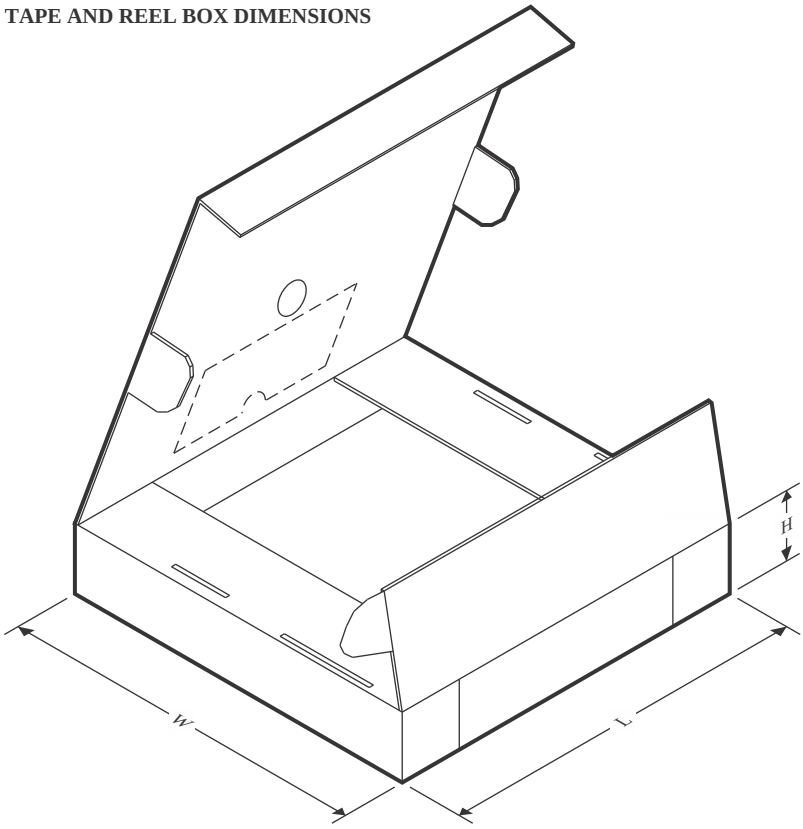
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TSM36CADBZRQ1	SOT-23	DBZ	3	3000	180.0	8.4	3.2	2.85	1.3	4.0	8.0	Q3
TSM36CADBZRQ1	SOT-23	DBZ	3	3000	180.0	8.4	2.9	3.35	1.35	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

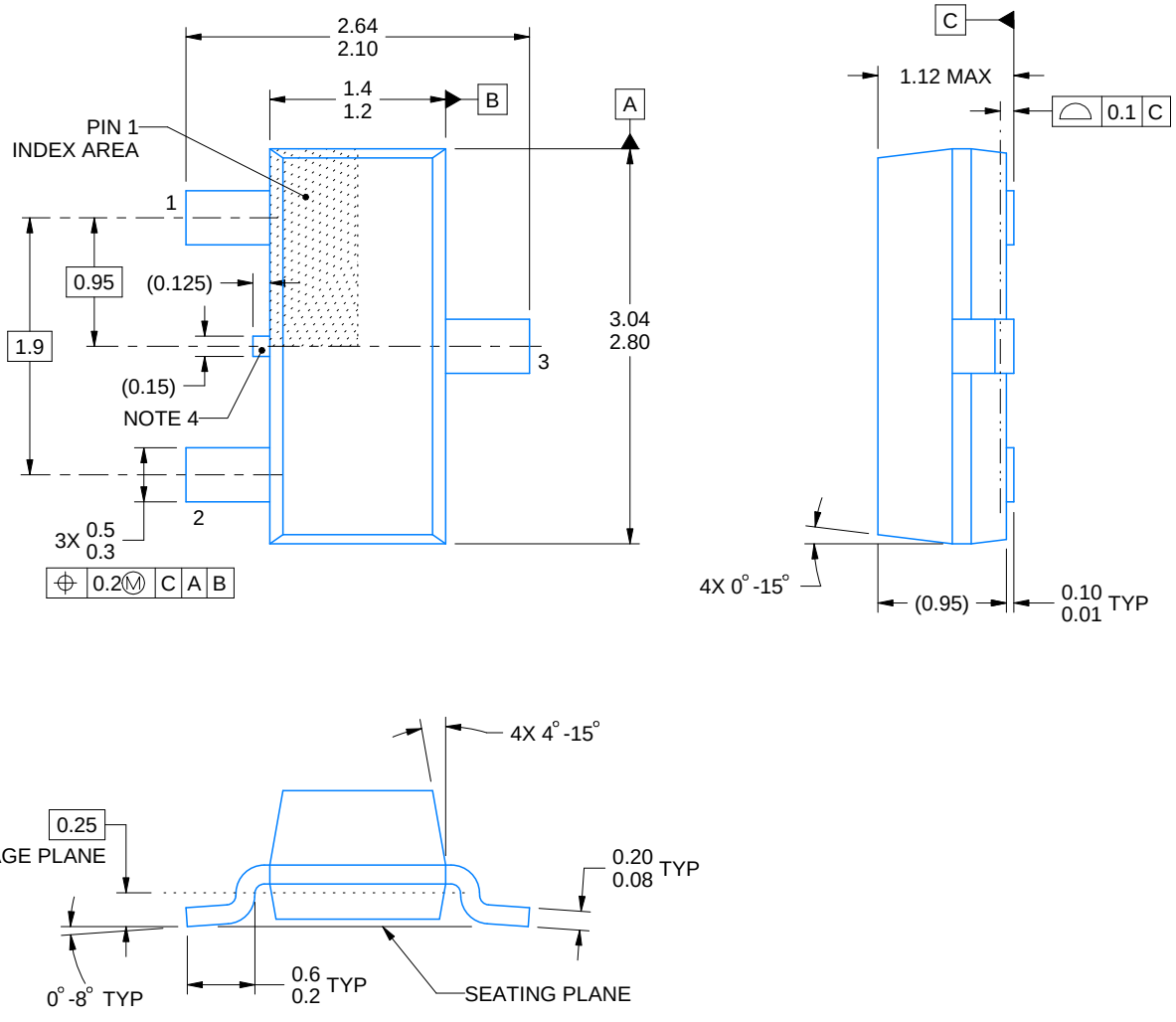
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TSM36CADBZRQ1	SOT-23	DBZ	3	3000	210.0	185.0	35.0
TSM36CADBZRQ1	SOT-23	DBZ	3	3000	210.0	185.0	35.0

PACKAGE OUTLINE

DBZ0003A

SOT-23 - 1.12 mm max height

SMALL OUTLINE TRANSISTOR



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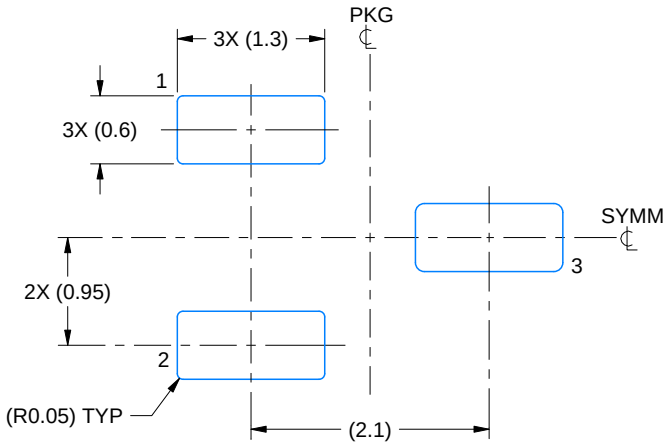
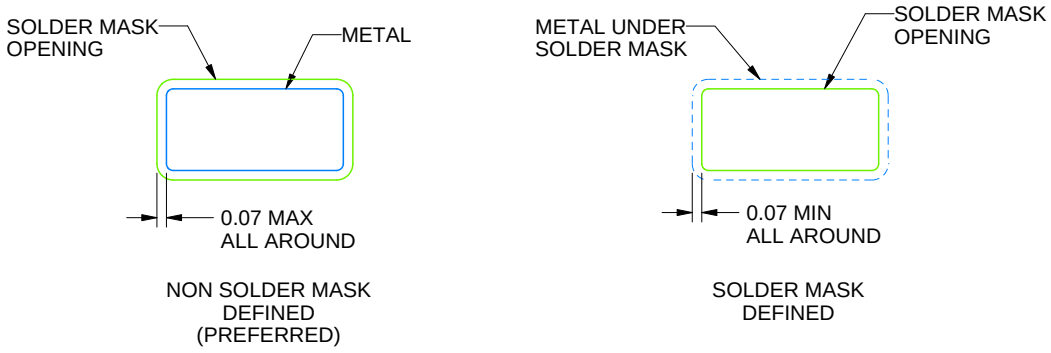
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC registration TO-236, except minimum foot length.
4. Support pin may differ or may not be present.
5. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25mm per side



LAND PATTERN EXAMPLE
SCALE:15X



SOLDER MASK DETAILS

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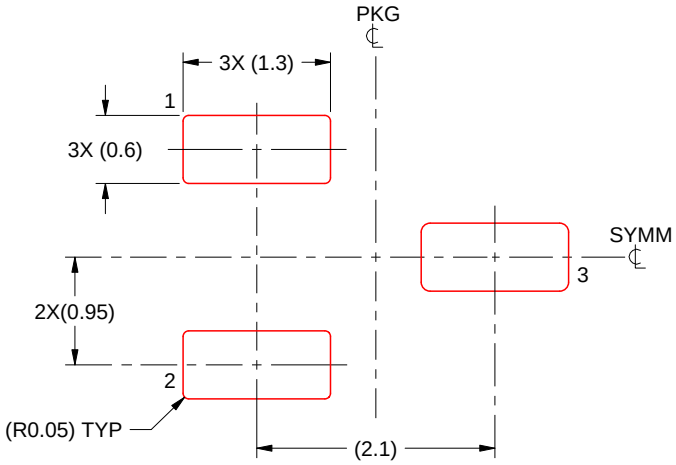
NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:15X

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NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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