

USB 2.0 High-Speed (480 Mbps) and Audio Switches with Negative Signal Capability and 1.8-V Logic Compatibility

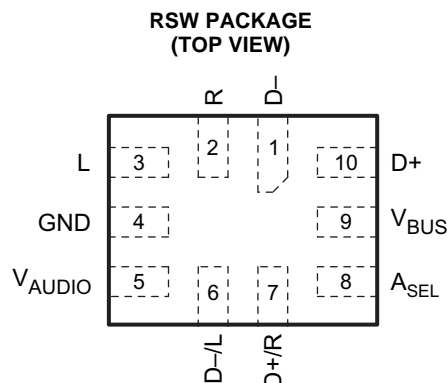
Check for Samples: [TS5USBA224](#)

FEATURES

- **High-Speed USB Switch:**
 - 4 Ω $R_{DS(on)}$ Typical
 - 12.5 pF C_{ON} Typical
 - 650-MHz Bandwidth (–3 dB)
- **Audio Switch:**
 - 3 Ω $R_{DS(on)}$ Typical
 - Negative Rail Capability
 - Low THD: <0.05%
 - Internal Shunt Resistors for Click-and-Pop Reduction
 - Powered From V_{AUDIO} (2.7V to 5.5V)
- **1.8-V Compatible Control Input (A_{SEL} and V_{BUS}) Threshold**
- **I_{OFF} Supports Partial Powerdown Mode**
- **ESD Performance Tested Per JESD 22**
 - 2000-V Human-Body Model (A114-B, Class II)
 - 1000-V Charged-Device Model (C101)
 - 200-V Machine Model (A115-A)

APPLICATIONS

- Cellular Phones
- Personal Digital Assistants (PDAs)
- Portable Instrumentation
- Digital Still Cameras
- Portable Navigation Devices



DESCRIPTION

The TS5USBA224 is a double-pole, double throw (DPDT) multiplexer that includes a low-distortion audio switch and a USB 2.0 High-Speed (480Mbps) switch in the same package. This configuration allows the system designer to use a common connector for audio and USB data. The audio switch is designed to allow audio signals to swing below ground which makes this common connector configuration possible.

The TS5USBA224 is powered up using V_{AUDIO} . When A_{SEL} =High, the audio path is selected regardless of the logic level at V_{BUS} . If A_{SEL} =Low and V_{BUS} =High, the USB path is selected. Otherwise if A_{SEL} =Low and V_{BUS} =Low, the audio path is selected.

The TS5USBA224 also features shunt resistors on the audio path to reduce clicks and pops that may be heard when the audio switches are selected.

ORDERING INFORMATION

T_A	PACKAGE ⁽¹⁾ ⁽²⁾		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	QFN 0.4-MM PITCH – RSW (Pb-Free)	Tape and reel	TS5USBA224RSWR	A5R

(1) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

(2) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

SUMMARY OF TYPICAL CHARACTERISTICS

	USB PATH	AUDIO PATH
Number of switches	2	2
ON-state resistance (r_{on})	4 Ω	3 Ω
ON-state resistance match (Δr_{on})	< 0.3 Ω	< 0.3 Ω
ON-state resistance flatness ($r_{on(flat)}$)	N/A	1.5 Ω
Turn-on/turn-off time (t_{ON}/t_{OFF})	< 2 μs	< 4 μs
Bandwidth (BW)	650 MHz	N/A
OFF isolation (O_{ISO})	–22 dB	–83 dB
Crosstalk (X_{TALK})	–31 dB	–83 dB
Total harmonic distortion (THD)	N/A	0.05%

PIN DESCRIPTION TABLE

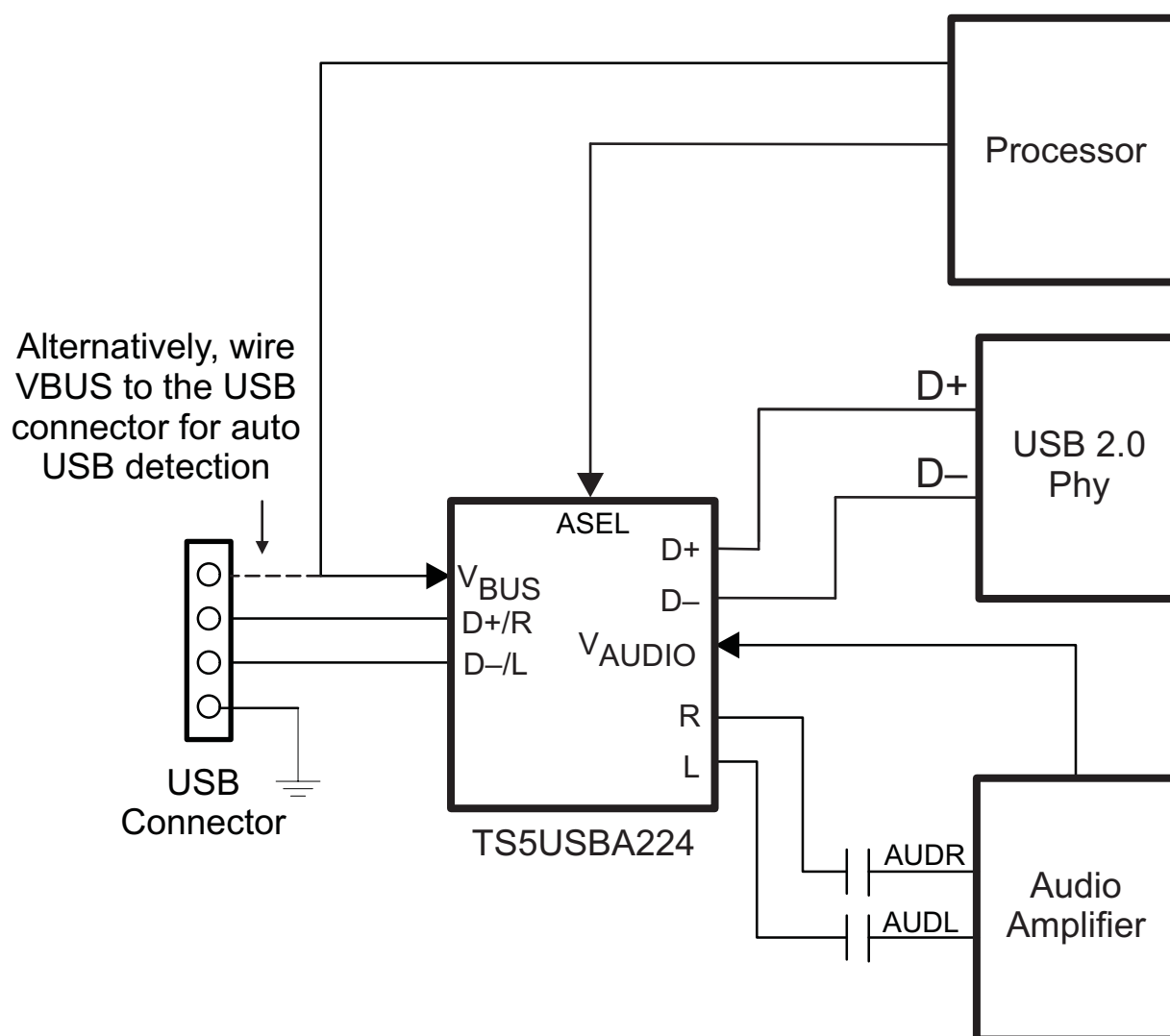
PIN			DESCRIPTION
NO.	NAME	TYPE	
1	D–	I/O	USB Data (Differential –)
2	R	I/O	Right Channel Audio
3	L	I/O	Left Channel Audio
4	GND	Ground	Ground
5	V _{AUDIO}	Power	Supply Voltage
6	D–/L	I/O	USB/Audio Common Connector
7	D+/R	I/O	USB/Audio Common Connector
8	A _{SEL}	Input	Control Input for Audio Path
9	V _{BUS}	Input	Control Input for USB Path
10	D+	I/O	USB Data (Differential +)

FUNCTION TABLE

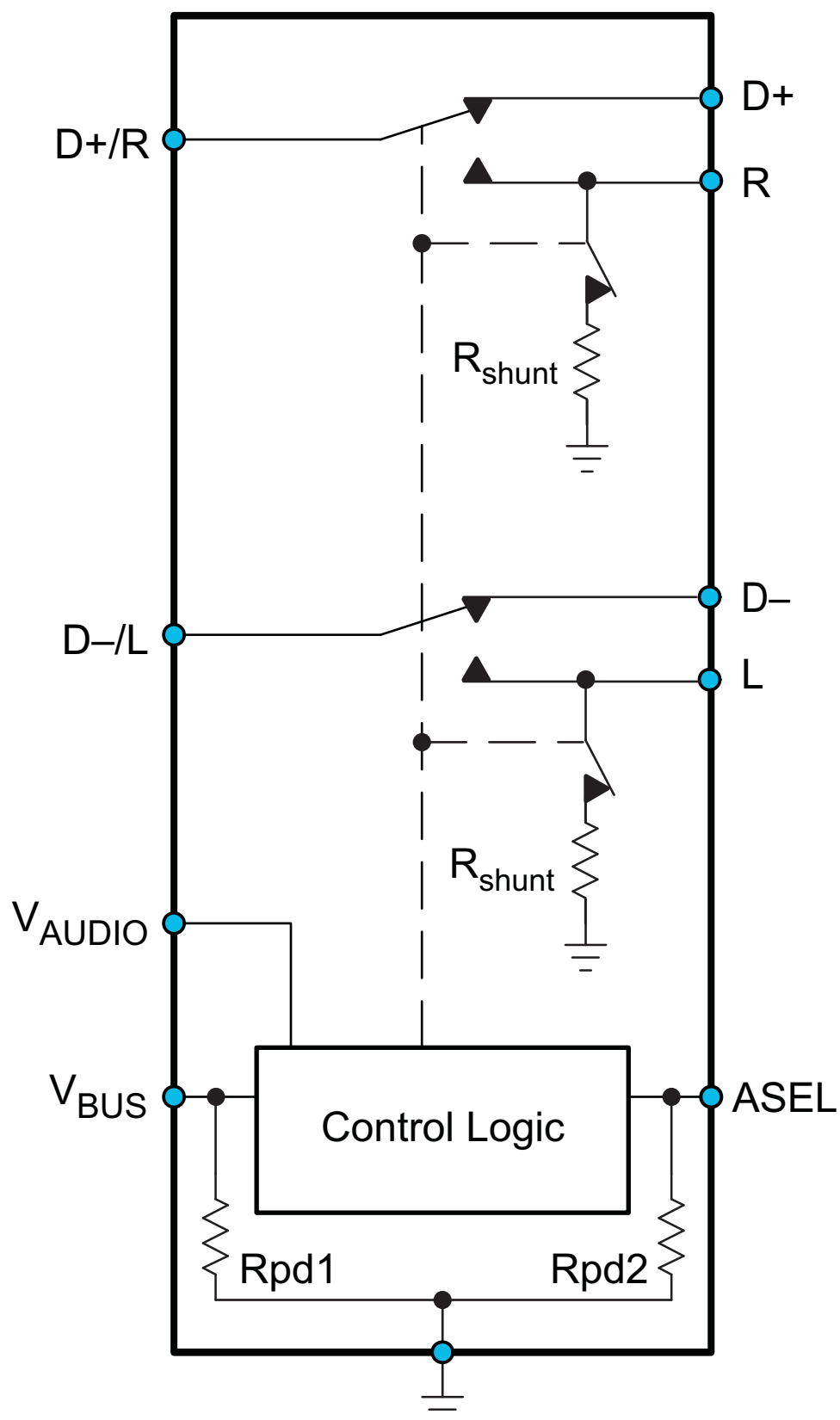
A _{SEL}	V _{AUDIO}	V _{BUS}	L,R	D+, D–
L	L	L	OFF	OFF
L	L	H	OFF	OFF
L	H	L	ON	OFF
L	H	H	OFF ⁽¹⁾	ON
H	L	L	OFF	OFF
H	L	H	OFF	OFF
H	H	L	ON	OFF
H	H	H	ON	OFF

(1) 100Ω shunt resistors are enabled in this state.

TYPICAL APPLICATION BLOCK DIAGRAM



SWITCH BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS⁽¹⁾⁽²⁾

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V _{AUDIO}	Supply voltage range ⁽³⁾		–0.5	6.5	V
V _{D+} V _{D–}	Analog voltage Range ⁽³⁾		–0.5	6.5	V
V _R V _L			V _{AUDIO} – 6.5	V _{AUDIO} + 0.5	V
I _K	Analog port diode current	V _{D+} , V _{D–} < 0	–50		mA
I _{D+} , I _{D–} I _R , I _L	ON-state switch current	V _{D+} , V _{D–} = 0 to V _{AUDIO} , V _R , V _L V _{D+/R} , V _{D–/L} = V _{AUDIO} – 5.5 V to V _{AUDIO}	–100	100	mA
I _{D+/R} I _{D–/L}	ON-state peak switch current ⁽⁴⁾		–200	200	
V _I	Digital input voltage range		–0.5	6.5	V
I _{IK}	Digital logic input clamp current ⁽³⁾	V _I < 0		–50	mA
I _{AUDIO}	Continuous current through V _{AUDIO}			100	mA
I _{GND}	Continuous current through GND		–100		mA
T _{stg}	Storage temperature range		–65	150	°C

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum.
- (3) All voltages are with respect to ground, unless otherwise specified.
- (4) Pulse at 1-ms duration <10% duty cycle.

PACKAGE THERMAL IMPEDANCE⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	TYP	UNIT
θ _{JA}	Package thermal impedance RSW package	175	°C/W

- (1) The package thermal impedance is calculated in accordance with JESD 51-7.

ELECTRICAL CHARACTERISTICS

T_A = –40°C to 85°C, typical values are at V_{AUDIO} = 3.3 V, T_A = 25°C (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
USB SWITCH					
V _{D+} , V _{D–}	Analog voltage range	0		5.5	V
r _{on}	ON-state resistance V _{AUDIO} = 3 V, V _{BUS} = 5 V, V _{ASEL} = 0 V, V _{D+/D–} = 0 V, 0.4 V, I _{ON} = –8 mA		4	7	Ω
Δr _{on}	ON-state resistance match between channels V _{AUDIO} = 3 V, V _{BUS} = 5 V, V _{ASEL} = 0 V, V _{D+/D–} = 0 V, 0.4 V, I _{ON} = –8 mA			0.3	Ω
I _{D+(OFF)} I _{D–(OFF)}	D+, D– OFF leakage current V _{AUDIO} = 3.6 V, V _{BUS} = 0 V, V _{ASEL} = 3.6 V, V _{D+} , V _{D–} = 0.3 V, V _{D+/R} , V _{D–/L} = 0.3 V			±50	nA
I _{D+(ON)} I _{D–(ON)}	D+, D– ON leakage current V _{AUDIO} = 3.6 V, V _{BUS} = 5 V, V _{ASEL} = 0 V, V _{D+} , V _{D–} = 0.3 V, V _{D+/R} = Open			±50	nA
AUDIO SWITCH					
V _R , V _L	Analog voltage range	V _{AUDIO} – 5.5	V _{AUDIO}		V
r _{on}	ON-state resistance V _{AUDIO} = 3 V, V _{BUS} = 0 V, V _{ASEL} = 3 V, V _{L/R} = –2 V, 0 V, 0.7 V, I _{ON} = –26 mA		3	5	Ω
Δr _{on}	ON-state resistance match between channels V _{AUDIO} = 3 V, V _{BUS} = 0 V, V _{ASEL} = 3 V, V _{L/R} = 0.7 V, I _{ON} = –26 mA			0.3	Ω
r _{on} (flat)	ON-state resistance flatness V _{AUDIO} = 3 V, V _{BUS} = 0 V, V _{ASEL} = 3 V, V _{L/R} = –2 V, 0 V, 0.7 V, I _{ON} = –26 mA		1.5	2.5	Ω

ELECTRICAL CHARACTERISTICS (continued)

$T_A = -40^{\circ}\text{C}$ to 85°C , typical values are at $V_{\text{AUDIO}} = 3.3\text{ V}$, $T_A = 25^{\circ}\text{C}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
r_{SHUNT}	Shunt resistance	$V_{\text{AUDIO}} = 3\text{ V}$, $V_{\text{BUS}} = 5\text{ V}$, $V_{\text{ASEL}} = 0\text{ V}$, $V_{\text{L/R}} = 0.7\text{ V}$, $I_{\text{OSHUNT}} = 10\text{ mA}$	Switch OFF		100	200	Ω
$I_{\text{L(OFF)}}$ $I_{\text{R(OFF)}}$	L , R OFF leakage current	$V_{\text{AUDIO}} = 3.6\text{ V}$, $V_{\text{BUS}} = 5\text{ V}$, $V_{\text{ASEL}} = 0\text{ V}$, $V_{\text{R}}, V_{\text{L}} = 0.3\text{ V}$, $V_{\text{AUDIO}} - 0.3\text{ V}$, $V_{\text{D+R}}, V_{\text{D-L}} = 0.3\text{ V}$, $V_{\text{AUDIO}} - 0.3\text{ V}$	Switch OFF			± 50	nA
$I_{\text{L(ON)}}$ $I_{\text{R(ON)}}$	L , R ON leakage current	$V_{\text{AUDIO}} = 3.6\text{ V}$, $V_{\text{BUS}} = 0\text{ V}$, $V_{\text{ASEL}} = 3.6\text{ V}$, $V_{\text{D+R}}, V_{\text{D-L}} = 0.3\text{ V}$, $V_{\text{R}}, V_{\text{L}} = 0.3\text{ V}$, $V_{\text{AUDIO}} - 0.3\text{ V}$, $V_{\text{AUDIO}} - 0.3\text{ V}$ $V_{\text{D+R}}, V_{\text{D-L}} = \text{Open}$	Switch ON			± 50	nA
DIGITAL CONTROL INPUTS (A_{SEL}, V_{BUS})							
V_{IH}	Input logic high	$V_{\text{AUDIO}} = 2.7\text{ V}$ to 5.5 V		1.2			V
V_{IL}	Input logic low	$V_{\text{AUDIO}} = 2.7\text{ V}$ to 5.5 V				0.5	V
I_{IN}	Input leakage current	$V_{\text{AUDIO}} = 3.6\text{ V}$	$V_{\text{IN}} = 3.6\text{ V}$			± 10	μA
			$V_{\text{IN}} = 0\text{ V}$			± 1	
r_{PD1}	Internal pulldown resistance				3		M Ω
r_{PD2}	Internal pulldown resistance				5		M Ω

DYNAMIC CHARACTERISTICS

$T_A = -40^{\circ}\text{C}$ to 85°C , typical values are at $V_{\text{AUDIO}} = 3.3\text{ V}$, $T_A = 25^{\circ}\text{C}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
USB SWITCH							
t _{ON}	Turn-on time	V _{AUDIO} = 3 V, V _{BUS} = 0 V to 5 V, V _{ASEL} = 0 V, V _{D+/R, D-/L} = 1 V, Figure 10		2			μs
t _{OFF}	Turn-off time	V _{AUDIO} = 3 V, V _{BUS} = 5 V to 0 V, V _{ASEL} = 0 V, V _{D+/R, D-/L} = 1 V, Figure 10		1			μs
t _{SK(O)}	Channel-to-channel skew	f = 240 MHz, Figure 11		35			ps
t _{SK(P)}	Skew of opposite transitions of same output	f = t 240 MHz, Figure 11		25			ps
C _{D+(OFF)} C _{D-(OFF)}	D+, D-OFF capacitance	V _{AUDIO} = 3 V, V _{BUS} = 0 V, A _{SEL} = 3 V, f = 240 MHz	Switch OFF	2.8			pF
C _{D+(ON)} C _{D-(ON)}	D+, D- ON capacitance	V _{AUDIO} = 3 V, V _{BUS} = 5 V, A _{SEL} = 0 V, f = 240 MHz	Switch ON	12.5			pF
C _I	Digital input capacitance	V _{AUDIO} = 3 V, V _{BUS} = 0 V, A _{SEL} = 0 V, f = 1 MHz		2.2			pF
BW	Bandwidth	V _{AUDIO} = 3 V, V _{BUS} = 5 V, V _{ASEL} = 0 V, Figure 12	Switch ON	650			MHz
O _{ISO}	OFF Isolation	V _{AUDIO} = 3 V, V _{BUS} = 0 V, V _{ASEL} = 3 V, R _L = 50 Ω, f = 240 MHz, Figure 14	Switch OFF	-22			dB
X _{TALK}	Crosstalk	V _{AUDIO} = 3 V, V _{BUS} = 5 V, V _{ASEL} = 0 V, R _L = 50 Ω, f = 240 MHz, Figure 13	Switch ON	-31			dB
AUDIO SWITCH							
t _{ON}	Turn-on time	V _{AUDIO} = 3 V, V _{BUS} = 0 V or 5 V, V _{ASEL} = 0 V to 3 V, V _{D+/R, D-/L} = 1 V, Figure 10		4			μs
t _{OFF}	Turn-off time	V _{AUDIO} = 3 V, V _{BUS} = 0 V, V _{ASEL} = 3 V to 0 V, V _{D+/R, D-/L} = 1 V, Figure 10		1			μs
C _{L(OFF)} C _{R(OFF)}	L , R OFF capacitance	V _{AUDIO} = 3 V, V _{BUS} = 5 V, V _{ASEL} = 0 V, f = 20 kHz	Switch OFF	4.5			pF
C _{L(ON)} C _{R(ON)}	L, R ON capacitance	V _{AUDIO} = 3 V, V _{BUS} = 0 V, V _{ASEL} = 3 V, f = 20 kHz	Switch ON	15			pF
O _{ISO}	OFF Isolation	V _{AUDIO} = 3 V, V _{BUS} = 5 V, V _{ASEL} = 0 V, R _L = 50 Ω, f = 20 kHz, Figure 14	Switch OFF	-83			dB
X _{TALK}	Crosstalk	V _{AUDIO} = 3 V, V _{BUS} = 0 V, V _{ASEL} = 3 V, R _L = 50 Ω, f = 20 kHz, Figure 13	Switch ON	-83			dB
THD	Total harmonic distortion	V _{AUDIO} = 3 V, V _{BUS} = 0 V, V _{ASEL} = 3 V, f = 20 Hz to 20 kHz, R _L = 600 Ω, V _{IN} = 2 V _{pp}		0.05			%
SUPPLY							
V _{AUDIO}	Power supply voltage			2.7		5.5	V
I _{AUDIO}	Positive supply current	V _{AUDIO} = 3.6 V, V _{BUS} = 0 or 5 V, V _{ASEL} = 0 to 3.6 V, I _{OUT} = 0		6		10	μA
I _{OFF}	Power off leakage current	V _{AUDIO} = 0 V, V _{D+/R, D-/L, D+, D-, L, R} = 0 to 5.5 V				±10	μA

TYPICAL CHARACTERISTICS

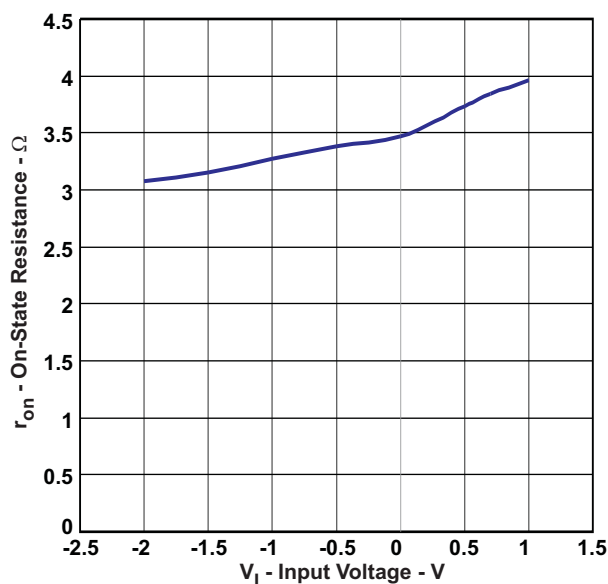
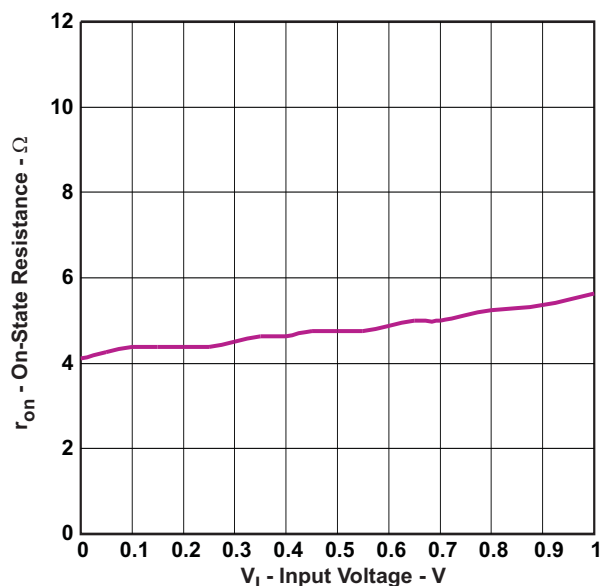
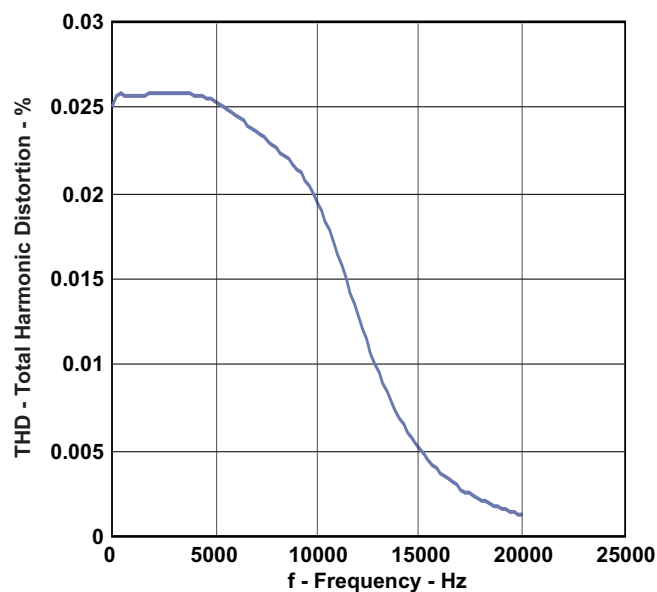
Figure 1. ON Resistance vs V_I for Audio SwitchFigure 2. ON Resistance vs V_I for USB Switch

Figure 3. THD vs Frequency for Audio Switch

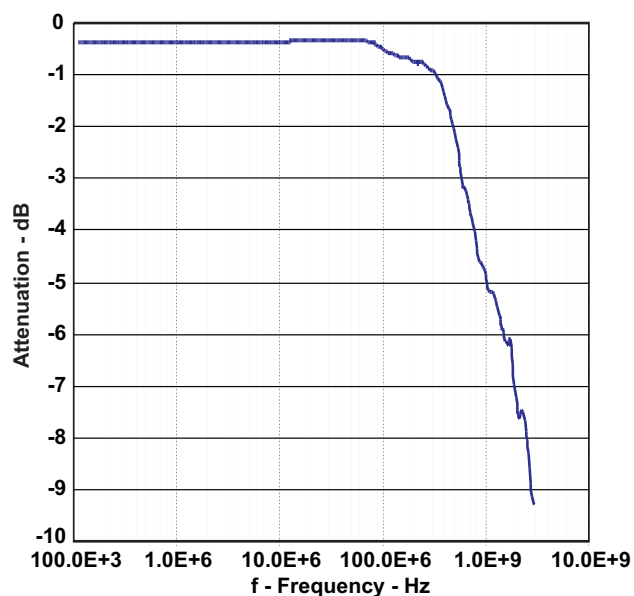


Figure 4. Gain vs Frequency for USB Switch

TYPICAL CHARACTERISTICS (continued)

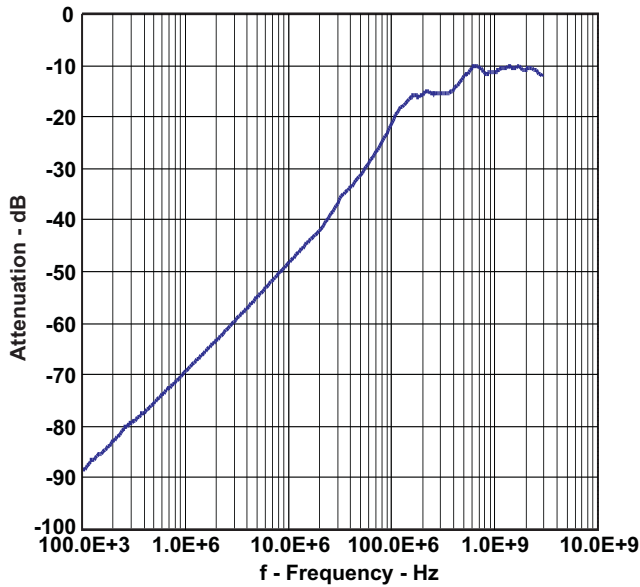


Figure 5. Off Isolation vs Frequency for Audio Switch

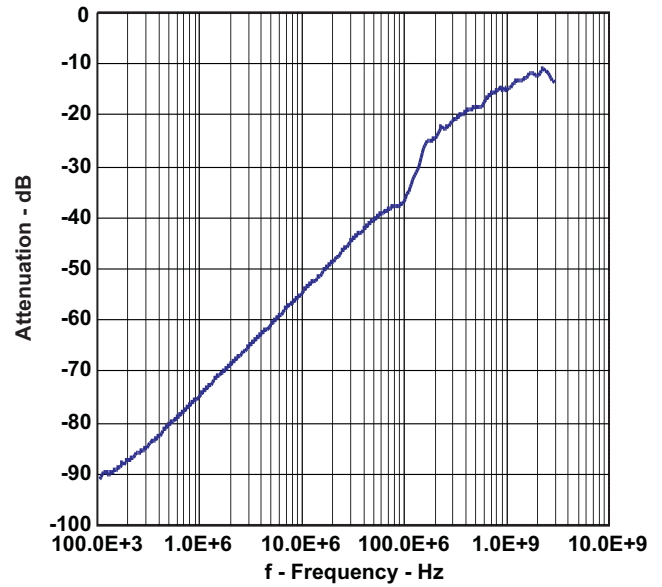


Figure 6. Off Isolation vs Frequency for USB Switch

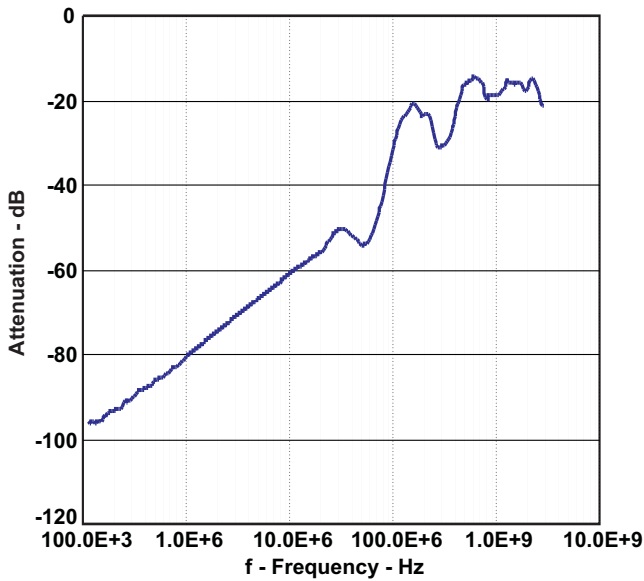


Figure 7. Cross Talk vs Frequency for Audio Switch

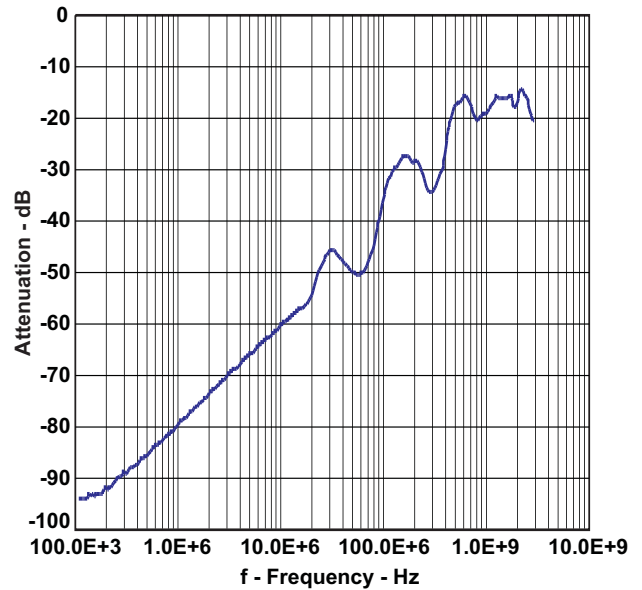


Figure 8. Cross Talk vs Frequency for USB Switch

TYPICAL CHARACTERISTICS (continued)

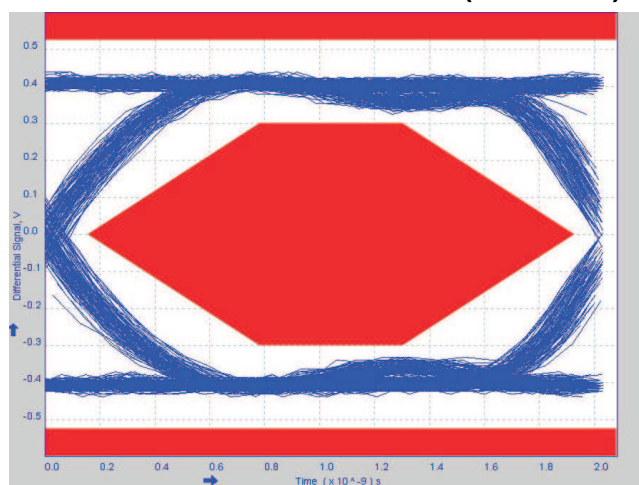
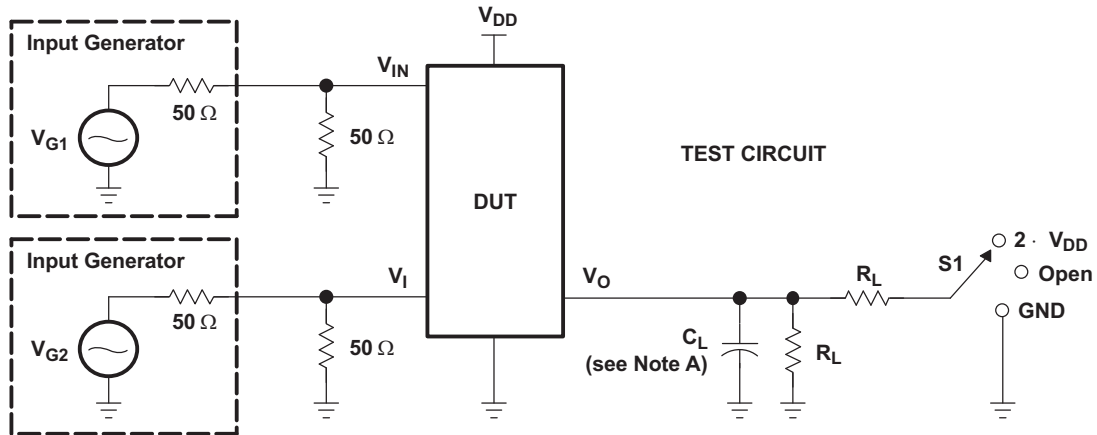
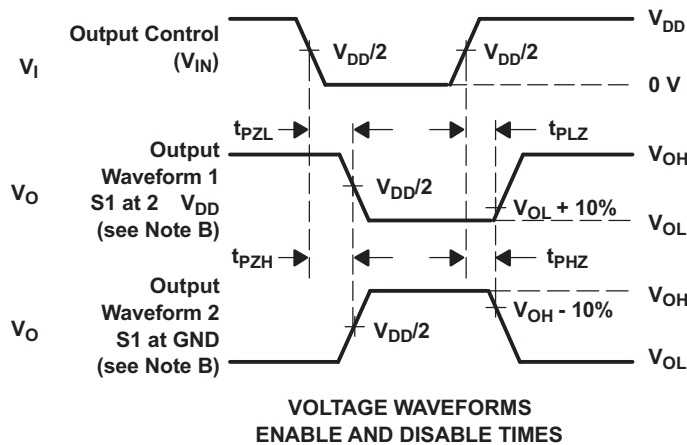


Figure 9. USB 2.0 Eye Pattern for USB Switch

PARAMETER MEASUREMENT INFORMATION (Enable and Disable Times)



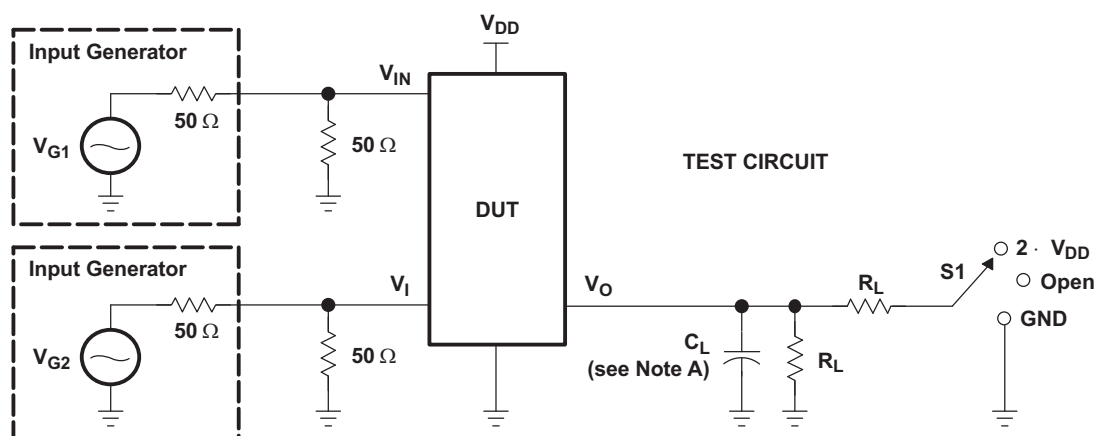
TEST	$V_{\text{AUDIO}} (V_{\text{DD}})$	S1	R_L	V_{in}	C_L	V_{Δ}
$t_{\text{PLZ}}/t_{\text{PZL}}$	3.3 V	$2 \cdot V_{\text{DD}}$	200 Ω	GND	10 pF	0.3 V
$t_{\text{PHZ}}/t_{\text{PZH}}$	3.3 V	GND	200 Ω	V_{DD}	10 pF	0.3 V



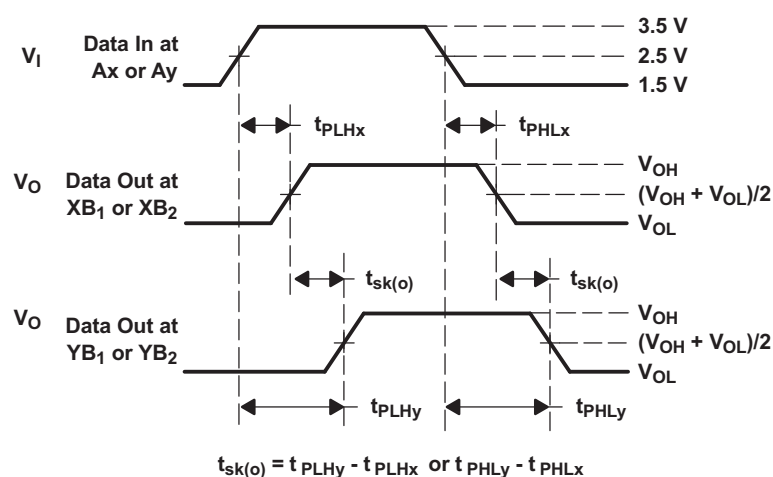
- NOTES:
- A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: $\text{PRR} \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$.
 - D. The outputs are measured one at a time, with one transition per measurement.
 - E. t_{PLZ} and t_{PHZ} are the same as t_{dis} or t_{OFF} .
 - F. t_{PZL} and t_{PZH} are the same as t_{en} or t_{ON} .

Figure 10. Test Circuit and Voltage Waveforms

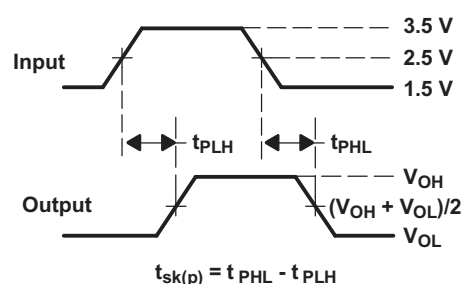
PARAMETER MEASUREMENT INFORMATION (Skew)



TEST	$V_{AUDIO} (V_{DD})$	S1	R_L	V_{in}	C_L
$t_{sk(o)}$	$3.3\text{ V} \pm 0.3\text{ V}$	Open	$200\ \Omega$	V_{DD} or GND	10 pF
$t_{sk(p)}$	$3.3\text{ V} \pm 0.3\text{ V}$	Open	$200\ \Omega$	V_{DD} or GND	10 pF



**VOLTAGE WAVEFORMS
OUTPUT SKEW ($t_{sk(o)}$)**

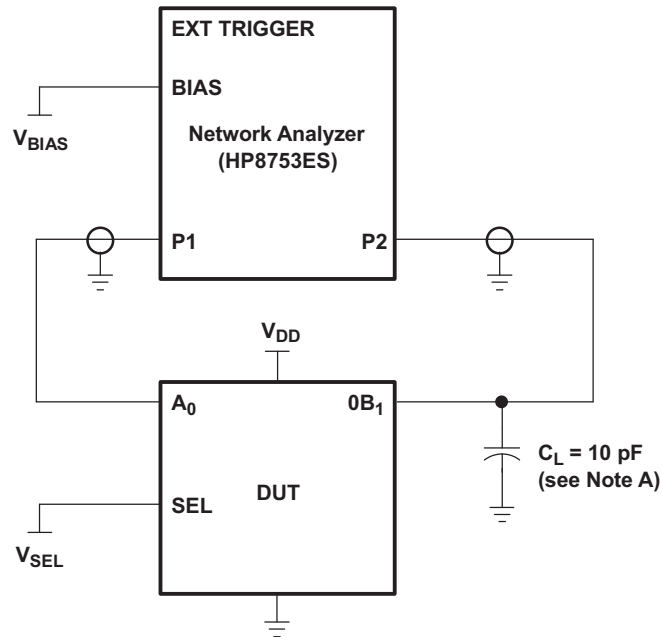


**VOLTAGE WAVEFORMS
PULSE SKEW [$t_{sk(p)}$]**

- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10\text{ MHz}$, $Z_O = 50\ \Omega$, $t_r \leq 2.5\text{ ns}$, $t_f \leq 2.5\text{ ns}$.
 D. The outputs are measured one at a time, with one transition per measurement.

Figure 11. Test Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION



A. C_L includes probe and jig capacitance.

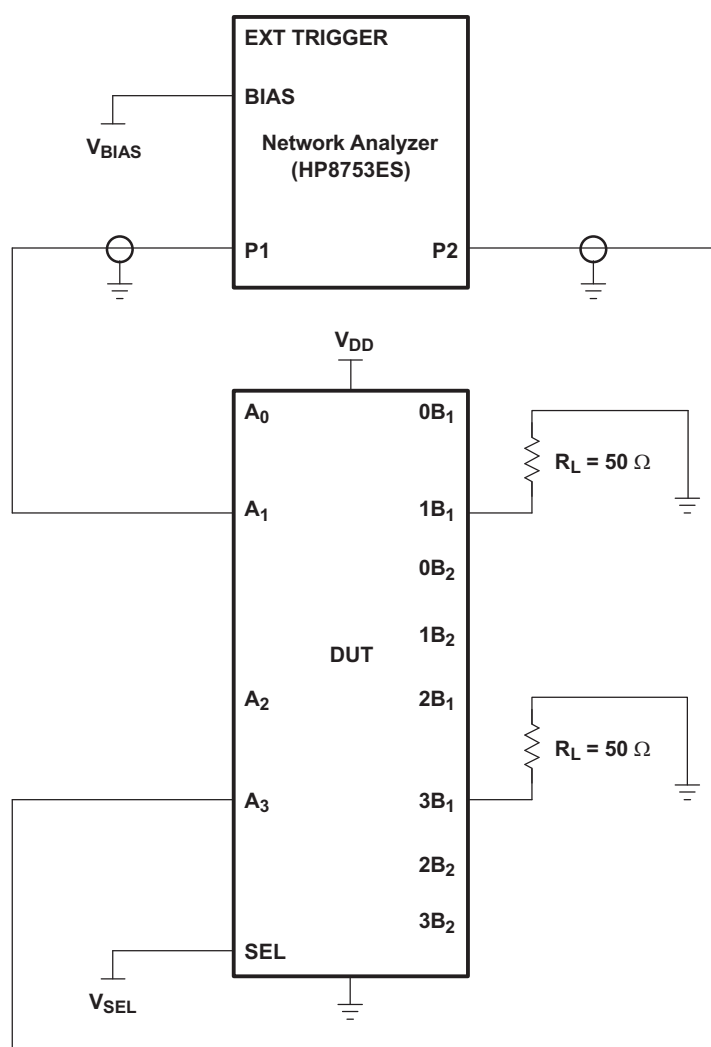
Figure 12. Test Circuit for Frequency Response (BW)

Frequency response is measured at the output of the ON channel. For example, when $V_{SEL} = 0$ and A₀ is the input, the output is measured at 0B₁. All unused analog I/O ports are left open.

HP8753ES Setup

Average = 4
 RBW = 3 kHz
 $V_{BIAS} = 0.35 \text{ V}$
 ST = 2 s
 P1 = 0 dBm

PARAMETER MEASUREMENT INFORMATION (continued)



- A. C_L includes probe and jig capacitance.
- B. A 50- Ω termination resistor is needed to match the loading of the network analyzer.

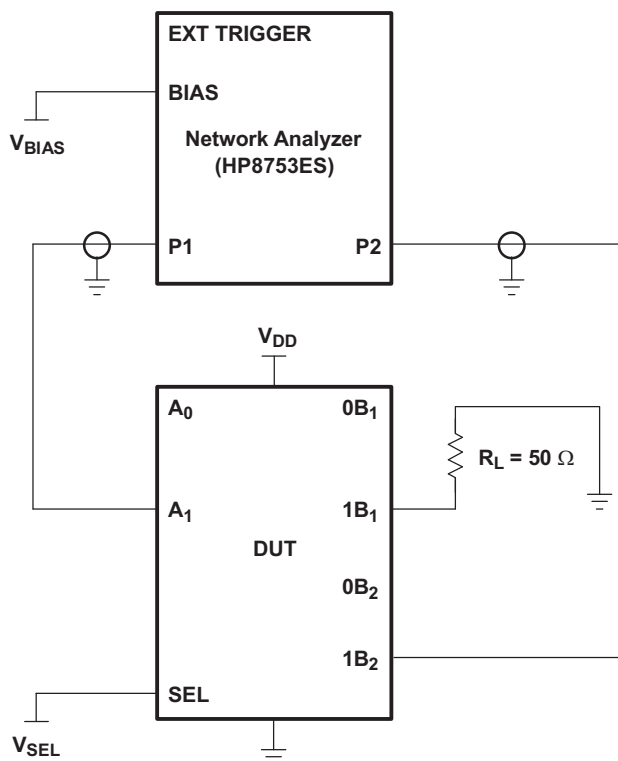
Figure 13. Test Circuit for Crosstalk (X_{TALK})

Crosstalk is measured at the output of the nonadjacent ON channel. For example, when $V_{SEL} = 0$ and A_1 is the input, the output is measured at A_3 . All unused analog input (A) ports are connected to GND, and output (B) ports are left open.

HP8753ES Setup

Average = 4
 RBW = 3 kHz
 $V_{BIAS} = 0.35$ V
 ST = 2 s
 P1 = 0 dBm

PARAMETER MEASUREMENT INFORMATION (continued)



- A. C_L includes probe and jig capacitance.
- B. A 50- Ω termination resistor is needed to match the loading of the network analyzer.

Figure 14. Test Circuit for OFF Isolation (O_{iso})

OFF isolation is measured at the output of the OFF channel. For example, when $V_{SEL} = GND$ and A_1 is the input, the output is measured at $1B_2$. All unused analog input (A) ports are connected to ground, and output (B) ports are left open.

HP8753ES Setup

Average = 4
 RBW = 3 kHz
 $V_{BIAS} = 0.35\text{ V}$
 ST = 2 s
 P1 = 0 dBm

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TS5USBA224RSWR	Active	Production	UQFN (RSW) 10	3000 LARGE T&R	Yes	NIPDAUAG NIPDAU	Level-1-260C-UNLIM	-40 to 85	(A5R, A5V)
TS5USBA224RSWR.B	Active	Production	UQFN (RSW) 10	3000 LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	(A5R, A5V)
TS5USBA224RSWRG4.B	Active	Production	UQFN (RSW) 10	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	A5V

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TS5USBA224RSWR	UQFN	RSW	10	3000	180.0	9.5	1.6	2.0	0.8	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TS5USBA224RSWR	UQFN	RSW	10	3000	189.0	185.0	36.0

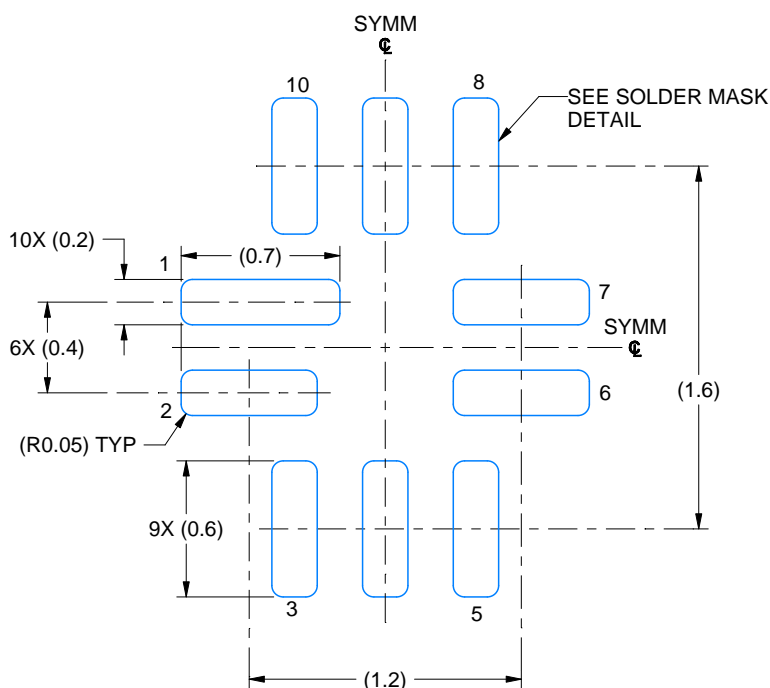
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package complies to JEDEC MO-288 variation UDEE, except minimum package height.

EXAMPLE BOARD LAYOUT

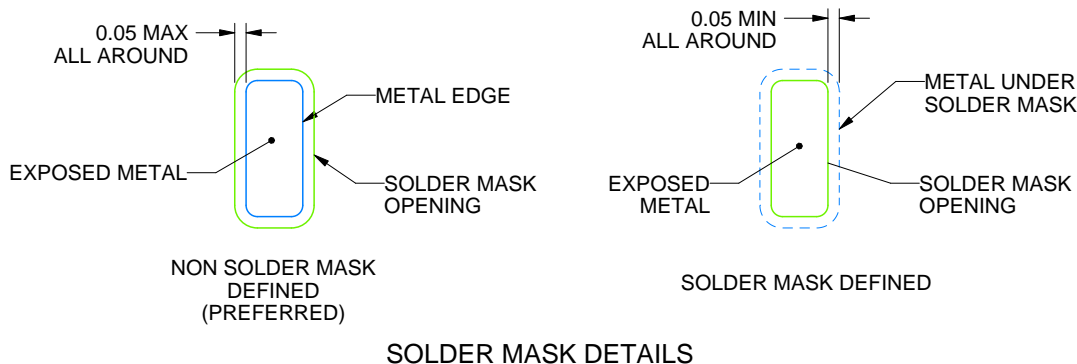
RSW0010A

UQFN - 0.55 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 30X



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NOTES: (continued)

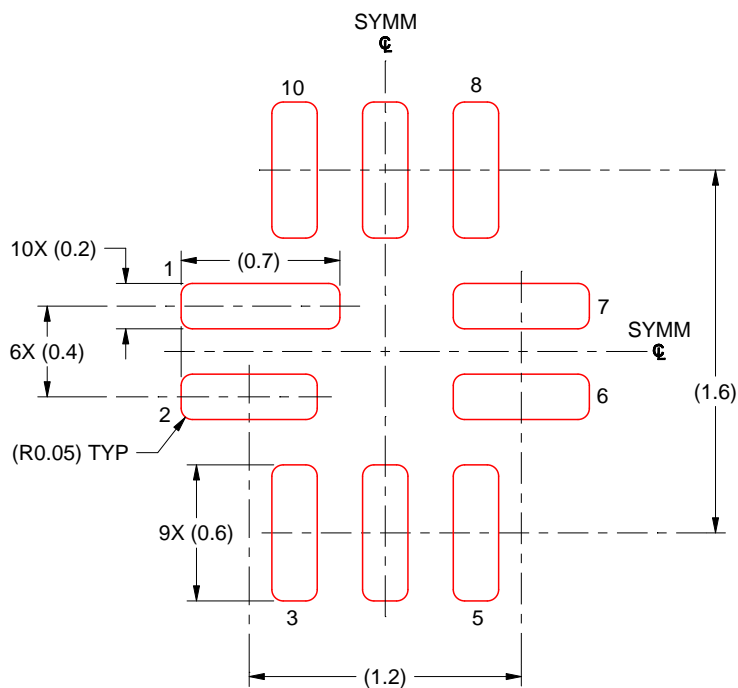
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/sluea271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

RSW0010A

UQFN - 0.55 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 30X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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